



TLVx316

10-MHz, Rail-to-Rail Input/Output, Low-Voltage, 1.8-V CMOS Operational Amplifiers

1 Features

- Unity-Gain Bandwidth: 10 MHz
- Low I_Q : 400 μ A/ch
 - Excellent Power-to-Bandwidth Ratio
 - Stable I_Q Over Temperature and Supply Range
- Wide Supply Range: 1.8 V to 5.5 V
- Low Noise: 12 nV/ $\sqrt{\text{Hz}}$ at 1 kHz
- Low Input Bias Current: ± 10 pA
- Offset Voltage: ± 0.75 mV
- Unity-Gain Stable
- Internal RFI/EMI Filter
- Extended Temperature Range: -40°C to $+125^\circ\text{C}$

2 Applications

- Battery-Powered Instruments:
 - Consumer, Industrial, Medical
 - Notebooks, Portable Media Players
- Sensor Signal Conditioning
- Barcode Scanners
- Active Filters
- Audio

3 Description

The TLV316 (single), TLV2316 (dual), and TLV4316 (quad) devices comprise a family of general-purpose, low-power operational amplifiers. Features such as rail-to-rail input and output swings, low quiescent current (400 μ A/ch typical) combined with a wide bandwidth of 10 MHz, and very-low noise (12 nV/ $\sqrt{\text{Hz}}$ at 1 kHz) make this family attractive for a variety of applications that require a good balance between cost and performance. The low input bias current supports operational amplifiers that are used in applications with megaohm source impedances.

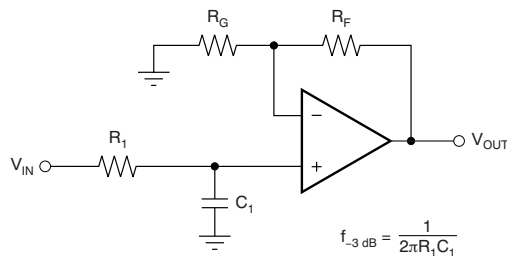
The robust design of the TLVx316 provides ease-of-use to the circuit designer—a unity-gain stable, integrated RFI/EMI rejection filter, no phase reversal in overdrive condition, and high electrostatic discharge (ESD) protection (4-kV HBM).

These devices are optimized for low-voltage operation as low as 1.8 V (± 0.9 V) and up to 5.5 V (± 2.75 V). This latest addition of low-voltage CMOS operational amplifiers to the portfolio, in conjunction with the [TLVx313](#) and [TLVx314](#) series, offer a family of bandwidth, noise, and power options to meet the needs of a wide variety of applications.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV316	SC70 (5)	1.25 mm × 2.00 mm
	SOT-23 (5)	1.60 mm × 2.90 mm
TLV2316	VSSOP (8)	3.00 mm × 3.00 mm
	SOIC (8)	3.91 mm × 4.90 mm
TLV4316	TSSOP (14)	4.40 mm × 5.00 mm
	SOIC (14)	8.65 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right) \left(\frac{1}{1 + sR_1C_1}\right)$$

Single-Pole, Low-Pass Filter

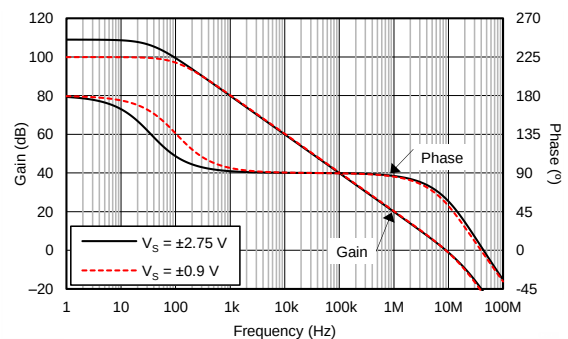
Low Supply Current (400 μ A/Ch) for 10-MHz Bandwidth

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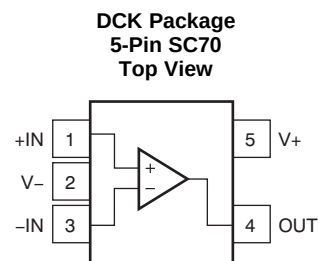
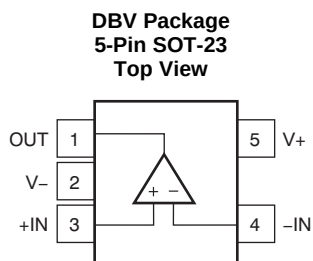
4 Revision History

Changes from Original (February 2016) to Revision A	Page
• Added 14-pin SOIC package information to <i>Device Information</i> table	1
• Added D package to PW package pinout drawing	5
• Added D (SOIC) thermal values to <i>Thermal Information: TLV4316</i> table	7

5 Device Comparison Table

DEVICE	NO. OF CHANNELS	PACKAGE-LEADS				
		DBV	DCK	D	DGK	PW
TLV316	1	5	5	—	—	—
TLV2316	2	—	—	8	8	—
TLV4316	4	—	—	14	—	14

6 Pin Configuration and Functions



Pin Functions: TLV316

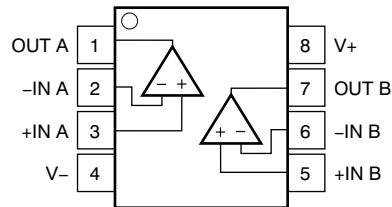
PIN			I/O	DESCRIPTION
NAME	DBV (SOT-23)	DCK (SC70)		
–IN	4	3	I	Inverting input
+IN	3	1	I	Noninverting input
OUT	1	4	O	Output
V–	2	2	—	Negative (lowest) supply or ground (for single-supply operation)
V+	5	5	—	Positive (highest) supply

TLV316, TLV2316, TLV4316

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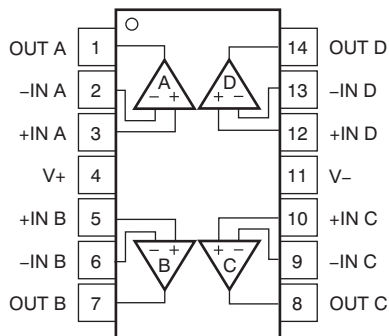
**D, DGK Packages
8-Pin SOIC, VSSOP
Top View**



Pin Functions: TLV2316

PIN		I/O	DESCRIPTION
NO.	NAME		
2	–IN A	I	Inverting input, channel A
3	+IN A	I	Noninverting input, channel A
6	–IN B	I	Inverting input, channel B
5	+IN B	I	Noninverting input, channel B
1	OUT A	O	Output, channel A
7	OUT B	O	Output, channel B
4	V–	—	Negative (lowest) supply or ground (for single-supply operation)
8	V+	—	Positive (highest) supply

**D, PW Packages
14-Pin SOIC, TSSOP
Top View**



Pin Functions: TLV4316

PIN		I/O	DESCRIPTION
NO.	NAME		
2	–IN A	I	Inverting input, channel A
3	+IN A	I	Noninverting input, channel A
6	–IN B	I	Inverting input, channel B
5	+IN B	I	Noninverting input, channel B
9	–IN C	I	Inverting input, channel C
10	+IN C	I	Noninverting input, channel C
13	–IN D	I	Inverting input, channel D
12	+IN D	I	Noninverting input, channel D
1	OUT A	O	Output, channel A
7	OUT B	O	Output, channel B
8	OUT C	O	Output, channel C
14	OUT D	O	Output, channel D
11	V–	—	Negative (lowest) supply or ground (for single-supply operation)
4	V+	—	Positive (highest) supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
Supply voltage			7		V
Signal input pins	Voltage ⁽²⁾	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential	(V+) – (V–) + 0.2		
	Current ⁽²⁾		–10	10	mA
Output short-circuit ⁽³⁾			Continuous		mA
Temperature	Specified, T _A		–40	125	°C
	Junction, T _J		150		
	Storage, T _{stg}		–65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input pins are diode-clamped to the power-supply rails. Current limit input signals that can swing more than 0.5 V beyond the supply rails to 10 mA or less.
- (3) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _S	Supply voltage	1.8		5.5	V
	Specified temperature range	–40		125	°C

7.4 Thermal Information: TLV316

THERMAL METRIC ⁽¹⁾		TLV316		UNIT
		DBV (SOT-23)	DCK (SC70)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	221.7	263.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	144.7	75.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.7	51.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	26.1	1.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	49.0	50.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#) (SPRA953).

7.5 Thermal Information: TLV2316

THERMAL METRIC ⁽¹⁾		TLV2316		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	127.2	186.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	71.6	78.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	68.2	107.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	22.0	15.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	67.6	106.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#) (SPRA953).

7.6 Thermal Information: TLV4316

THERMAL METRIC ⁽¹⁾		TLV4316		UNIT
		PW (TSSOP)	D (SOIC)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	117.2	87.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	46.2	44.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	58.9	41.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.9	11.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	58.3	41.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#) (SPRA953).

7.7 Electrical Characteristics

at $T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted); V_S (total supply voltage) = $(V+) - (V-) = 1.8\text{ V to } 5.5\text{ V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V _{OS}	Input offset voltage	V _S = 5 V		±0.75	±3	mV
		V _S = 5 V, T _A = −40°C to +125°C			±4.5	
dV _{OS} /dT	Drift	V _S = 5 V, T _A = −40°C to +125°C		±2		μV/°C
PSRR	Power-supply rejection ratio	V _S = 1.8 V – 5.5 V, V _{CM} = (V−)		±30	±175	μV/V
	Channel separation, dc	At dc		100		dB
INPUT VOLTAGE RANGE						
V _{CM}	Common-mode voltage range	V _S = 5.5 V	(V−) − 0.2		(V+) + 0.2	V
CMRR	Common-mode rejection ratio	V _S = 5.5 V, (V−) − 0.2 V < V _{CM} < (V+) − 1.4 V, T _A = −40°C to +125°C	72	90		dB
		V _S = 5.5 V, V _{CM} = −0.2 V to 5.7 V, T _A = −40°C to +125°C		75		
INPUT BIAS CURRENT						
I _B	Input bias current			±10		pA
I _{OS}	Input offset current			±10		pA
NOISE						
E _n	Input voltage noise (peak-to-peak)	V _S = 5 V, f = 0.1 Hz to 10 Hz		5		μV _{PP}
e _n	Input voltage noise density	V _S = 5 V, f = 1 kHz		12		nV/√Hz
i _n	Input current noise density	f = 1 kHz		1.3		fA/√Hz
INPUT IMPEDANCE						
Z _{ID}	Differential			2 2		10 ¹⁶ Ω pF
Z _{IC}	Common-mode			2 4		10 ¹¹ Ω pF
OPEN-LOOP GAIN						
A _{OL}	Open-loop voltage gain	V _S = 5.5 V, (V−) + 0.05 V < V _O < (V+) − 0.05 V, R _L = 10 kΩ	100	104		dB
		V _S = 5.5 V, (V−) + 0.15 V < V _O < (V+) − 0.15 V, R _L = 2 kΩ		104		
FREQUENCY RESPONSE						
GBP	Gain bandwidth product	V _S = 5 V, G = +1		10		MHz
φ _m	Phase margin	V _S = 5 V, G = +1		60		Degrees
SR	Slew rate	V _S = 5 V, G = +1		6		V/μs
t _S	Settling time	To 0.1%, V _S = 5 V, 2-V step , G = +1, C _L = 100 pF		1		μs
t _{OR}	Overload recovery time	V _S = 5 V, V _{IN} × gain = V _S		0.8		μs
THD + N	Total harmonic distortion + noise ⁽¹⁾	V _S = 5 V, V _O = 0.5 V _{RMS} , G = +1, f = 1 kHz		0.008%		
OUTPUT						
V _O	Voltage output swing from supply rails	V _S = 1.8 V to 5.5 V, R _L = 10 kΩ,			35	mV
		V _S = 1.8 to 5.5 V, R _L = 2 kΩ,			125	
I _{SC}	Short-circuit current	V _S = 5 V		±50		mA
Z _O	Open-loop output impedance	V _S = 5 V, f = 10 MHz		250		Ω
POWER SUPPLY						
V _S	Specified voltage range		1.8		5.5	V
I _Q	Quiescent current per amplifier	V _S = 5 V, I _O = 0 mA, T _A = −40°C to 125°C		400	575	μA
TEMPERATURE						
T _A	Specified		−40		125	°C
T _{sto}	Storage		−65		150	°C

(1) Third-order filter; bandwidth = 80 kHz at -3 dB.

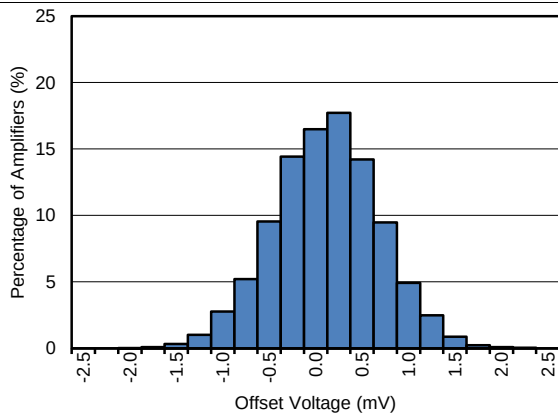
7.8 Typical Characteristics

Table 1. Table of Graphs

TITLE	FIGURE
Offset Voltage Production Distribution	Figure 1
Offset Voltage vs Common-Mode Voltage	Figure 2
Open- Loop Gain and Phase vs Frequency	Figure 3
Input Bias and Offset Current vs Temperature	Figure 4
Input Voltage Noise Spectral Density vs Frequency	Figure 5
Quiescent Current vs Supply Voltage	Figure 6
Small-Signal Overshoot vs Load Capacitance	Figure 7
No Phase Reversal	Figure 8
Small-Signal Step Response	Figure 9
Large-Signal Step Response	Figure 10
Short-Circuit Current vs Temperature	Figure 11
Electromagnetic Interference Rejection Ratio Referred to Noninverting Input vs Frequency	Figure 12
Channel Separation vs Frequency	Figure 13

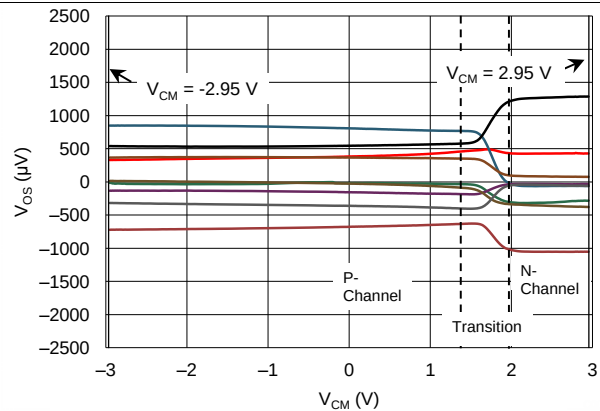
7.9 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = 5.5\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)



Distribution taken from 12551 amplifiers

Figure 1. Offset Voltage Production Distribution



$V_+ = 2.75\text{ V}$, $V_- = -2.75\text{ V}$, 9 typical units shown

Figure 2. Offset Voltage vs Common-Mode Voltage

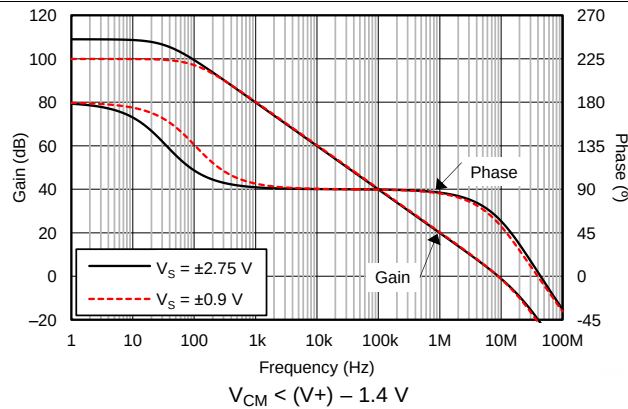


Figure 3. Open-Loop Gain and Phase vs Frequency

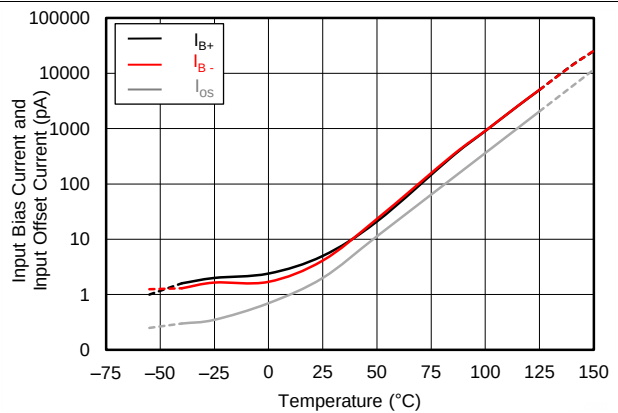


Figure 4. Input Bias and Offset Current vs Temperature

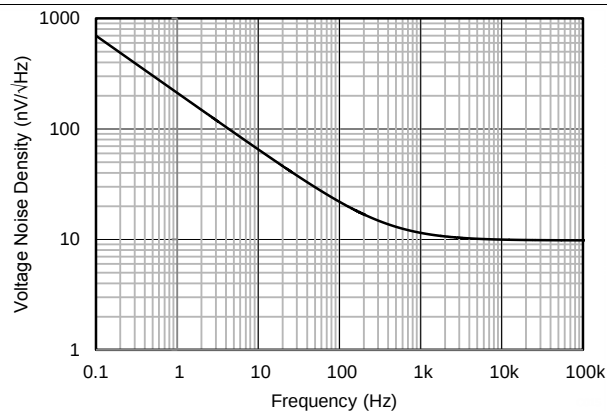


Figure 5. Input Voltage Noise Spectral Density vs Frequency

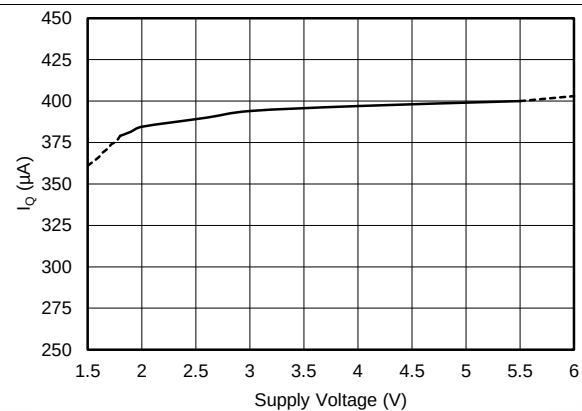


Figure 6. Quiescent Current vs Supply Voltage

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5.5\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

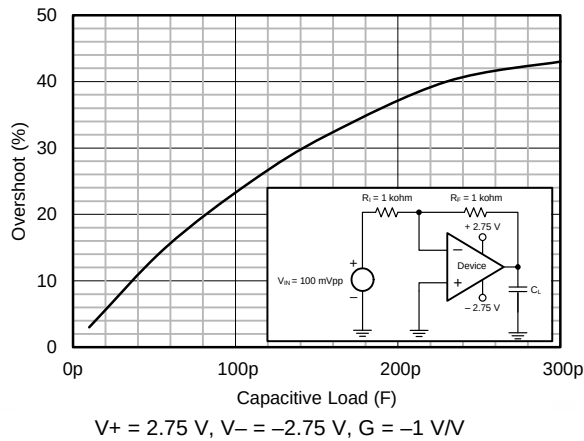


Figure 7. Small-Signal Overshoot vs Load Capacitance

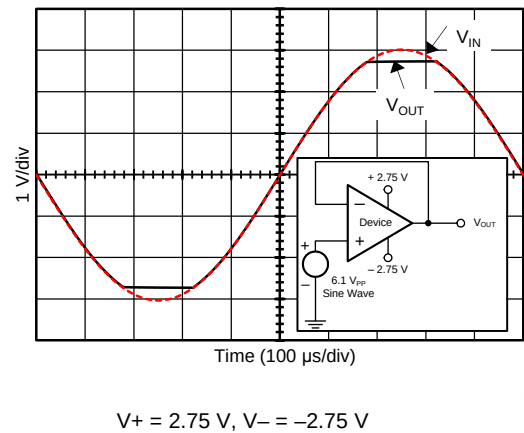


Figure 8. No Phase Reversal

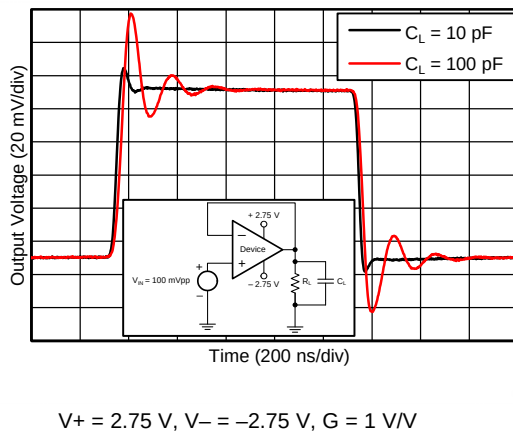


Figure 9. Small-Signal Step Response

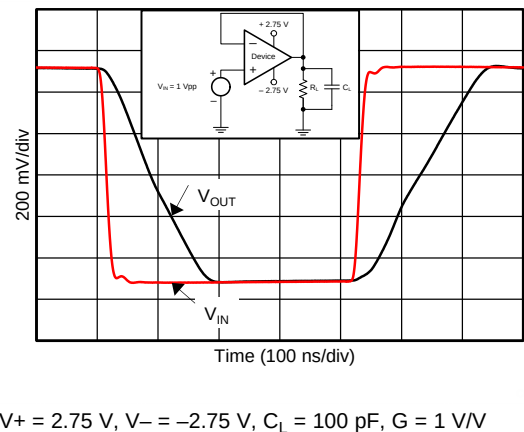


Figure 10. Large-Signal Step Response

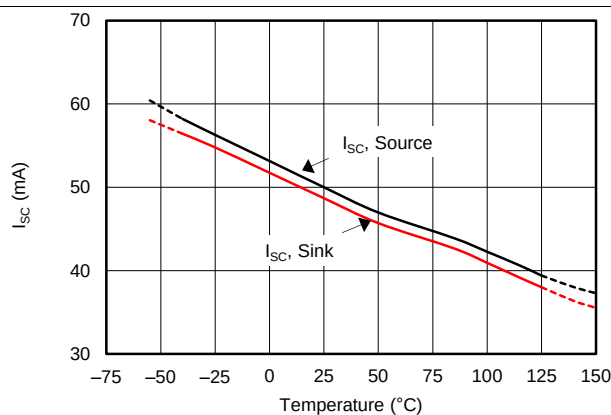


Figure 11. Short-Circuit Current vs Temperature

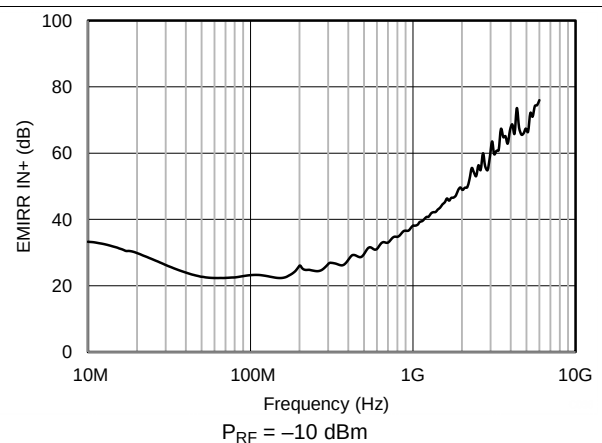


Figure 12. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input vs Frequency

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5.5\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

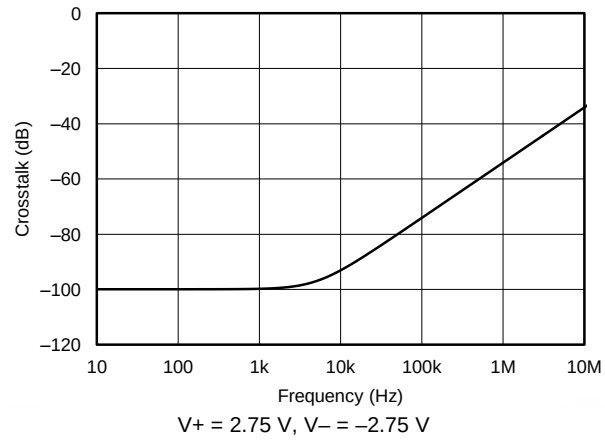


Figure 13. Channel Separation vs Frequency

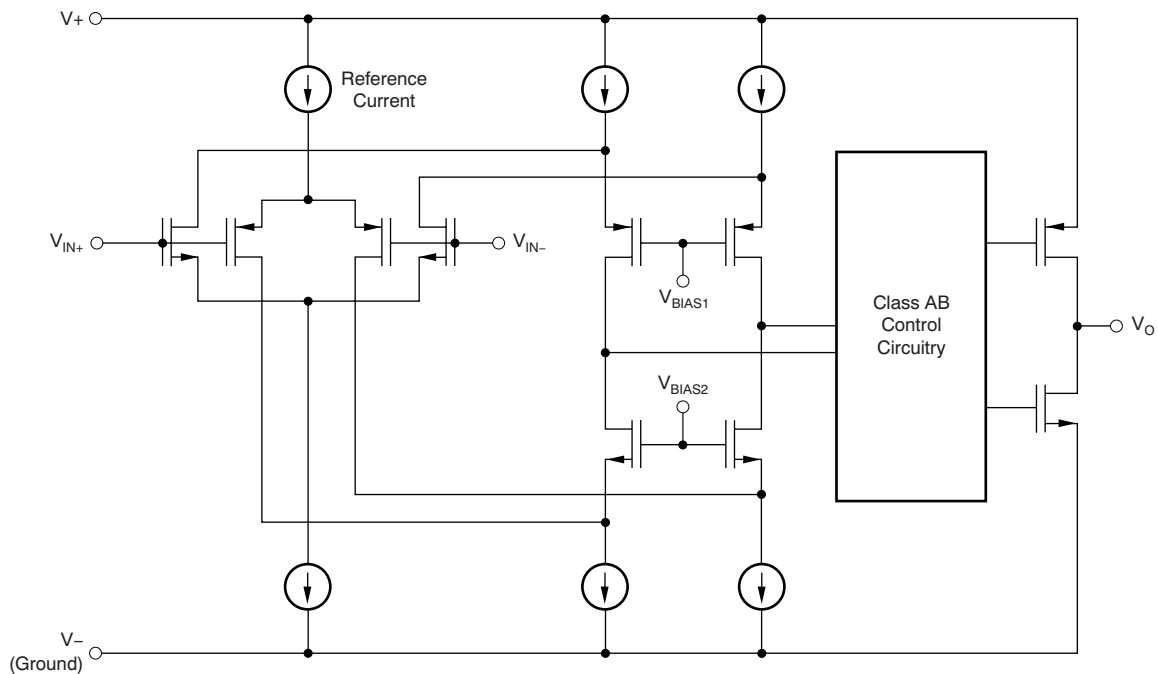
8 Detailed Description

8.1 Overview

The TLVx316 is a family of low-power, rail-to-rail input and output operational amplifiers. These devices operate from 1.8 V to 5.5 V, are unity-gain stable, and are suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving $\leq 10\text{-k}\Omega$ loads connected to any point between V+ and ground. The input common-mode voltage range includes both rails and allows the TLVx316 to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes them suitable for driving sampling analog-to-digital converters (ADCs).

The TLVx316 features 10-MHz bandwidth and 6-V/ μ s slew rate with only 400- μ A supply current per channel, providing good ac performance at very-low power consumption. DC applications are well served with a very-low input noise voltage of 12 nV/ $\sqrt{\text{Hz}}$ at 1 kHz, low input bias current (5 pA), and an input offset voltage of 0.5 mV (typical).

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Operating Voltage

The TLVx316 operational amplifiers are fully specified and ensured for operation from 1.8 V to 5.5 V. In addition, many specifications apply from -40°C to $+125^{\circ}\text{C}$. Parameters that vary significantly with operating voltages or temperature are illustrated in the [Typical Characteristics](#) section.

8.3.2 Rail-to-Rail Input

The input common-mode voltage range of the TLVx316 extends 200 mV beyond the supply rails for supply voltages greater than 2.5 V. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair; see the [Functional Block Diagram](#) section. The N-channel pair is active for input voltages close to the positive rail, typically $(V+) - 1.4\text{ V}$ to 200 mV above the positive supply, whereas the P-channel pair is active for inputs from 200 mV below the negative supply to approximately $(V+) - 1.4\text{ V}$. There is a small transition region, typically $(V+) - 1.2\text{ V}$ to $(V+) - 1\text{ V}$, in which both pairs are on. This 200-mV transition region can vary up to 200 mV with process variation. Thus, the transition region (both stages on) can range from $(V+) - 1.4\text{ V}$ to $(V+) - 1.2\text{ V}$ on the low end, up to $(V+) - 1\text{ V}$ to $(V+) - 0.8\text{ V}$ on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can be degraded compared to device operation outside this region.

8.3.3 Rail-to-Rail Output

Designed as a low-power, low-voltage operational amplifier, the TLVx316 delivers a robust output drive capability. A class AB output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. For resistive loads of 10 k Ω , the output swings typically to within 30 mV of either supply rail regardless of the power-supply voltage applied. Different load conditions change the ability of the amplifier to swing close to the rails; see typical characteristic graph *Output Voltage Swing vs Output Current* ().

8.3.4 Common-Mode Rejection Ratio (CMRR)

CMRR for the TLVx316 is specified in two ways so the best match for a given application can be selected. First, the [Electrical Characteristics](#) table provides the CMRR of the device in the common-mode range below the transition region [$V_{\text{CM}} < (V+) - 1.4\text{ V}$]. This specification is the best indicator of device capability when the application requires using one of the differential input pairs. Second, the CMRR over the entire common-mode range is specified at $V_{\text{CM}} = -0.2\text{ V}$ to 5.7 V for $V_{\text{S}} = 5.5\text{ V}$. This last value includes the variations through the transition region.

8.3.5 Capacitive Load and Stability

The TLVx316 is designed to be used in applications where driving a capacitive load is required. As with all operational amplifiers, there may be specific instances where the TLVx316 can become unstable. The particular operational amplifier circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether or not an amplifier is stable in operation. An operational amplifier in the unity-gain (1 V/V) buffer configuration that drives a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the operational amplifier output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases when the capacitive loading increases. For a conservative best practice, designing for 25% overshoot (40° phase margin) provides improved stability over process variations. The equivalent series resistance (ESR) of some very-large capacitors (C_{L} greater than 1 μF) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when observing the overshoot response of the amplifier at higher voltage gains. See typical characteristic graph, *Small-Signal Overshoot vs Capacitive Load* ([Figure 7](#), $G = -1\text{ V/V}$).

Feature Description (continued)

One technique for increasing the capacitive load drive capability of the amplifier operating in a unity-gain configuration is to insert a small resistor (typically $10\ \Omega$ to $20\ \Omega$) in series with the output, as shown in Figure 14. This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. One possible problem with this technique, however, is that a voltage divider is created with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing.

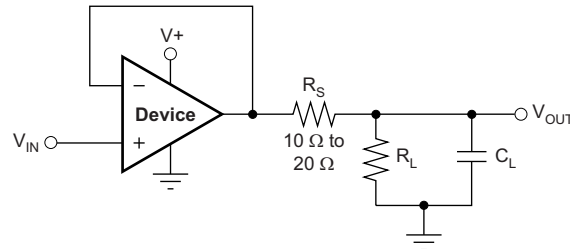


Figure 14. Improving Capacitive Load Drive

8.3.6 EMI Susceptibility and Input Filtering

Operational amplifiers vary with regard to the susceptibility of the device to electromagnetic interference (EMI). If conducted EMI enters the operational amplifier, the dc offset measured at the amplifier output can shift from its nominal value when EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although all operational amplifier pin functions can be affected by EMI, the signal input pins are likely to be the most susceptible. The TLVx316 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifier response to EMI. This filter provides both common-mode and differential-mode filtering. The filter is designed for a cutoff frequency of approximately 80 MHz ($-3\ \text{dB}$), with a roll-off of 20 dB per decade.

The immunity of an operational amplifier can be accurately measured and quantified over a broad frequency spectrum extending from 10 MHz to 6 GHz. The EMI rejection ratio (EMIRR) metric allows operational amplifiers to be directly compared by the EMI immunity. Figure 12 illustrates the results of this testing on the TLVx316. Detailed information can be found in *EMI Rejection Ratio of Operational Amplifiers* (SBOA128), available for download from www.ti.com.

8.3.7 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, either because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the TLVx316 is approximately 300 ns.

8.4 Device Functional Modes

The TLVx316 have a single functional mode. These devices are powered on as long as the power-supply voltage is between 1.8 V ($\pm 0.9\ \text{V}$) and 5.5 V ($\pm 2.75\ \text{V}$).

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLV316, TLV2316, and TLV4316 are powered on when the supply is connected. The devices can be operated as a single-supply operational amplifier or a dual-supply amplifier, depending on the application.

9.2 System Examples

When receiving low-level signals, the device often requires limiting the bandwidth of the incoming signals into the system. The simplest way to establish this limited bandwidth is to place an RC filter at the noninverting pin of the amplifier, as shown in [Figure 15](#).

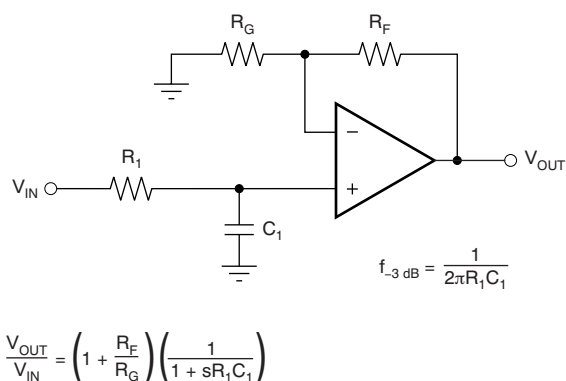


Figure 15. Single-Pole, Low-Pass Filter

If even more attenuation is needed, the device requires a multiple-pole filter. The Sallen-Key filter can be used for this task, as shown in [Figure 16](#). For best results, the amplifier must have a bandwidth that is eight to ten times the filter frequency bandwidth. Failure to follow this guideline can result in a phase shift of the amplifier.

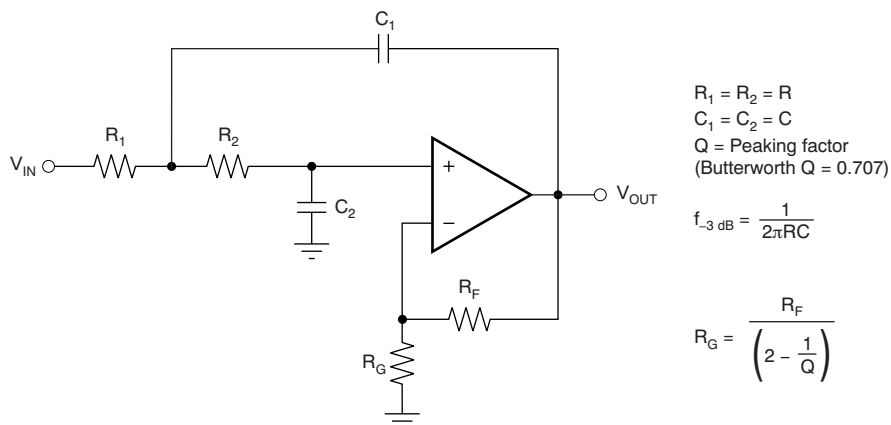


Figure 16. Two-Pole, Low-Pass, Sallen-Key Filter

10 Power Supply Recommendations

The TLVx316 is specified for operation from 1.8 V to 5.5 V (± 0.9 V to ± 2.75 V); many specifications apply from -40°C to $+125^{\circ}\text{C}$. [Typical Characteristics](#) presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 7 V can permanently damage the device (see the [Absolute Maximum Ratings](#) table).

Place 0.1- μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see [Layout Guidelines](#).

10.1 Input and ESD Protection

The TLVx316 incorporates internal ESD protection circuits on all pins. For input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA, as stated in the [Absolute Maximum Ratings](#) table. [Figure 17](#) shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value must be kept to a minimum in noise-sensitive applications.

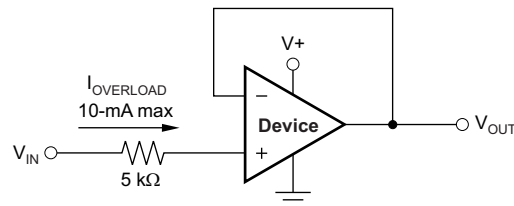


Figure 17. Input Current Protection

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1- μ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are typically devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see , [Circuit Board Layout Techniques](#) (SLOA089).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in [Layout Example](#).
- Keep the length of input traces as short as possible. Remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example

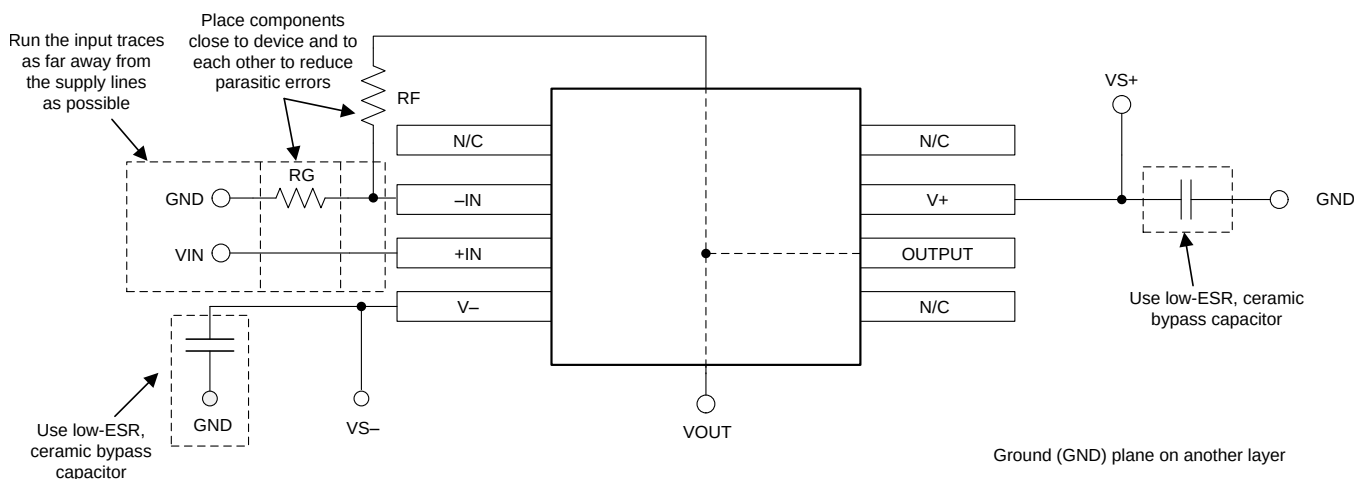


Figure 18. Operational Amplifier Board Layout for a Noninverting Configuration

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

[TLVx313 Low-Power, Rail-to-Rail In/Out, 500- \$\mu\$ V Typical Offset, 1-MHz Operational Amplifier for Cost-Sensitive Systems](#) (SBOS753).

[TLVx314 3-MHz, Low-Power, Internal EMI Filter, RRIO, Operational Amplifier](#) (SBOS754).

[EMI Rejection Ratio of Operational Amplifiers](#) (SBOA128).

[QFN/SON PCB Attachment](#) (SLUA271).

[Quad Flatpack No-Lead Logic Packages](#) (SCBA017).

[Circuit Board Layout Techniques](#) (SLOA089).

[Single-Ended Input to Differential Output Conversion Circuit Reference Design](#) (TIPD131).

12.2 Related Links

[Table 2](#) lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLV316	Click here	Click here	Click here	Click here	Click here
TLV2316	Click here	Click here	Click here	Click here	Click here
TLV4316	Click here	Click here	Click here	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV2316IDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	12X6
TLV2316IDGKR.B	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	12X6
TLV2316IDGKT	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	12X6
TLV2316IDGKT.B	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	12X6
TLV2316IDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	V2316
TLV2316IDR.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	V2316
TLV316IDBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12C
TLV316IDBVR.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	12C
TLV316IDBVRG4.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	-	Call TI	Call TI	-40 to 125	
TLV316IDBVT	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU SN NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12C
TLV316IDBVT.B	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	12C
TLV316IDCKR	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	12D
TLV316IDCKR.B	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	12D
TLV316IDCKT	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	12D
TLV316IDCKT.B	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	12D
TLV4316IDR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T4316D
TLV4316IDR.B	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T4316D
TLV4316IPWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 125	TLV4316
TLV4316IPWR.B	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV4316

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV2316, TLV316, TLV4316 :

- Automotive : [TLV2316-Q1](#), [TLV316-Q1](#), [TLV4316-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2316IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2316IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2316IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV316IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV316IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV316IDCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
TLV316IDCKT	SC70	DCK	5	250	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
TLV4316IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV4316IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

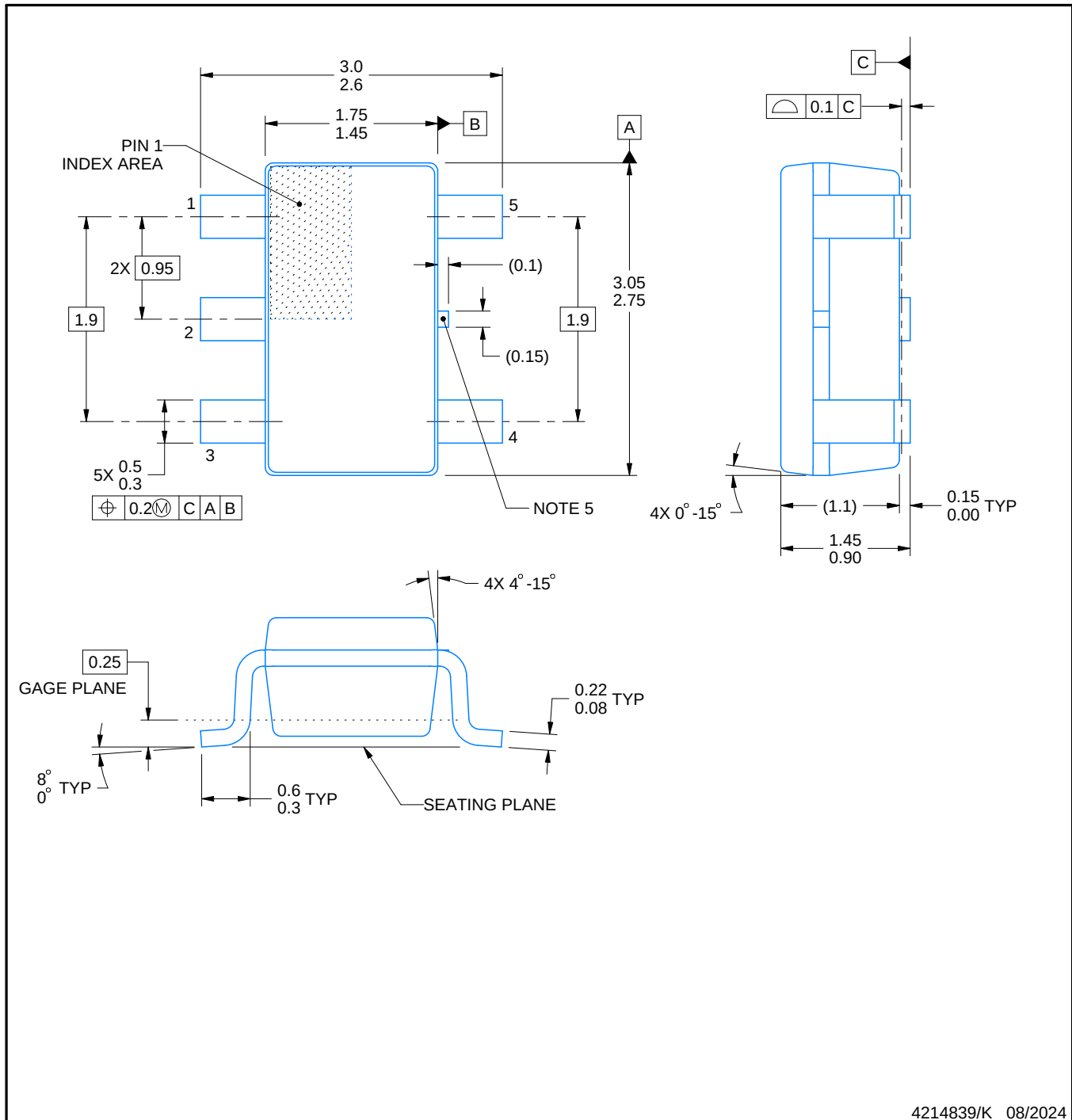


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2316IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV2316IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
TLV2316IDR	SOIC	D	8	2500	356.0	356.0	35.0
TLV316IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV316IDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV316IDCKR	SC70	DCK	5	3000	210.0	185.0	35.0
TLV316IDCKT	SC70	DCK	5	250	210.0	185.0	35.0
TLV4316IDR	SOIC	D	14	2500	353.0	353.0	32.0
TLV4316IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0

DBV0005A**PACKAGE OUTLINE****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



4214839/K 08/2024

NOTES:

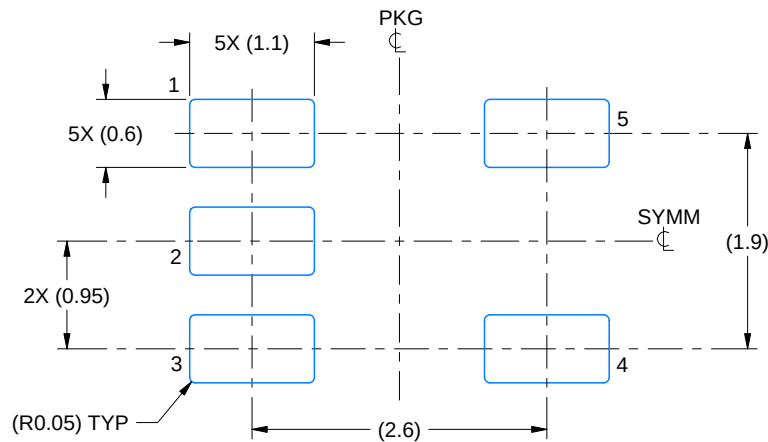
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

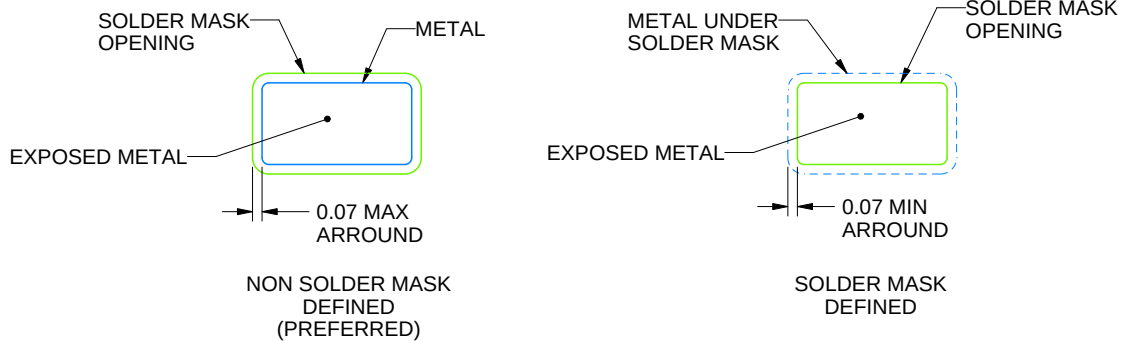
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

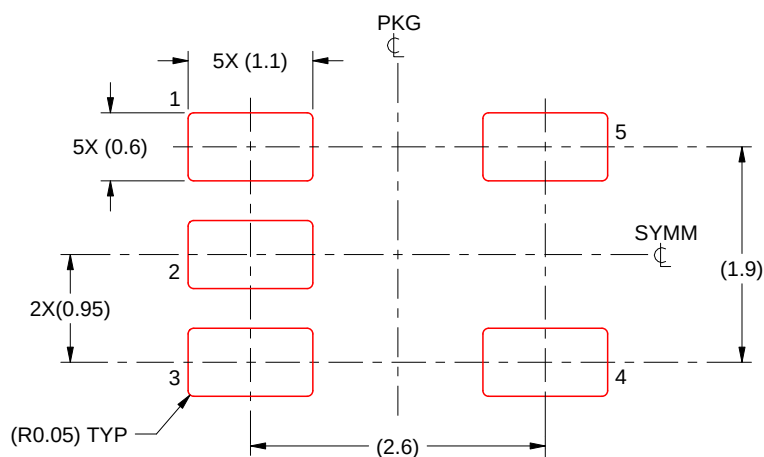
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



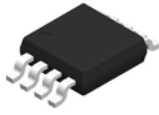
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

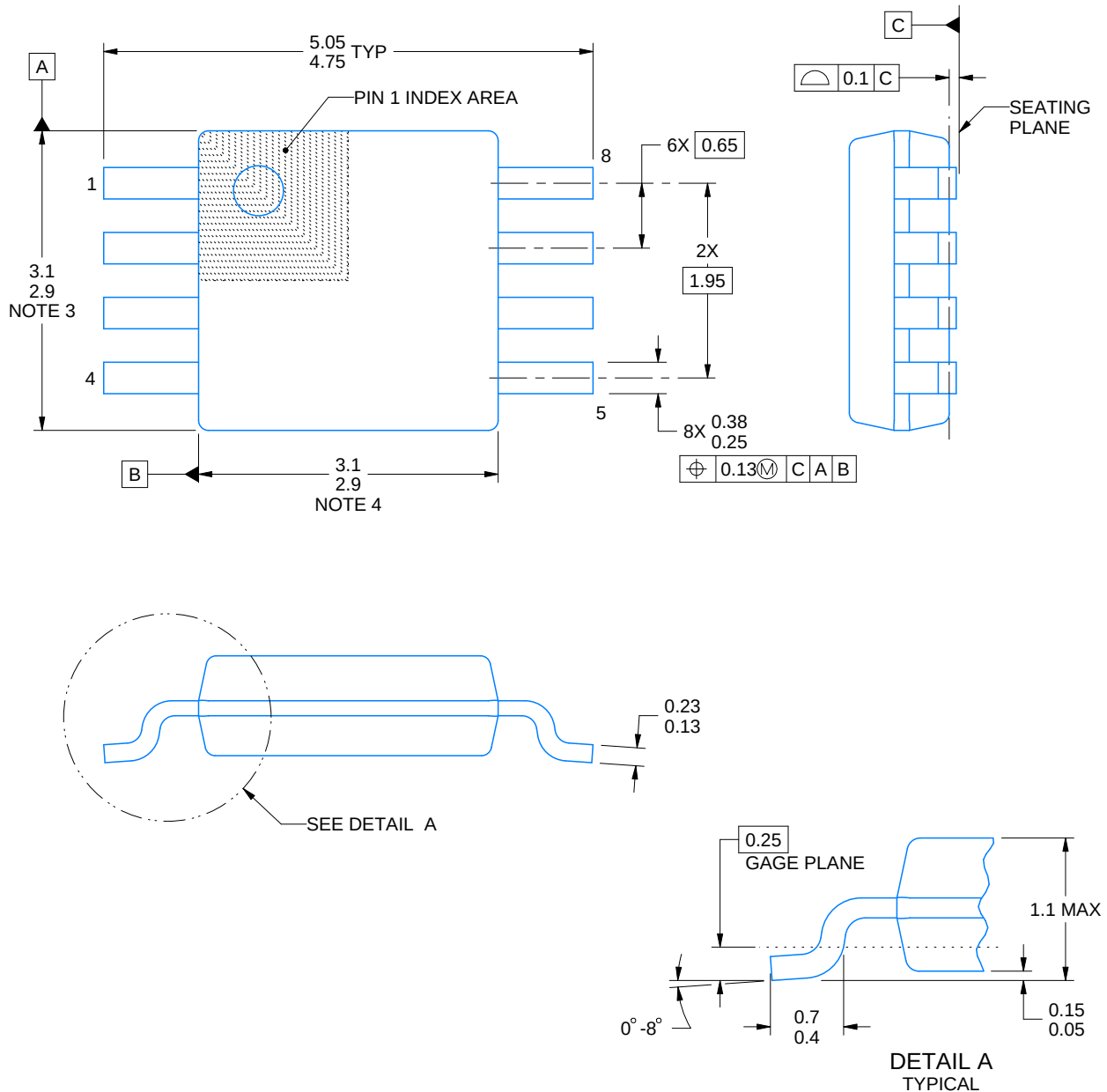
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK0008A



PACKAGE OUTLINE
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

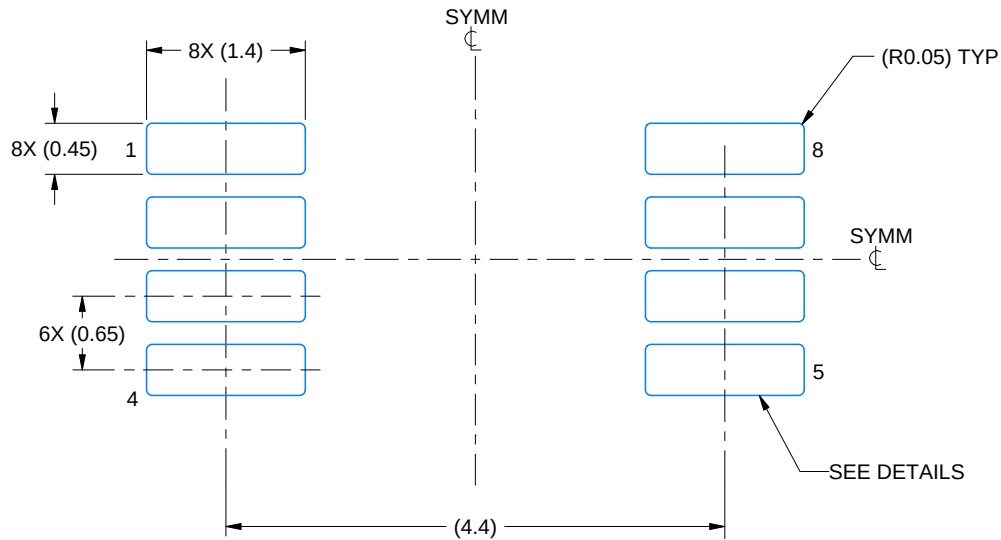
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

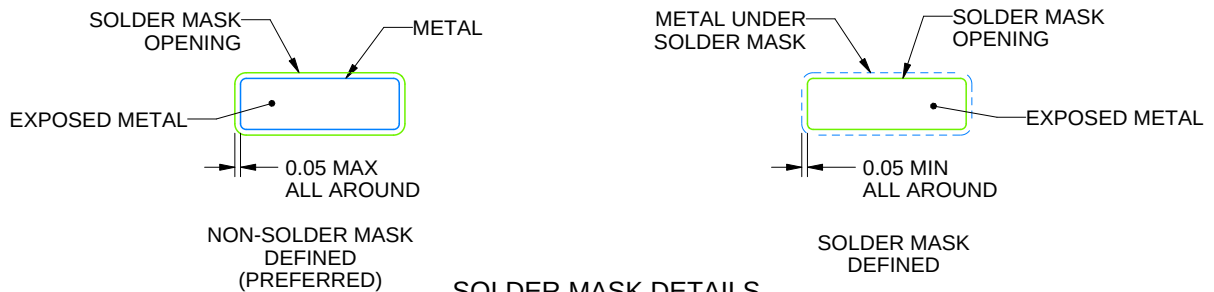
DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

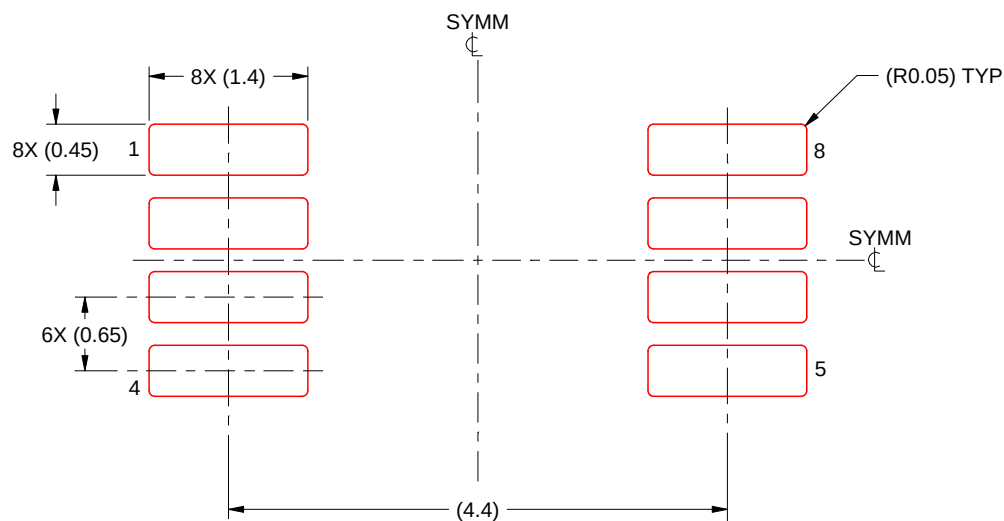
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

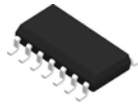


SOLDER PASTE EXAMPLE
SCALE: 15X

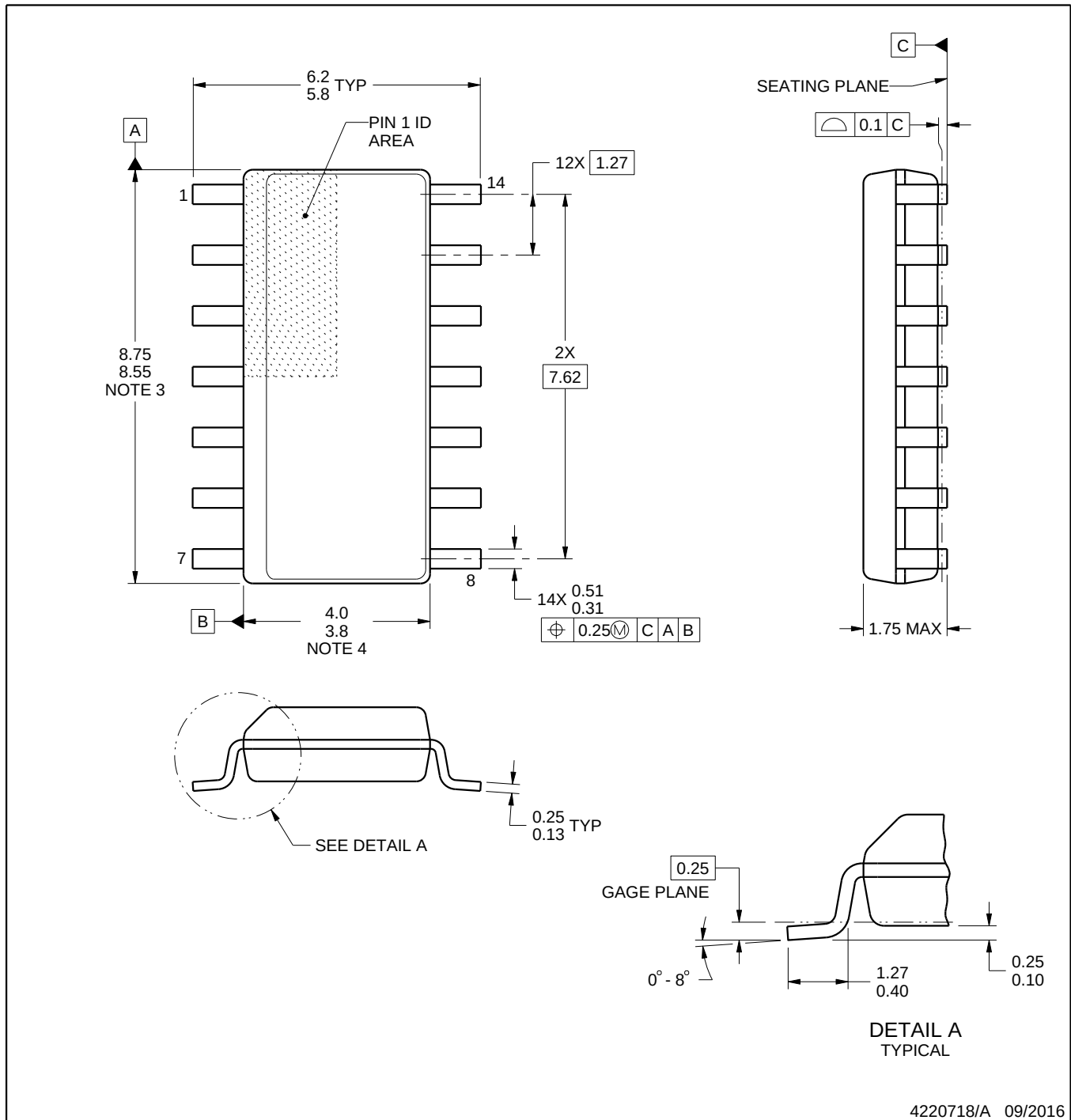
4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT

**NOTES:**

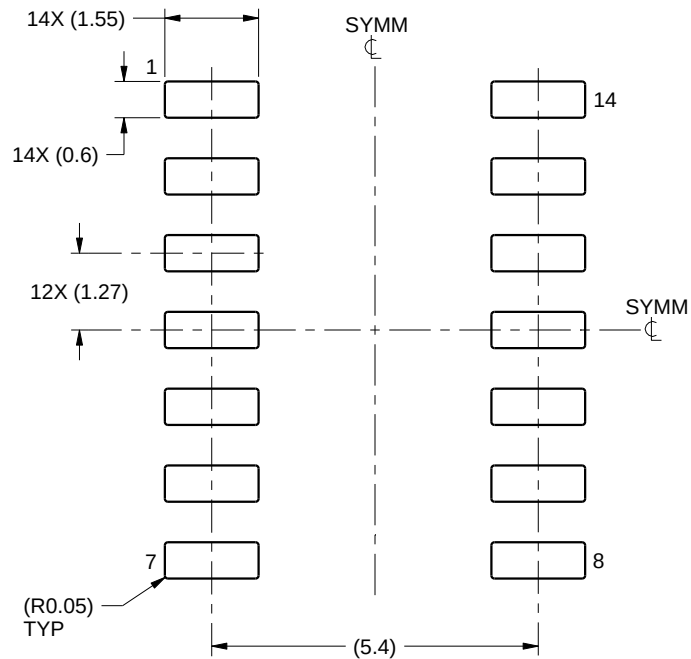
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

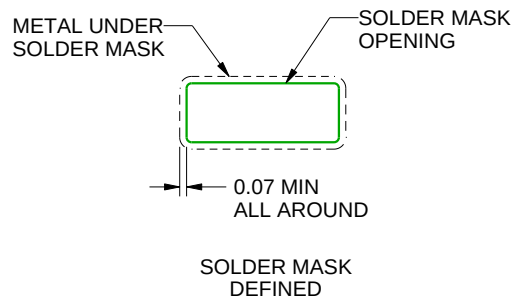
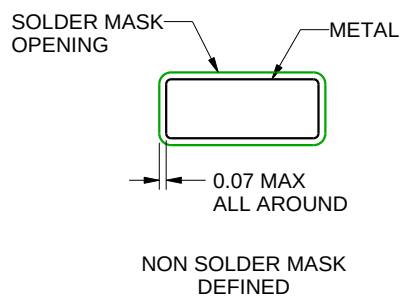
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

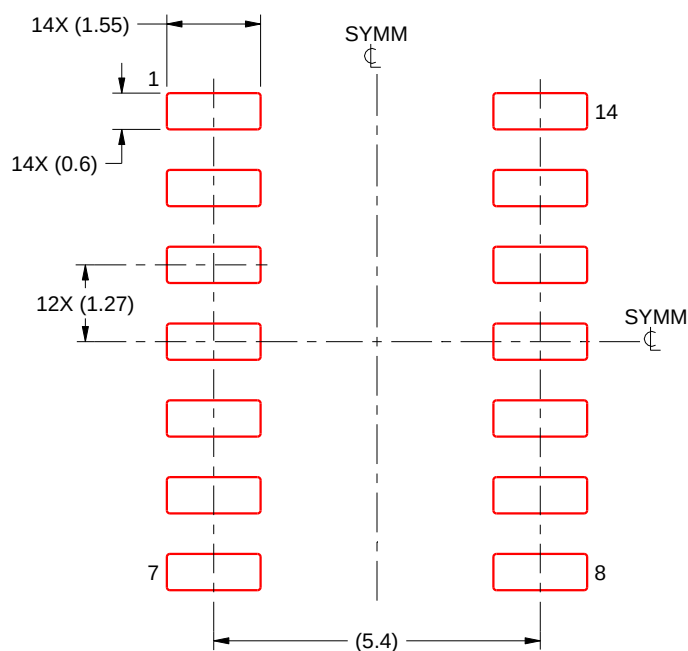
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

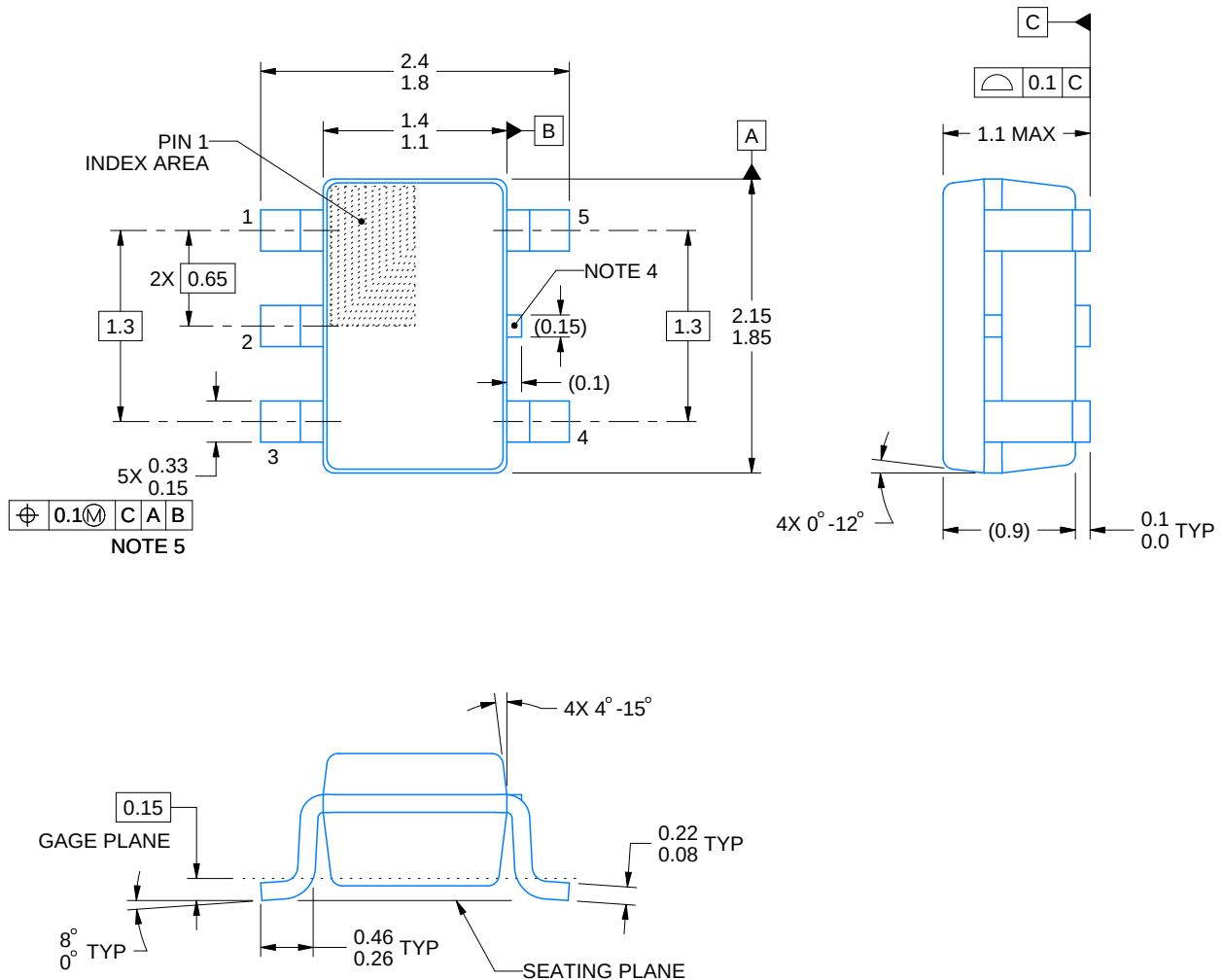


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

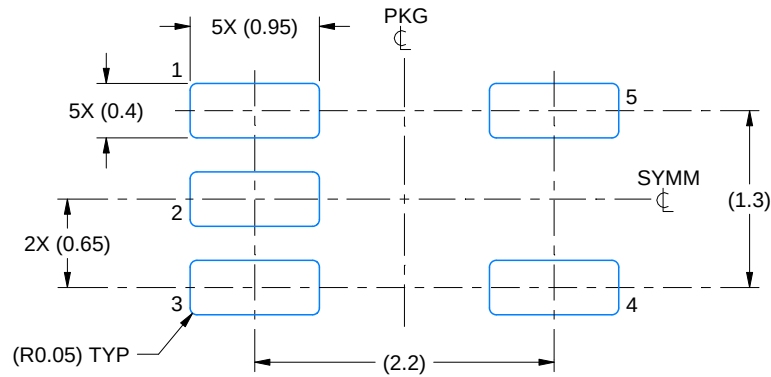
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



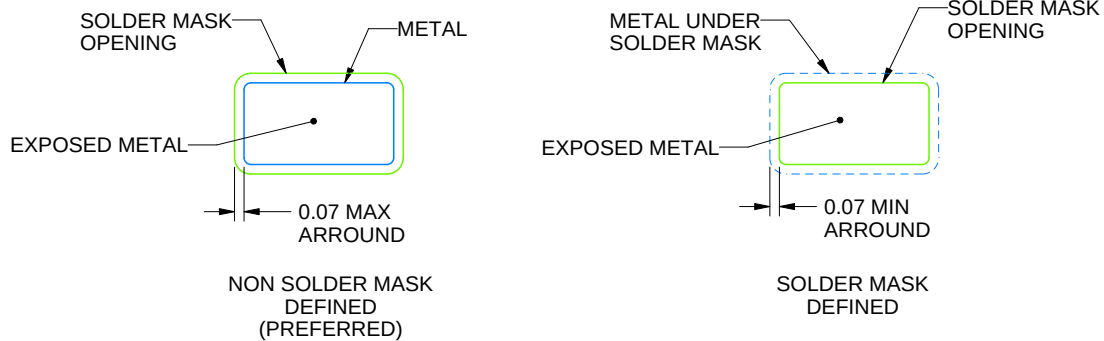
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

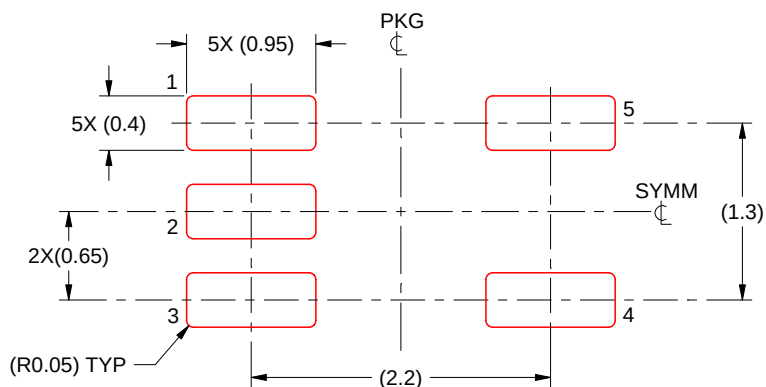


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



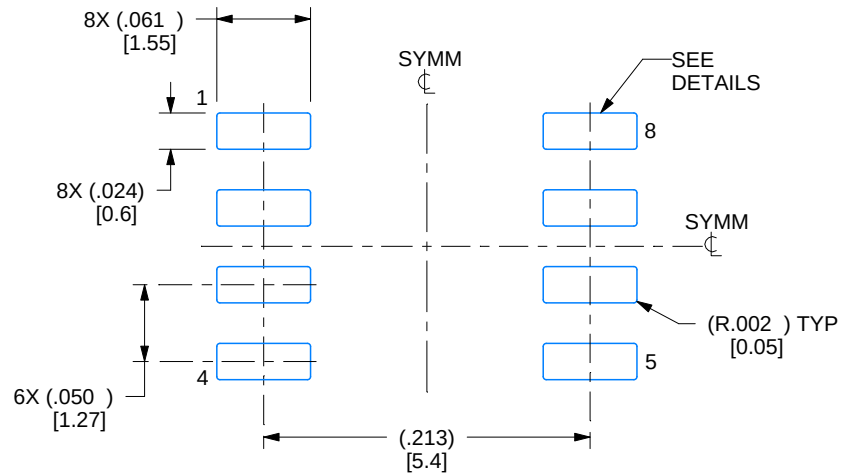
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

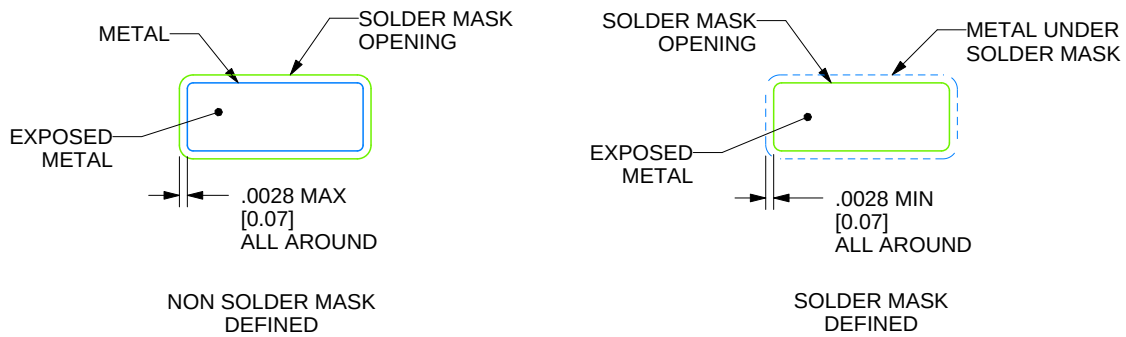
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

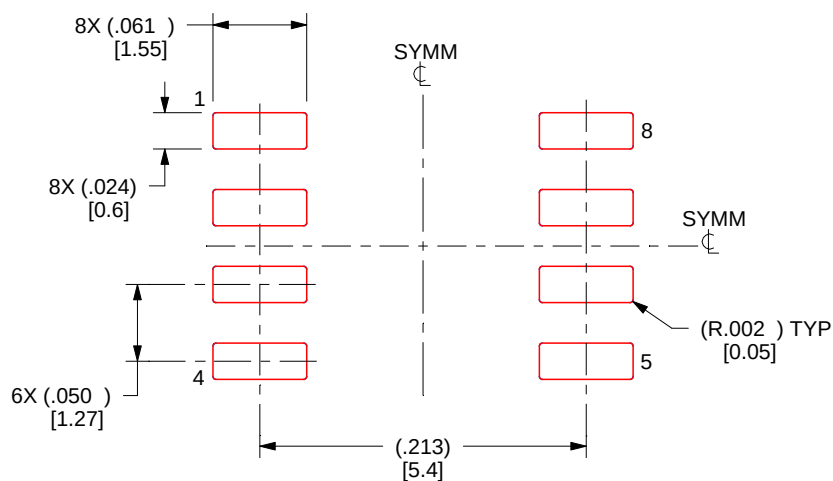
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

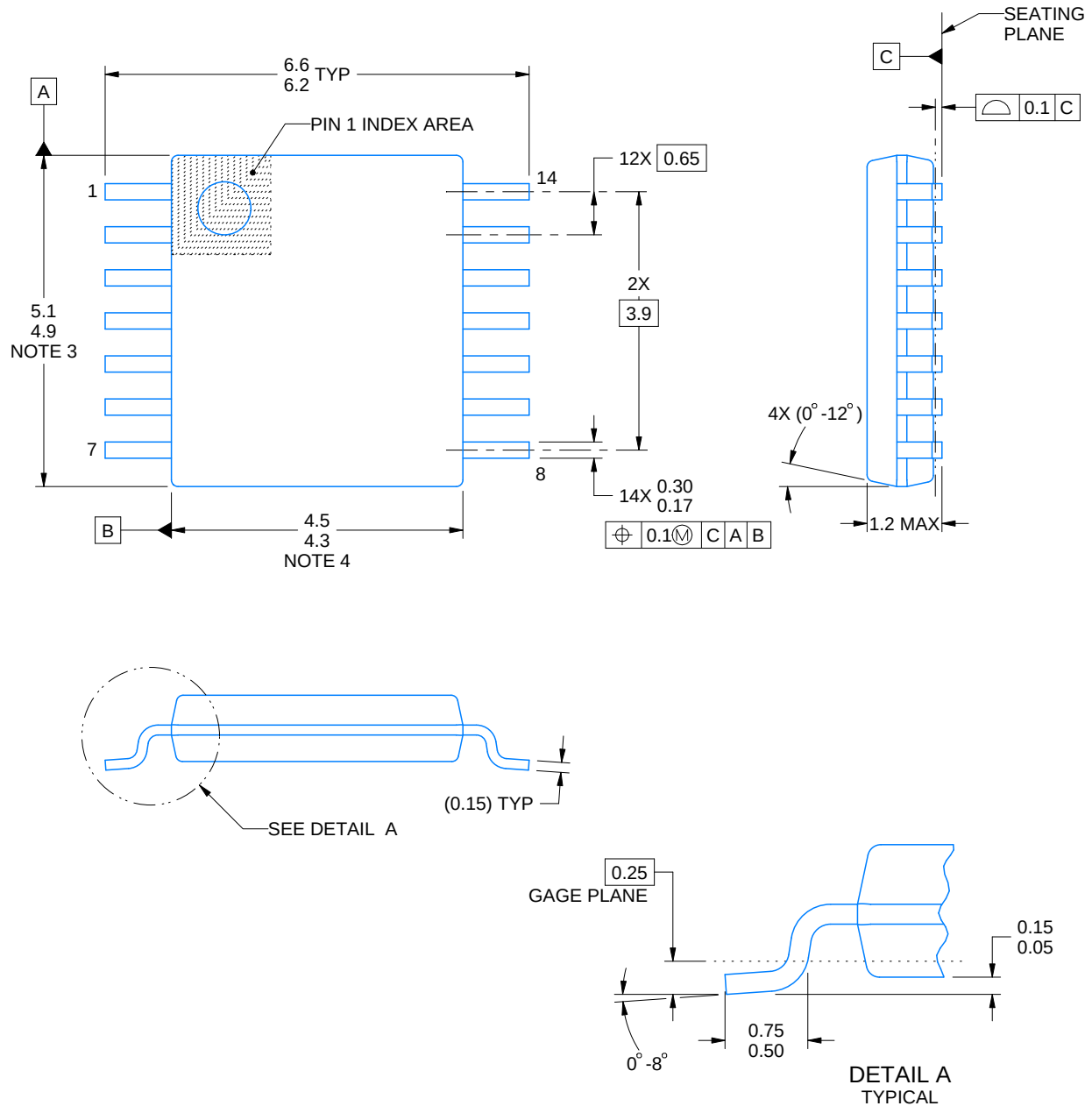
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW0014A

PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

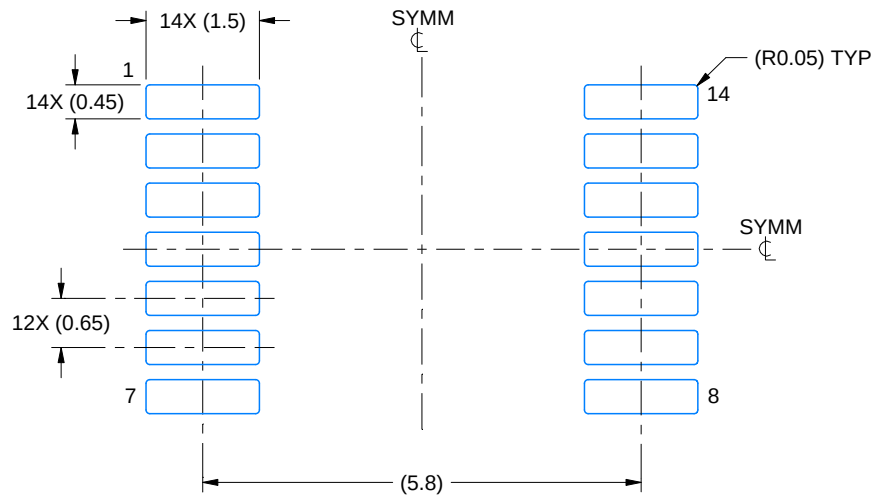
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

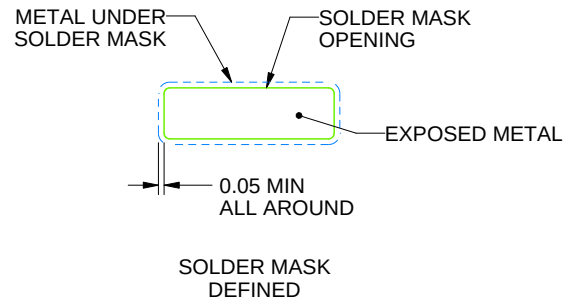
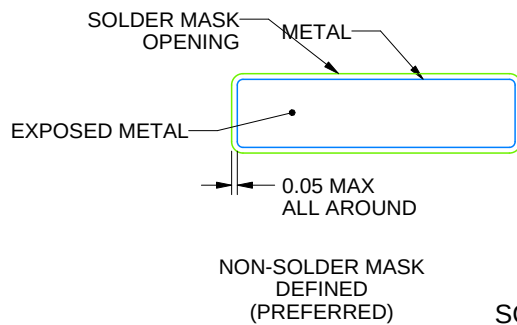
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

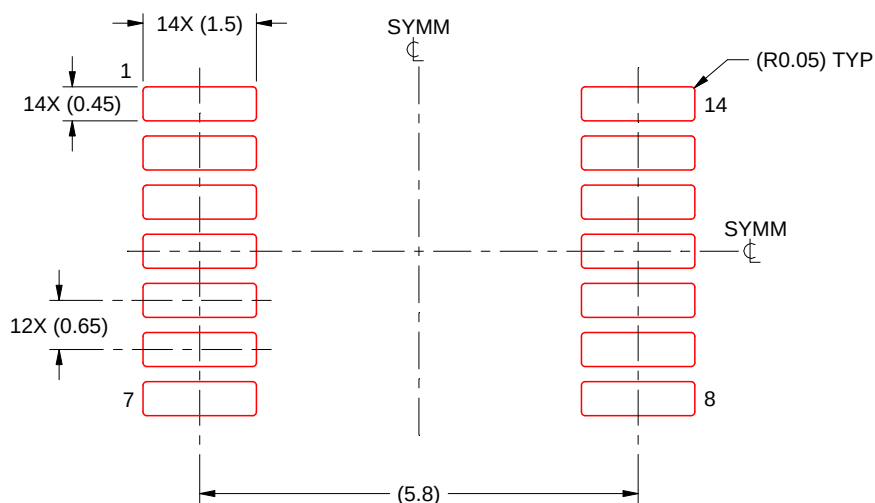
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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