ADC3544 14-bit, 125-MSPS, Low Noise, Low Power ADC

1 Features

- 14-bit 125 MSPS ADC
- Noise floor: –153 dBFS/Hz
- Ultra-low power with optimized power scaling: 97 mW/ch (125 MSPS)
- Latency: 1 clock cycle
- INL: ±1.5 LSB; DNL: ±0.5 LSB
- Reference: external or internal
- Industrial temperature range: –40°C to +105°C
- On-chip digital filter (optional)
  - Decimation by 2, 4, 8, 16, 32
  - 32-bit NCO
- SDR/DDR and Serial CMOS interface
- Small footprint: 40-WQFN (5 mm × 5 mm) package
- Single 1.8-V supply
- Spectral performance (f_{IN} = 5 MHz):
  - SNR: 74.0 dBFS
  - SFDR: 85-dBc HD2, HD3
  - SFDR: 93-dBFS worst spur
- Spectral performance (f_{IN} = 70 MHz):
  - SNR: 70.6dBFS
  - SFDR: 79-dBc HD2, HD3
  - SFDR: 85-dBFS worst spur

2 Applications

- High-speed data acquisition
- Industrial monitoring
- Thermal imaging
- Imaging and sonar
- Software defined radio
- Power quality
- Communications infrastructure
- High-speed control loops
- Instrumentation
- Smart grids
- Spectroscopy
- Radar

3 Description

The ADC3544 device is a low-noise, ultra-low power, 14-bit, 125-MSPS, high-speed analog-to-digital converter (ADC). Designed for low power consumption, the device delivers a noise spectral density of –153 dBFS/Hz, combined with a good linearity and dynamic range. The ADC3544 offers IF sampling support, which make these devices an excellent choice for a wide range of applications. High-speed control loops benefit from the short latency of only one clock cycle. The ADC consumes only 97 mW/ch at 125 MSPS, and the power consumption scales well with lower sampling rates.

The ADC3544 uses an SDR or DDR interface to output the data offering the lowest power digital interface, together with the flexibility to minimize the number of digital interconnects. These devices are a pin-to-pin compatible family with different speed grades. These devices support the extended industrial temperature range of –40°C to 105ºC.

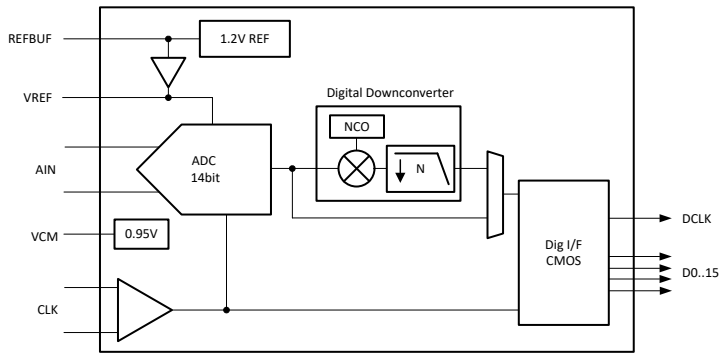
Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
ADC3544	WQFN (40)	5.00 mm × 5.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

Device Comparison

PART NUMBER	RESOLUTION	SAMPLING RATE
ADC3541	14 bit	10 MSPS
ADC3542	14 bit	25 MSPS
ADC3543	14 bit	65 MSPS
ADC3544	14 bit	125 MSPS



Block Diagram

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2022	*	Initial release.

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5 Pin Configuration and Functions

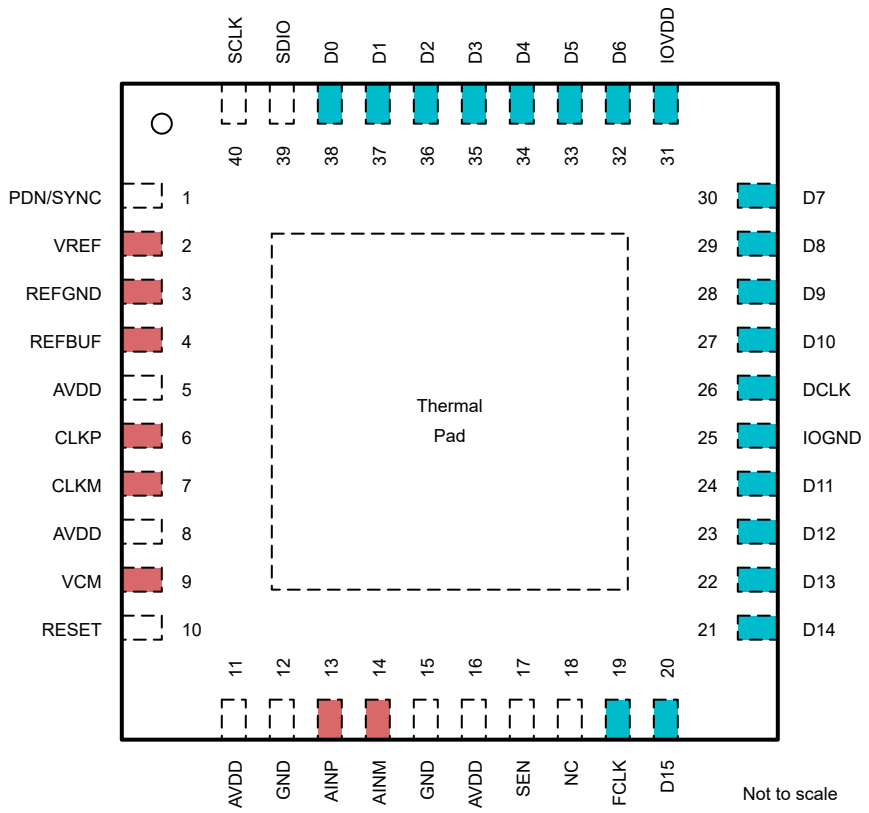

Figure 5-1. RSB Package, 40-Pin WQFN (Top View)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
INPUT/REFERENCE			
AINM	14	I	Negative analog input
AINP	13	I	Positive analog input
REFBUF	4	I	1.2-V external voltage reference input for use with internal reference buffer. Internal 100 kΩ pull-up resistor to AVDD. This pin is also used to configure default operating conditions.
REFGND	3	I	Reference ground input, 0 V
VCM	9	O	Common-mode voltage output for the analog inputs, 0.95 V
VREF	2	I	External voltage reference input, 1.6 V.
CLOCK			
CLKM	7	I	Negative differential sampling clock input for the ADC
CLKP	6	I	Positive differential sampling clock input for the ADC
CONFIGURATION			
NC	18	-	Do not connect
PDN/SYNC	1	I	Power down, synchronization input. This pin can be configured via the SPI interface. Active high. This pin has an internal 21 kΩ pull-down resistor.

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Table 5-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
RESET	10	I	Hardware reset; active high. This pin has an internal 21 kΩ pull-down resistor.
SCLK	40	I	Serial interface clock input. This pin has an internal 21 kΩ pull-down resistor.
SDIO	39	I	Serial interface data input and output. This pin has an internal 21 kΩ pull-down resistor.
SEN	17	I	Serial interface enable. Active low. This pin has an internal 21 kΩ pull-up resistor to AVDD.
DIGITAL INTERFACE			
D0	38	O	CMOS output used with 16 bit output (configured via output bit formatter). This becomes LSB. When not used can be left unconnected.
D1	37	O	CMOS output used with 16 bit output (configured via output bit formatter). This becomes LSB-1. When not used can be left unconnected.
D2	36	O	CMOS output for data bit D0.
D3	35	I/O	CMOS output for data bit D1. Used as DCLKIN in serial CMOS output modes.
D4	34	O	CMOS output for data bit D2.
D5	33	O	CMOS output for data bit D3.
D6	32	O	CMOS output for data bit D4.
D7	30	O	CMOS output for data bit D5.
D8	29	O	CMOS output for data bit D6.
D9	28	O	CMOS output for data bit D7.
D10	27	O	CMOS output for data bit D8.
D11	24	O	CMOS output for data bit D9. Lane 0 in serial CMOS output mode.
D12	23	O	CMOS output for data bit D10. Lane 1 in serial CMOS output mode.
D13	22	O	CMOS output for data bit D11.
D14	21	O	CMOS output for data bit D12.
D15	20	O	CMOS output for data bit D13 (MSB).
DCLK	26	O	CMOS output for data bit clock
FCLK	19	O	Frame clock output in serial CMOS output mode.
POWER SUPPLY			
AVDD	5,8,11,16	I	Analog 1.8-V power supply
GND	12,15	I	Ground, 0 V
IOGND	25	I	Ground, 0 V for digital interface
IOVDD	31	I	1.8-V power supply for digital interface
PowerPAD™	--	--	Connect to ground

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Supply voltage range, AVDD, IOVDD		–0.3	2.1	V
Supply voltage range, GND, IOGND, REFGND		–0.3	0.3	V
Voltage applied to input pins	AINP/M, CLKP/M, VREF, REFBUF, D3 (DCLKIN)	–0.3	MIN(2.1, AVDD+0.3)	V
	PDN, RESET, SCLK, SEN, SDIO	–0.3	MIN(2.1, AVDD+0.3)	
Junction temperature, T_J			105	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	2500	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins[2]	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage range	AVDD[1]	1.75	1.8	1.85	V
	IOVDD[1]	1.75	1.8	1.85	V
T_A	Operating free-air temperature	–40		105	°C
T_J	Operating junction temperature			105[2]	°C

(1) Measured to GND.
(2) Prolonged use above this junction temperature may increase the device failure-in-time (FIT) rate.

6.4 Thermal Information

THERMAL METRIC[1]		ADC354x RSB (QFN) 40 Pins	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	30.7	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	16.4	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	10.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	10.5	°C/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics - Power Consumption

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 105°C, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD, IOVDD = 1.8 V, external 1.6 V reference, 5 pF output load, and –1-dBFS differential input, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Consumption						
I_{AVDD}	Analog supply current	External reference		36	46	mA
I_{IOVDD}	I/O supply current(1)	SDR CMOS		18	28	mA
P_{DIS}	Power dissipation(1)	External reference, SDR CMOS		97	133	mW
MISCELLANEOUS						
I_{AVDD}	Internal reference, additional analog supply current			3		mA
	External reference, Internal reference buffer (REFBUF), additional analog supply current			0.5		mA
	Single ended clock input, reduces analog supply current by	Enabled via SPI		1		mA
P_{DIS}	Power consumption in global power down mode	Default mask settings, internal reference		5		mW
		Default mask settings, external reference		9		mW

(1) Measured with a full-scale sine wave input signal with ~ 5 pF loading on each CMOS output pin.

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6.6 Electrical Characteristics - DC Specifications

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 105°C, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD, IOVDD = 1.8 V, external 1.6 V reference, 5 pF output load, and –1-dBFS differential input, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC ACCURACY						
No missing codes			14			bits
PSRR		F_{IN} = 1 MHz		35		dB
DNL	Differential nonlinearity	F_{IN} = 5 MHz		± 0.5	± 0.97	LSB
INL	Integral nonlinearity	F_{IN} = 5 MHz		± 1.5	± 8	LSB
V_{OS_ERR}	Offset error			-8	85	LSB
V_{OS_DRIFT}	Offset drift over temperature			0.02		ppm/ºC
$GAIN_{ERR}$	Gain error	External 1.6 V reference		0.5		%FSR
$GAIN_{DRIFT}$	Gain drift over temperature	External 1.6 V reference		9		ppm/ºC
$GAIN_{ERR}$	Gain error	Internal reference		-0.4		%FSR
$GAIN_{DRIFT}$	Gain drift over temperature	Internal reference		74		ppm/ºC
Transition Noise	Transition Noise			0.71		LSB_{RMS}
DC ACCURACY						
ADC ANALOG INPUT (AINP/M)						
FS	Input full scale	Default, differential		2.25		Vpp
V_{CM}	Input common mode voltage		0.9	0.95	1.0	V
R_{IN}	Input resistance	Differential at DC		8		kΩ
C_{IN}	Input capacitance	Each pin to GND		5.4		pF
V_{OCM}	Output common mode voltage			0.95		V
BW	Analog input bandwidth (-3dB)			1.4		GHz
Internal Voltage Reference						
V_{REF}	Internal reference voltage			1.6		V
V_{REF} Output Impedance				8		Ω
Reference Input Buffer (REFBUF)						
External reference voltage				1.2		V
External voltage reference (VREF)						
V_{REF}	External voltage reference			1.6		V
Input Current				1		mA
Input impedance				5.3		kΩ
Clock Input (CLKP/M)						
Input clock frequency		External Reference	10	125	125	MHz
Input clock frequency		Internal Reference	100	125	125	MHz
V_{ID}	Differential input voltage		250	1000	2000	mV
V_{CM}	Input common mode voltage			0.9		V
Clock duty cycle			40	50	60	%
Digital Inputs (RESET, PDN, SCLK, SEN, SDIO)						
V_{IH}	High level input voltage		1.4			V
V_{IL}	Low level input voltage				0.4	
I_{IH}	High level input current			90	150	uA
I_{IL}	Low level input current		-150	-90		
C_I	Input capacitance			1.5		pF

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6.6 Electrical Characteristics - DC Specifications (continued)

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 105°C, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD, IOVDD = 1.8 V, external 1.6 V reference, 5 pF output load, and –1-dBFS differential input, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Output (SDOUT)						
V_{OH}	High level output voltage	I_{LOAD} = -400 uA	IOVDD – 0.1	IOVDD		V
V_{OL}	Low level output voltage	I_{LOAD} = 400 uA			0.1	
CMOS Interface (D0:D17)						
Output data rate		per CMOS output pin			250	MHz
V_{OH}	High level output voltage	I_{LOAD} = -400 uA	IOVDD – 0.1	IOVDD		V
V_{OL}	Low level output voltage	I_{LOAD} = 400 uA			0.1	
V_{IH}	High level input voltage	Input clock (Serial CMOS)	IOVDD – 0.1	IOVDD		V
V_{IL}	Low level input voltage				0.1	

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6.7 Electrical Characteristics - AC Specifications

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 105°C, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD, IOVDD = 1.8 V, external 1.6V reference, 5 pF output load, and –1-dBFS differential input, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD	Noise Spectral Density	No input signal		-153		dBFS/Hz
SNR	Signal to noise ratio	f_{IN} = 5 MHz	71.5	74.0		dBFS
		f_{IN} = 10 MHz		73.9		
		f_{IN} = 40 MHz		73.0		
		f_{IN} = 70 MHz		70.6		
		f_{IN} = 100 MHz		69.2		
SINAD	Signal to noise and distortion ratio	f_{IN} = 5 MHz	71	74.0		dBFS
		f_{IN} = 10 MHz		73.9		
		f_{IN} = 40 MHz		73.0		
		f_{IN} = 70 MHz		70.6		
		f_{IN} = 100 MHz		69.2		
ENOB	Effective number of bits	f_{IN} = 5 MHz	11.5	12.0		bit
		f_{IN} = 10 MHz		11.9		
		f_{IN} = 40 MHz		11.9		
		f_{IN} = 70 MHz		11.8		
		f_{IN} = 100 MHz		11.7		
THD	Total Harmonic Distortion (First five harmonics)	f_{IN} = 5 MHz	75	82		dBc
		f_{IN} = 10 MHz		81		
		f_{IN} = 40 MHz		80		
		f_{IN} = 70 MHz		75		
		f_{IN} = 100 MHz		72		
HD2	Second Harmonic Distortion	f_{IN} = 5 MHz	80	85		dBc
		f_{IN} = 10 MHz		82		
		f_{IN} = 40 MHz		83		
		f_{IN} = 70 MHz		79		
		f_{IN} = 100 MHz		72		
HD3	Third Harmonic Distortion	f_{IN} = 5 MHz	77	90		dBc
		f_{IN} = 10 MHz		96		
		f_{IN} = 40 MHz		92		
		f_{IN} = 70 MHz		82		
		f_{IN} = 100 MHz		83		
Non HD2,3	Spur free dynamic range (excluding HD2 and HD3)	f_{IN} = 5 MHz	90	93		dBFS
		f_{IN} = 10 MHz		94		
		f_{IN} = 40 MHz		89		
		f_{IN} = 70 MHz		85		
		f_{IN} = 100 MHz		83		
IMD3	Two tone inter-modulation distortion	f_1 = 10 MHz, f_2 = 12 MHz, A_{IN} = -7 dBFS/tone		93		dBc

6.8 Timing Requirements

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 105°C, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD, IOVDD = 1.8 V, external 1.6 V reference, 5 pF output load, and –1-dBFS differential input, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
ADC Timing Specifications						
t_{AD}	Aperture delay			0.85		ns
t_A	Aperture jitter	Square wave clock with fast edges		230		fs
t_J	Jitter on DCLKIN	Serial CMOS output mode			± 50	ps (pk-pk)
t_{ACQ}	Signal acquisition period	Referenced to sampling clock falling edge		$-T_S/4$		Sampling Clock Period
t_{CONV}	Signal conversion period	Referenced to sampling clock falling edge		6		ns
Wake up time	Time to valid data after coming out of power down. Internal reference.	Bandgap reference enabled, single ended clock		13		us
		Bandgap reference enabled, differential clock		15		
		Bandgap reference disabled, single ended clock		2.4		ms
		Bandgap reference disabled, differential clock		2.3		
	Time to valid data after coming out of power down. External 1.6V reference.	Bandgap reference enabled, single ended clock		13		us
		Bandgap reference enabled, differential clock		14		
		Bandgap reference disabled, single ended clock		2.0		ms
		Bandgap reference disabled, differential clock		2.2		
$t_{S,SYNC}$	Setup time for SYNC input signal	Referenced to sampling clock rising edge	500			ps
$t_{H,SYNC}$	Hold time for SYNC input signal		600			
ADC Latency	Signal input to data output	SDR CMOS		1		Clock cycles
		DDR CMOS		1		
		Serialized CMOS: 2-wire		2		
		Serialized CMOS: 1-wire		1		
Add Latency	Real decimation by 2			21		Output clock cycles
	Complex decimation by 2			22		
	Real or complex decimation by 4, 8, 16, 32			23		
INTERFACE TIMING - SDR CMOS						
t_{PD}	Propagation delay: sampling clock falling edge to DCLK rising edge	Propagation delay: sampling clock falling edge to DCLK rising edge	3	5	7	ns
t_{CD}	DCLK rising edge to output data delay	Fout = 125 MSPS	-0.5	-0.2		
t_{DV}	Data valid, SDR CMOS	Fout = 125 MSPS	7.7	7.9		
INTERFACE TIMING - DDR CMOS						
t_{PD}	Propagation delay: sampling clock falling edge to DCLK rising edge	Propagation delay: sampling clock falling edge to DCLK rising edge	3	5	7	ns
t_{CD}	DCLK rising edge to output data delay	Fout = 125 MSPS	-0.5	-0.3		
t_{DV}	Data valid, DDR CMOS	Fout = 125 MSPS	3.5	3.8		

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6.8 Timing Requirements

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 105°C, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD, IOVDD = 1.8 V, external 1.6 V reference, 5 pF output load, and –1-dBFS differential input, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
INTERFACE TIMING - SERIAL CMOS						
t_{PD}	Propagation delay: sampling clock falling edge to DCLK rising edge	Delay between sampling clock falling edge to DCLKIN falling edge < 2.5ns. T_{DCLK} = DCLK period t_{CDCLK} = Sampling clock falling edge to DCLKIN falling edge	2 + T_{DCLK} + t_{CDCLK}	3 + T_{DCLK} + t_{CDCLK}	4 + T_{DCLK} + t_{CDCLK}	ns
t_{PD}	Propagation delay: sampling clock falling edge to DCLK rising edge	Delay between sampling clock falling edge to DCLKIN falling edge >= 2.5ns. T_{DCLK} = DCLK period t_{CDCLK} = Sampling clock falling edge to DCLKIN falling edge	2 + t_{CDCLK}	3 + t_{CDCLK}	4 + t_{CDCLK}	ns
t_{CD}	DCLK rising edge to output data delay, 2-wire serial CMOS	Fout = 10 MSPS, D11/D12 = 80 MBPS	-0.24	0.10		ns
	DCLK rising edge to output data delay, 2-wire serial CMOS	Fout = 20 MSPS, D11/D12 = 160 MBPS	-0.29	0.10		
	DCLK rising edge to output data delay, 2-wire serial CMOS	Fout = 30 MSPS, D11/D12 = 240 MBPS	-0.28	0.09		
	DCLK rising edge to output data delay, 1-wire series CMOS	Fout = 5 MSPS, D11 = 80 MBPS	-0.22	0.11		
	DCLK rising edge to output data delay, 1-wire series CMOS	Fout = 10 MSPS, D11 = 160 MBPS	-0.27	0.11		
	DCLK rising edge to output data delay, 1-wire series CMOS	Fout = 15 MSPS, D11 = 240 MBPS	-0.52	0.08		
t_{DV}	Data valid, 2-wire serial CMOS	Fout = 10 MSPS, D11/D12 = 80 MBPS	12.19	12.36		ns
	Data valid, 2-wire serial CMOS	Fout = 20 MSPS, D11/D12 = 160 MBPS	5.93	6.1		
	Data valid, 2-wire serial CMOS	Fout = 30 MSPS, D11/D12 = 240 MBPS	3.91	4.07		
	Data valid, 1-wire serial CMOS	Fout = 5 MSPS, D11 = 80 MBPS	12.21	12.39		
	Data valid, 1-wire serial CMOS	Fout = 10 MSPS, D11 = 160 MBPS	5.95	6.1		
	Data valid, 1-wire serial CMOS	Fout = 15 MSPS, D11 = 240 MBPS	3.83	4.08		
SERIAL PROGRAMMING INTERFACE (SCLK, SEN, SDIO) - Input						
$f_{CLK(SCLK)}$	Serial clock frequency				20	MHz
$t_{SU(SEN)}$	SEN to rising edge of SCLK		10			ns
$t_{H(SEN)}$	SEN from rising edge of SCLK		9			ns
$t_{SU(SDIO)}$	SDIO to rising edge of SCLK		17			ns
$t_{H(SDIO)}$	SDIO from rising edge of SCLK		9			ns
SERIAL PROGRAMMING INTERFACE (SDIO) - Output						
$t_{(OZD)}$	SDIO tri-state to driven		3.9		10.8	ns
$t_{(ODZ)}$	SDIO data to tri-state		3.4		14	ns
$t_{(OD)}$	SDIO valid from falling edge of SCLK		3.9		10.8	ns

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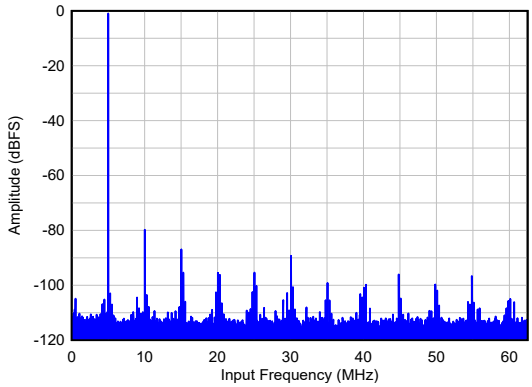
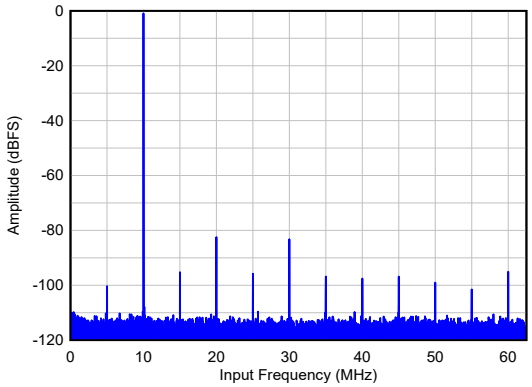
6.9 Typical Characteristics

Typical values at T_A = 25 °C, ADC sampling rate = 125 MSPS, A_{IN} = –1 dBFS differential input, AVDD = IOVDD = 1.8 V, 1.6 V external reference, 5 pF load capacitance, unless otherwise noted.



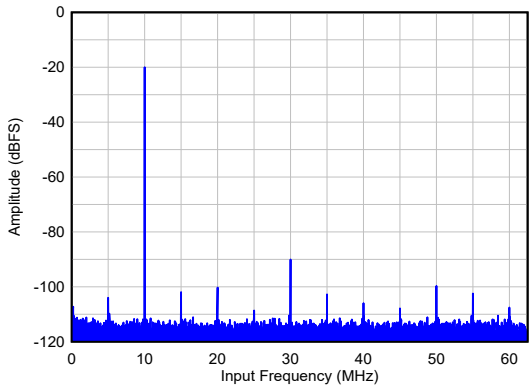
A_{IN} = - 1 dBFS, SNR = 74 dBFS

Figure 6-1. Single Tone FFT at F_{IN} = 5 MHz



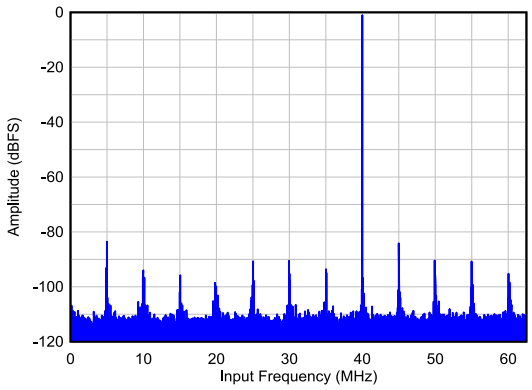
A_{IN} = - 1 dBFS, SNR = 74 dBFS

Figure 6-2. Single Tone FFT at F_{IN} = 10 MHz



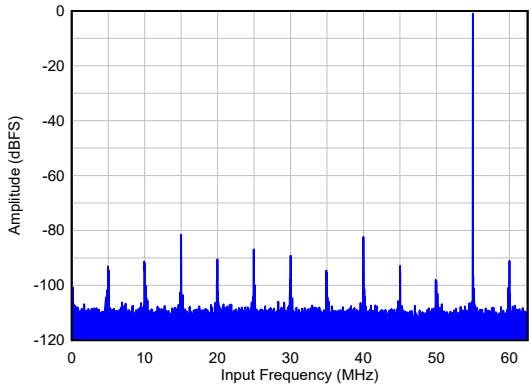
A_{IN} = - 20 dBFS, SNR = 75 dBFS

Figure 6-3. Single Tone FFT at F_{IN} = 10 MHz



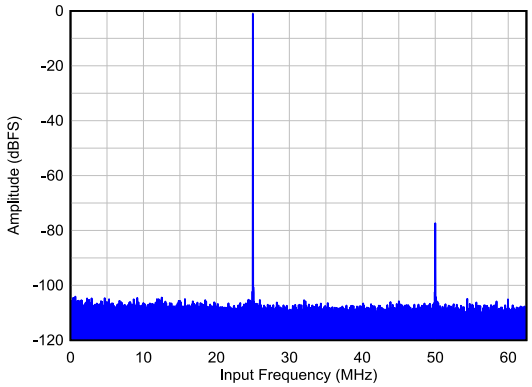
A_{IN} = - 1 dBFS, SNR = 73 dBFS

Figure 6-4. Single Tone FFT at F_{IN} = 40 MHz



A_{IN} = - 1 dBFS, SNR = 70.7 dBFS

Figure 6-5. Single Tone FFT at F_{IN} = 70 MHz



A_{IN} = - 1 dBFS, SNR = 69 dBFS

Figure 6-6. Single Tone FFT at F_{IN} = 100 MHz

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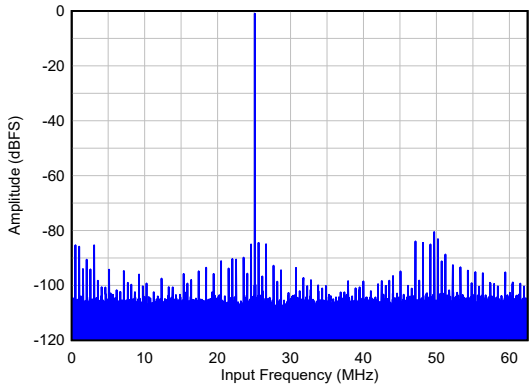
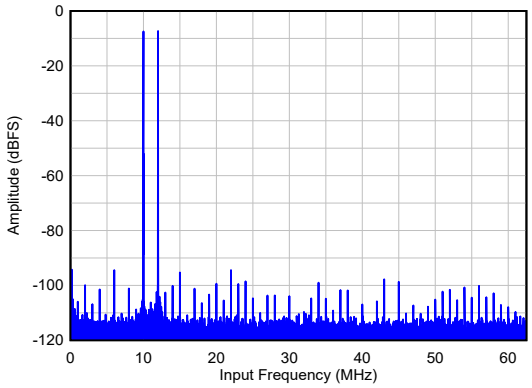


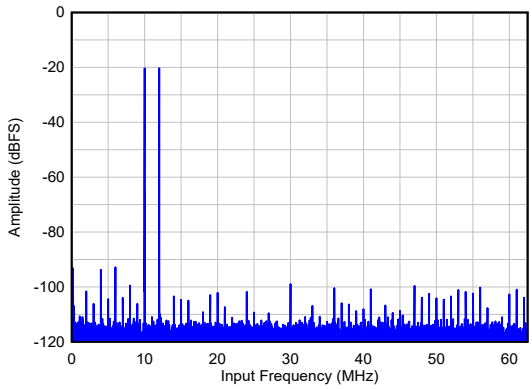
A_{IN} = - 1 dBFS, SNR = 67 dBFS

Figure 6-7. Single Tone FFT at F_{IN} = 150 MHz



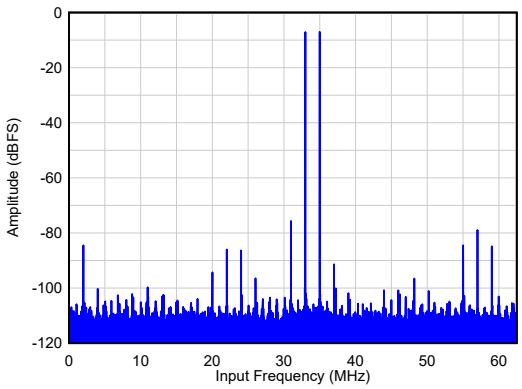
A_{IN} = -7 dBFS, IMD3 = 93 dBc

Figure 6-8. Two Tone FFT at F_{IN} = 10/12 MHz



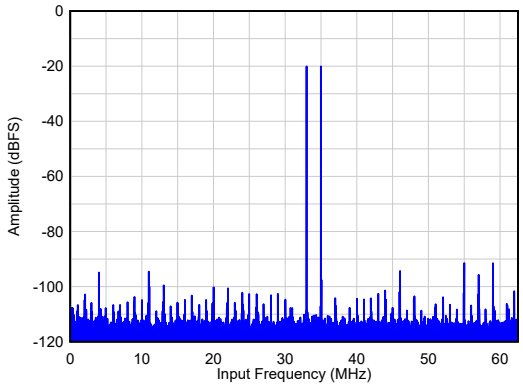
A_{IN} = -20 dBFS, IMD3 = 93 dBc

Figure 6-9. Two Tone FFT at F_{IN} = 10/12 MHz



A_{IN} = -7 dBFS, IMD3 = 72 dBc

Figure 6-10. Two Tone FFT at F_{IN} = 90/92 MHz



A_{IN} = -20 dBFS, IMD3 = 84 dBc

Figure 6-11. Two Tone FFT at F_{IN} = 90/92 MHz

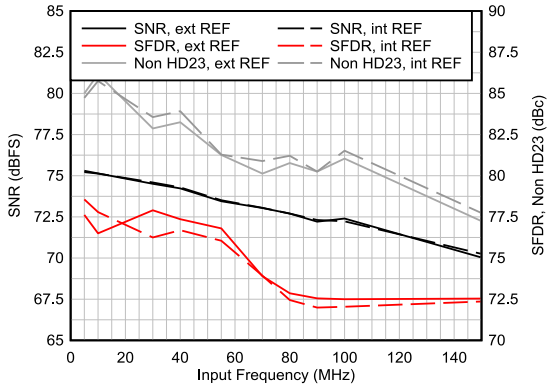


Figure 6-12. AC Performance vs Input Frequency

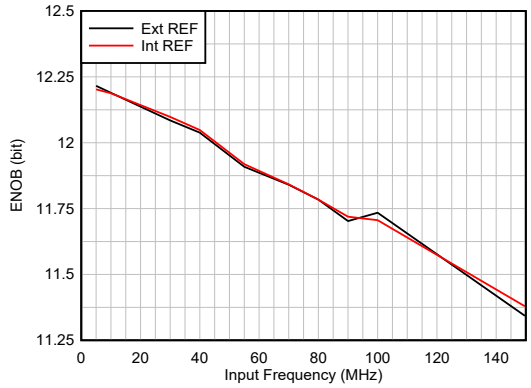
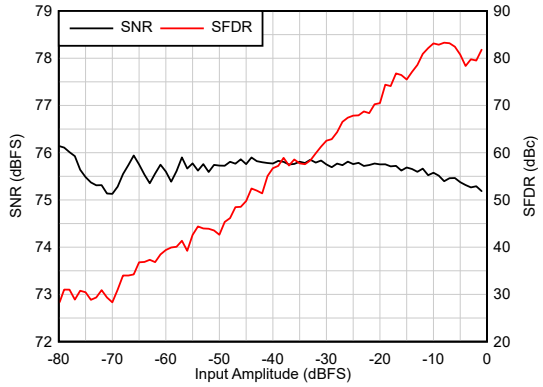
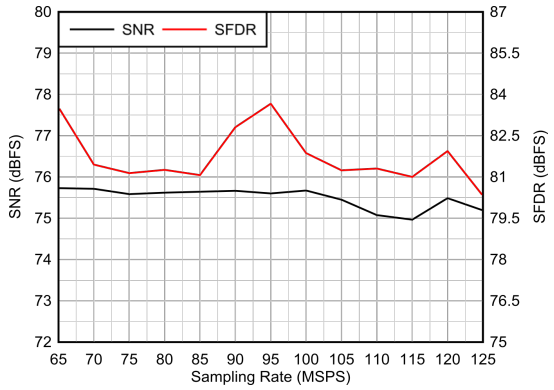


Figure 6-13. ENOB vs Input Frequency



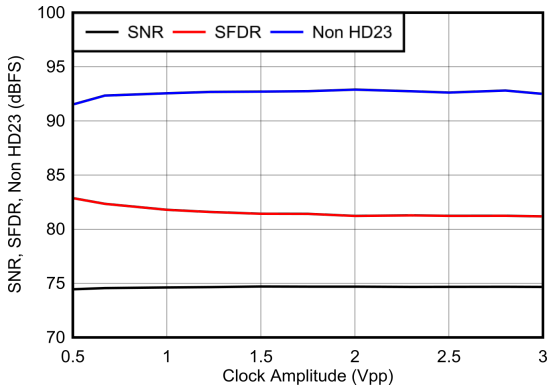
F_{IN} = 5 MHz

Figure 6-14. SNR, SFDR vs Input Amplitude



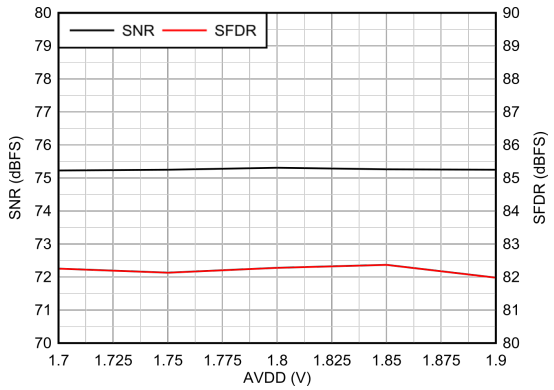
F_{IN} = 5 MHz

Figure 6-15. AC Performance vs Sampling Rate



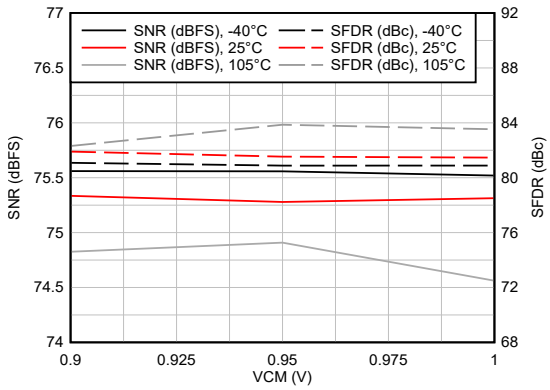
F_{IN} = 5 MHz

Figure 6-16. AC Performance vs Clock Amplitude



F_{IN} = 5 MHz

Figure 6-17. AC Performance vs AVDD



F_{IN} = 5 MHz

Figure 6-18. AC Performance vs VCM vs Temperature

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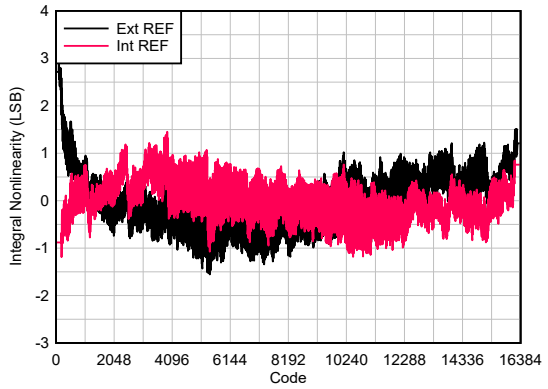
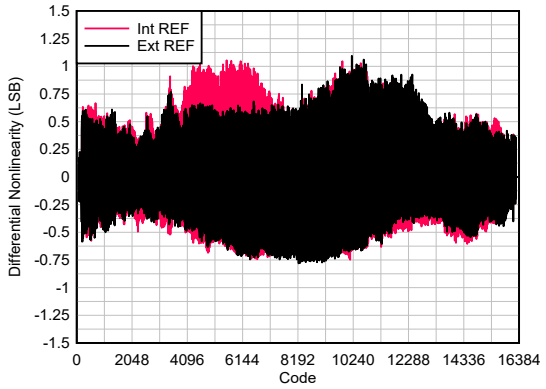


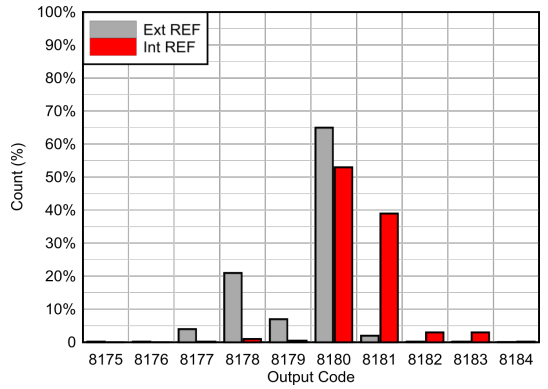
F_{IN} = 5 MHz

Figure 6-19. INL vs Code



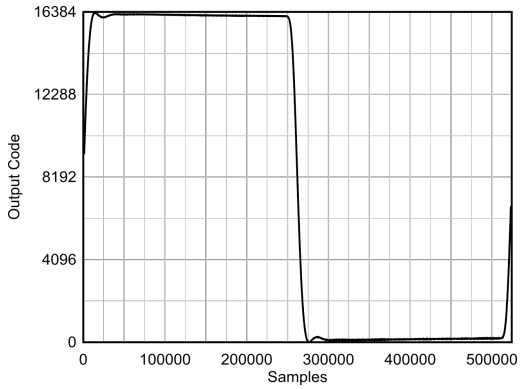
F_{IN} = 5 MHz

Figure 6-20. DNL vs Code



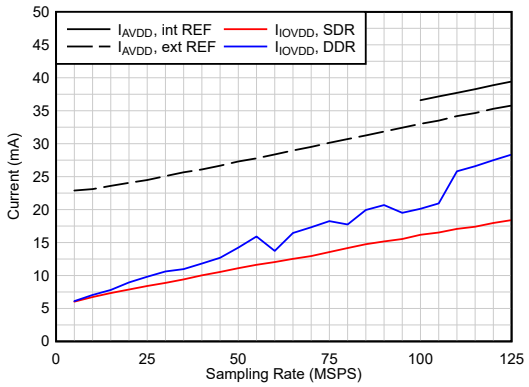
DC Input = +0.95V

Figure 6-21. DC Offset Histogram



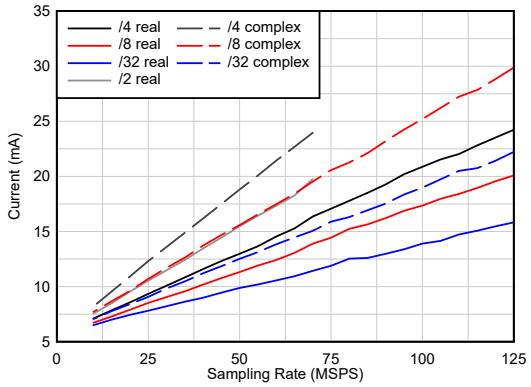
Pulse Input = 1 MHz

Figure 6-22. Two Tone FFT at F_{IN} = 10/12 MHz



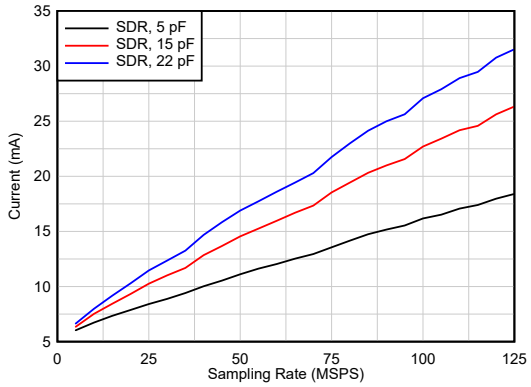
F_{IN} = 1 MHz

Figure 6-23. Current vs Sampling Rate



F_{IN} = 1 MHz, 2-w serial CMOS

Figure 6-24. I_{IOVDD} Current vs Decimation



F_{IN} = 1 MHz, DDR CMOS

Figure 6-25. I_{IOVDD} Current vs Load Capacitance

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7 Parameter Measurement Information

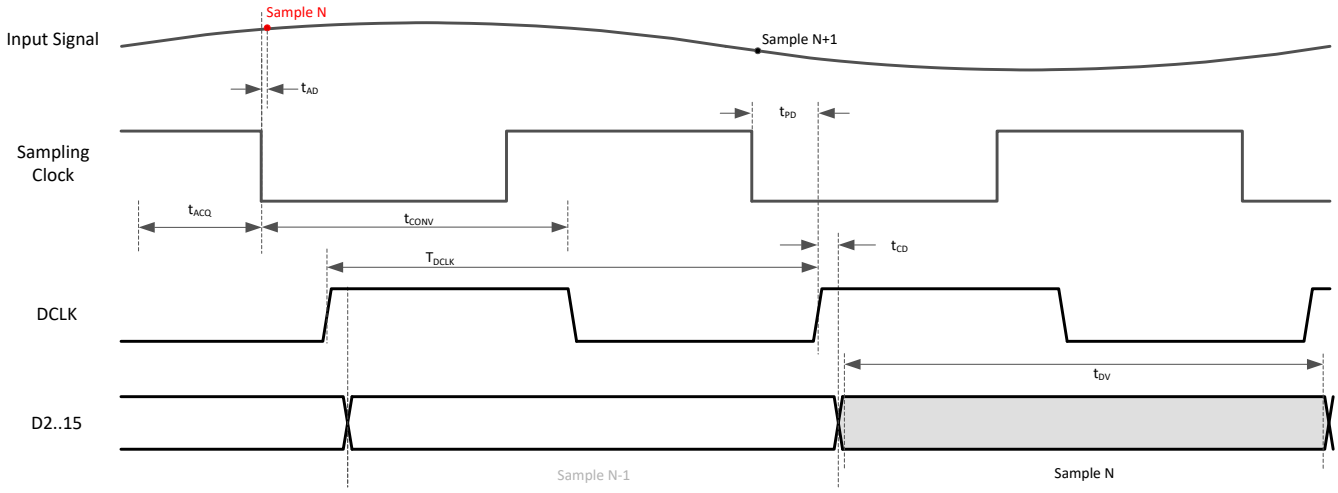

Figure 7-1. Timing Diagram: SDR CMOS

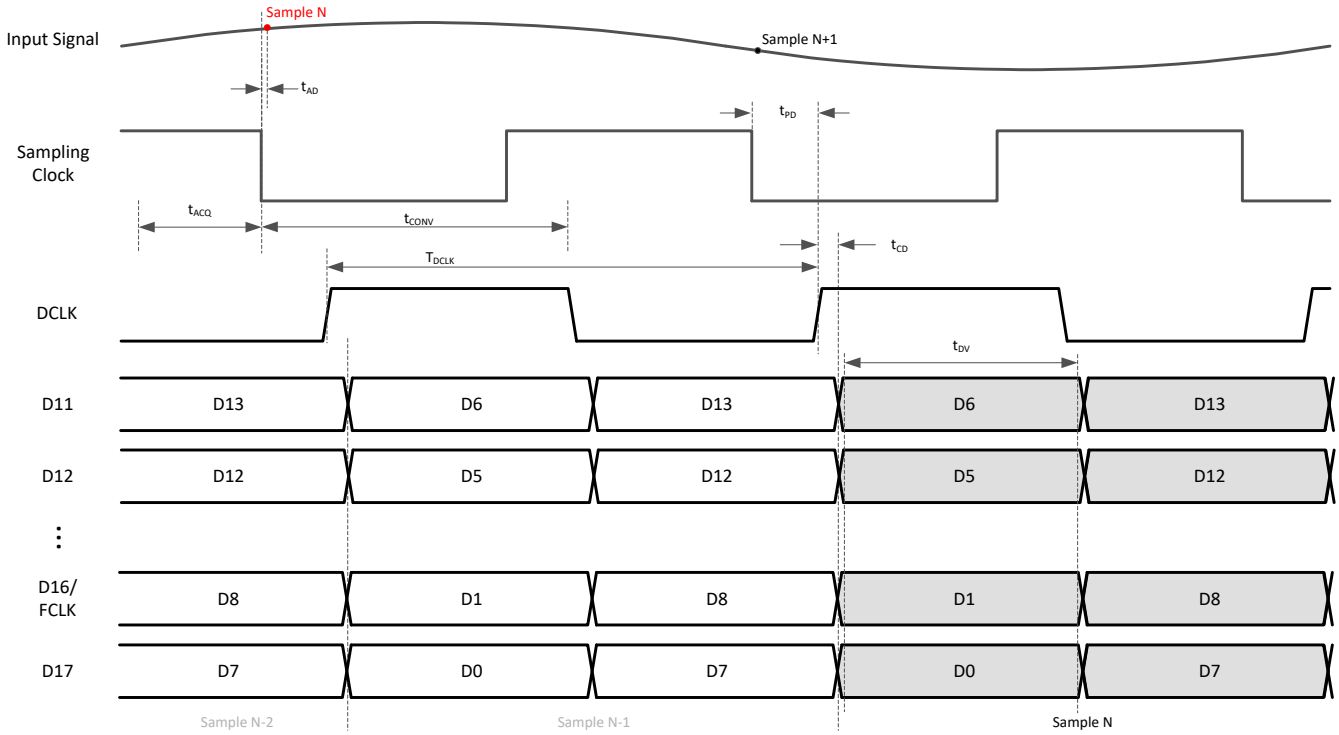

Figure 7-2. Timing Diagram: DDR CMOS (default bit mapper)

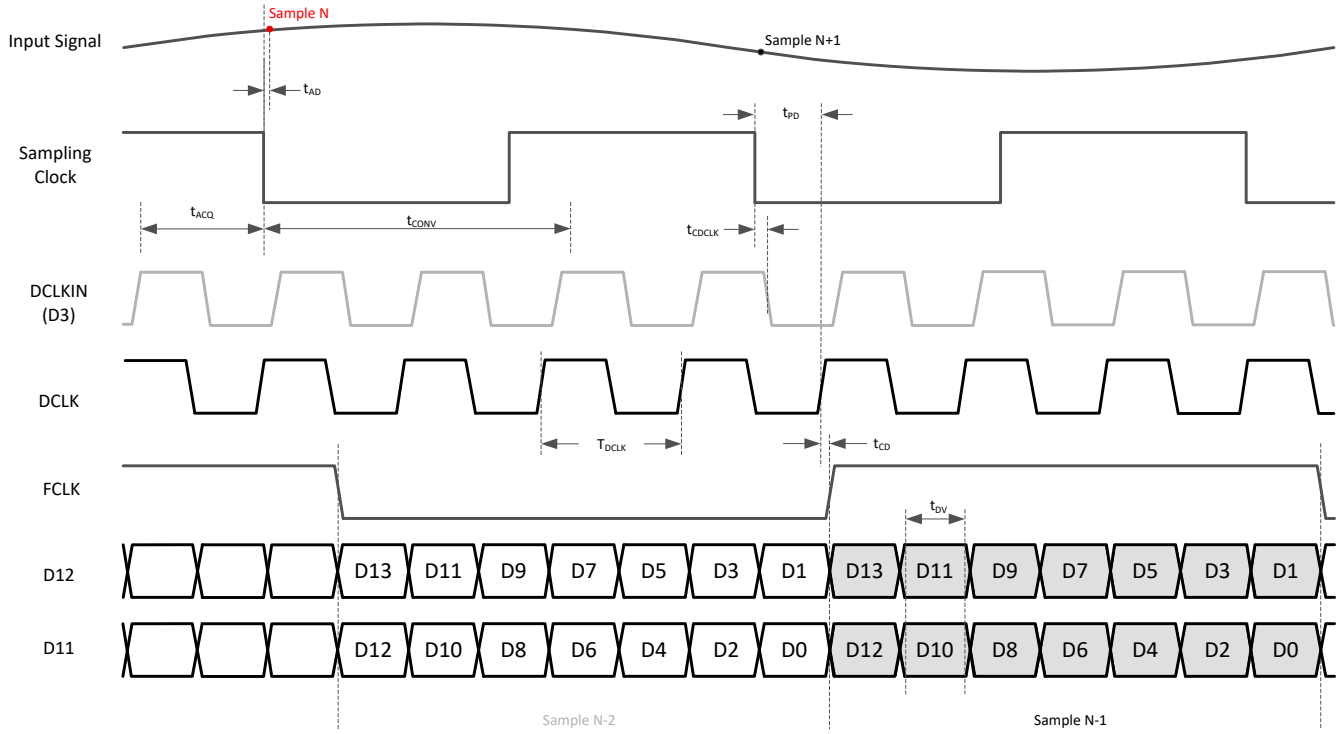

Figure 7-3. Timing Diagram: Serial CMOS 2-wire (default bit mapper)

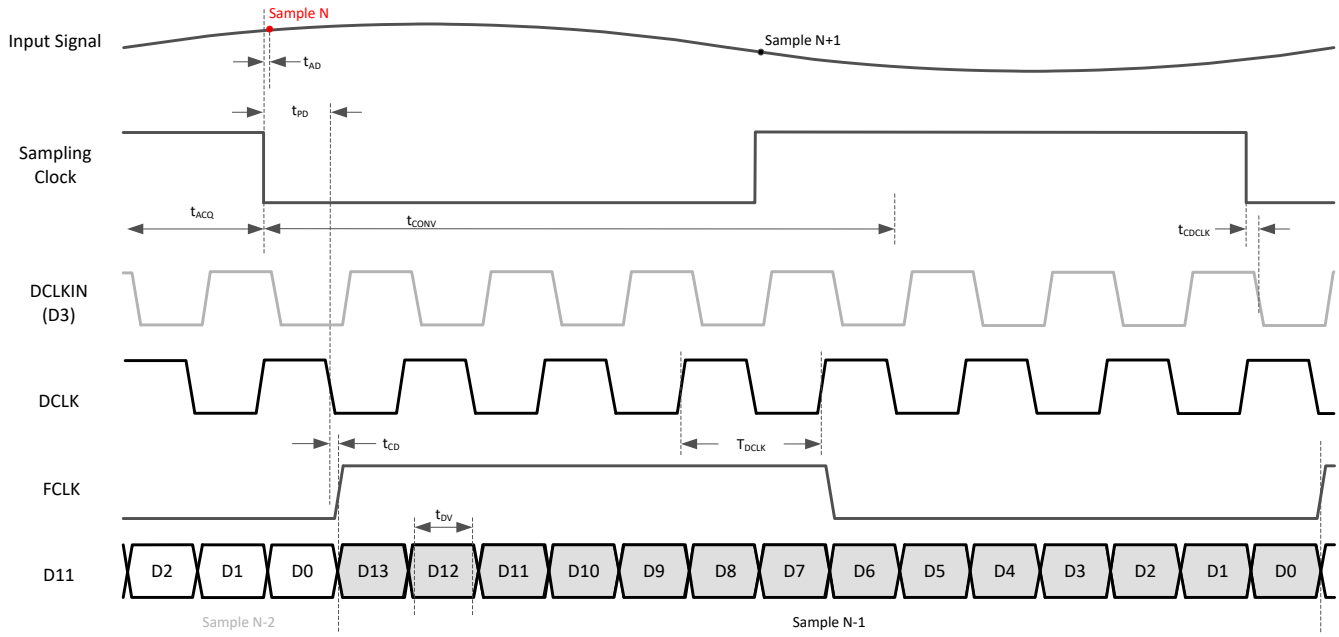

Figure 7-4. Timing Diagram: Serial CMOS 1-wire (default bit mapper)

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8 Detailed Description

8.1 Overview

The ADC3544 is a low noise, ultra-low power 14-bit high-speed ADC supporting sampling rates up to 125 MSPS. It offers good DC precision together with IF sampling support which makes it ideally suited for a wide range of applications. The ADC3544 is equipped with an on-chip internal reference option but it also supports the use of an external, high precision 1.6 V voltage reference or an external 1.2 V reference which is buffered and gained up internally. Because of the inherent low latency architecture, the digital output result is available after only one clock cycle. Single ended as well as differential input signaling is supported.

Note

The ADC3544 supports the following sampling rates:

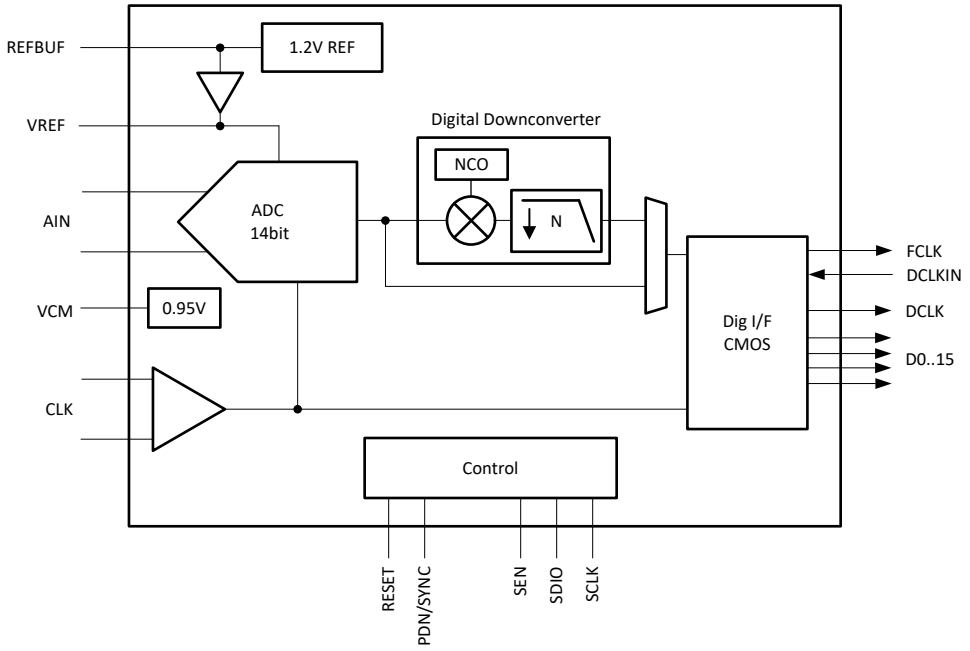
- External Reference: 10 to 125 MSPS
- Internal Reference: 100 to 125 MSPS

An optional programmable digital down converter enables external anti-alias filter relaxation as well as output data rate reduction.

The ADC3544 uses a SDR or DDR as well as a 2-wire or 1-wire serial CMOS interface to output the data offering lowest power digital interface together with the flexibility to minimize the number of digital interconnects. The ADC3544 includes a digital output formatter which supports output resolutions from 14 to 20-bit. The device is a pin-to-pin compatible with different speed grades.

The device features and control options can be set up either through pin configurations or via SPI register writes.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Analog Input

The analog inputs of ADC3544 are intended to be driven differentially. Both AC coupling and DC coupling of the analog inputs is supported. The analog inputs are designed for an input common mode voltage of 0.95 V which must be provided externally on each input pin. DC-coupled input signals must have a common mode voltage that meets the device input common mode voltage range.

The equivalent input network diagram is shown in Figure 8-1. All four sampling switches, on-resistance shown in red, are in same position (open or closed) simultaneously.

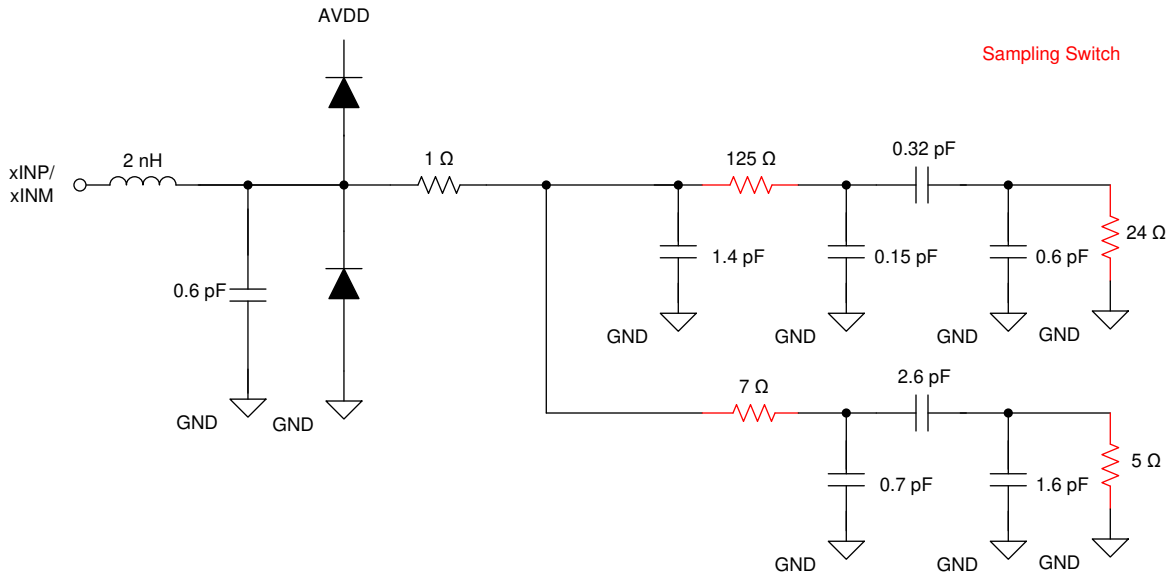


Figure 8-1. Equivalent Input Network: ADC3544

8.3.1.1 Analog Input Bandwidth

Figure 8-2 shows the analog full power input bandwidth of the ADC3544 with a 50 Ω differential termination. The -3 dB bandwidth is approximately 1.4 GHz and the useful input bandwidth with good AC performance is approximately 200 MHz.

The equivalent differential input resistance R_{IN} and input capacitance C_{IN} vs frequency are shown in Figure 8-3.

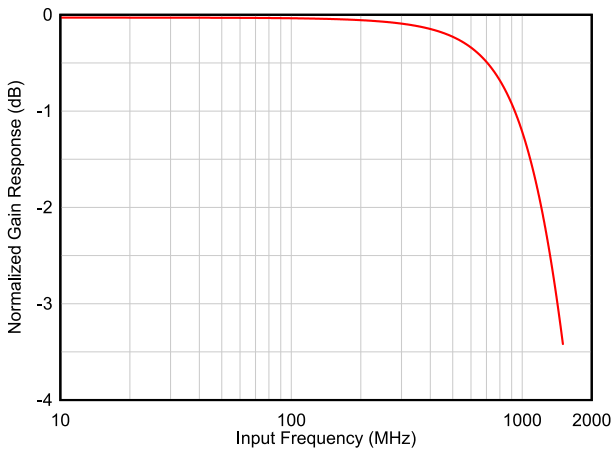


Figure 8-2. ADC Analog Input bandwidth response

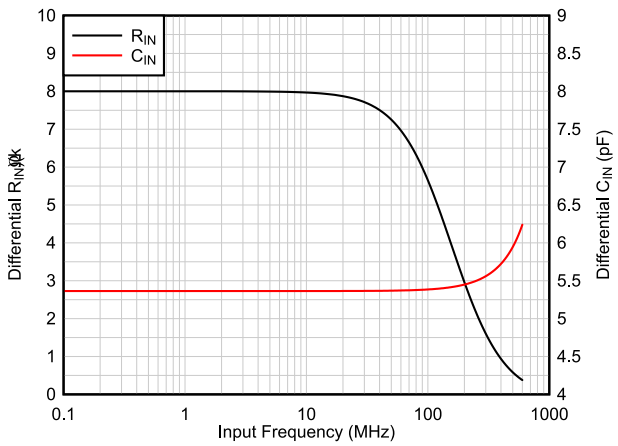


Figure 8-3. Equivalent R_{IN}/C_{IN} vs Input Frequency

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8.3.1.2 Analog Front End Design

The ADC3544 is an unbuffered ADC and thus a passive kick-back filter is recommended to absorb the glitch from the sampling operation. Depending on if the input is driven by a balun or a differential amplifier with low output impedance, a termination network may be needed. Additionally a passive DC bias circuit is needed in AC-coupled applications which can be combined with the termination network.

8.3.1.2.1 Sampling Glitch Filter Design

The front end sampling glitch filter is designed to optimize the SNR and HD3 performance of the ADC. The filter performance is dependent on input frequency and therefore the following filter designs are recommended for different input frequency ranges as shown in Figure 8-4 and Figure 8-5.

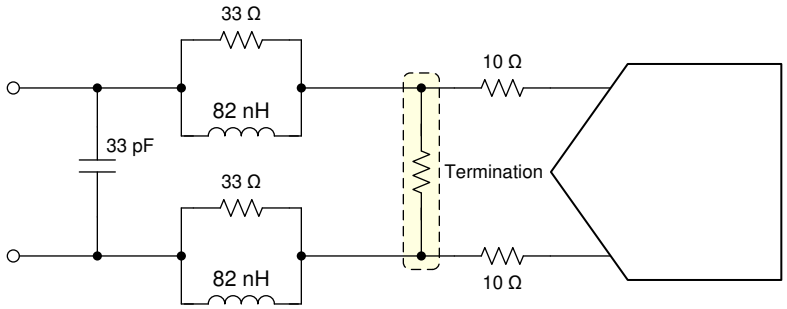

Figure 8-4. Sampling glitch filter example for input frequencies from DC to 60 MHz

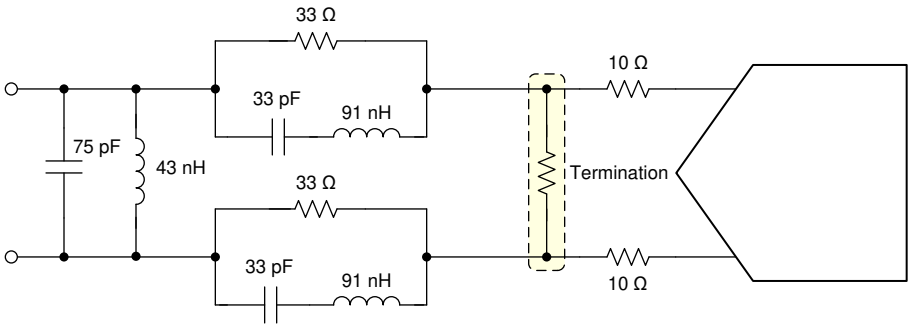

Figure 8-5. Sampling glitch filter example for input frequencies from 60 to 120 MHz

8.3.1.2.2 Single Ended Input

The ADC can be configured to operate with single ended input instead of differential using just the positive signal input. This operating mode must be enabled via SPI register write (address 0x11). The single ended signal is connected to the negative ADC input and both the positive and negative input need to be biased to VCM as shown in Figure 8-6.

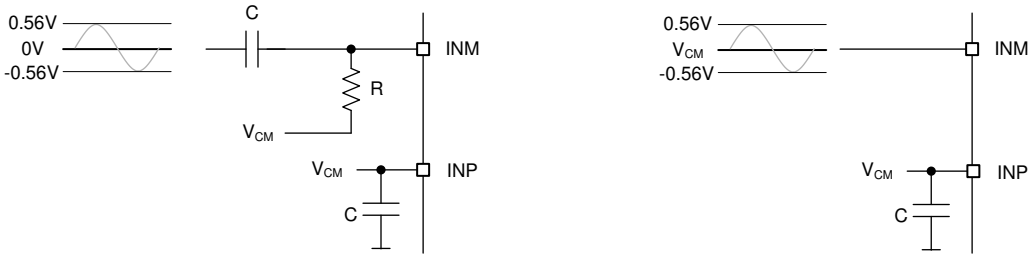

Figure 8-6. Single ended analog input: AC coupled (left) and DC coupled (right)

The signal swing is now reduced by 6-dB (single ended input with 1.125 Vpp vs differential 2.25 Vpp), and the resulting SNR is reduced by 3-dB.

8.3.1.2.3 Analog Input Termination and DC Bias

Depending on the input drive circuitry, a termination network and/or DC biasing needs to be provided.

8.3.1.2.3.1 AC-Coupling

The ADC3544 requires external DC bias using the common mode output voltage (VCM) of the ADC together with the termination network as shown in Figure 8-7. The termination is located within the glitch filter network. When using a balun on the input, the termination impedance has to be adjusted to account for the turns ratio of the transformer. When using an amplifier, the termination impedance can be adjusted to optimize the amplifier performance.

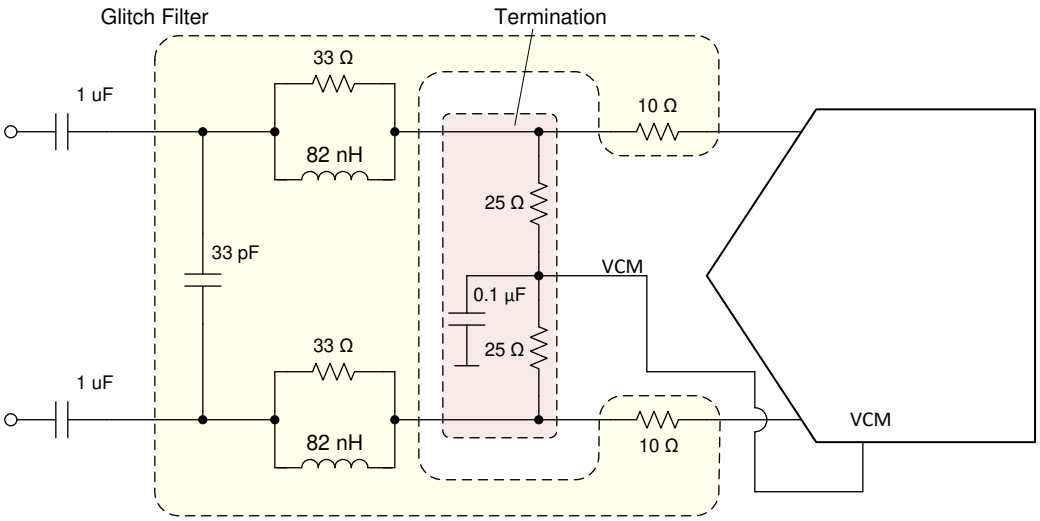

Figure 8-7. AC-Coupling: termination network provides DC bias (glitch filter example for up to 60 MHz)

8.3.1.2.3.2 DC-Coupling

In DC coupled applications the DC bias needs to be provided from the fully differential amplifier (FDA) using VCM output of the ADC as shown in Figure 8-8. The glitch filter in this case is located between the anti-alias filter and the ADC. No termination may be needed if amplifier is located close to the ADC or if the termination is part of the anti-alias filter.

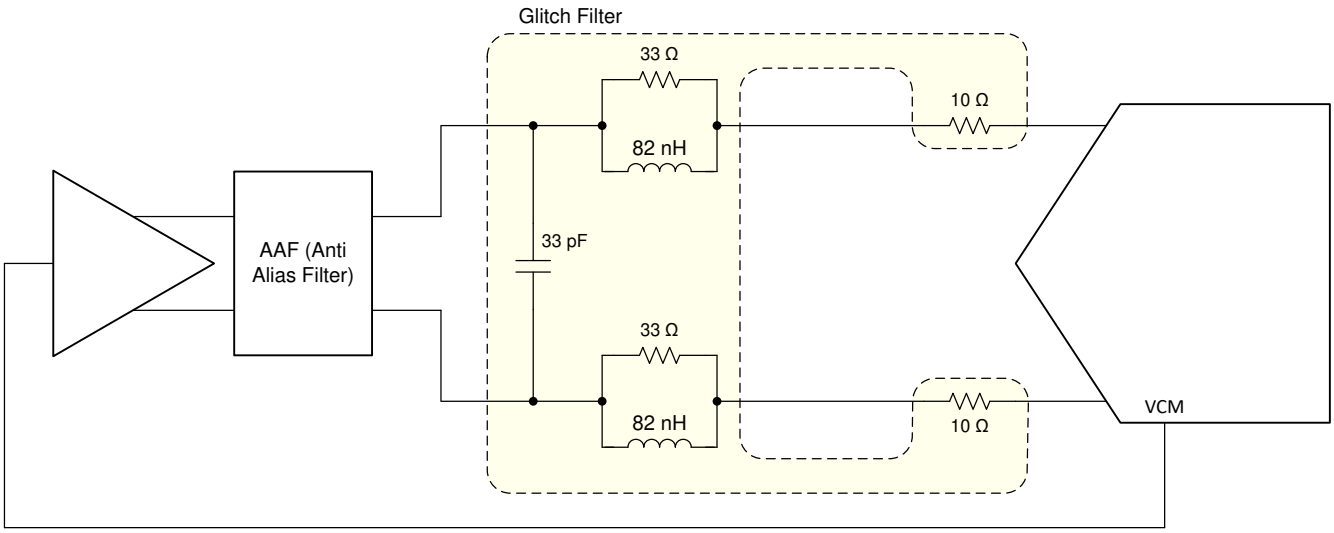

Figure 8-8. DC-Coupling: DC bias provided by FDA (glitch filter example for DC - 60 MHz)

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8.3.2 Clock Input

In order to maximize the ADC SNR performance, the external sampling clock should be low jitter and differential signaling with a high slew rate. This is especially important in IF sampling applications. For less jitter sensitive applications, the ADC3544 provides the option to operate with single ended signaling which saves additional power consumption.

8.3.2.1 Single Ended vs Differential Clock Input

The ADC3544 can be operated using a differential or a single ended clock input where the single ended clock consumes less power consumption. However clock amplitude impacts the ADC aperture jitter and consequently the SNR. For maximum SNR performance, a large clock signal with fast slew rates needs to be provided.

- Differential Clock Input: The clock input can be AC coupled externally. The ADC3544 provides internal biasing for that use case.
- Single Ended Clock Input: This mode needs to be configured using SPI register (0x0E, D2 and D0) or with the REFBUF pin. In this mode there is no internal clock biasing and thus the clock input needs to be DC coupled around a 0.9V center. The unused input needs to be AC coupled to ground.

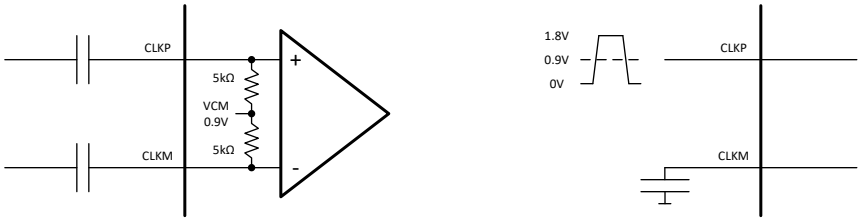

Figure 8-9. External and internal connection using differential (left) and single ended (right) clock input

8.3.3 Voltage Reference

The ADC3544 provides three different options for supplying the voltage reference to the ADC. An external 1.6 V reference can be directly connected to the VREF input; a voltage 1.2 V reference can be connected to the REFBUF input using the internal gain buffer or the internal 1.2V reference can be enabled to generate a 1.6 V reference voltage. For best performance, the reference noise should be filtered by connecting a 10 uF and a 0.1 uF ceramic bypass capacitor to the VREF pin. The internal reference circuitry of the ADC3544 is shown in Figure 8-10.

Note

The voltage reference mode can be selected by using the REFBUF pin as a control pin (Section 8.5.1). If the REFBUF pin is not used for configuration, the REFBUF pin should be connected to AVDD (even though the REFBUF pin has a weak internal pullup to AVDD) and the voltage reference option has to be selected using the SPI interface.

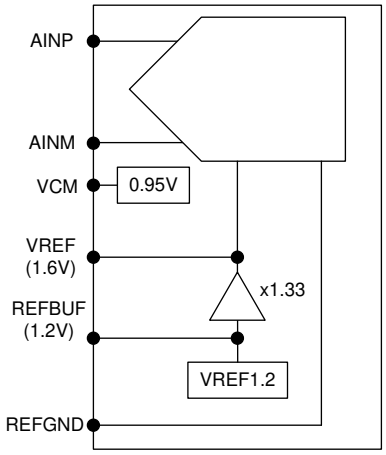

Figure 8-10. Different voltage reference options for ADC3544

8.3.3.1 Internal voltage reference

The 1.6 V reference for the ADC can be generated internal using the on-chip 1.2 V reference along with the internal gain buffer. A 10 uF and a 0.1 uF ceramic bypass capacitor (C_{VREF}) should be connected between the VREF and REFGND pins as close to the pins as possible.

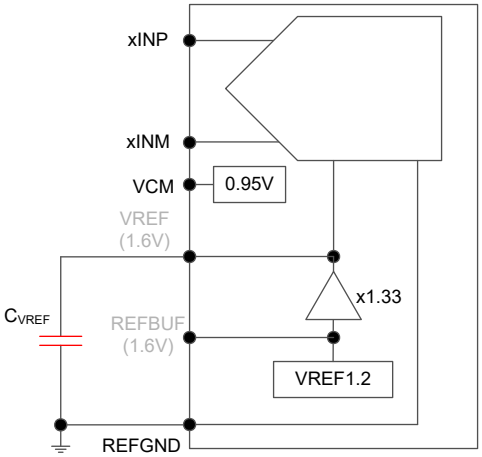

Figure 8-11. Internal reference

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8.3.3.2 External voltage reference (VREF)

For highest accuracy and lowest temperature drift, the VREF input can be directly connected to an external 1.6 V reference. A 10 µF and a 0.1 uF ceramic bypass capacitor (C_{VREF}) connected between the VREF and REFGND pins and placed as close to the pins as possible is recommended. The load current from the external reference is about 1 mA.

Note

The internal reference is also used for other functions inside the device, therefore the reference amplifier should only be powered down in power down state but not during normal operation.

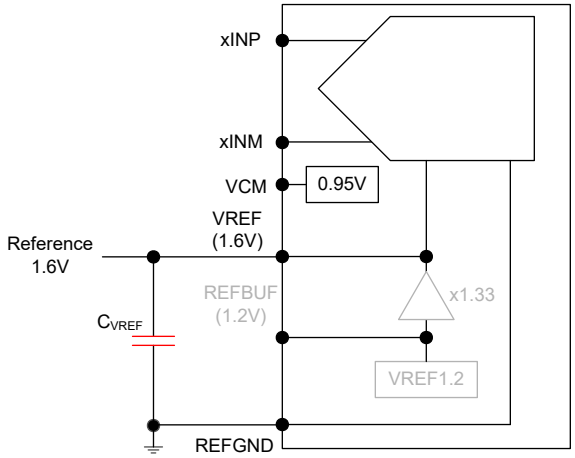

Figure 8-12. External 1.6 V reference

8.3.3.3 External voltage reference with internal buffer (REFBUF)

The ADC3544 is equipped with an on-chip reference buffer that also includes gain to generate the 1.6 V reference voltage from an external 1.2 V reference. A 10 uF and a 0.1 uF ceramic bypass capacitor (C_{VREF}) between the VREF and REFGND pins and a 10 uF and a 0.1 uF ceramic bypass capacitor between the REFBUF and REFGND pins are recommended. Both capacitors should be placed as close to the pins as possible. The load current from the external reference is less than 100 uA.

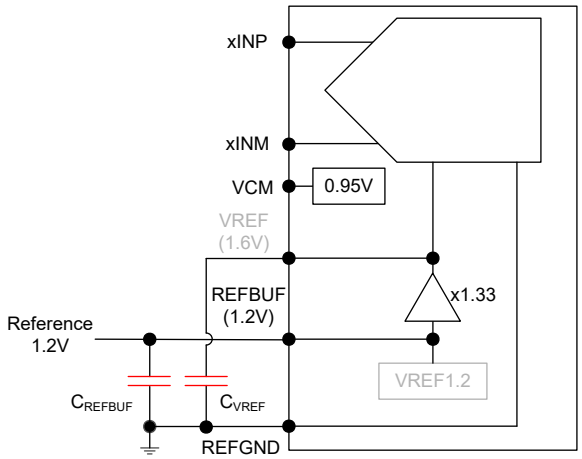

Figure 8-13. External 1.2 V reference using internal reference buffer

8.3.4 Digital Down Converter

The ADC3544 includes an optional on-chip digital down conversion (DDC) decimation filter that can be enabled via SPI register setting. It supports complex decimation by 2, 4, 8, 16 and 32 using a digital mixer and a 32-bit numerically controlled oscillator (NCO) as shown in Figure 8-14. Furthermore it supports a mode with real decimation where the complex mixer is bypassed (NCO should be set to 0 for lowest power consumption) and the digital filter acts as a low pass filter.

Internally the decimation filter calculations are performed with a 20-bit resolution in order to avoid any SNR degradation due to quantization noise. The output formatter Section 8.3.5.4 truncates to the selected resolution prior to outputting the data on the digital interface.

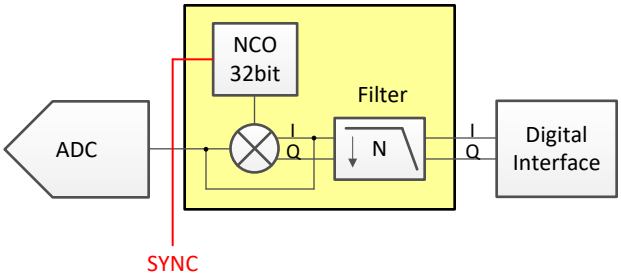

Figure 8-14. Internal Digital Decimation Filter

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8.3.4.1 Digital Filter Operation

The complex decimation operation is illustrated with an example in Figure 8-15. First the input signal (and the negative image) are frequency shifted by the NCO frequency as shown on the left. Next a digital filter is applied (centered around 0 Hz) and the output data rate is decimated - in this example the output data rate $F_{S,OUT}$ = F_S/8 with a Nyquist zone of F_S/16. During the complex mixing the spectrum (signal and noise) is split into real and complex parts and thus the amplitude is reduced by 6-dB. In order to compensate this loss, there is a 6-dB digital gain option in the decimation filter block that can be enabled via SPI write.

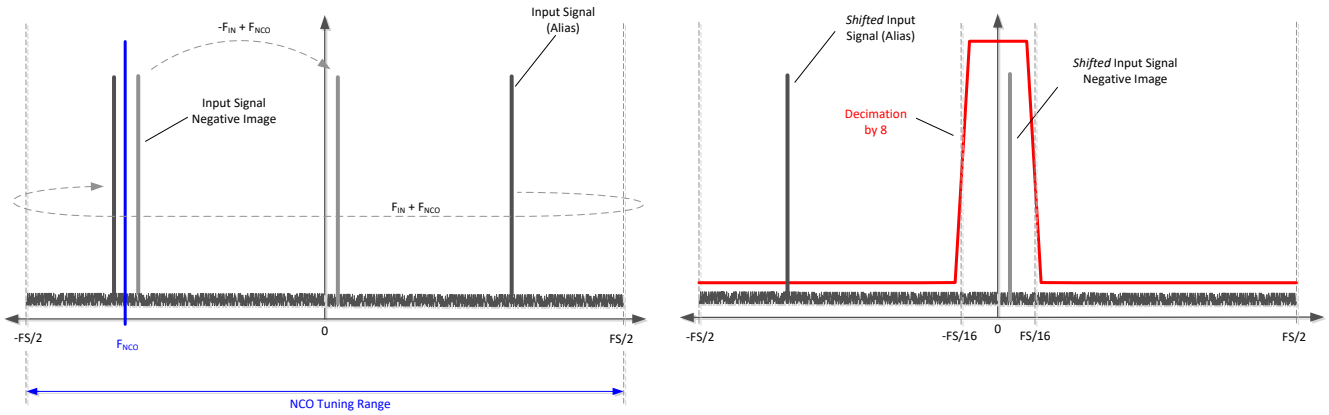

Figure 8-15. Complex decimation illustration

The real decimation operation is illustrated with an example in Figure 8-16. There is no frequency shift happening and only the real portion of the complex digital filter is exercised. The output data rate is decimated - a decimation of 8 would result in an output data rate $F_{S,OUT}$ = F_S/8 with a Nyquist zone of F_S/16.

During the real mixing the spectrum (signal and noise) amplitude is reduced by 3-dB. In order to compensate this loss, there is a 3-dB digital gain option in the decimation filter block that can be enabled via SPI write.

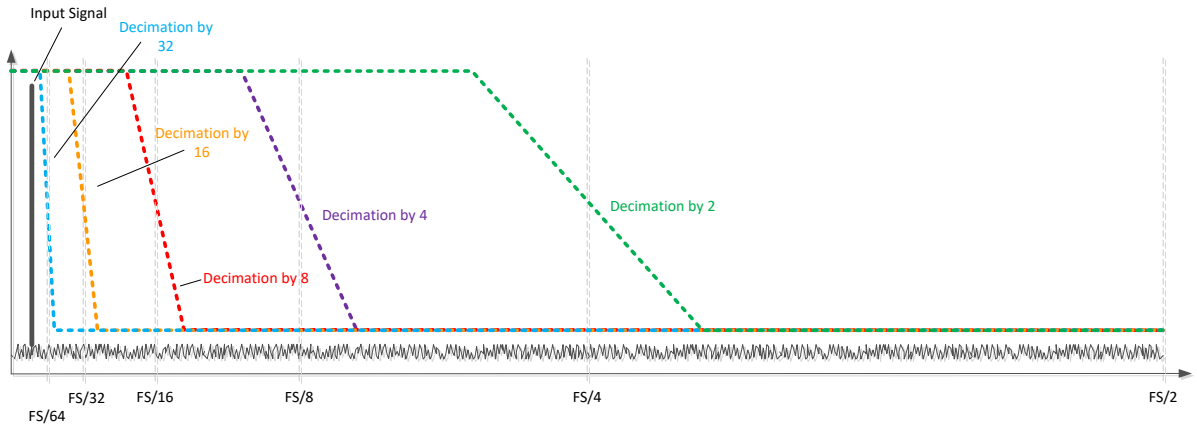

Figure 8-16. Real decimation illustration

8.3.4.2 FS/4 Mixing with Real Output

In this mode, the output after complex decimation gets mixed with FS/4 (FS = output data rate in this case). Instead of a complex output with the input signal centered around 0 Hz, the output is transmitted as a real output at twice the data rate and the signal is centered around FS/4 (Fout/4) as illustrated in Figure 8-17.

In this example, complex decimation by 8 is used. The output data is transmitted as a real output with an output rate of Fout = FS'/4 (FS' = ADC sampling rate). The input signal is now centered around FS/4 (Fout/4) or FS'/16.

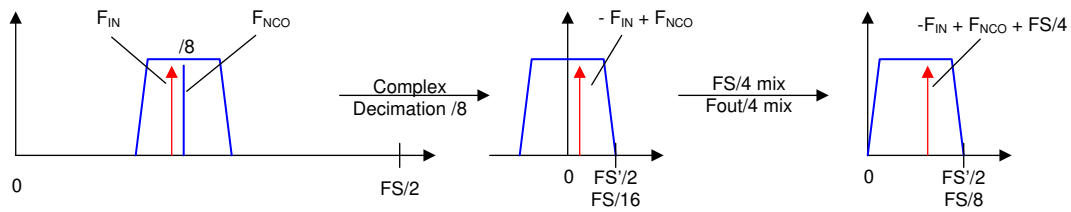

Figure 8-17. FS/4 Mixing with real output

8.3.4.3 Numerically Controlled Oscillator (NCO) and Digital Mixer

The decimation block is equipped with a 32-bit NCO and a digital mixer to fine tune the frequency placement prior to the digital filtering. The oscillator generates a complex exponential sequence of:

$$e^{j\omega n} \text{ (default) or } e^{-j\omega n} \quad (1)$$

where: frequency (ω) is specified as a signed number by the 32-bit register setting

The complex exponential sequence is multiplied with the real input from the ADC to mix the desired carrier to a frequency equal to $f_{IN} + f_{NCO}$. The NCO frequency can be tuned from $-F_S/2$ to $+F_S/2$ and is processed as a signed, 2s complement number. After programming a new NCO frequency, the MIXER RESTART register bit or SYNC pin has to be toggled for the new frequency to get active. Additionally the ADC3544 provides the option via SPI to invert the mixer phase.

The NCO frequency setting is set by the 32-bit register value given and calculated as:

$$\text{NCO frequency} = 0 \text{ to } + F_S/2\text{: NCO} = f_{NCO} \times 2^{32} / F_S \quad (2)$$

$$\text{NCO frequency} = -F_S/2 \text{ to } 0\text{: NCO} = (f_{NCO} + F_S) \times 2^{32} / F_S \quad (3)$$

where:

- NCO = NCO register setting (decimal value)
- f_{NCO} = Desired NCO frequency (MHz)
- F_S = ADC sampling rate (MSPS)

The NCO programming is further illustrated with this example:

- ADC sampling rate F_S = 125 MSPS
- Input signal f_{IN} = 10 MHz
- Desired output frequency f_{OUT} = 0 MHz

For this example there are actually four ways to program the NCO and achieve the desired output frequency as shown in Table 8-1.

Table 8-1. NCO value calculations example

Alias or negative image	f_{NCO}	NCO Value	Mixer Phase	Frequency translation for f_{OUT}
f_{IN} = –10 MHz	f_{NCO} = 10 MHz	343597384	as is	$f_{OUT} = f_{IN} + f_{NCO}$ = –10 MHz +10 MHz = 0 MHz
f_{IN} = 10 MHz	f_{NCO} = –10 MHz	373475417		$f_{OUT} = f_{IN} + f_{NCO}$ = 10 MHz + (–10 MHz) = 0 MHz
f_{IN} = 10 MHz	f_{NCO} = 10 MHz	343597384	inverted	$f_{OUT} = f_{IN} - f_{NCO}$ = 10 MHz – 10 MHz = 0 MHz
f_{IN} = –10 MHz	f_{NCO} = –10 MHz	373475417		$f_{OUT} = f_{IN} - f_{NCO}$ = –10 MHz – (–10 MHz) = 0 MHz

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8.3.4.4 Decimation Filter

The ADC3544 supports complex decimation by 2, 4, 8, 16 and 32 with a pass-band bandwidth of ~ 80% and a stopband rejection of at least 85 dB. Table 8-2 gives an overview of the pass-band bandwidth of the different decimation settings with respect to ADC sampling rate F_S. In real decimation mode the output bandwidth is half of the complex bandwidth.

Table 8-2. Decimation Filter Summary and Maximum Available Output Bandwidth

REAL/COMPLEX DECIMATION	DECIMATION SETTING N	OUTPUT RATE	OUTPUT BANDWIDTH	OUTPUT RATE (F_S = 125 MSPS)	OUTPUT BANDWIDTH (F_S = 125 MSPS)
Complex	2	F_S / 2 complex	0.8 × F_S / 2	62.5 MSPS complex	50 MHz
	4	F_S / 4 complex	0.8 × F_S / 4	31.25 MSPS complex	25 MHz
	8	F_S / 8 complex	0.8 × F_S / 8	15.625 MSPS complex	12.5 MHz
	16	F_S / 16 complex	0.8 × F_S / 16	7.8125 MSPS complex	6.25 MHz
	32	F_S / 32 complex	0.8 × F_S / 32	3.90625 MSPS complex	3.125 MHz
Real	2	F_S / 2 real	0.4 × F_S / 2	62.5 MSPS	25 MHz
	4	F_S / 4 real	0.4 × F_S / 4	31.25 MSPS	12.5 MHz
	8	F_S / 8 real	0.4 × F_S / 8	15.625 MSPS	6.25 MHz
	16	F_S / 16 real	0.4 × F_S / 16	7.8125 MSPS	3.125 MHz
	32	F_S / 32 real	0.4 × F_S / 32	3.90625 MSPS	1.5625 MHz

The decimation filter responses are normalized to the ADC sampling clock frequency F_S and illustrated in Figure 8-19 to Figure 8-28. They are interpreted as follows:

Each figure contains the filter pass-band, transition band(s) and alias or stop-band(s) as shown in Figure 8-18. The x-axis shows the offset frequency (after the NCO frequency shift) normalized to the ADC sampling rate F_S.

For example, in the divide-by-4 complex setup, the output data rate is F_S / 4 complex with a Nyquist zone of F_S / 8 or 0.125 × F_S. The transition band (colored in blue) is centered around 0.125 × F_S and the alias transition band is centered at 0.375 × F_S. The stop-bands (colored in red), which alias on top of the pass-band, are centered at 0.25 × F_S and 0.5 × F_S. The stop-band attenuation is greater than 85 dB.

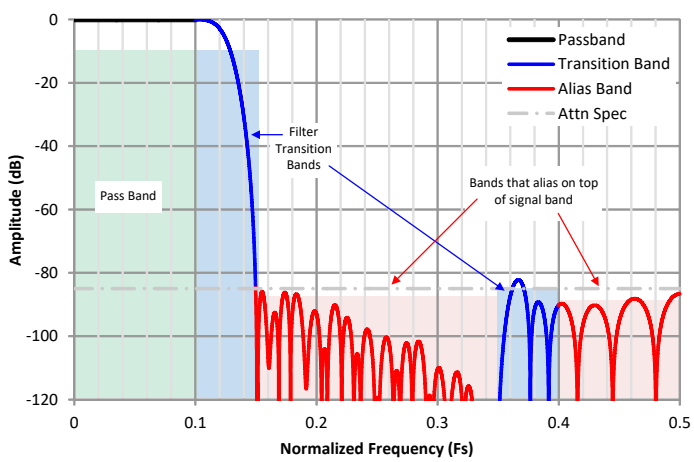

Figure 8-18. Interpretation of the Decimation Filter Plots

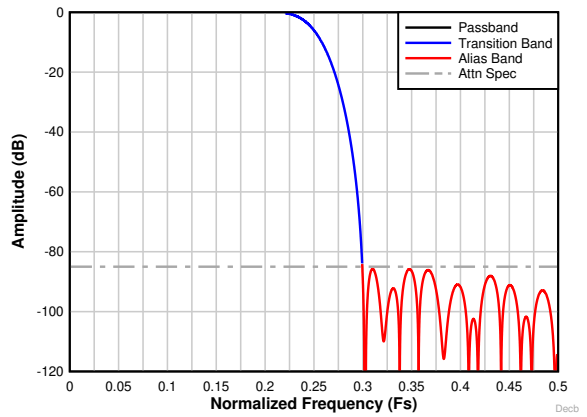

Figure 8-19. Decimation by 2 complex frequency response

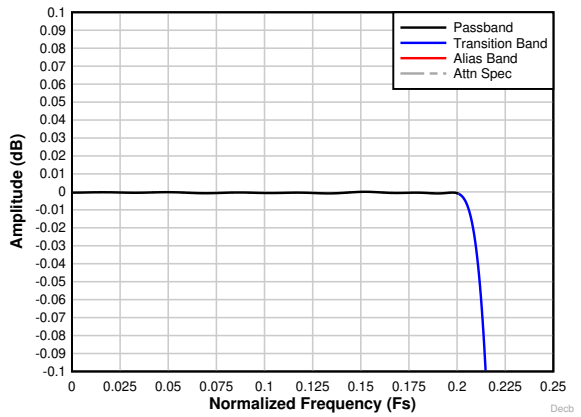

Figure 8-20. Decimation by 2 complex passband ripple response

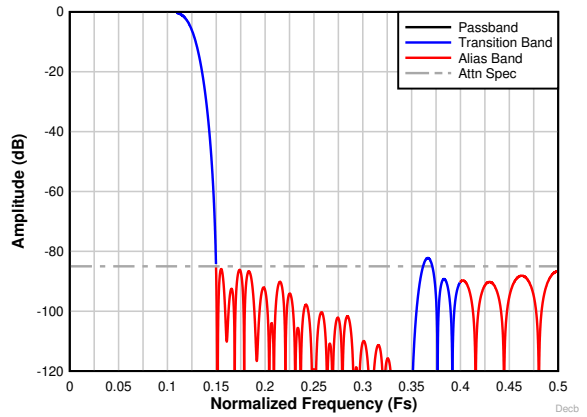

Figure 8-21. Decimation by 4 complex frequency response

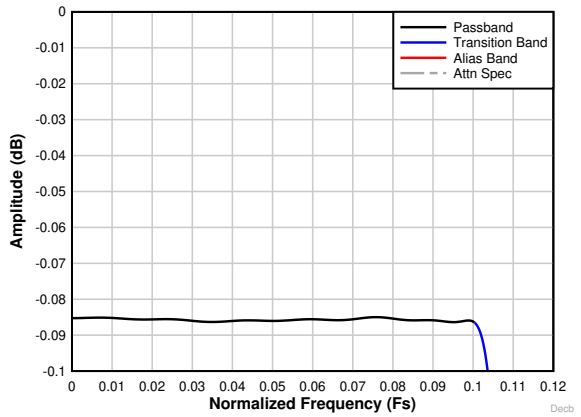

Figure 8-22. Decimation by 4 complex passband ripple response

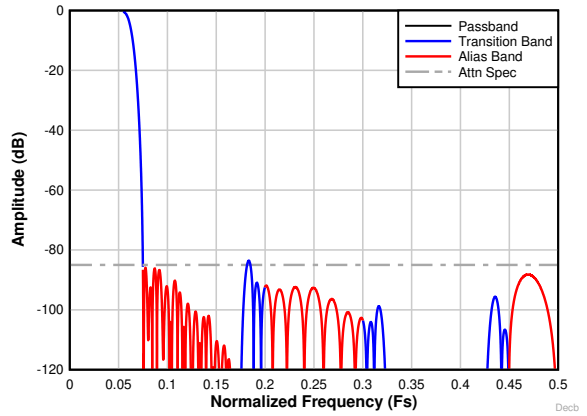

Figure 8-23. Decimation by 8 complex frequency response

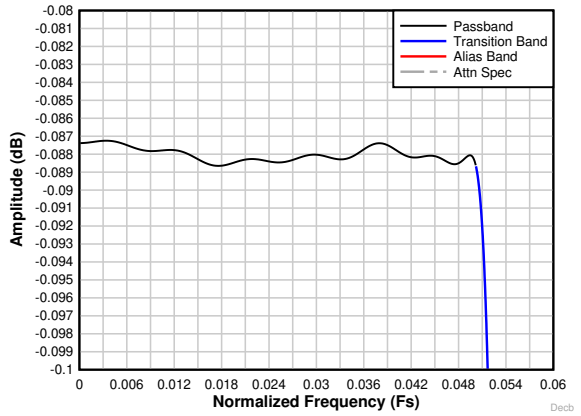

Figure 8-24. Decimation by 8 complex passband ripple response

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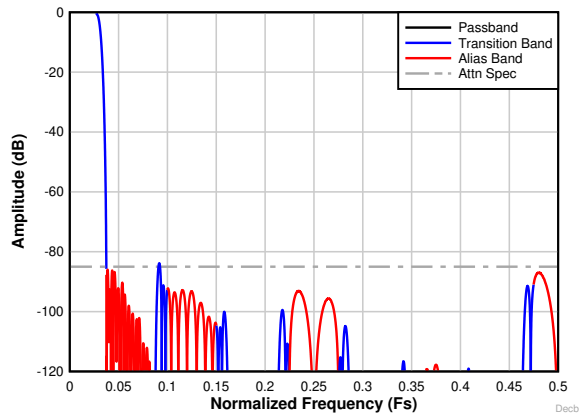

Figure 8-25. Decimation by 16 complex frequency response

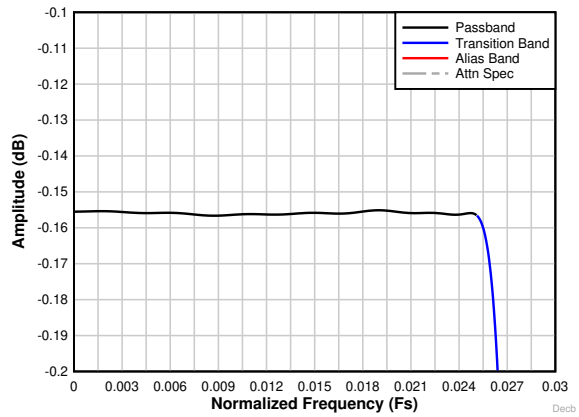

Figure 8-26. Decimation by 16 complex passband ripple response

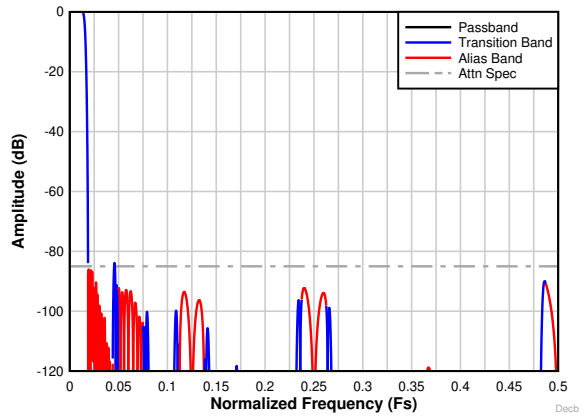

Figure 8-27. Decimation by 32 complex frequency response

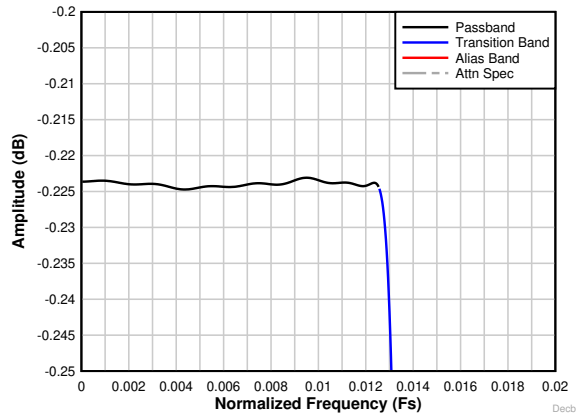

Figure 8-28. Decimation by 32 complex passband ripple response

8.3.4.5 SYNC

The PDN/SYNC pin can be used to synchronize multiple devices using an external SYNC signal. The PDN/SYNC pin can be configured via SPI (SYNC EN bit) from power down to synchronization functionality and is latched in by the rising edge of the sampling clock as shown in Figure 8-29.

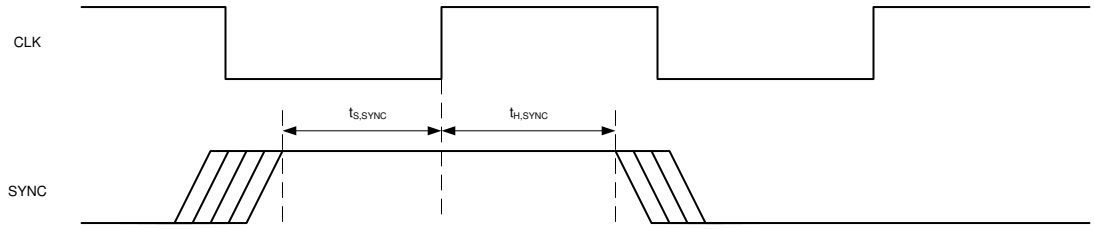

Figure 8-29. External SYNC timing diagram

The synchronization signal is only required when using the decimation filter - either using the SPI SYNC register or the PDN/SYNC pin. It resets internal clock dividers used in the decimation filter and aligns the internal clocks as well as I and Q data within the same sample. If no SYNC signal is given the internal clock dividers will not be synchronized, which can lead to a fractional delay across different devices. The SYNC signal also resets the NCO phase and loads the new NCO frequency (same as the MIXER RESTART bit).

When trying to resynchronize during operation, the SYNC toggle should occur at 64*K clock cycles, where K is an integer. This ensures phase continuity of the clock divider.

8.3.4.6 Output Formatting with Decimation

8.3.4.6.1 Parallel CMOS

In parallel CMOS mode, the ADC3544 device supports complex decimation output with DDR CMOS interface and real output with SDR and DDR CMOS interface as shown in Figure 8-30 (complex decimation) and Figure 8-31 (real decimation). In this illustration the output format is selected to 16-bit.

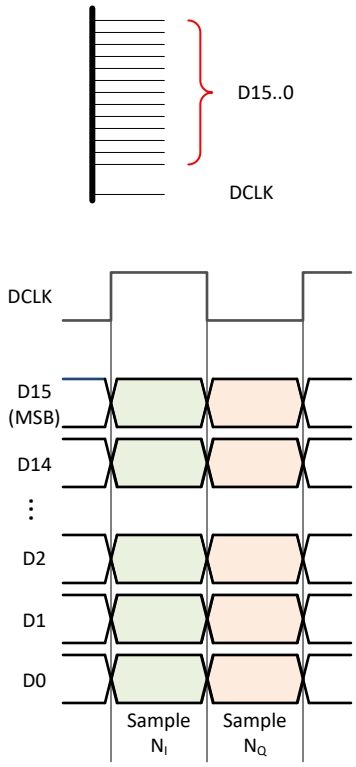

Figure 8-30. Output Data Format in Complex Decimation

Table 8-3 illustrates the output interface data rate along with the corresponding DCLK frequency based on complex decimation setting (N).

Furthermore the table shows an actual lane rate example with complex decimation by 4.

Table 8-3. Parallel CMOS Data Rate Examples with Complex Decimation

REAL/COMPLEX DECIMATION	DECIMATION SETTING	ADC SAMPLING RATE	DCLK	DOUT (MHz)
Complex	N	F_S	F_S x 2 / N	F_S x 4 / N
	4	125 MHz	62.5 MHz	125 MHz

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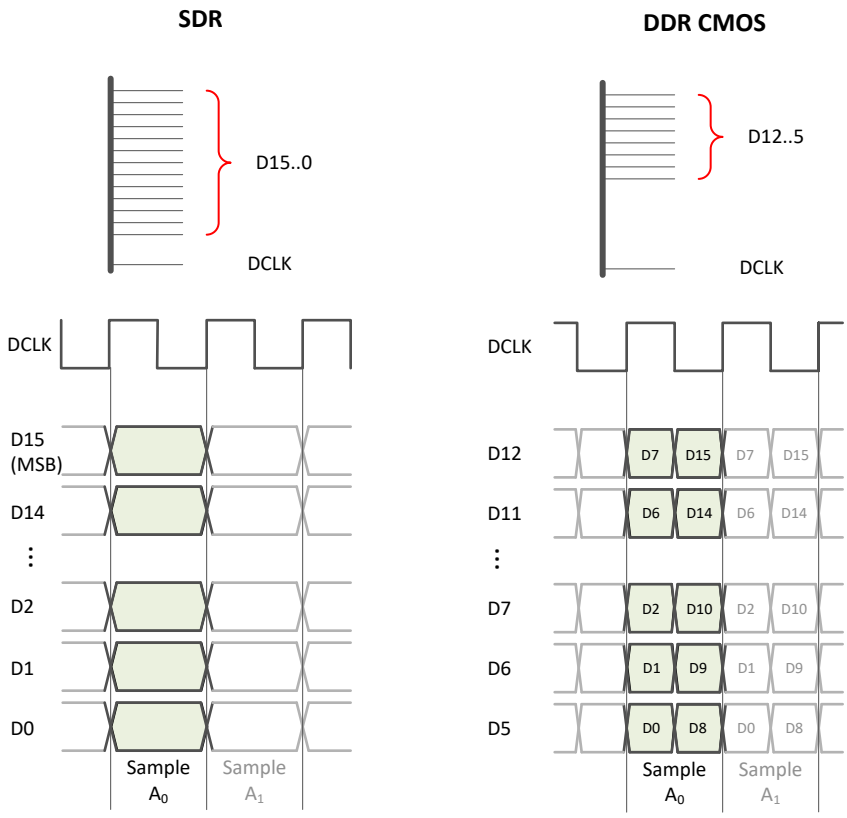

Figure 8-31. Output Data Format in Real Decimation

Table 8-4 illustrates the output interface data rate along with the corresponding DCLK frequency based on real decimation setting (M).

Furthermore the table shows an actual lane rate example with complex decimation by 4.

Table 8-4. Parallel CMOS Data Rate Examples with Decimation

REAL/COMPLEX DECIMATION	DECIMATION SETTING	ADC SAMPLING RATE	SDR/DDR CMOS	DCLK	DOUT
Real	M	F_S	SDR	F_S / M	F_S / M
			DDR		F_S x 2 / M
	4	125 MHz	SDR	31.25 MHz	31.25 MHz
			DDR		62.5 MHz

8.3.4.6.2 Serialized CMOS Interface

In serialized CMOS mode, the ADC3544 device supports complex decimation output Figure 8-32 and real decimation output Figure 8-33. The examples are shown for 16-bit output for 2-wire (8x serialization) and 1-wire (16x serialization).

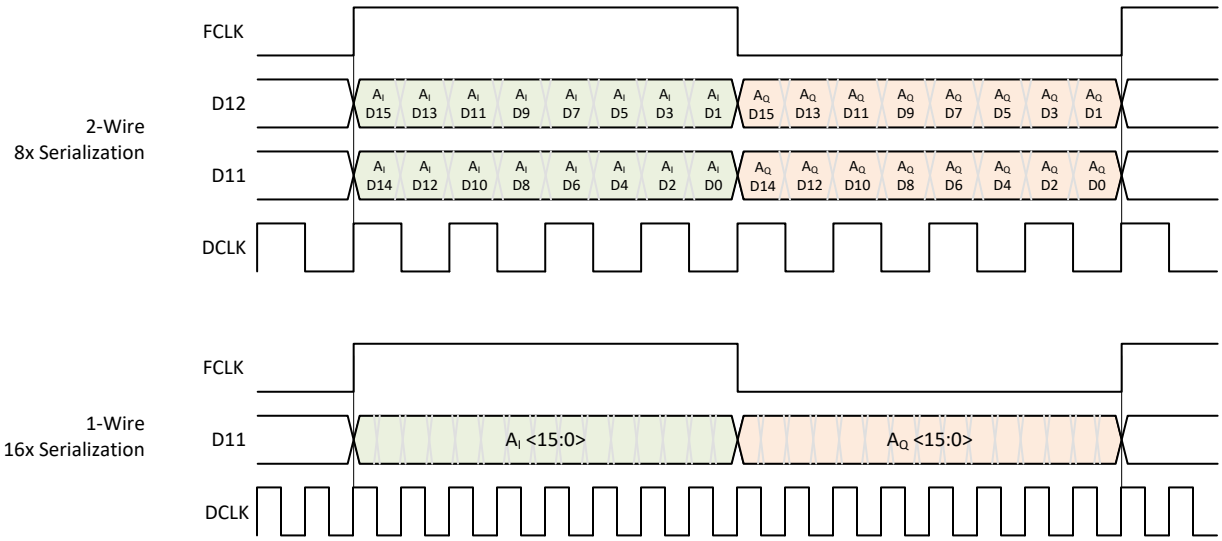

Figure 8-32. Output Data Format in Complex Decimation

Table 8-5 illustrates the output interface data rate along with the corresponding DCLK/DCLKIN and FCLK frequencies based on output resolution (R), number of serial CMOS lanes (L) and complex decimation setting (N).

Furthermore the table shows an actual lane rate example for the 2-, 1- and 1/2-wire interface, 16-bit output resolution and complex decimation by 16.

Table 8-5. Serial CMOS Lane Rate Examples with Complex Decimation and 16-bit Output Resolution

DECIMATION SETTING	ADC SAMPLING RATE	OUTPUT RESOLUTION	# of WIRES	FCLK	DCLKIN, DCLK	DOUT
N	F_S	R	L	F_S / N	[DOUT] / 2	F_S x 2 x R / L / N
16	125 MSPS	16	2	7.8125 MHz	62.5 MHz	125 MHz
			1		125 MHz	250 MHz
	62.5 MSPS		1/2	3.90625 MHz	125 MHz	250 MHz

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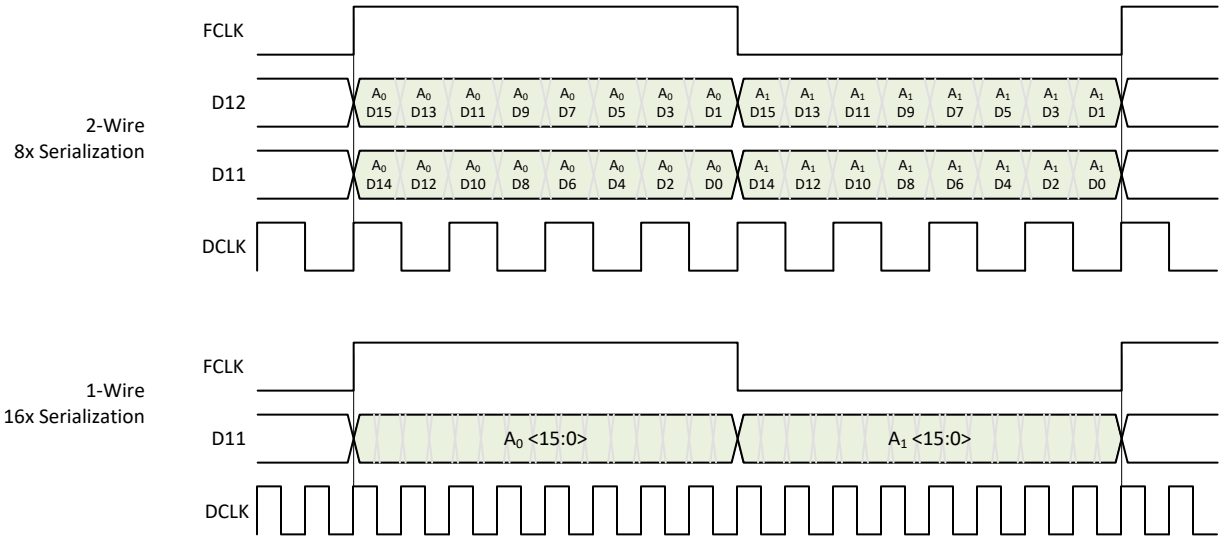

Figure 8-33. Output Data Format in Real Decimation

Table 8-6 illustrates the output interface data rate along with the corresponding DCLK/DCLKIN and FCLK frequencies based on output resolution (R), number of serial CMOS lanes (L) and real decimation setting (M).

Furthermore the table shows an actual lane rate example for the 2- and 1-wire interface, 16-bit output resolution and real decimation by 16.

Table 8-6. Serial CMOS Lane Rate Examples with Real Decimation and 16-bit Output Resolution

DECIMATION SETTING	ADC SAMPLING RATE	OUTPUT RESOLUTION	# of WIRES	FCLK	DCLKIN, DCLK	DOUT
M	F_S	R	L	F_S / M / 2 (L = 2) F_S / M (L = 1)	[DOUT] / 2	F_S x R / L / M
16	125 MSPS	16	2	3.90625 MHz	31.25 MHz	62.5 MHz
			1	7.8125 MHz	62.5 MHz	125 MHz

8.3.5 Digital Interface

The ADC3544 family supports two different CMOS output modes - parallel SDR/DDR output and serialized CMOS output formats.

8.3.5.1 Parallel CMOS Output

The low power CMOS interface supports single data rate (SDR) and double data rate (DDR) output options. In SDR and DDR output mode the output clock is generated inside the ADC3544. The different interface options are configured using SPI register writes.

8.3.5.2 Serialized CMOS output

In this mode the output data is serialized and transmitted over 2 or 1 wires. Due to CMOS output speed limitation this mode is only available for reduced output data rates. This mode is similar to the multi-SPI interface.

8.3.5.2.1 SDR Output Clocking

The ADC3544 provides a SDR output clocking option for all serial CMOS output modes (including decimation) which is enabled using the SPI interface. In serial CMOS mode by default the data is output on rising and falling edge of DCLK. In SDR clocking mode, DCLKIN has to be twice as fast as the default DCLKIN so that the output data are clocked out only on DCLK rising edge.

Internally DCLKIN is divided by 2 for data processing and this operation can add 1 extra clock cycle latency to the ADC latency.

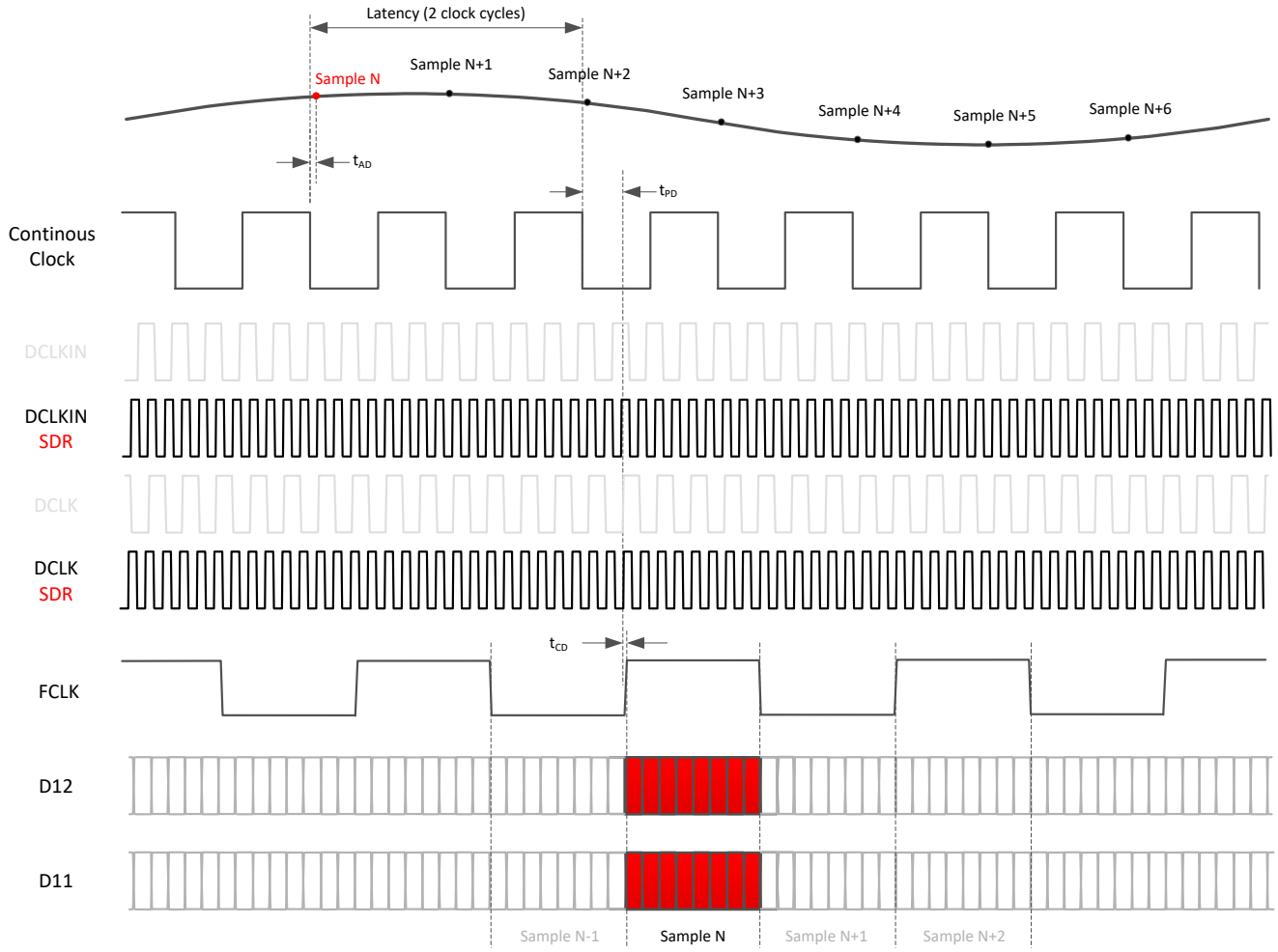

Figure 8-34. SDR Output Clocking

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8.3.5.3 Output Data Format

The output data can be configured to two's complement (default) or offset binary formatting using SPI register writes (register 0x8F and 0x92). Table 8-7 provides an overview for minimum and maximum output codes for the two formatting options. The actual output resolution is set by the output bit mapper.

Table 8-7. Overview of minimum and maximum output codes vs resolution for different formatting

	Two's Complement (default)				Offset Binary			
RESOLUTION (BIT)	14	16	18	20	14	16	18	20
$V_{IN,MAX}$	0x1FFF	0x7FFF	0x1FFFF	0x7FFFF	0x3FFF	0xFFFF	0x3FFFF	0xFFFFF
0	0x0000		0x00000		0x2000	0x8000	0x20000	0x80000
$V_{IN,MIN}$	0x2000	0x8000	0x20000	0x80000	0x0000		0x00000	

8.3.5.4 Output Formatter

The digital output interface uses a flexible output bit mapper Figure 8-35. The bit mapper takes the 14-bit output directly from the ADC or from digital filter block and reformats it to a resolution of 14, 16, 18 or 20-bit. With parallel output format the maximum output resolution supported is 16-bit. With serial CMOS output the output serialization factor gets adjusted accordingly for 2-, 1- and 1/2-wire interface mode. The maximum output data rate can not be exceeded independently of output resolution and serialization factor.

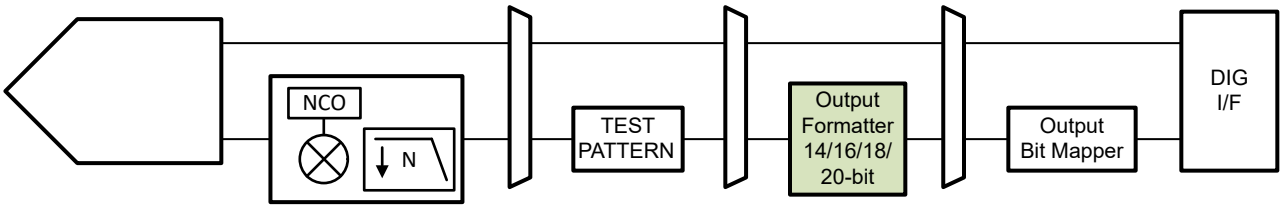

Figure 8-35. Interface output bit mapper

Table 8-8 provides an overview for the resulting serialization factor depending on output resolution and output modes. Note that the DCLKIN frequency needs to be adjusted accordingly as well. Changing the output resolution to 14-bit, 2-wire mode for example would result in DCLKIN = F_S * 3.5 instead of * 4.

The output bit mapper can be used for bypass and decimation filter.

Table 8-8. Serialization factor vs output resolution for different output modes

OUTPUT RESOLUTION	Interface	SERIALIZATION	FCLK	DCLKIN	DCLK	D0/D1
14-bit (default)	2-Wire	7x	F_S/2	F_S* 3.5	F_S* 3.5	F_S* 7
	1-Wire	14x	F_S	F_S* 7	F_S* 7	F_S* 14
16-bit	2-Wire	8x	F_S/2	F_S* 4	F_S* 4	F_S* 8
	1-Wire	16x	F_S	F_S* 8	F_S* 8	F_S* 16
18-bit	2-Wire	9x	F_S/2	F_S* 4.5	F_S* 4.5	F_S* 9
	1-Wire	18x	F_S	F_S* 9	F_S* 9	F_S* 18
20-bit	2-Wire	10x	F_S/2	F_S* 5	F_S* 5	F_S* 10
	1-Wire	20x	F_S	F_S* 10	F_S* 10	F_S* 20

The programming sequence to change the output interface and/or resolution from default settings is shown in Section 8.3.5.6.

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8.3.5.5 Output Bit Mapper

The output bit mapper allows to change the output bit order for any selected interface mode.

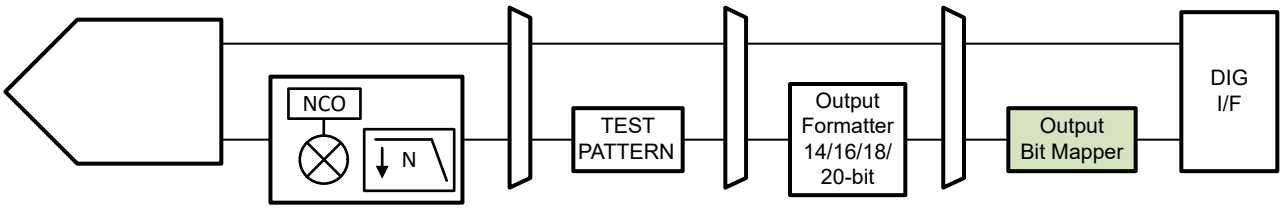

Figure 8-36. Output Bit Mapper

There is a two step process to change the output bit mapping and assemble the output data bus:

1. In parallel interface mode, the maximum output resolution is 18-bit, in serial interface mode the maximum output resolution is 20-bit. Each output bit of either channel has a unique identifier bit as shown in the Table 8-9. The MSB starts with bit D19. Depending on output resolution chosen, the LSB is D6 (14-bit) to D0 (20-bit). The *previous sample* is only needed in 2-w mode.
2. The bit mapper is then used to assemble the output sample. The following sections detail how to remap both a parallel and a serial output format.

Table 8-9. Unique identifier of each data bit

Bit	Previous sample (2w only)	Current sample
D19 (MSB)	0x2D	0x6D
D18	0x2C	0x6C
D17	0x27	0x67
D16	0x26	0x66
D15	0x25	0x65
D14	0x24	0x64
D13	0x1F	0x5F
D12	0x1E	0x5E
D11	0x1D	0x5D
D10	0x1C	0x5C
D9	0x17	0x57
D8	0x16	0x56
D7	0x15	0x55
D6	0x14	0x54
D5	0x0F	0x4F
D4	0x0E	0x4E
D3	0x0D	0x4D
D2	0x0C	0x4C
D1	0x07	0x47
D0 (LSB)	0x06	0x46

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In **parallel SDR** mode, a data bit (with unique identifier) needs to be assigned to each output pin using the register addresses as shown in Figure 8-37. The example on the right shows the output data bus reversed to where the MSB starts on pin D2 instead of pin D15.

PIN #	PIN NAME	ADDR	14-BIT DEFAULT	16-BIT DEFAULT	18-BIT DEFAULT
38	D0	0x39	-	-	D0
37	D1	0x3A	-	D0	D1
36	D2	0x3B	D0	D1	D2
35	D3	0x3C	D1	D2	D3
34	D4	0x3D	D2	D3	D4
33	D5	0x3E	D3	D4	D5
32	D6	0x3F	D4	D5	D6
30	D7	0x40	D5	D6	D7
29	D8	0x41	D6	D7	D8
28	D9	0x42	D7	D8	D9
27	D10	0x43	D8	D9	D10
24	D11	0x4A	D9	D10	D11
23	D12	0x49	D10	D11	D12
22	D13	0x48	D11	D12	D13
21	D14	0x47	D12	D13	D14
20	D15	0x46	D13	D14	D15
19	D16	0x45	-	D15	D16
18	D17	0x44	-	-	D17

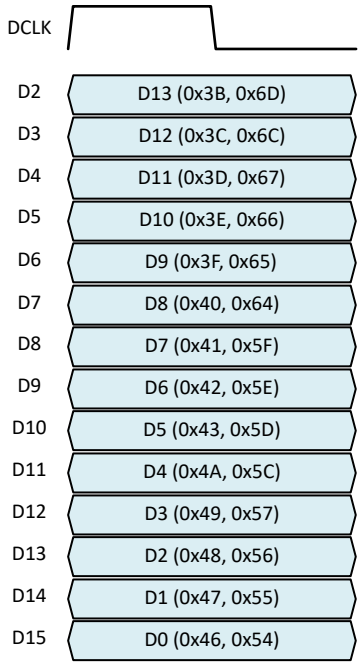

Figure 8-37. SDR output mapping (left) and example (right)

In **parallel DDR** mode, a data bit (with unique identifier) needs to be assigned to each output pin for both the rising and the falling edge of the DCLK using the register addresses as shown in Figure 8-38. D9 and D10 are used for 16 and 18-bit output. The example on the right shows the output data bus remapped to where the MSB starts on D17 instead of D11.

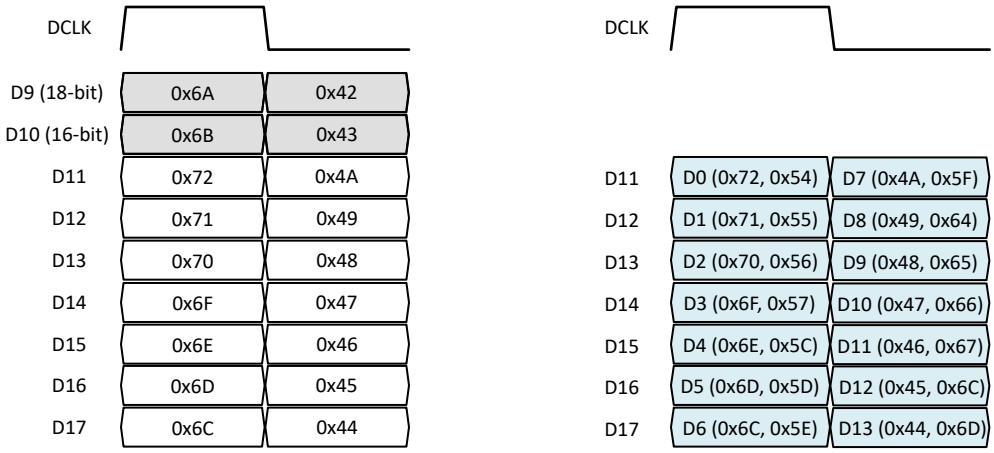

Figure 8-38. DDR output timing diagram with output mapping (left) and example (right)

In the serial output mode, a data bit (with unique identifier) needs to be assigned to each location within the serial output stream. There are a total of 40 addresses (0x39 to 0x60). When using complex decimation, the output bit mapper is applied to both the “I” and the “Q” sample.

2-wire mode: in this mode, both the current and the previous sample have to be used in the address space as shown in Figure 8-39. The address order is different for 14/18-bit and 16/20-bit. Note: there are unused addresses between samples for resolution less than 20-bit (grey back ground), which can be skipped if not used.

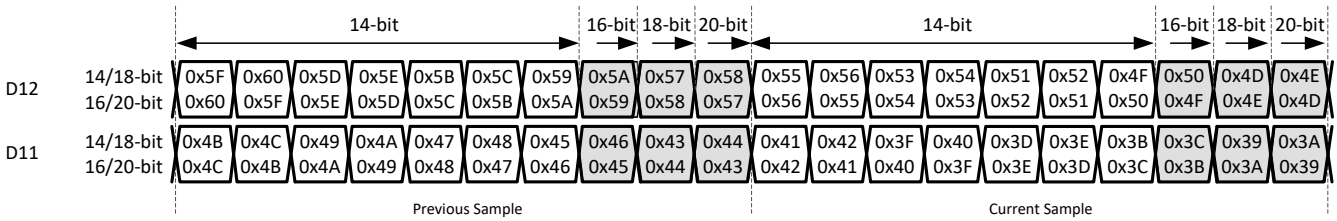

Figure 8-39. 2-wire output bit mapper

In the following example (Figure 8-40), the 16-bit 2-wire serial output is reordered to where pin D12 carries the 8 MSB and pin D11 carries 8 LSBs.

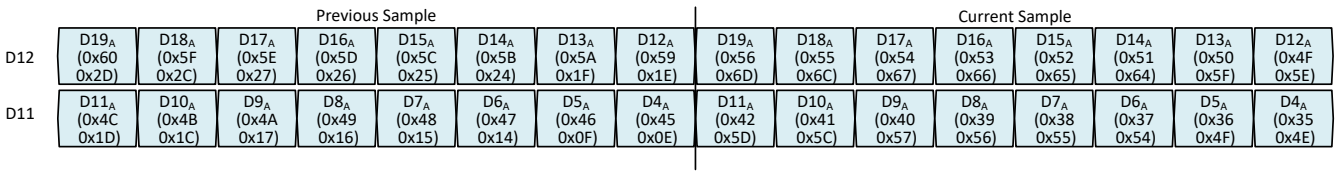

Figure 8-40. Example: 2-wire output mapping

1-wire mode: Only the ‘current’ sample needs to programmed in the address space.

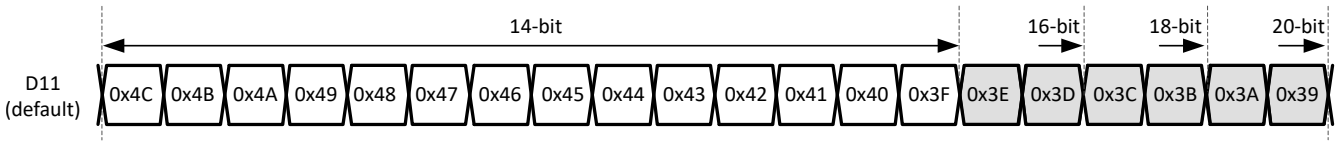

Figure 8-41. 1-wire output bit mapping

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8.3.5.6 Output Interface/Mode Configuration

The following sequence summarizes all the relevant registers for changing the output interface and/or enabling the decimation filter. Steps 1 and 2 must come first since the E-Fuse load reset the SPI writes, the remaining steps can come in any order.

Table 8-10. Configuration steps for changing interface or decimation

STEP	FEATURE	ADDRESS	DESCRIPTION				
1	Output Interface	0x07	Select the output interface bit mapping depending on resolution and output interface.				
			Output Resolution	SDR	DDR	2-wire	1-wire
			14-bit	0xC8	0xA9	0x2B	0x6C
			16-bit			0x4B	
			18-bit	N/A	N/A	0x2B	
			20-bit	N/A	N/A	0x4B	
2		0x13	Load the output interface bit mapping using the E-fuse loader (0x13, D0). Program register 0x13 to 0x01, wait ~ 1ms so that bit mapping is loaded properly followed by 0x13 0x00				
3		0x0A/B/C	Power down relevant CMOS output buffers to avoid contention.				
4		0x18	For serial CMOS modes, DCLKIN EN (D4) needs to be enabled.				
5		0x19	When using serial CMOS, configure the FCLK frequency based on bypass/decimation and number of lanes used.				
			Bypass/Dec	SCMOS	FCLK SRC (D7)	FCLK DIV (D4)	
			Bypass/ Real Decimation	2-wire	0	1	
				1-wire	0	0	
				1/2-wire	0	0	
			Complex Decimation	2-wire	1	0	
				1-wire	1	0	
				1/2-wire	0	0	
6		0x1B	Select the output interface resolution using the bit mapper (D5-D3).				
7		0x1F	For serial CMOS modes, DCLKIN EN (D6) and DCLK OB EN (D4) need to be enabled.				
8		0x20 0x21 0x22	When using serial CMOS, select the FCLK pattern for decimation for proper duty cycle output of the frame clock.				
			Decimation	Output Resolution	2-wire	1-wire	
			Real Decimation	14-bit	use default	0xFE000	
				16-bit		0xFF000	
				18-bit		0xFF800	
				20-bit		0xFFC00	
			Complex Decimation	14-bit		0xFFFFF	
				16-bit			
				18-bit			
				20-bit			
9		0x39..0x60	Change output bit mapping if desired. This works also with the default interface selection.				

Table 8-10. Configuration steps for changing interface or decimation (continued)

STEP	FEATURE	ADDRESS	DESCRIPTION		
10	Decimation Filter	0x24	Enable the decimation filter		
11		0x25	Configure the decimation filter		
12		0x2A/B/C/D	Program the NCO frequency for complex decimation (can be skipped for real decimation)		
13		0x27	Configure the complex output data stream (set both bits to 0 for real decimation)		
			Serial CMOS	OP-Order (D4)	Q-Delay (D3)
			2-wire	1	0
			1-wire	0	1
			1/2-wire	1	1
14		0x26	Set the mixer gain and toggle the mixer reset bit to update the NCO frequency.		

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8.3.5.6.1 Configuration Example

The following is a step by step programming example to configure the ADC3544 to complex decimation by 8 with 1-wire serial CMOS and 16-bit output.

1. 0x07 (address) 0x6C (load bit mapper configuration for 16-bit output with 1-wire serial CMOS)
2. 0x13 0x01, wait 1 ms, 0x13 0x00 (load e-fuse)
3. 0x0A 0xFF, 0x0B 0xFF, 0x0C 0xFD (Power down unused CMOS output buffers to avoid contention)
4. 0x18 0x10 (DCLKIN EN for serial CMOS mode)
5. 0x19 0x82 (configure FCLK)
6. 0x1B 0x88 (select 16-bit output resolution)
7. 0x1F 0x50 (DCLKIN EN for serial CMOS mode)
8. 0x20 0xFF, 0x21 0xFF, 0x22 0x0F (configure FCLK pattern)
9. 0x24 0x06 (enable decimation filter)
10. 0x25 0x30 (configure complex decimation by 8)
11. 0x2A/B/C/D (program NCO frequency)
12. 0x27/0x2E 0x08 (configure Q-delay register bit)
13. 0x26 0xAA (set digital mixer gain to 6-dB and toggle the mixer update)

8.3.6 Test Pattern

In order to enable in-circuit testing of the digital interface, the following test patterns are supported and enabled via SPI register writes (0x14/0x15/0x16). The test pattern generator is located after the decimation filter as shown in Figure 8-42. In decimation mode (real and complex), the test patterns replace the output data of the DDC - however channel A controls the test patterns for both channels.

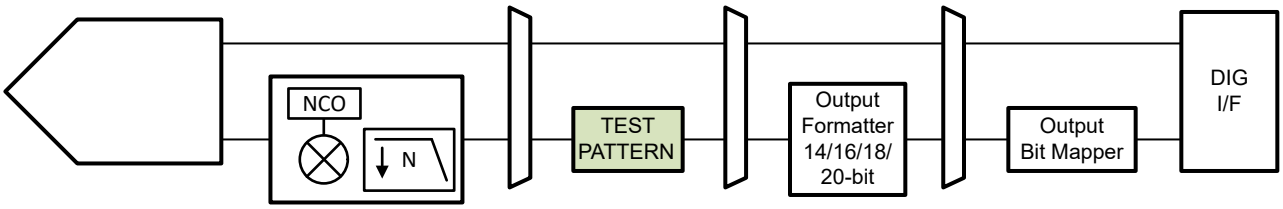

Figure 8-42. Test Pattern Generator

- RAMP Pattern: The step size needs to be configured in the CUSTOM PAT register according to the native resolution of the ADC. When selecting a higher output resolution then the additional LSBs will still be 0 in RAMP pattern mode.
  - 00001: 18-bit output resolution
  - 00100: 16-bit output resolution
  - 10000: 14-bit output resolution
- Custom Pattern: Configured in the CUSTOM PAT register

8.4 Device Functional Modes

8.4.1 Normal operation

In normal operating mode, the entire ADC full scale range gets converted to a digital output with 14bit resolution. The output is available in as little as 1 clock cycle on the digital CMOS outputs.

8.4.2 Power Down Options

A global power down mode can be enabled via SPI as well as using the power down pin (PDN/SYNC). There is an internal pull-down 21 kΩ resistor on the PDN/SYNC input pin and the pin is active high - so the pin needs to be pulled high externally to enter global power down mode.

The SPI register map provides the capability to enable/disable individual blocks directly or via PDN pin mask in order to trade off power consumption vs wake up time as shown in Table 8-11.

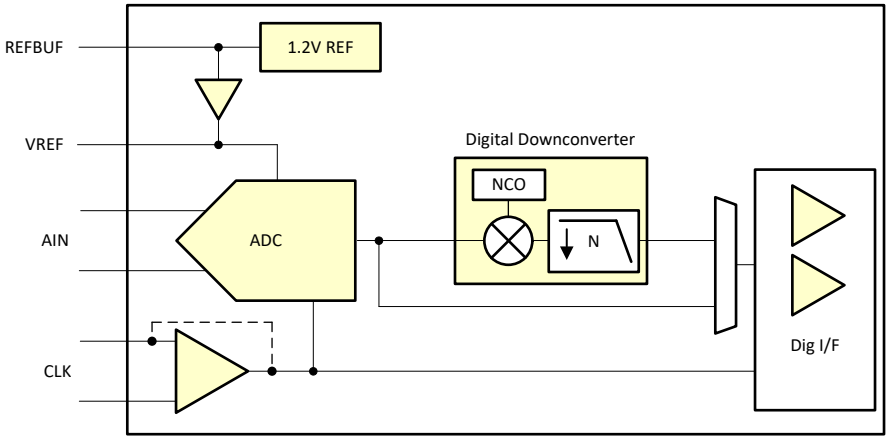

Figure 8-43. Power Down Configurations

Table 8-11. Overview of Power Down Options

Function/ Register	PDN via SPI	Mask for Global PDN	Feature - Default	Power Impact	Wake-up time	Comment
ADC	Yes	-	Enabled			ADC is included in Global PDN automatically
Reference gain amplifier	Yes	Yes	Enabled	~ 0.4 mA	~3 us	Should only be powered down in power down state.
Internal 1.2V reference	Yes		External ref	~ 1-3.5 mA	~3 ms	Internal/external reference selection is available through SPI and REFBUF pin.
Clock buffer	Yes		Differential clock	~ 1 mA	n/a	Single ended clock input saves ~ 1mA compared to differential. Some programmability is available through the REFBUF pin.
Output interface drivers	Yes	-	Enabled	varies	n/a	Depending on output interface mode, unused output drivers can be powered down for maximum power savings
Decimation filter	Yes	-	Disabled	see electrical table	n/a	

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8.5 Programming

The device is primarily configured and controlled using the serial programming interface (SPI); however, the device can operate in a default configuration without requiring the SPI interface. Furthermore, the power down function as well as internal/external reference configuration is possible via pin control (PDN/SYNC and REFBUF pin).

Note

The power down command (via PIN or SPI) only goes in effect with the ADC sampling clock present.

After initial power up, the default operating configuration for each device is shown in Table 8-12.

Table 8-12. Default device configuration after power up

FEATURE	DEFAULT
Signal Input	Differential
Clock Input	Differential
Reference	External
Decimation	DDC bypass
Interface	SDR CMOS
Output Format	2s complement

8.5.1 Configuration using PINs only

The ADC voltage reference can be selected using the REFBUF pin. Even though there is an internal 100 kΩ pull-up resistor to AVDD, the REFBUF pin should be set to a voltage externally and not left floating.

When using a voltage divider to set the REFBUF voltage (R1 and R2 in Figure 8-44), resistor values < 5 kΩ should be used.

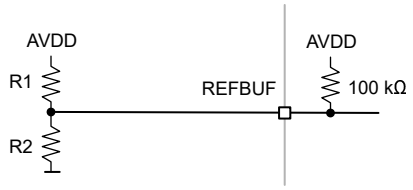

Figure 8-44. Configuration of external voltage on REFBUF pin

Table 8-13. REFBUF voltage levels control voltage reference selection

REFBUF VOLTAGE	VOLTAGE REFERENCE OPTION	CLOCKING OPTION	Digital Interface
> 1.7 V (Default)	External reference	Differential clock input	SDR CMOS
1.2 V (1.15-1.25V)	External 1.2V input on REFBUF pin using internal gain buffer	Differential clock input	SDR CMOS
0.5 - 0.7V	Internal reference	Differential clock input	SDR CMOS
< 0.1V	Internal reference	Single ended clock input	Serial CMOS 2-wire

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8.5.2 Configuration using the SPI interface

The device has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock) and SDIO (serial interface data input/output) pins. Serially shifting bits into the device is enabled when SEN is low. Serial data input are latched at every SCLK rising edge when SEN is active (low). The serial data are loaded into the register at every 24th SCLK rising edge when SEN is low. When the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data can be loaded in multiples of 24-bit words within a single active SEN pulse. The interface can function with SCLK frequencies from 20 MHz down to low speeds (of a few hertz) and also with a non-50% SCLK duty cycle.

8.5.2.1 Register Write

The internal registers can be programmed following these steps:

1. Drive the SEN pin low
2. Set the R/W bit to 0 (bit A15 of the 16-bit address) and bits A[14:12] in address field to 0.
3. Initiate a serial interface cycle by specifying the address of the register (A[11:0]) whose content is written and
4. Write the 8-bit data that are latched in on the SCLK rising edges

Figure 8-45 show the timing requirements for the serial register write operation.

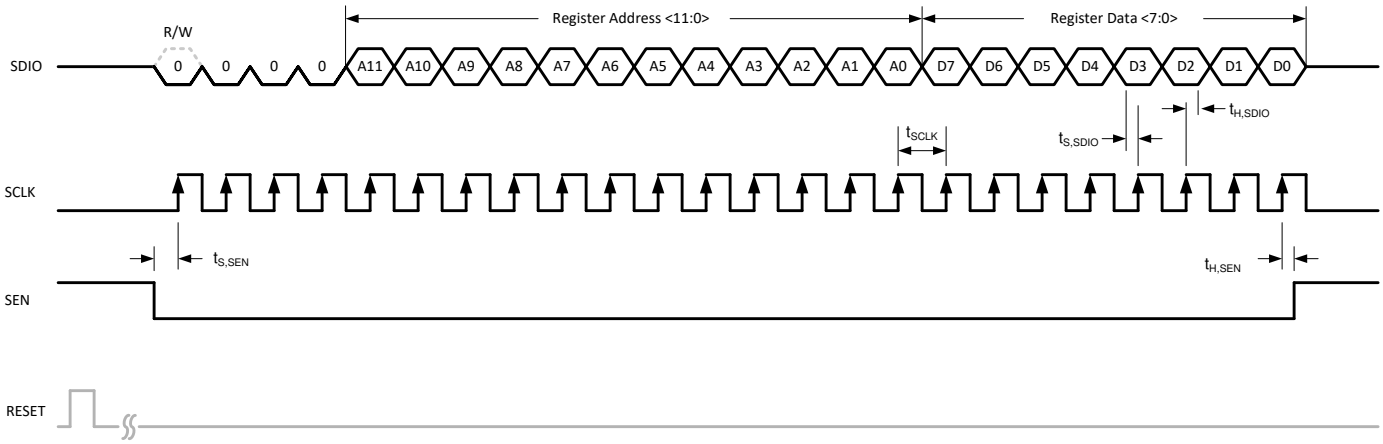

Figure 8-45. Serial Register Write Timing Diagram

8.5.2.2 Register Read

The device includes a mode where the contents of the internal registers can be read back using the SDIO pin. This readback mode can be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC. The procedure to read the contents of the serial registers is as follows:

1. Drive the SEN pin low
2. Set the R/W bit (A15) to 1. This setting disables any further writes to the registers. Set A[14:12] in address field to 0.
3. Initiate a serial interface cycle specifying the address of the register (A[11:0]) whose content must be read
4. The device launches the contents (D[7:0]) of the selected register on the SDIO pin on SCLK falling edge
5. The external controller can capture the contents on the SCLK rising edge

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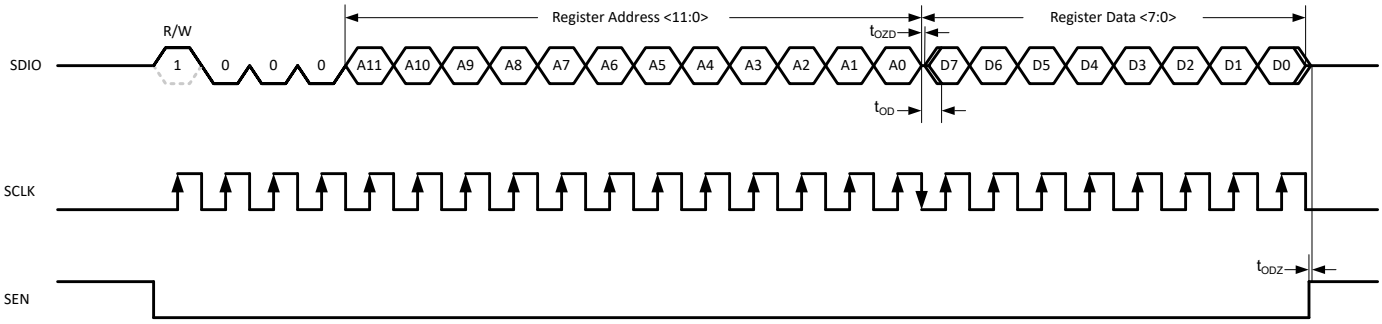

Figure 8-46. Serial Register Read Timing Diagram

8.6 Register Maps

Table 8-14. Register Map Summary

REGISTER ADDRESS	REGISTER DATA							
A[11:0]	D7	D6	D5	D4	D3	D2	D1	D0
0x00	0	0	0	0	0	0	0	RESET
0x07	OP IF MAPPER			0	OP IF EN	OP IF SEL		
0x08	0	0	PDN CLKBUF	PDN REFAMP	0	PDN A	1	PDN GLOBAL
0x0A	CMOS OB DIS [7:0]							
0x0B	CMOS OB DIS [15:8]							
0x0C	CMOS OB DIS [23:16]							
0x0D	0	0	0	0	MASK CLKBUF	MASK REFAMP	MASK BG DIS	0
0x0E	SYNC PIN EN	SPI SYNC	SPI SYNC EN	0	REF CTRL	REF SEL		SE CLK EN
0x11	0	0	SE A	0	0	0	0	0
0x13	0	0	0	0	0	0	0	E-FUSE LD
0x14	CUSTOM PAT [7:0]							
0x15	CUSTOM PAT [15:8]							
0x16	0	0	0	TEST PAT A			CUSTOM PAT [17:16]	
0x18	0	0	0	DCLKIN EN	0	0	0	0
0x19	FCLK SRC	0	0	FCLK DIV	0	0	FCLK EN	0
0x1B	MAPPER EN	20B EN	BIT MAPPER RES			0	0	0
0x1E	0	0	CMOS DCLK DEL		0	0	0	0
0x1F	LOW DR EN	DCLKIN EN	0	DCLK OB EN	2X DCLK	0	0	0
0x20	FCLK PAT [7:0]							
0x21	FCLK PAT [15:8]							
0x22	0	0	0	0	FCLK PAT [19:16]			
0x24	0	0	0	0	0	DIG BYP	DDC EN	0
0x25	0	DECIMATION			REAL OUT	0	0	MIX PHASE
0x26	MIX GAIN A		MIX RES A	FS/4 MIX A	0	0	0	0
0x27	0	0	0	OP ORDER A	Q-DEL A	FS/4 MIX PH A	0	0
0x2A	NCO A [7:0]							
0x2B	NCO A [15:8]							
0x2C	NCO A [23:16]							
0x2D	NCO A [31:24]							
0x31..0x60	OUTPUT BIT MAPPER							
0x8F	0	0	0	0	0	0	FORMAT A	0

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8.6.1 Detailed Register Description

Figure 8-47. Register 0x00

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	RESET
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 8-15. Register 0x00 Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	R/W	0	Must write 0
0	RESET	R/W	0	This bit resets all internal registers to the default values and self clears to 0.

Figure 8-48. Register 0x07

7	6	5	4	3	2	1	0
OP IF MAPPER			0	OP IF EN	OP IF SEL		
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 8-16. Register 0x07 Field Descriptions

Bit	Field	Type	Reset	Description
7-5	OP IF MAPPER	R/W	000	Output interface mapper. This register contains the proper output interface bit mapping for the different interfaces. The interface bit mapping is internally loaded from e-fuses and also requires a fuse load command to go into effect (0x13, D0). Register 0x07 along with the E-Fuse Load (0x13, D0) needs to be loaded first in the programming sequence since the E-Fuse load resets the SPI writes. After initial reset the default output interface variant is loaded automatically from fuse internally. However when reading back this register reads 000 until a value is written using SPI. 001: 2-wire, 18 and 14-bit 010: 2-wire, 16-bit 011: 1-wire 100: 0.5-wire 101: DDR 110: SDR others: not used
4	0	R/W	0	Must write 0
3	OP IF EN	R/W	0	Enables changing the default output interface mode (D2-D0).
2-0	OP IF SEL	R/W	000	Selection of the output interface mode. OP IF EN (D3) needs to be enabled also. After initial reset the default output interface is loaded automatically from fuse internally. However when reading back this register reads 000 until a value is written using SPI. 000: SDR CMOS 001: DDR CMOS 011: 2-wire 100: 1-wire 101: 0.5-wire others: not used

Figure 8-49. Register 0x08

7	6	5	4	3	2	1	0
0	0	PDN CLKBUF	PDN REFAMP	0	PDN A	1	PDN GLOBAL
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 8-17. Register 0x08 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	R/W	0	Must write 0
5	PDN CLKBUF	R/W	0	Powers down sampling clock buffer 0: Clock buffer enabled 1: Clock buffer powered down
4	PDN REFAMP	R/W	0	Powers down internal reference gain amplifier 0: REFAMP enabled 1: REFAMP powered down
3	0	R/W	0	Must write 0
2	PDN A	R/W	0	Powers down ADC channel A 0: ADC channel A enabled 1: ADC channel A powered down
1	1	R/W	1	Must write 1
0	PDN GLOBAL	R/W	0	Global power down via SPI 0: Global power disabled 1: Global power down enabled. Power down mask (register 0x0D) determines which internal blocks are powered down.

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Figure 8-50. Register 0x0A, B, C

7	6	5	4	3	2	1	0
CMOS OB DIS [23:0]							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 8-18. Register 0x0A, B, C Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CMOS OB DIS [23:0]	R/W	0	These register bits power down the individual CMOS output buffers. See Table 8-19 for the actual bit to pin mapping. Unused pins should be powered down (ie set to 1) for maximum power savings. Even though unused outputs don't toggle there is still a small amount of static power (< 1mA) that can be saved by disabling the output buffers. There is a separate control to enable the DCLKIN buffer in register 0x1F (D6) and 0x18 (D4). DCLK output buffer is powered down using register 0x1F (D4). NOTE: When using serial CMOS interface the CMOS output buffer (D3) has to be powered down because it shares the pin with DCLKIN. 0: Output buffer enabled 1: Output buffer powered down

Table 8-19. Output buffer enable bit mapping vs output interface mode

ADDRESS (HEX)	BIT	PIN NAME	SDR CMOS	DDR CMOS	SCMOS 2-w	SCMOS 1-w
0x0A	D7	D7	D7	D7	-	-
	D6	-	-	-	-	-
	D5	-	-	-	-	-
	D4	D4	D4	-	-	-
	D3	D3	D3	-	DCLKIN	DCLKIN
	D2	D2	D2	-	-	-
	D1	D1	D1	-	-	-
	D0	D0	D0	-	-	-
	Register setting		0x60	0x7F	0xFF	0xFF
0x0B	D7	D13	D13	-	-	-
	D6	D14	D14	-	-	-
	D5	D15	D15	-	-	-
	D4	FCLK	-	-	FCLK	FCLK
	D3	-	-	-	-	-
	D2	-	-	-	-	-
	D1	-	-	-	-	-
	D0	D8	D8	D8	-	-
	Register setting		0x1E	0xFE	0xEF	0xEF
0x0C	D7	D10	D10	D10	-	-
	D6	D9	D9	D9	-	-
	D5	D6	D6	D6	-	-
	D4	D5	D5	D5	-	-
	D3	-	-	-	-	-
	D2	-	-	-	-	-
	D1	D11	D11	D11	D11	D11
	D0	D12	D12	D12	D12	-
	Register setting		0x0C	0x0C	0xFC	0xFD

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Figure 8-51. Register 0x0D (PDN GLOBAL MASK)

7	6	5	4	3	2	1	0
0	0	0	0	MASK CLKBUF	MASK REFAMP	MASK BG DIS	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 8-20. Register 0x0D Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	R/W	0	Must write 0
3	MASK CLKBUF	R/W	0	Global power down mask control for sampling clock input buffer. 0: Clock buffer will get powered down when global power down is exercised. 1: Clock buffer will NOT get powered down when global power down is exercised.
2	MASK REFAMP	R/W	0	Global power down mask control for reference amplifier. 0: Reference amplifier will get powered down when global power down is exercised. 1: Reference amplifier will NOT get powered down when global power down is exercised.
1	MASK BG DIS	R/W	0	Global power down mask control for internal 1.2V bandgap voltage reference. Setting this bit reduces power consumption in global power down mode but increases the wake up time. See the power down option overview. 0: Internal 1.2V bandgap voltage reference will NOT get powered down when global power down is exercised. 1: Internal 1.2V bandgap voltage reference will get powered down when global power down is exercised.
0	0	R/W	0	Must write 0

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Figure 8-52. Register 0x0E

7	6	5	4	3	2	1	0
SYNC PIN EN	SPI SYNC	SPI SYNC EN	0	REF CTL	REF SEL		SE CLK EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 8-21. Register 0x0E Field Descriptions

Bit	Field	Type	Reset	Description
7	SYNC PIN EN	R/W	0	This bit controls the functionality of the SYNC/PDN pin. 0: SYNC/PDN pin exercises global power down mode when pin is pulled high. 1: SYNC/PDN pin issues the SYNC command when pin is pulled high.
6	SPI SYNC	R/W	0	Toggling this bit issues the SYNC command using the SPI register write. SYNC using SPI must be enabled as well (D5). This bit doesn't self reset to 0. 0: Normal operation 1: SYNC command issued.
5	SPI SYNC EN	R/W	0	This bit enables synchronization using SPI instead of the SYNC/PDN pin. 0: Synchronization using SPI register bit disabled. 1: Synchronization using SPI register bit enabled.
4	0	R/W	0	Must write 0
3	REF CTL	R/W	0	This bit determines if the REFBUF pin controls the voltage reference selection or the SPI register (D2-D1). 0: The REFBUF pin selects the voltage reference option. 1: Voltage reference is selected using SPI (D2-D1) and single ended clock using D0.
2-1	REF SEL	R/W	00	Selects of the voltage reference option. REF CTRL (D3) must be set to 1. 00: Internal reference 01: External voltage reference (1.2V) using internal reference buffer (REFBUF) 10: External voltage reference 11: not used
0	SE CLK EN	R/W	0	Selects single ended clock input and powers down the differential sampling clock input buffer. REF CRTL (D3) must be set to 1. 0: Differential clock input 1: Single ended clock input

Figure 8-53. Register 0x11

7	6	5	4	3	2	1	0
0	0	SE A	0	0	0	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 8-22. Register 0x11 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	R/W	0	Must write 0
5	SE A	R/W	0	This bit enables single ended analog input, channel A. In this mode the SNR is reduced by 3-dB. 0: Differential input 1: Single ended input
4-0	0	R/W	0	Must write 0

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Figure 8-54. Register 0x13

7	6	5	4	3	2	1	0
0	0	0	0	0	0		E-FUSE LD
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 8-23. Register 0x13 Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	R/W	0	Must write 0
0	E-FUSE LD	R/W	0	This register bit loads the internal bit mapping for different interfaces. After setting the interface in register 0x07, this E-FUSE LD bit needs to be set to 1 and reset to 0 for loading to go into effect. Register 0x07 along with the E-Fuse Load (0x13, D0) needs to be loaded first in the programming sequence since the E-Fuse load resets the SPI writes. 0: E-FUSE LOAD set 1: E-FUSE LOAD reset

Figure 8-55. Register 0x14, 15, 16

7	6	5	4	3	2	1	0
CUSTOM PAT [7:0]							
CUSTOM PAT [15:8]							
0	0	0	TEST PAT A			CUSTOM PAT [17:16]	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 8-24. Register 0x14, 15, 16 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CUSTOM PAT [17:0]	R/W	00000000	This register is used for two purposes: • It sets the constant custom pattern starting from MSB • It sets the RAMP pattern increment step size. 00001: Ramp pattern for 18-bit ADC 00100: Ramp pattern for 16-bit ADC 10000: Ramp pattern for 14-bit ADC
7-5	0	R/W	0	Must write 0.
4-2	TEST PAT A	R/W	000	Enables test pattern output mode for channel A (NOTE: The test pattern is set prior to the bit mapper and is based on native resolution of the ADC starting from the MSB). These work in either output format.
				000: Normal output mode (test pattern output disabled) 010: Ramp pattern: need to set proper increment using CUSTOM PAT register 011: Constant Pattern using CUSTOM PAT [17:0] in register 0x14/15/16. others: not used

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Figure 8-56. Register 0x18

7	6	5	4	3	2	1	0
0	0	0	DCLKIN EN	0	0	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 8-25. Register 0x18 Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	R/W	0	Must write 0
4	DCLKIN EN	R/W	0	This bit enables the DCLKIN clock input buffer for serial CMOS modes. Also DCLKIN EN (0x1F, D6) needs to be set as well. 0: DCLKIN buffer powered down. 1: DCLKIN buffer enabled.
3-0	0	R/W	0	Must write 0

Figure 8-57. Register 0x19

7	6	5	4	3	2	1	0
FCLK SRC	0	0	FCLK DIV	0	0	FCLK EN	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 8-26. Register 0x19 Field Descriptions

Bit	Field	Type	Reset	Description
7	FCLK SRC	R/W	0	User has to select if FCLK signal comes from ADC or from DDC block. Here real decimation is treated same as bypass mode 0: FCLK generated from ADC. FCLK SRC set to 0 for DDC bypass and real decimation mode. 1: FCLK generated from DDC block. In complex decimation mode only this bit needs to be set for 2-w and 1-w output interface mode.
6-5	0	R/W	0	Must write 0
4	FCLK DIV	R/W	0	This bit needs to be set to 1 for 2-w output mode in bypass mode only (non decimation). 0: All output interface modes except 2-w bypass mode.. 1: 2-w output interface mode.
3-2	0	R/W	0	Must write 0
1	FCLK EN	R/W	0	This bit enables FCLK output for CMOS output. 0: Data output pin is used for parallel output data. 1: Data output pin is used for FCLK output in serialized CMOS mode.
0	0	R/W	0	Must write 0

Table 8-27. Configuration of FCLK SRC and FCLK DIV Register Bits vs Serial Interface

BYPASS/DECIMATION	SERIAL INTERFACE	FCLK SRC	FCLK DIV
Decimation Bypass/ Real Decimation	2-wire	0	1
	1-wire	0	0
Complex Decimation	2-wire	1	0
	1-wire	1	0

Figure 8-58. Register 0x1B

7	6	5	4	3	2	1	0
MAPPER EN	20B EN	BIT MAPPER RES			0	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 8-28. Register 0x1B Field Descriptions

Bit	Field	Type	Reset	Description
7	MAPPER EN	R/W	0	This bit enables changing the resolution of the output (including output serialization factor) in bypass mode only. This bit is not needed for 20-bit resolution output. 0: Output bit mapper disabled. 1: Output bit mapper enabled.
6	20B EN	R/W	0	This bit enables 20-bit output resolution which can be useful for a high decimation settings so that quantization noise doesn't impact the ADC performance. 0: 20-bit output resolution disabled. 1: 20-bit output resolution enabled.
5-3	BIT MAPPER RES	R/W	000	Sets the output resolution using the bit mapper. MAPPER EN bit (D6) needs to be enabled when operating in bypass mode.. 000: 18 bit 001: 16 bit 010: 14 bit all others, n/a
2-0	0	R/W	0	Must write 0

Table 8-29. Register Settings for Output Bit Mapper vs Operating Mode

BYPASS/ DECIMATION	OUTPUT RESOLUTION	MAPPER EN (D7)	BIT MAPPER RES (D5-D3)
Decimation Bypass	Resolution Change	1	000: 18-bit 001: 16-bit 010: 14-bit
Real Decimation	Resolution Change (default 18-bit)	0	
Complex Decimation		0	

Figure 8-59. Register 0x1E

7	6	5	4	3	2	1	0
0	0	CMOS DCLK DEL		0	0	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 8-30. Register 0x1E Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	R/W	0	Must write 0
5-4	CMOS DCLK DEL	R/W	00	These bits adjust the output timing of CMOS DCLK output. 00: no delay 01: DCLK advanced by 50 ps 10: DCLK delayed by 50 ps 11: DCLK delayed by 100 ps
3-0	0	R/W	0	Must write 0

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Figure 8-60. Register 0x1F

7	6	5	4	3	2	1	0
LOW DR EN	DCLKIN EN	0	DCLK OB EN	2X DCLK	0	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 8-31. Register 0x1F Field Descriptions

Bit	Field	Type	Reset	Description
7	LOW DR EN	R/W	0	This bit impacts the output drive strength of the CMOS output buffers. This bit can be enabled at slow speeds in order to save power consumption but it will also degrade the rise and fall times. 0: Low drive strength disabled. 1: Low drive strength enabled.
6	DCLKIN EN	R/W	0	This bit enables the DCLKIN clock input buffer for serial CMOS modes. Also DCLKIN EN (0x18, D4) needs to be set as well. 0: DCLKIN buffer powered down. 1: DCLKIN buffer enabled.
5	0	R/W	0	Must write 0
4	DCLK OB EN	R/W	1	This bit enables DCLK output buffer. 0: DCLK output buffer powered down. 1: DCLK output buffer enabled.
3	2X DCLK	R/W	0	This bit enables SDR output clocking with serial CMOS mode. When this mode is enabled, DCLKIN required is twice as fast and data is output only on rising edge of DCLK. 0: Normal operation with data output on DCLK rising and falling edge. 1: 2x DCLK mode enabled with data output on DCLK rising edge only.
2-0	0	R/W	0	Must write 0

Figure 8-61. Register 0x20/21/22

7	6	5	4	3	2	1	0
FCLK PAT [7:0]							
FCLK PAT [15:8]							
0	0	0	0	FCLK PAT [19:16]			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 8-32. Register 0x20, 21, 22 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FCLK PAT [19:0]	R/W	0xFFC00	These bits can adjust the duty cycle of the FCLK. In decimation bypass mode the FCLK pattern gets adjusted automatically for the different output resolutions. Table 8-33 shows the proper FCLK pattern values for 1-wire.

Table 8-33. FCLK Pattern for different resolution based on interface

DECIMATION	OUTPUT RESOLUTION	2-WIRE	1-WIRE
REAL DECIMATION	14-bit	Use Default	0xFE000
	16-bit		0xFF000
	18-bit		0xFF800
	20-bit		0xFFC00
COMPLEX DECIMATION	14-bit		0xFFFFF
	16-bit		
	18-bit		
	20-bit		

Figure 8-62. Register 0x24

7	6	5	4	3	2	1	0
0	0	0	0	0	DIG BYP	DDC EN	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 8-34. Register 0x24 Field Descriptions

Bit	Field	Type	Reset	Description
7-3	0	R/W	0	Must write 0
2	DIG BYP	R/W	0	This bit needs to be set to enable digital features block which includes decimation. 0: Digital feature block bypassed - lowest latency 1: Data path includes digital features
1	DDC EN	R/W	0	Enables internal decimation filter for both channels 0: DDC disabled. 1: DDC enabled.
0	0	R/W	0	Must write 0

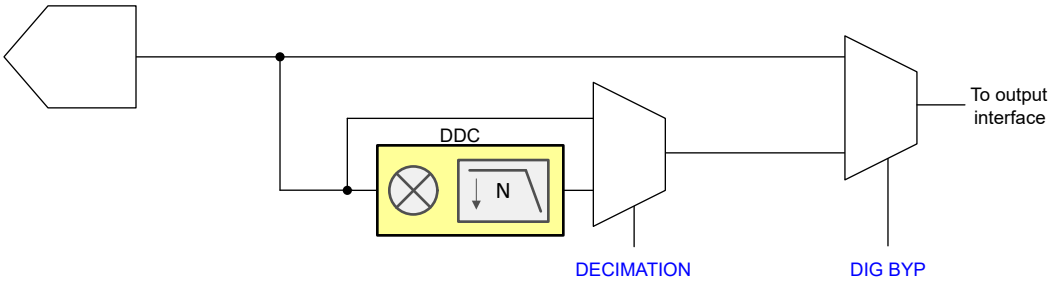

Figure 8-63. Register control for digital features

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Figure 8-64. Register 0x25

7	6	5	4	3	2	1	0
0	DECIMATION			REAL OUT	0	0	MIX PHASE
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 8-35. Register 0x25 Field Descriptions

Bit	Field	Type	Reset	Description
7	0	R/W	0	Must write 0
6-4	DECIMATION	R/W	000	Complex decimation setting. This applies to both channels. 000: Bypass mode (no decimation) 001: Decimation by 2 010: Decimation by 4 011: Decimation by 8 100: Decimation by 16 101: Decimation by 32 others: not used
3	REAL OUT	R/W	0	This bit selects real output decimation. This mode applies to both channels. In this mode, the decimation filter is a low pass filter and no complex mixing is performed to reduce power consumption. For maximum power savings the NCO in this case should be set to 0. 0: Complex decimation 1: Real decimation
2-1	0	R/W	0	Must write 0
0	MIX PHASE	R/W	0	This bit used to invert the NCO phase 0: NCO phase as is. 1: NCO phase inverted.

Figure 8-65. Register 0x26

7	6	5	4	3	2	1	0
MIX GAIN A		MIX RES A	FS/4 MIX A	0	0	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 8-36. Register 0x26 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	MIX GAIN A	R/W	00	This bit applies a 0, 3 or 6-dB digital gain to the output of digital mixer to compensate for the mixing loss for channel A. 00: no digital gain added 01: 3-dB digital gain added 10: 6-dB digital gain added 11: not used
5	MIX RES A	R/W	0	Toggling this bit resets the NCO phase of channel A and loads the new NCO frequency. This bit does not self reset.
4	FS/4 MIX A	R/W	0	Enables FS/4 mixing for DDC A (complex decimation only). 0: FS/4 mixing disabled. 1: FS/4 mixing enabled.
3-0	0	R/W	0	Must write 0.

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Figure 8-66. Register 0x27

7	6	5	4	3	2	1	0
0	0	0	OP ORDER A	Q-DEL A	FS/4 MIX PH A	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 8-37. Register 0x27 Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	R/W	0	Must write 0
4	OP ORDER A	R/W	0	Swaps the I and Q output order for channel A 0: Output order is I[n], Q[n] 1: Output order is swapped: Q[n], I[n]
3	Q-DEL A	R/W	0	This delays the Q-sample output of channel A by one. 0: Output order is I[n], Q[n] 1: Q-sample is delayed by 1 sample: I[n], Q[n+1], I[n+1], Q[n+2]
2	FS/4 MIX PH A	R/W	0	Inverts the mixer phase for channel A when using FS/4 mixer 0: Mixer phase is non-inverted 1: Mixer phase is inverted
1-0	0	R/W	0	Must write 0

Figure 8-67. Register 0x2A, B, C, D

7	6	5	4	3	2	1	0
NCO A [7:0]							
NCO A [15:8]							
NCO A [23:16]							
NCO A [31:24]							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 8-38. Register 0x2A, 2B, 2C, 2D Field Descriptions

Bit	Field	Type	Reset	Description
7-0	NCO A [31:0]	R/W	0	Sets the 32 bit NCO value for decimation filter channel A. The NCO value is $f_{NCO} \times 2^{32}/F_S$ In real decimation mode these registers are automatically set to 0.

Figure 8-68. Register 0x39..0x60

7	6	5	4	3	2	1	0
OUTPUT BIT MAPPER							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 8-39. Register 0x39..0x60 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUTPUT BIT MAPPER	R/W	0	These registers are used to reorder the output data bus. See the Section 8.3.5.5 on how to program it.

Figure 8-69. Register 0x8F

7	6	5	4	3	2	1	0
0	0	0	0	0	0	FORMAT A	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 8-40. Register 0x8F Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	R/W	0	Must write 0

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Table 8-40. Register 0x8F Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	FORMAT A	R/W	0	This bit sets the output data format for channel A. Digital bypass register bit (0x24, D2) needs to be enabled as well. 0: 2s complement 1: Offset binary
0	0	R/W	0	Must write 0

9 Application Information Disclaimer

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

A spectrum analyzer is a typical frequency domain application for the ADC3544 and its front end circuitry is similar to several other systems such as software defined radio (SDR), sonar, radar or communications. Some applications require frequency coverage including DC or near DC (that is, sonar) so it is included in this example.

9.2 Typical Application

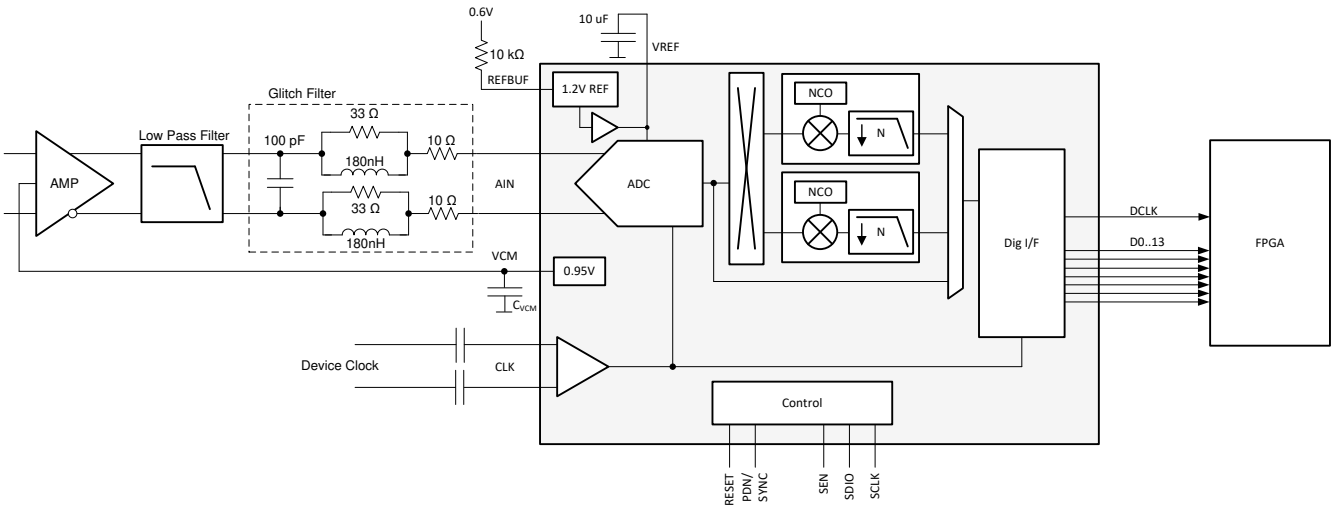

Figure 9-1. Typical configuration for a spectrum analyzer with DC support

9.2.1 Design Requirements

Frequency domain applications cover a wide range of frequencies from low input frequencies at or near DC in the 1st Nyquist zone to undersampling in higher Nyquist zones. If low input frequency is supported, then the input has to be DC coupled and the ADC driven by a fully differential amplifier (FDA). If low frequency support is not needed, then AC coupling and use of a balun may be more suitable.

The internal reference is used since DC precision is not needed. However, the ADC AC performance is dependent on the quality of the external clock source. If in-band interferers can be present, then the ADC SFDR performance is a key care about. A higher ADC sampling rate is desirable in order to relax the external anti-aliasing filter – an internal decimation filter can be used to reduce the digital output rate afterwards.

Table 9-1. Design key care-abouts

FEATURE	DESCRIPTION
Signal Bandwidth	DC to 30 MHz
Input Driver	Single ended to differential signal conversion and DC coupling
Clock Source	External clock with low jitter

When designing the amplifier/filter driving circuit, the ADC input full-scale voltage needs to be taken into consideration. For example, the ADC3544 input full-scale is 2.25 Vpp. When factoring in ~ 1 dB for insertion loss of the filter, then the amplifier needs to deliver close to 2.5 Vpp. The amplifier distortion performance degrades

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with a larger output swing and considering the ADC common mode input voltage the amplifier may not be able to deliver the full swing. The ADC3544 provides an output common mode voltage of 0.95V and the THS4541 for example can only swing within 250 mV of its negative supply. A unipolar 3.3 V amplifier power supply will thus limit the maximum voltage swing to ~ 2.8Vpp. Additionally input voltage protection diodes may be needed to protect the ADC from over-voltage events.

Table 9-2. Output voltage swing of THS4541 vs power supply

DEVICE	MIN OUTPUT VOLTAGE	MAX SWING WITH 3.3 V/ 0 V SUPPLY
THS4541	VS- + 250 mV	2.8 Vpp

9.2.2 Detailed Design Procedure

9.2.2.1 Input Signal Path

The THS4541 provides a good low power option to drive the ADC inputs. Table 9-3 provides an overview of the THS4541 with power consumption and usable frequency.

Table 9-3. Fully Differential Amplifier Options

DEVICE	CURRENT (IQ) PER CHANNEL	USABLE FREQUENCY RANGE
THS4541	10 mA	< 70 MHz

The low pass filter design (topology, filter order) is driven by the application itself. However, when designing the low pass filter, the optimum load impedance for the amplifier must be taken into consideration as well. Between the low pass filter and the ADC input the sampling glitch filter needs to added as well as shown in Section 8.3.1.2.1. In this example the DC - 30 MHz glitch filter is selected.

9.2.2.2 Sampling Clock

Applications operating with low input frequencies (such as DC to 20 MHz) typically are less sensitive to performance degradation due to clock jitter. The internal ADC aperture jitter improves with faster rise and fall times (i.e. square wave vs sine wave). Table 9-4 provides an overview of the estimated SNR performance of the ADC3544 based on different amounts of jitter of the external clock source. The SNR is estimated based on ADC3544 thermal noise of 74 dBFS and input signal at -1dBFS.

Table 9-4. ADC SNR performance across vs input frequency for different amounts of external clock jitter

INPUT FREQUENCY	$T_{J,EXT}$ = 100 fs	$T_{J,EXT}$ = 250 fs	$T_{J,EXT}$ = 500 fs	$T_{J,EXT}$ = 1 ps
10 MHz	74.0	74.0	73.9	73.7
20 MHz	73.9	73.9	73.6	72.8
30 MHz	73.8	73.7	73.2	71.6

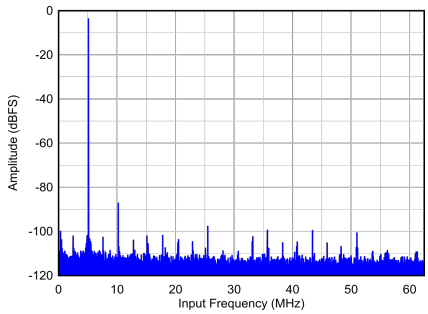
Termination of the clock input should be considered for long clock traces.

9.2.2.3 Voltage Reference

The ADC3544 is configured to internal reference operation by applying 0.6 V to the REFBUF pin.

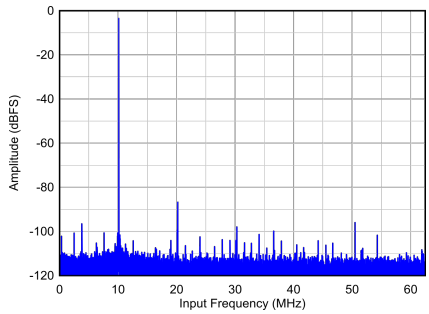
9.2.3 Application Curves

The following FFT plots show the performance of THS4541 driving the ADC3544 operated at 125 MSPS with a full-scale input at -1 dBFS. The FFT spectrum also shows the response of the low pass filter located between the THS4541 and the glitch filter with a 30 MHz corner frequency.



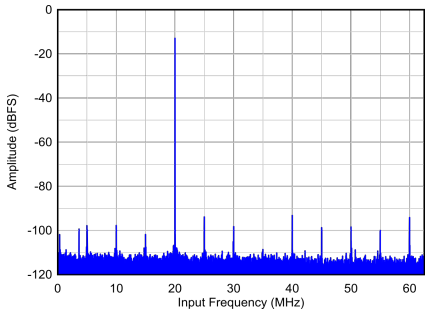
A_{IN} = - 1 dBFS, SNR = 73.2 dBFS, SFDR = 84 dBFS

Figure 9-2. 5 MHz FFT (THS4541 FDA)



A_{IN} = - 1 dBFS, SNR = 73 dBFS, SFDR = 84 dBFS

Figure 9-3. 10.1 MHz FFT (THS4541 FDA)



A_{IN} = - 10 dBFS, SNR = 73.5 dBFS, SFDR = 90 dBFS

Figure 9-4. 20 MHz FFT (THS4541 FDA)

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9.3 Initialization Set Up

After power-up, the internal registers must be initialized to their default values through a hardware reset by applying a high pulse on the RESET pin, as shown in Figure 9-5.

1. Apply AVDD and IOVDD (no specific sequence required). After AVDD is applied the internal bandgap reference will power up and settle out in ~ 2 ms.
2. Configure REFBUF pin (pull high or low even if configured via SPI later on) and apply the sampling clock.
3. Apply hardware reset. After hardware reset is released, the default registers are loaded from internal fuses and the internal power up capacitor calibration is initiated. The calibration takes approximately 200000 clock cycles.
4. Begin programming using SPI interface.

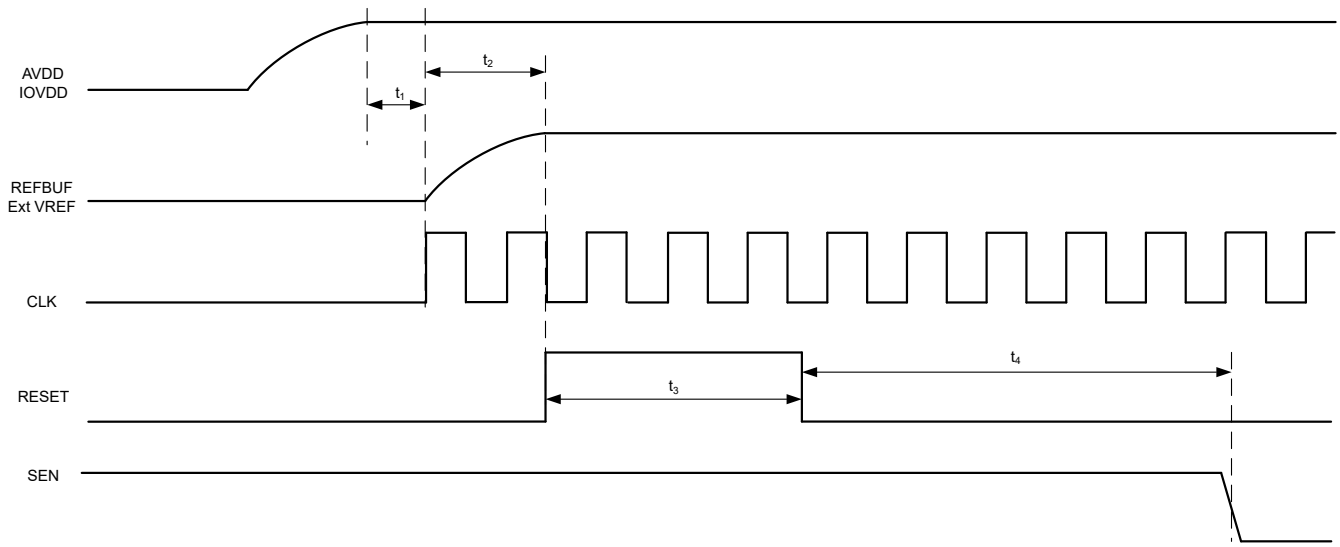

Figure 9-5. Initialization of serial registers after power up

Table 9-5. Power-up timing

		MIN	TYP	MAX	UNIT
t_1	Power-on delay: delay from power up to logic level of REFBUF pin	2			ms
t_2	Delay from REFBUF pin logic level to RESET rising edge	100			ns
t_3	RESET pulse width	1			us
t_4	Delay from RESET disable to SEN active	~ 200000			clock cycles

9.3.1 Register Initialization During Operation

If required, the serial interface registers can be cleared and reset to default settings during operation either:

- through a hardware reset or
- by applying a software reset. When using the serial interface, set the RESET bit (D0 in register address 0x00) high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low.

After hardware or software reset the wait time is also ~ 200000 clock cycles before the SPI registers can be programmed.

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9.4 Power Supply Recommendations

The ADC3544 requires two different power-supplies. The AVDD rail provides power for the internal analog circuits and the ADC itself while the IOVDD rail powers the digital interface and the internal digital circuits like decimation filter or output interface mapper. Power sequencing is not required.

The AVDD power supply must be low noise in order to achieve data sheet performance. In applications operating near DC, the 1/f noise contribution of the power supply must be considered as well. The ADC is designed for good PSRR which aides with the power supply filter design.

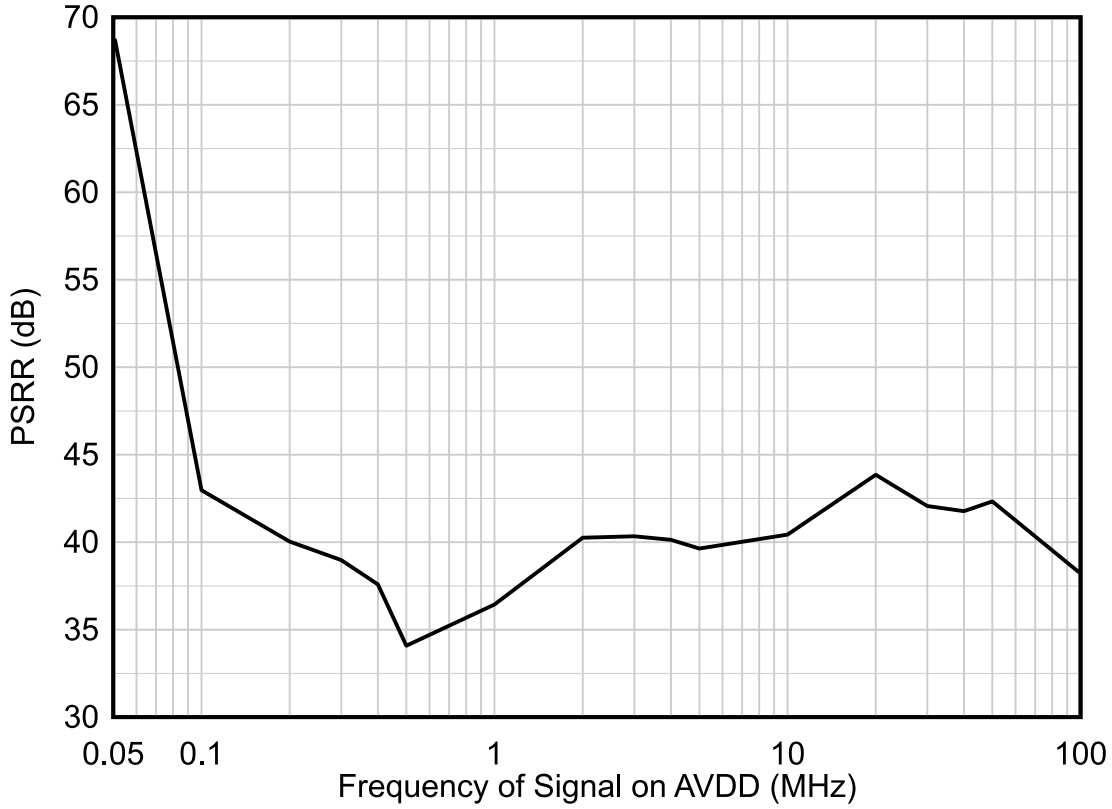

Figure 9-6. Power supply rejection ratio (PSRR) vs frequency

There are two recommended power-supply architectures:

1. Step down using high-efficiency switching converters, followed by a second stage of regulation using a low noise LDO to provide switching noise reduction and improved voltage accuracy.
2. Directly step down the final ADC supply voltage using high-efficiency switching converters. This approach provides the best efficiency, but care must be taken to ensure switching noise is minimized to prevent degraded ADC performance.

TI WEBENCH® Power Designer can be used to select and design the individual power-supply elements needed: see the WEBENCH® Power Designer

Recommended switching regulators for the first stage include the TPS62821, and similar devices.

Recommended low dropout (LDO) linear regulators include the TPS7A4701, TPS7A90, LP5901, and similar devices.

For the switch regulator only approach, the ripple filter must be designed with a notch frequency that aligns with the switching ripple frequency of the DC/DC converter. Note the switching frequency reported from WEBENCH® and design the EMI filter and capacitor combination to have the notch frequency centered as needed. Figure 9-7 and Figure 9-8 illustrate the two approaches.

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AVDD and IOVDD supply voltages should not be shared in order to prevent digital switching noise from coupling into the analog signal chain.

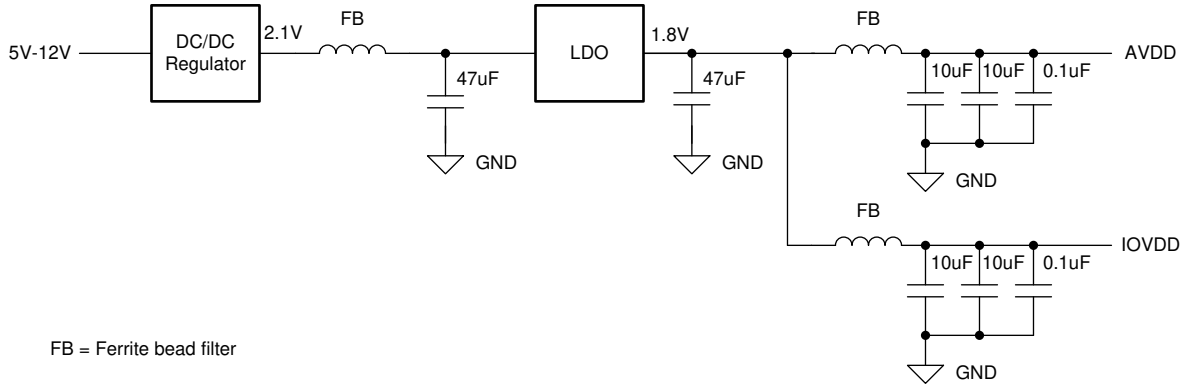

Figure 9-7. Example: LDO Linear Regulator Approach

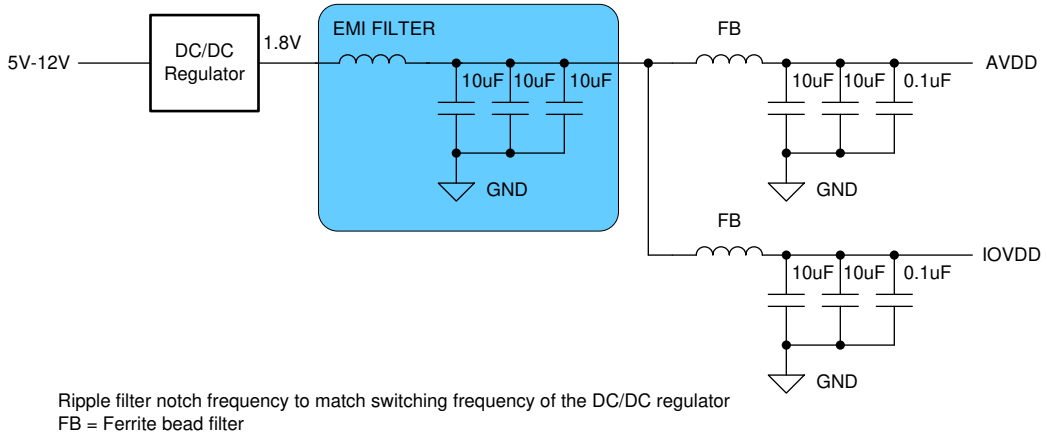

Figure 9-8. Example Switcher-Only Approach

9.5 Layout

9.5.1 Layout Guidelines

There are several critical signals which require specific care during board design:

1. Analog input and clock signals
   - Traces should be as short as possible and vias should be avoided where possible to minimize impedance discontinuities.
   - Traces should be routed using loosely coupled 100-Ω differential traces.
   - Differential trace lengths should be matched as close as possible to minimize phase imbalance and HD2 degradation.
2. Digital output interface
   - A 20 ohm series isolation resistor should be used on each CMOS output and placed close the digital output. This isolation resistor limits the output current into the capacitive load and thus minimizes the switching noise inside the ADC. When driving longer distances a buffer should be used. The resistor value should be optimized for the desired output data rate.
3. Voltage reference
   - The bypass capacitor should be placed as close to the device pins as possible and connected between VREF and REFGND – on top layer avoiding vias.
   - Depending on configuration an additional bypass capacitor between REFBUF and REFGND may be recommended and should also be placed as close to pins as possible on top layer.
4. Power and ground connections
   - Provide low resistance connection paths to all power and ground pins.
   - Use power and ground planes instead of traces.
   - Avoid narrow, isolated paths which increase the connection resistance.
   - Use a signal/ground/power circuit board stackup to maximize coupling between the ground and power plane.

9.5.2 Layout Example

The following screen shot shows the top layer of the ADC3544 EVM.

- Signal and clock inputs are routed as differential signals on the top layer avoiding vias.
- CMOS output interface lanes with isolation resistor and digital buffer.
- Bypass caps are close to the VREF pin on the top layer avoiding vias.

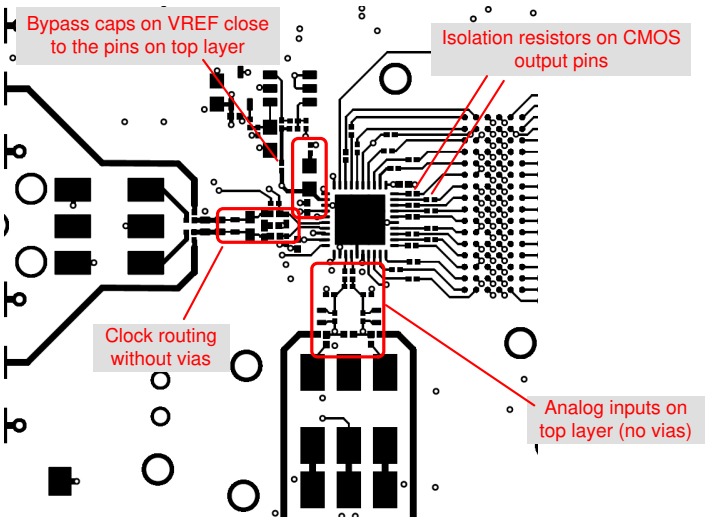

Figure 9-9. Layout example: top layer of ADC3544 EVM

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10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Trademarks

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10.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.4 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADC3544IRSBR	Active	Production	WQFN (RSB) | 40	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	AZ3544
ADC3544IRSBR.A	Active	Production	WQFN (RSB) | 40	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	AZ3544
ADC3544IRSBT	Active	Production	WQFN (RSB) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	AZ3544
ADC3544IRSBT.A	Active	Production	WQFN (RSB) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	AZ3544

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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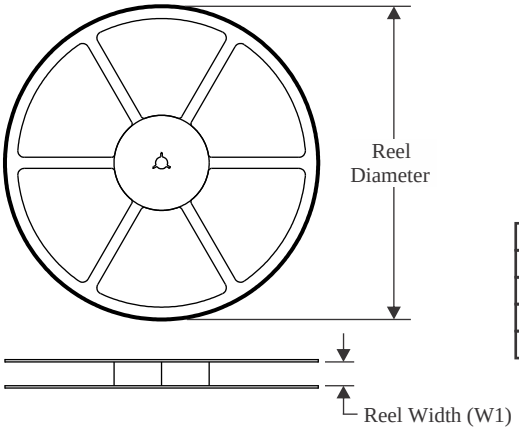
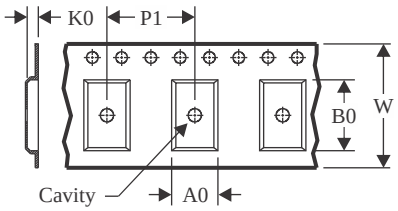
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

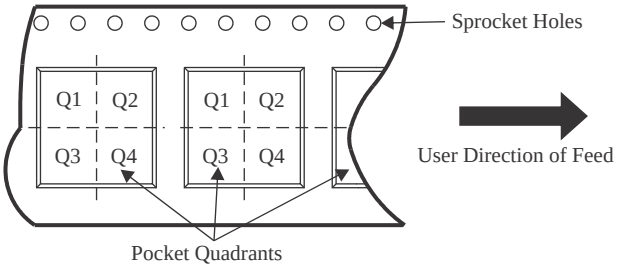


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

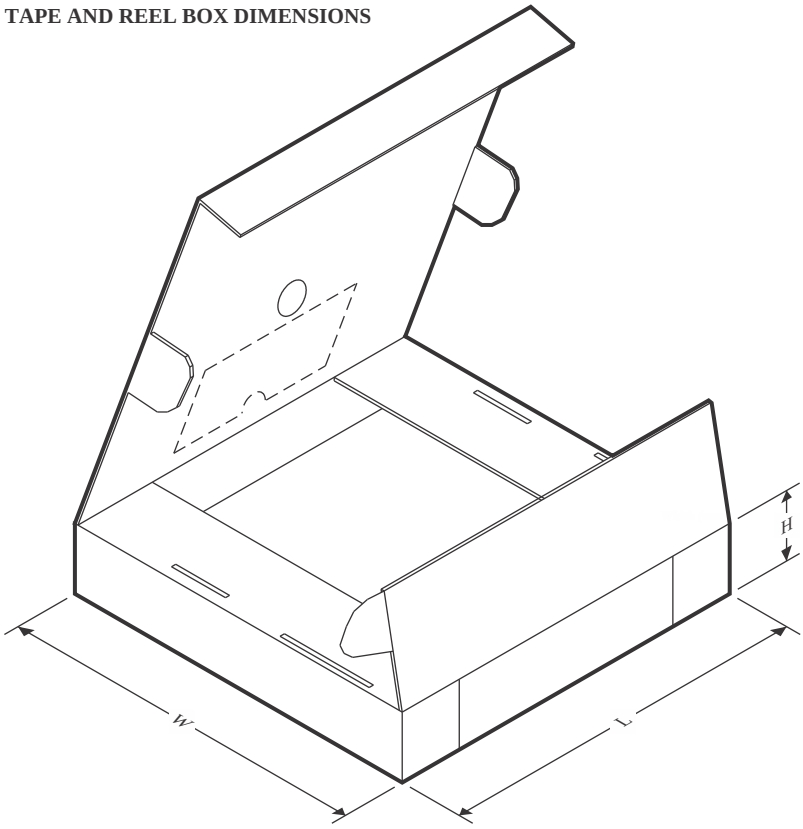
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC3544IRSBR	WQFN	RSB	40	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

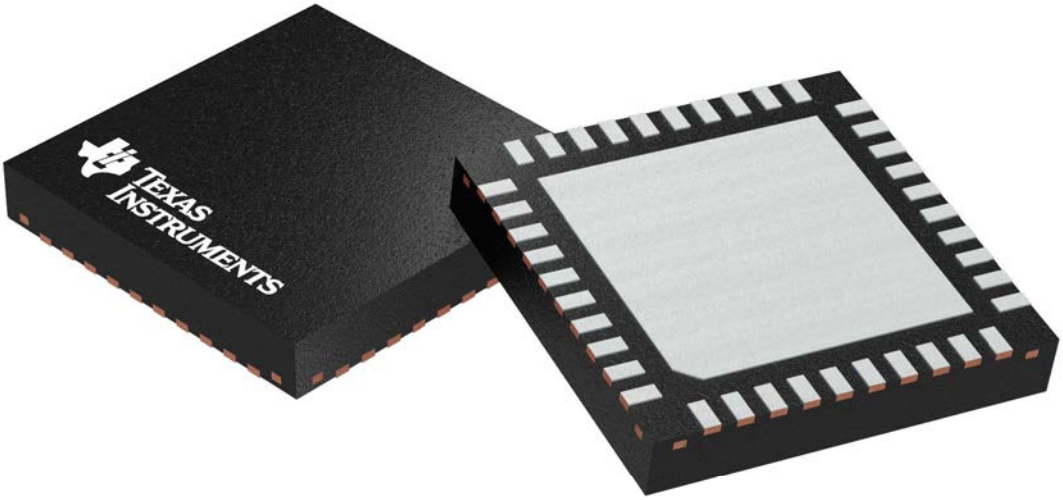
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC3544IRSBR	WQFN	RSB	40	3000	350.0	350.0	43.0

RSB 40

WQFN - 0.8 mm max height

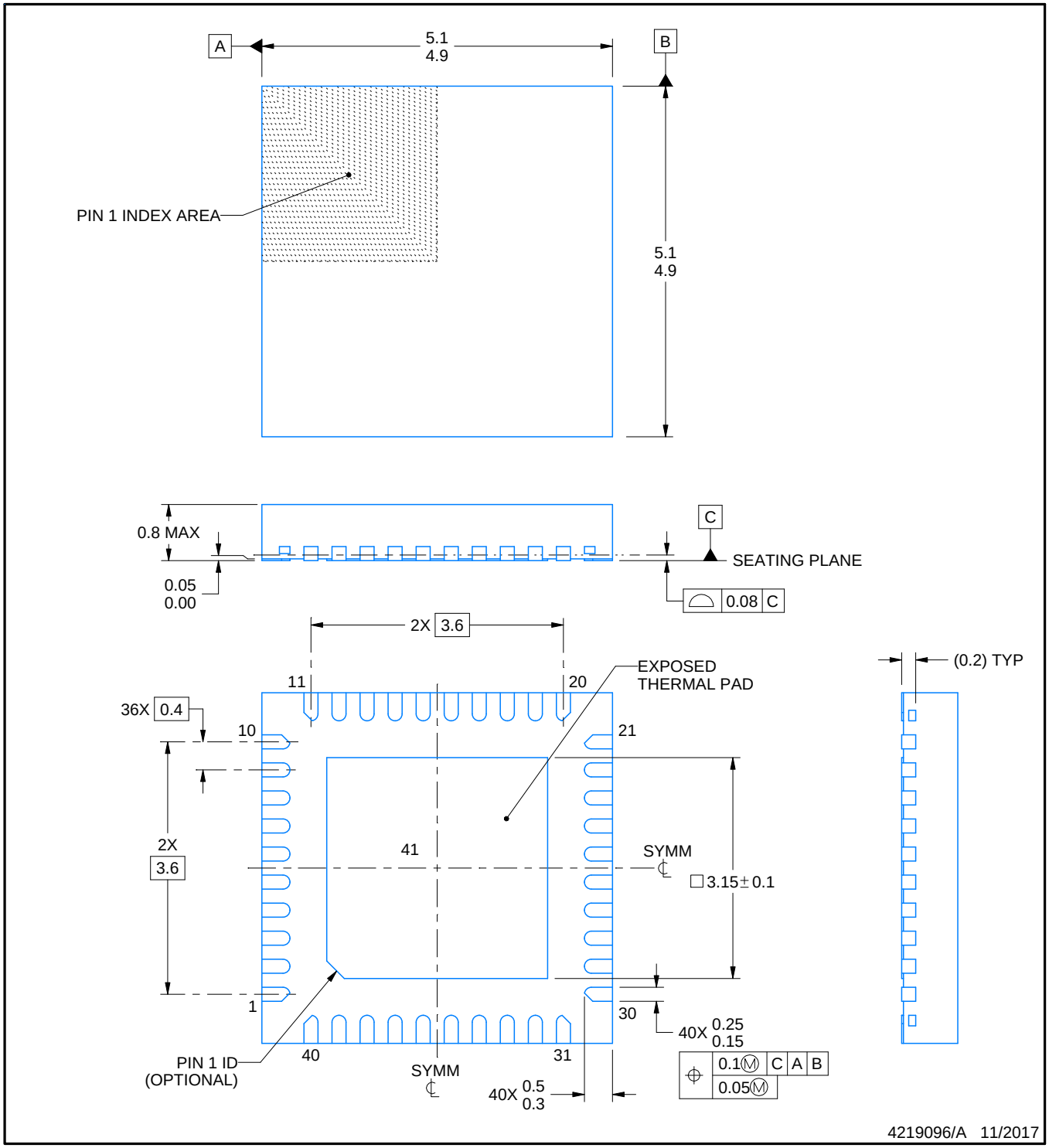
PLASTIC QUAD FLATPACK - NO LEAD

5 x 5 mm, 0.4 mm pitch



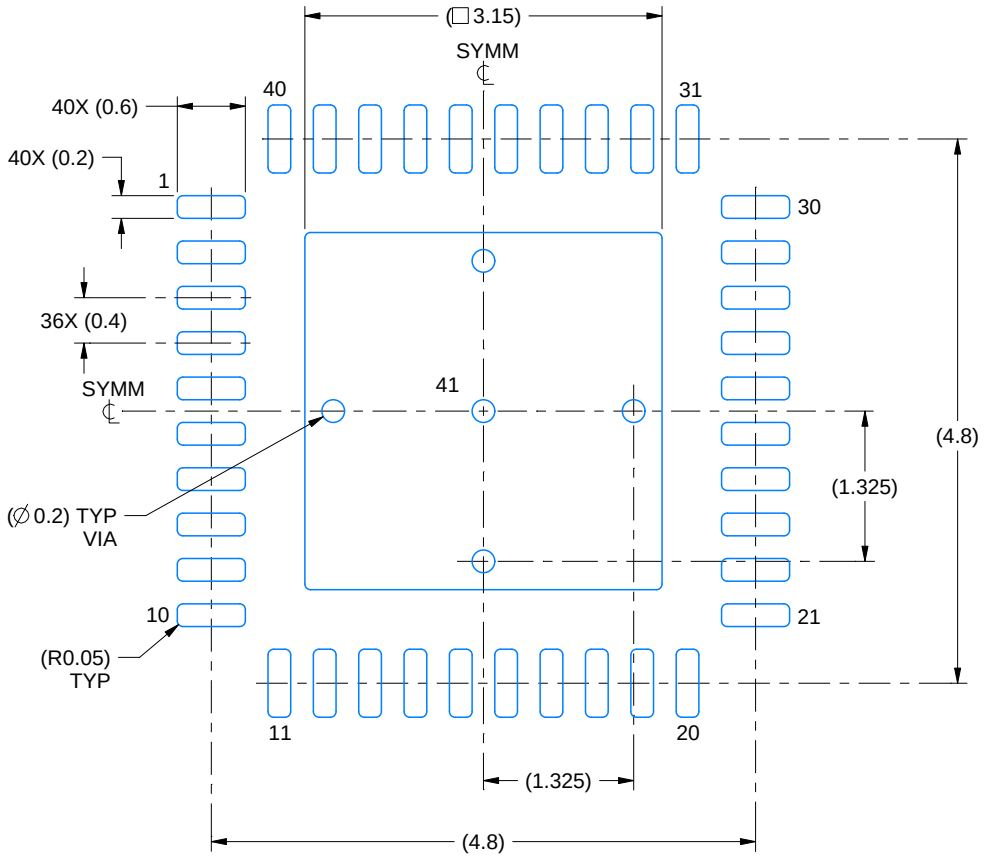
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

TEXAS INSTRUMENTS

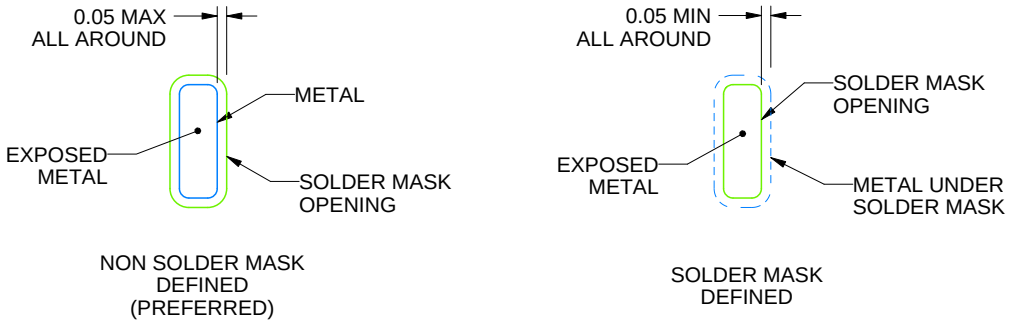


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

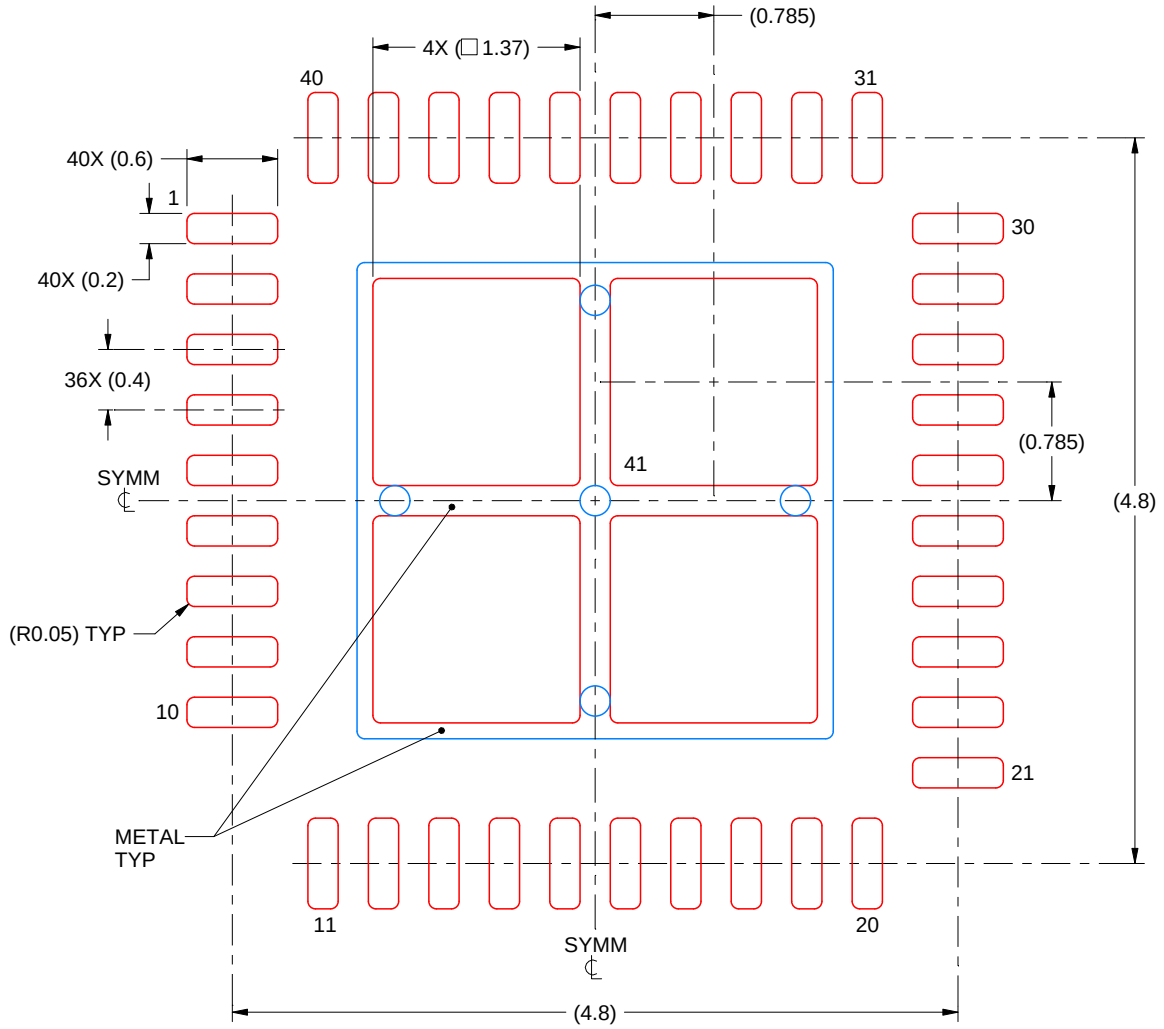


SOLDER MASK DETAILS

4219096/A 11/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 41
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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