

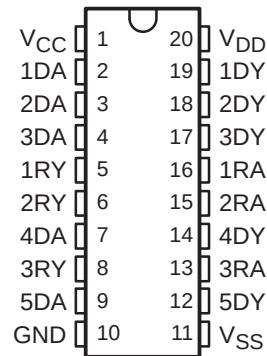
SN75196

MULTIPLE RS-232 DRIVERS AND RECEIVERS

SLLS188B – MAY 1995 – REVISED APRIL 1998

- Single Chip With Easy Interface Between UART and Serial-Port Connector of an External Modem or Other Computer Peripheral
- Five Drivers and Three Receivers Meet or Exceed the Requirements of TIA/EIA-232-F and ITU Recommendation V.28
- Designed to Support Data Rates up to 120 kbit/s
- ESD Protection Meets Or Exceeds 10 kV on RS-232 Pins and 5 kV on All Other Pins (Human-Body Model)
- Complement to the SN75185
- Pin-to-Pin Replacement for the Goldstar GD75323
- Functional Replacement for the MC145405

DW OR N PACKAGE
(TOP VIEW)



description

The SN75196 combines five drivers and three receivers from the trade-standard SN75188 and SN75189 bipolar quadruple drivers and receivers, respectively. The flow-through design of the SN75196 decreases the part count, reduces the board space required, and allows easy interconnection of the UART and serial-port connector. The all-bipolar circuits and processing of the SN75196 provide a rugged, low-cost solution for this function.

The SN75196 complies with the requirements of TIA/EIA-232-F and ITU (formerly CCITT) V.28 standards. These standards are for data interchange between a host computer and peripheral at signal rates of up to 20 kbit/s. The switching speeds of the SN75196 are fast enough to support rates of up to 120 kbit/s with lower capacitive loads (shorter cables). Interoperability at the higher signaling rates cannot be assured unless the designer has design control of the cable and the interface circuits at both ends. For interoperability at signaling rates of up to 120 kbit/s, use of TIA/EIA-423-B (ITU V.10) and TIA/EIA-422-B (ITU V.11) standards are recommended.

The SN75196 is characterized for operation over a temperature range of 0°C to 70°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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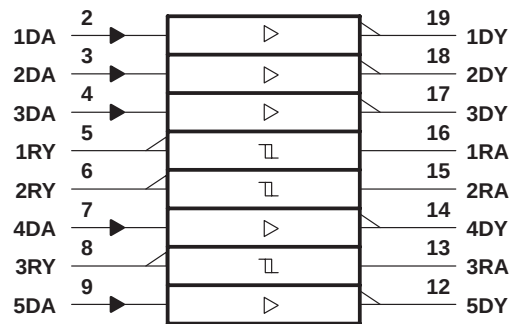
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SN75196

MULTIPLE RS-232 DRIVERS AND RECEIVERS

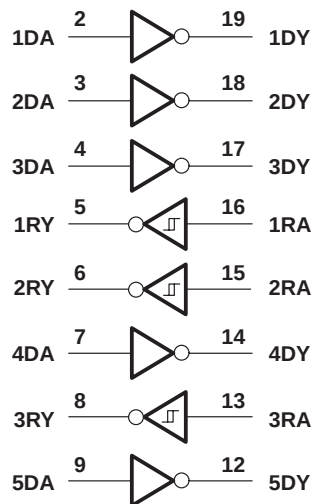
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logic symbol†

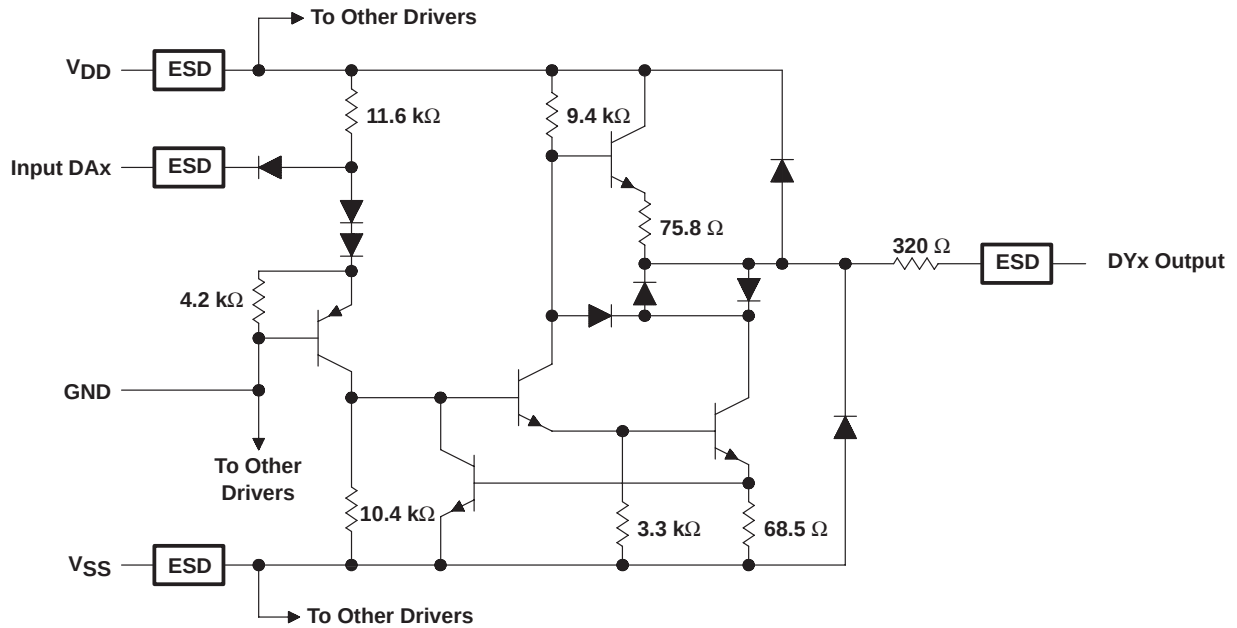


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

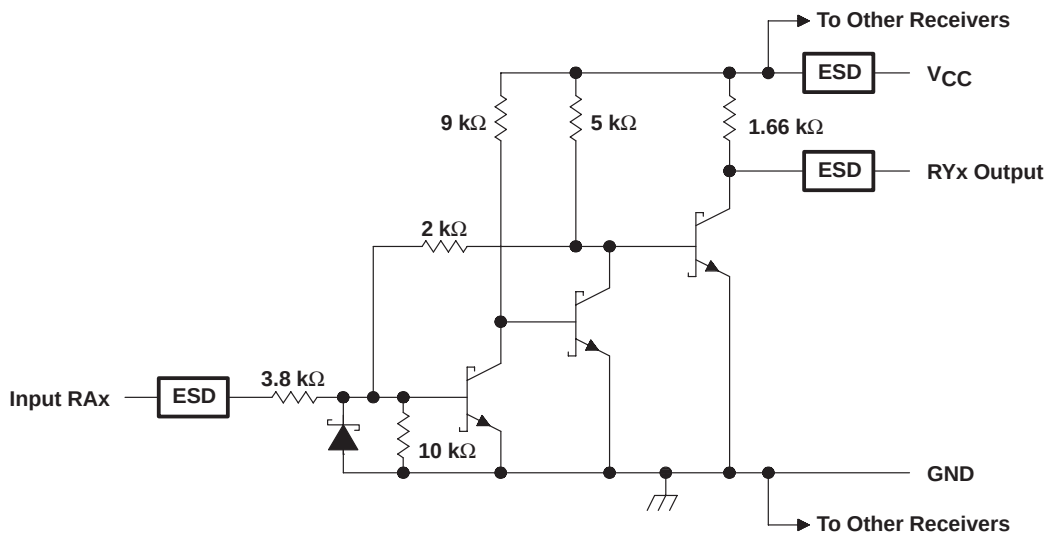


schematic of each driver



Resistor values shown are nominal.

schematic of each receiver



Resistor values shown are nominal.

SN75196

MULTIPLE RS-232 DRIVERS AND RECEIVERS

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absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Supply voltage, V_{CC} (see Note 1)	10 V
Supply voltage, V_{DD} (see Note 1)	15 V
Supply voltage, V_{SS} (see Note 1)	–15 V
Input voltage range, V_I : Driver	–15 V to 7 V
Receiver	–30 V to 30 V
Output voltage range, V_O (Driver)	–15 V to 15 V
Low-level output current, I_{OL} (Receiver)	20 mA
Continuous total power dissipation	See Dissipation Rating Table
Electrostatic discharge: DY and RA to GND (see Note 2)	Class 3, A: 10 kV, B: 500 V
All pins (see Note 2)	Class 3, A: 5 kV, B: 300 V
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to the network ground terminal.
2. Per MIL-PRF-38535, Method 3015.7

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR [‡] ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
N	1150 mW	9.2 mW/°C	736 mW

[‡] This is the inverse of the traditional junction-to-case thermal resistance ($R_{\theta JA}$).

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		7.5	9	13.5	V
Supply voltage, V_{SS}		–7.5	–9	–13.5	V
Supply voltage, V_{CC}		4.5	5	5.5	V
High-level input voltage, V_{IH}	Driver	1.9			V
Low-level input voltage, V_{IL}	Driver			0.8	V
High-level output current, I_{OH}	Driver			–6	mA
	Receiver			–0.5	
High-level output current, I_{OL}	Driver			6	mA
	Receiver			16	
Operating free-air temperature, T_A		0		70	°C



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supply currents over operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
I _{DD}	Supply current from V _{DD}	All inputs at 1.9 V,	No load	V _{DD} = 9 V, V _{SS} = −9 V	25	mA
				V _{DD} = 12 V, V _{SS} = −12 V	32	
		All inputs at 0.8 V,	No load	V _{DD} = 9 V, V _{SS} = −9 V	7.5	
				V _{DD} = 12 V, V _{SS} = −12 V	9.5	
I _{SS}	Supply current from V _{SS}	All inputs at 1.9 V,	No load	V _{DD} = 9 V, V _{SS} = −9 V	−25	mA
				V _{DD} = 12 V, V _{SS} = −12 V	−32	
		All inputs at 0.8 V,	No load	V _{DD} = 9 V, V _{SS} = −9 V	−5.3	
				V _{DD} = 12 V, V _{SS} = −12 V	−5.3	
I _{CC}	Supply current from V _{CC}	V _{CC} = 5 V,	All inputs at 5 V,	No load	20	mA

DRIVER SECTION

electrical characteristics over operating free-air temperature range, $V_{DD} = 9\text{ V}, V_{SS} = -9\text{ V}, V_{CC} = 5\text{ V},$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH} High-level output voltage	$V_{IL} = 0.8\text{ V},$	$R_L = 3\text{ k}\Omega,$	See Figure 1	6	7.5		V
V_{OL} Low-level output voltage (see Note 3)	$V_{IH} = 1.9\text{ V},$	$R_L = 3\text{ k}\Omega,$	See Figure 1	-7.5	-6		V
I_{IH} High-level input current	$V_I = 5\text{ V},$	See Figure 2				10	μA
I_{IL} Low-level input current	$V_I = 0,$	See Figure 2				-1.6	mA
$I_{OS(H)}$ High-level short-circuit output current (see Note 4)	$V_{IL} = 0.8\text{ V},$	$V_O = 0,$	See Figure 1	-4.5	-9	-19.5	mA
$I_{OS(L)}$ Low-level short-circuit output current (see Note 4)	$V_{IH} = 2\text{ V},$	$V_O = 0,$	See Figure 1	4.5	9	19.5	mA
r_o Output resistance (see Note 5)	$V_{CC} = V_{DD} = V_{SS} = 0, V_O = -2\text{ V to } 2\text{ V}$			300			Ω

NOTES: 3. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if -10 V is a maximum, the typical value is a more negative voltage.
4. Output short-circuit conditions must maintain the total power dissipation below absolute maximum ratings.
5. Test conditions are those specified by TIA/EIA-232-F and as listed above.

switching characteristics, $V_{DD} = 12\text{ V}, V_{SS} = -12\text{ V}, V_{CC} = 5\text{ V} \pm 10\%, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low- to high-level output	$R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega,$	$C_L = 15\text{ pF},$	See Figure 3		315	500	ns
t_{PHL} Propagation delay time, high- to low-level output	$R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega,$	$C_L = 15\text{ pF},$	See Figure 3		75	175	ns
t_{TLH} Transition time, low- to high-level output (see Note 6)	$R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$	$C_L = 15\text{ pF},$	See Figure 3		60	100	ns
		$C_L = 2500\text{ pF},$	See Figure 3 and Note 6		1.7	2.5	μs
t_{THL} Transition time, high- to low-level output (see Note 7)	$R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$	$C_L = 15\text{ pF},$	See Figure 3		40	75	ns
		$C_L = 2500\text{ pF},$	See Figure 3 and Note 7		1.5	2.5	μs

NOTES: 6. Measured between -3-V and 3-V points of the output waveform (TIA/EIA-232-F conditions), all unused inputs are tied either high or low.
7. Measured between 3-V and -3-V points of the output waveform (TIA/EIA-232-F conditions), all unused inputs are tied either high or low.

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MULTIPLE RS-232 DRIVERS AND RECEIVERS

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RECEIVER SECTION

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{IT+}	Positive-going input threshold voltage	See Figure 5	T _A = 25°C	1.75	1.9	2.3	V
			T _A = 0°C to 70 °C	1.55		2.3	
V _{IT–}	Negative-going input threshold voltage	See Figure 5		0.75	0.97	1.25	V
V _{hys}	Input hysteresis (V _{IT+} – V _{IT–})	See Figure 5		0.5			V
V _{OH}	High-level output voltage	I _{OH} = –0.5 mA, See Figure 5	V _{IH} = 0.75 V	2.6	4	5	V
			Inputs open	2.6			
V _{OL}	Low-level input voltage	I _{OL} = 10 mA, V _I = 3 V, See Figure 5			0.2	0.45	V
I _{IH}	High-level input current	V _I = 25 V		3.6		8.3	mA
		V _I = 3 V		0.43			
I _{IL}	Low-level input current	V _I = –25 V		–3.6		–8.3	mA
		V _I = –3 V		–0.43			
I _{OS}	Short-circuit output current	See Figure 4			–3.4	–12	mA

[†] All typical values are at $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$, $V_{DD} = 9\text{ V}$, and $V_{SS} = -9\text{ V}$.

switching characteristics, $V_{CC} = 5\text{ V}$, $V_{DD} = 12\text{ V}$, $V_{SS} = -12\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low- to high-level output	$C_L = 50\text{ pF}$, $R_L = 5\text{ k}\Omega$, See Figure 6		107	500	ns
t_{PHL} Propagation delay time, high- to low-level output	$C_L = 50\text{ pF}$, $R_L = 5\text{ k}\Omega$, See Figure 6		42	150	ns
t_{TLH} Transition time, low- to high-level output	$C_L = 50\text{ pF}$, $R_L = 5\text{ k}\Omega$, See Figure 6		175	525	ns
t_{THL} Transition time, high- to low-level output	$C_L = 50\text{ pF}$, $R_L = 5\text{ k}\Omega$, See Figure 6		16	60	ns



PARAMETER MEASUREMENT INFORMATION

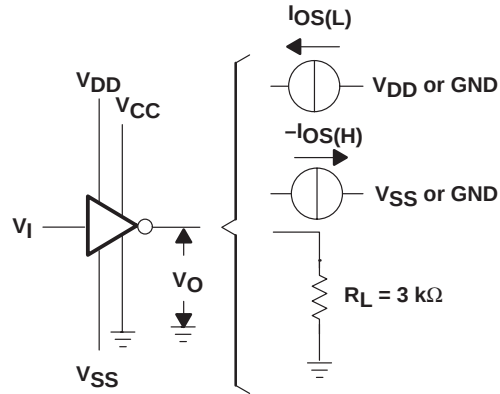


Figure 1. Driver Test Circuit for V_{OH} , V_{OL} , $I_{OS(H)}$, and $I_{OS(L)}$

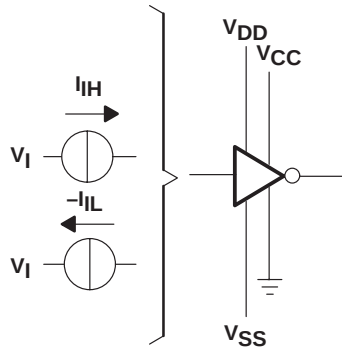
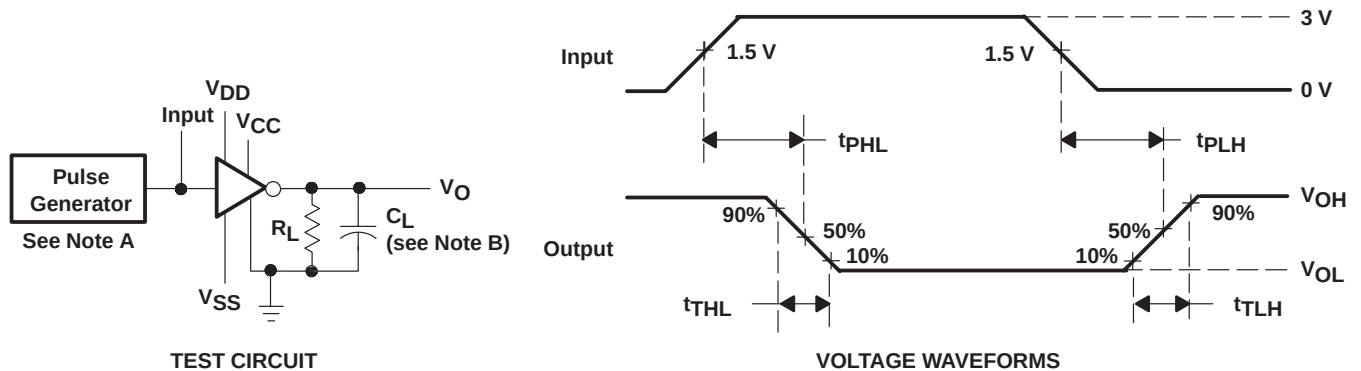


Figure 2. Driver Test Circuit for I_{IH} and I_{IL}



- NOTES: A. The pulse generator has the following characteristics: $t_W = 25\text{ }\mu\text{s}$, $\text{PRR} = 20\text{ kHz}$, $Z_O = 50\text{ }\Omega$, $t_r = t_f < 50\text{ ns}$.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION

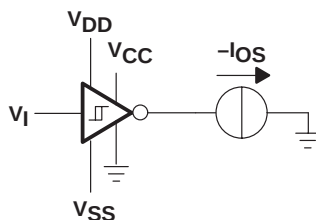


Figure 4. Receiver Test Circuit for I_{OS}

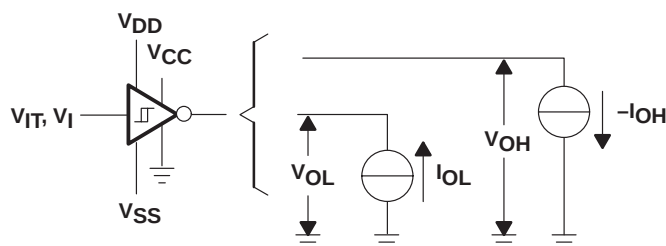
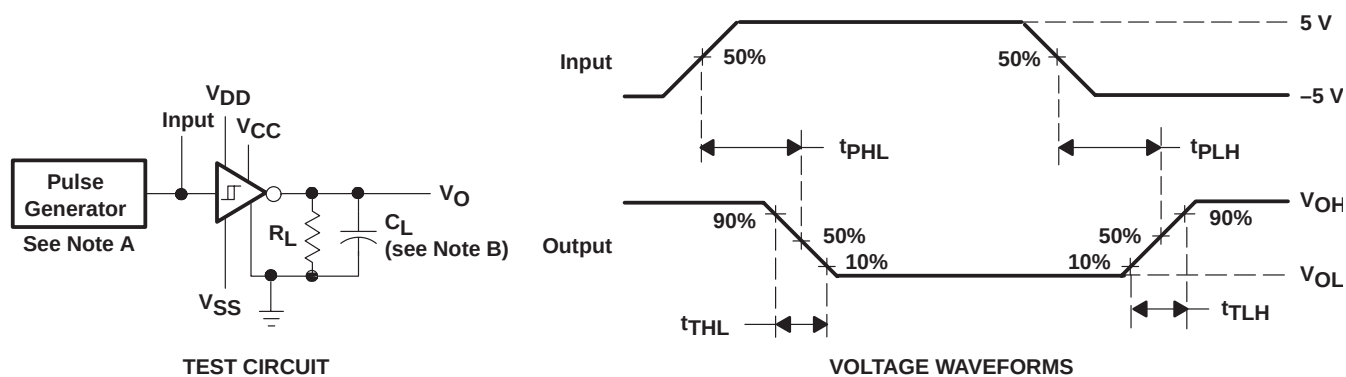


Figure 5. Receiver Test Circuit for V_{IT} , V_{OH} , and V_{OL}



NOTES: A. The pulse generator has the following characteristics: $t_W = 25 \mu s$, $PRR = 20 \text{ kHz}$, $Z_O = 50 \Omega$, $t_r = t_f < 50 \text{ ns}$.
B. C_L includes probe and jig capacitance.

Figure 6. Receiver Propagation and Transition Times

TYPICAL CHARACTERISTICS

DRIVER SECTION

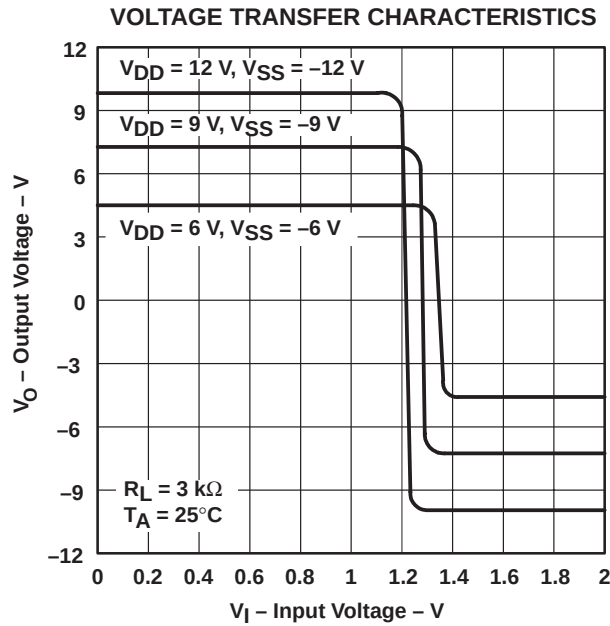


Figure 7

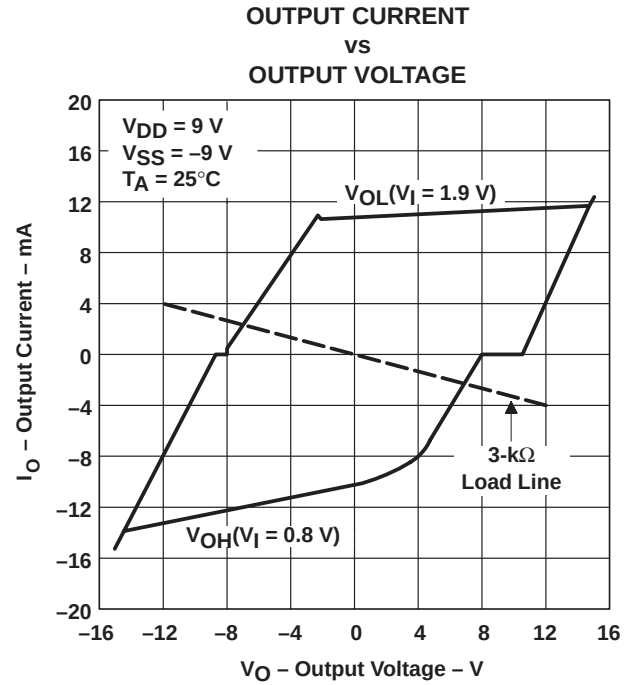


Figure 8

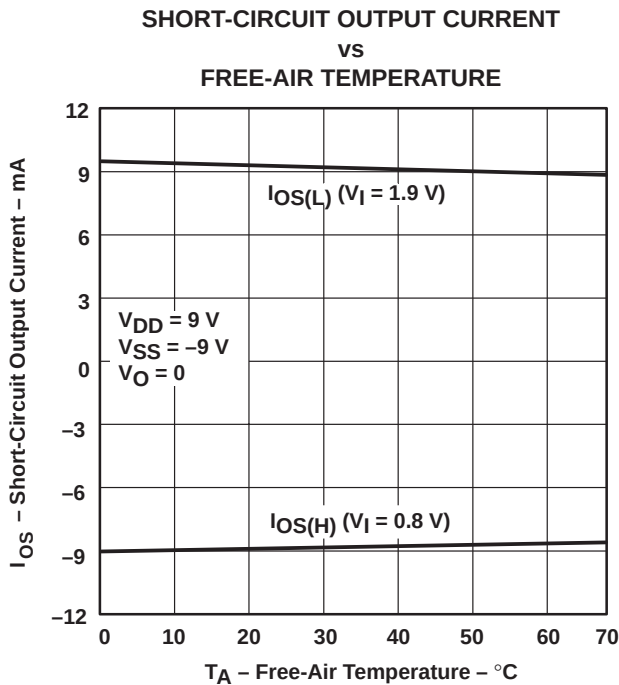


Figure 9

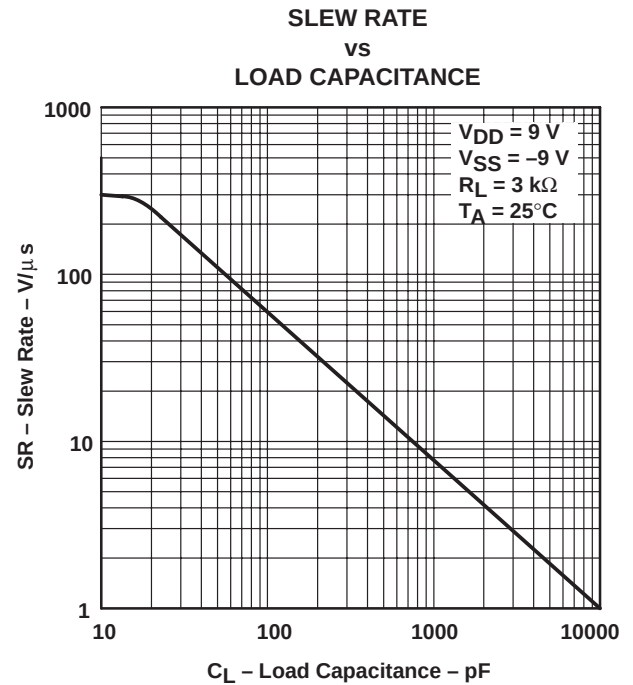


Figure 10

TYPICAL CHARACTERISTICS
RECEIVER SECTION

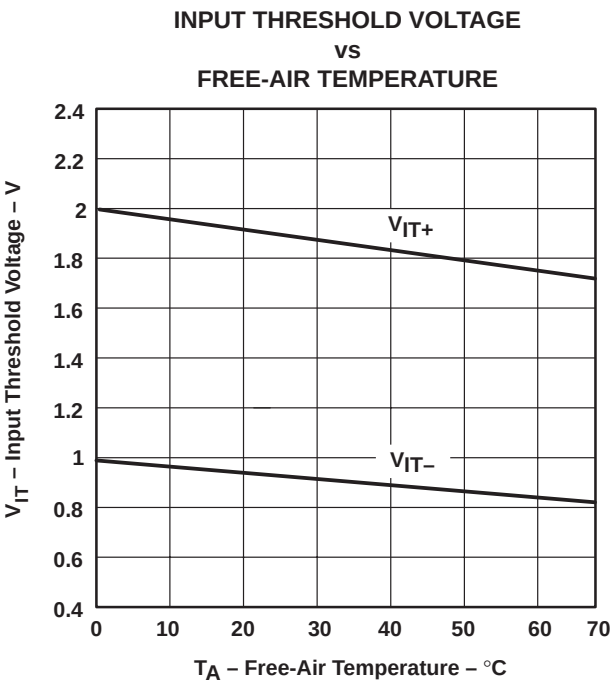


Figure 11

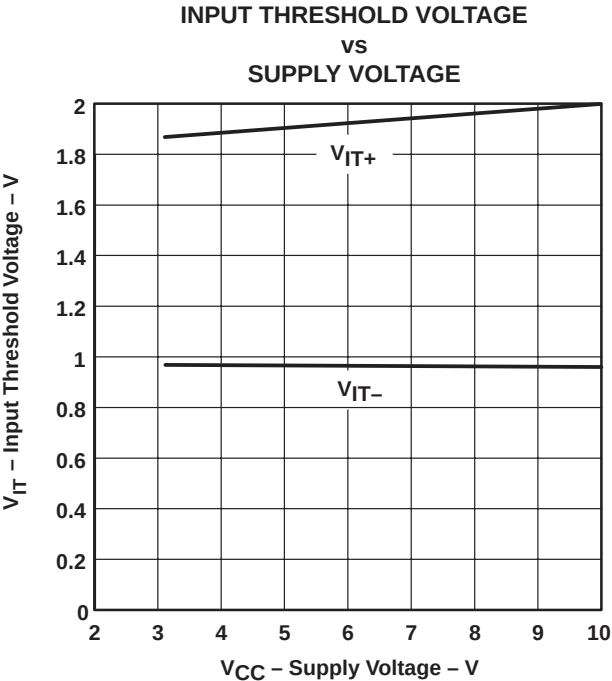
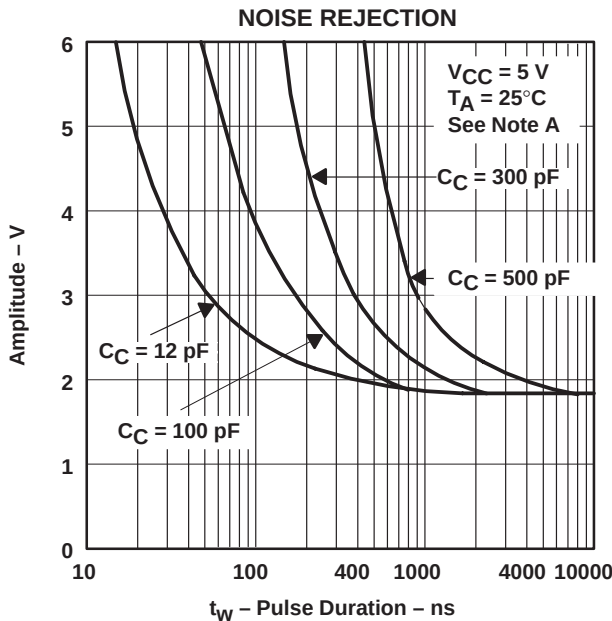


Figure 12



NOTE A: This figure shows the maximum amplitude of a positive-going pulse that, starting from 0 V, does not cause a change of the output level.

Figure 13

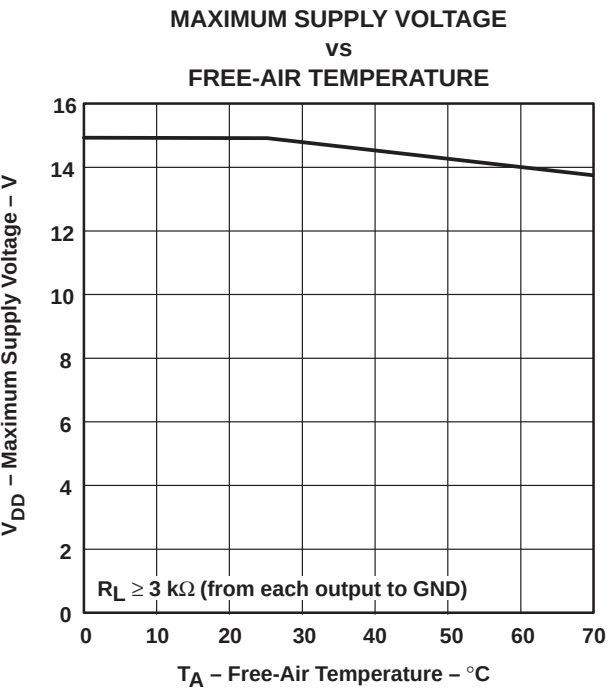


Figure 14

APPLICATION INFORMATION

Diodes placed in series with the V_{DD} and V_{SS} terminals protect the SN75196 in the fault condition when the device outputs are shorted to V_{DD} or V_{SS} and the power supplies are at low and provide low-impedance paths to ground (see Figure 15).

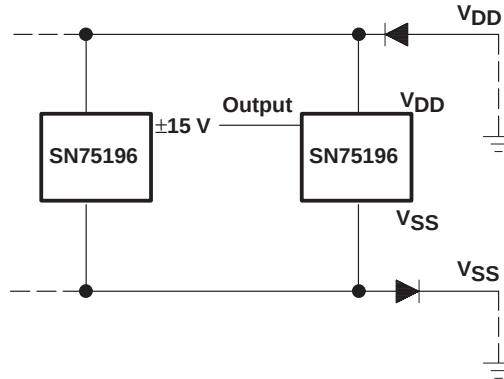
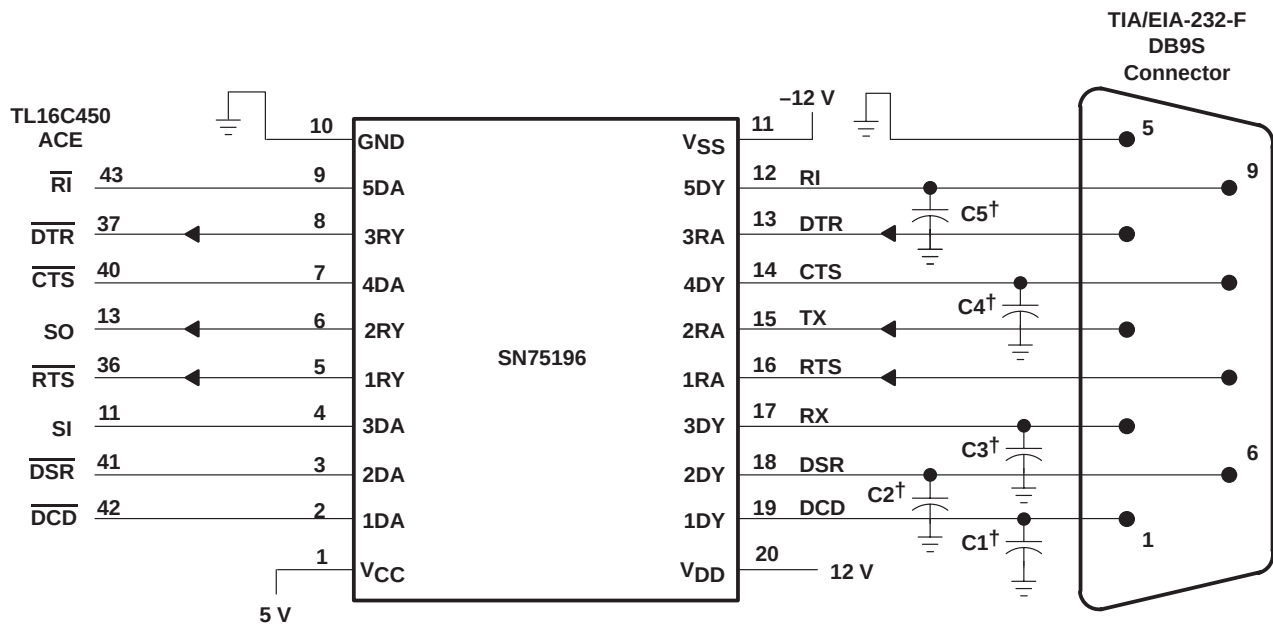


Figure 15. Power-Supply Protection to Meet Power-Off Fault Conditions of TIA/EIA-232-F



† See Figure 10 to select the correct values for the loading capacitors (C1, C2, C3, C4, and C5), which may be required to meet the RS-232 maximum slew-rate requirement of 30 V/μs. The value of the loading capacitors required depends upon the line length and desired slew rate, but is typically 330 pF.

NOTE A: To use the receivers only, V_{DD} and V_{SS} must both be powered or tied to ground.

Figure 16. Typical TIA/EIA-232-F Connection

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75196DW	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75196
SN75196DW.A	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75196
SN75196DWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75196
SN75196DWR.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75196

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

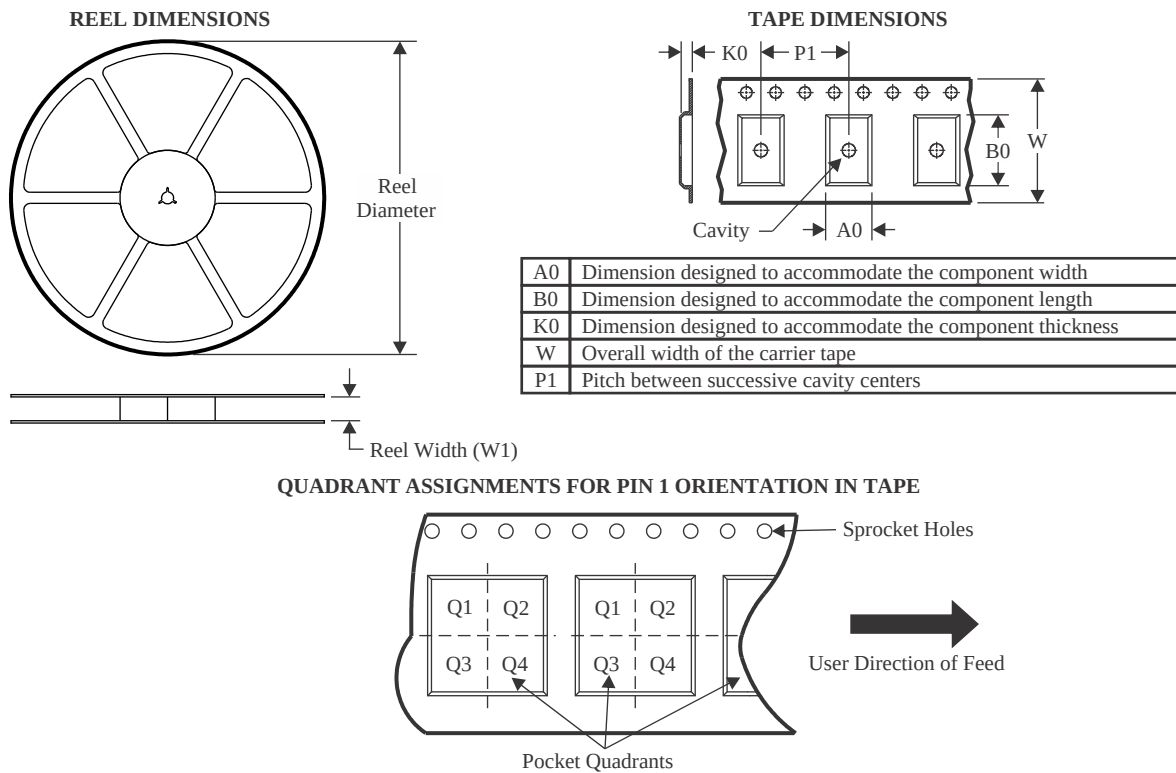
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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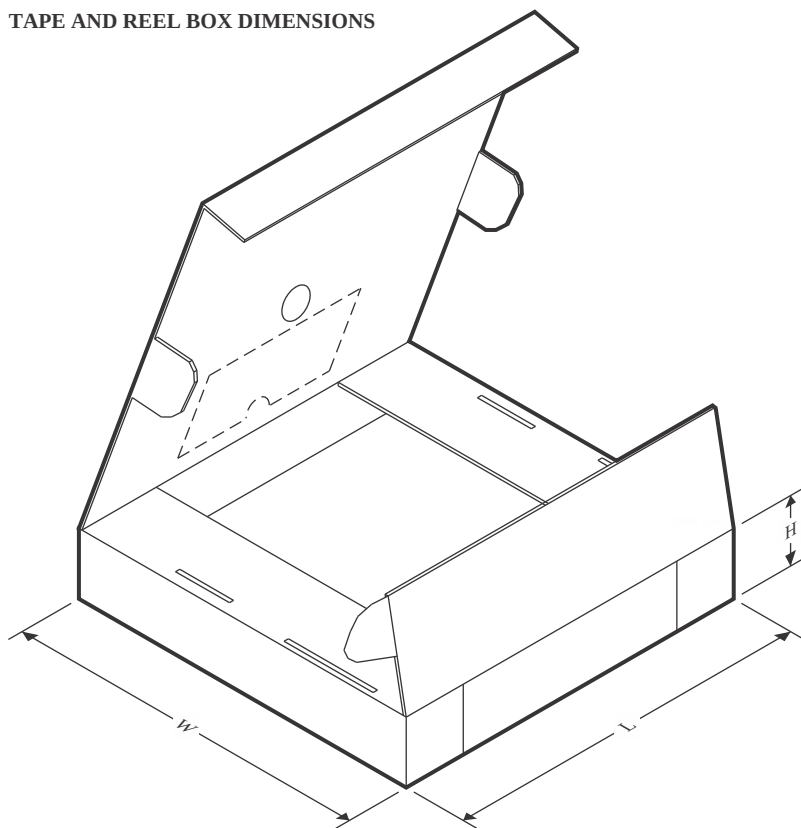
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75196DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

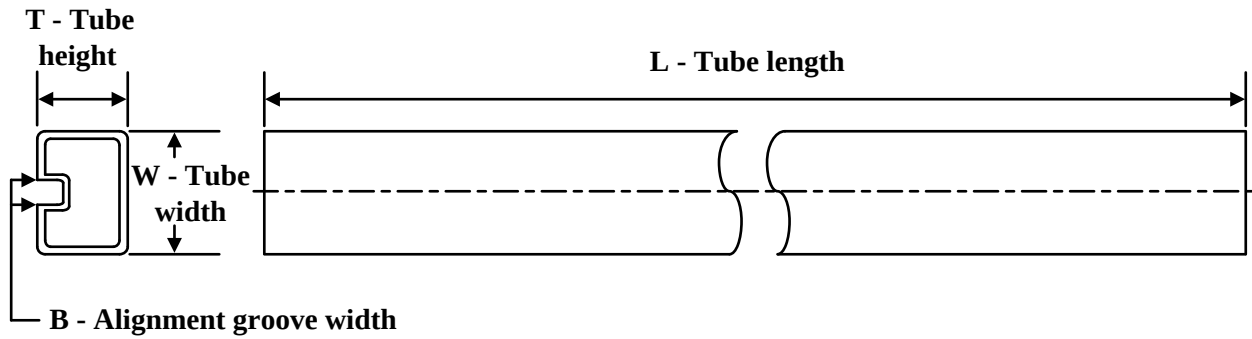
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

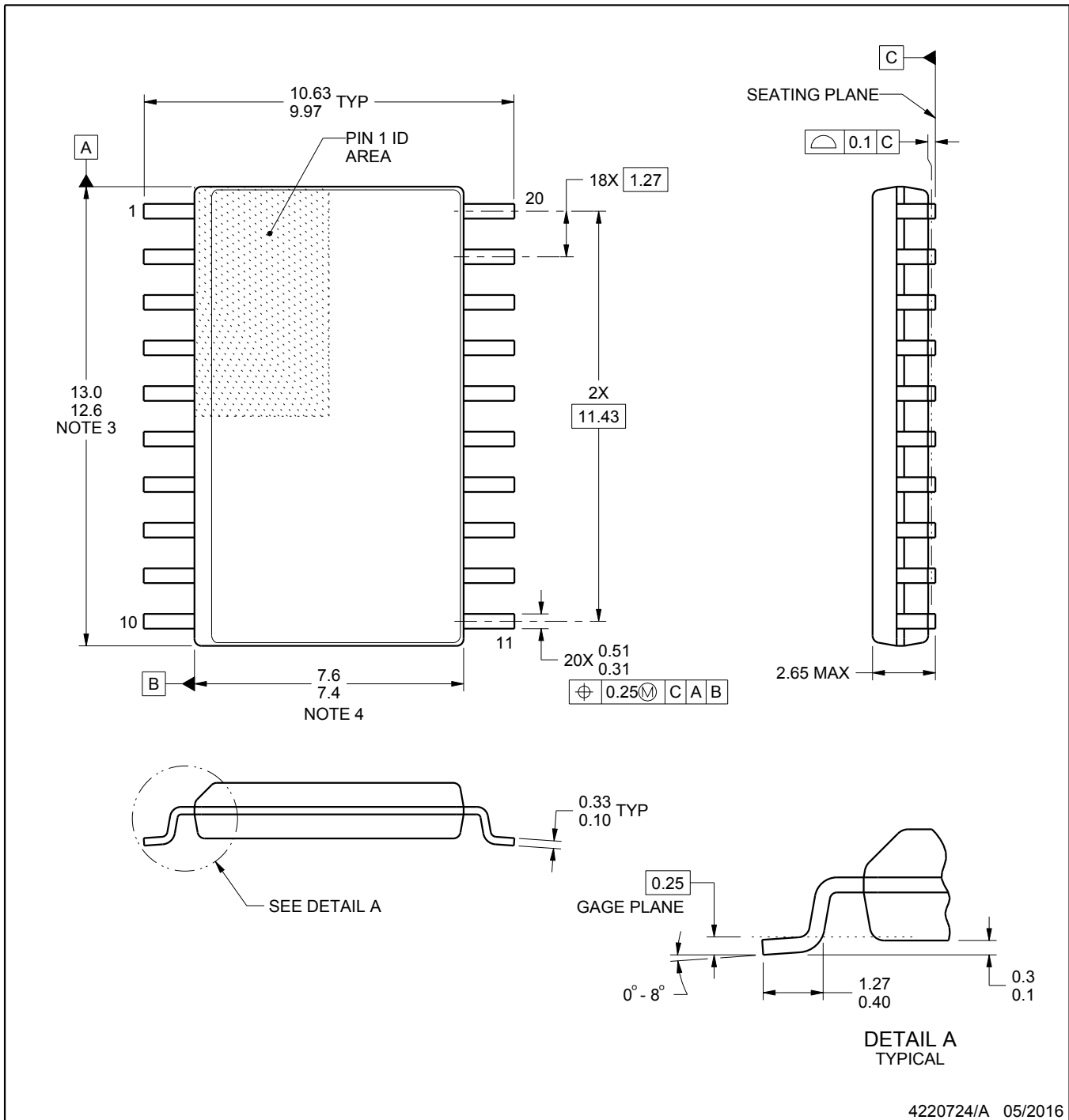
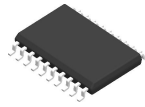
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75196DWR	SOIC	DW	20	2000	367.0	367.0	45.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN75196DW	DW	SOIC	20	25	506.98	12.7	4826	6.6
SN75196DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN75196DW.A	DW	SOIC	20	25	506.98	12.7	4826	6.6
SN75196DW.A	DW	SOIC	20	25	507	12.83	5080	6.6



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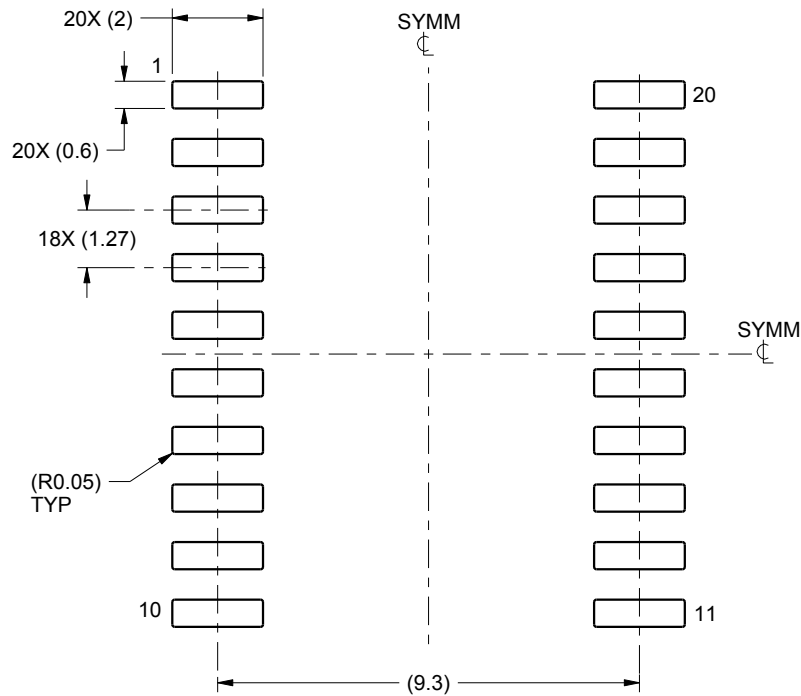
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

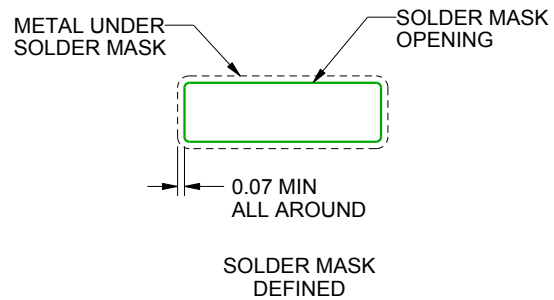
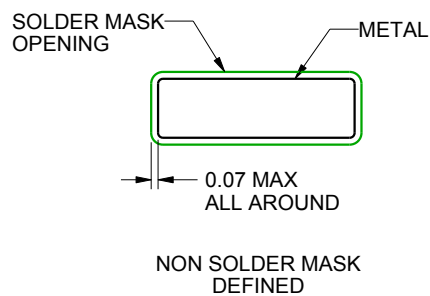
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

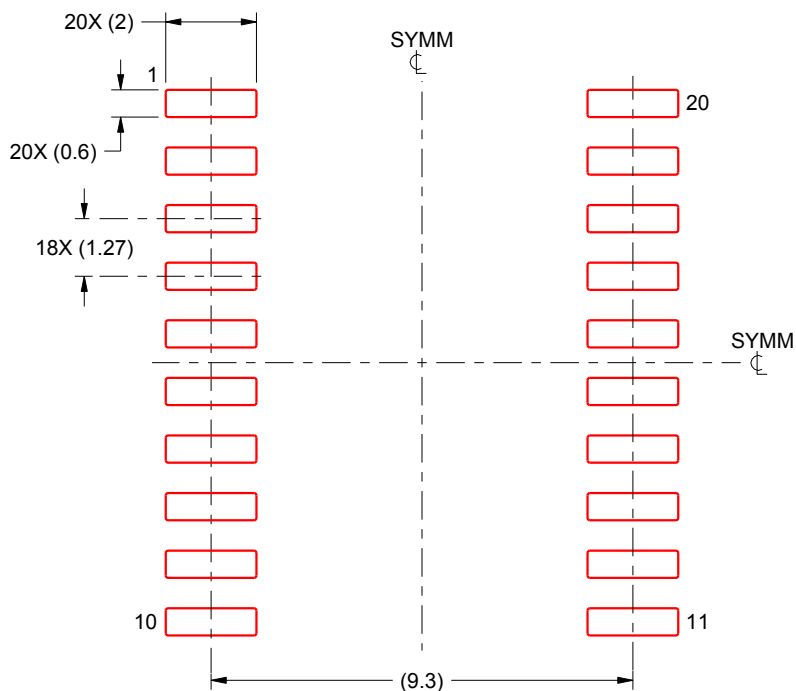
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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