# SN74CB3Q6800
# 10-BIT FET BUS SWITCH WITH PRECHARGED OUTPUTS
# 2.5-V/3.3-V LOW-VOLTAGE HIGH-BANDWIDTH BUS SWITCH

SCDS142A – OCTOBER 2003 – REVISED MARCH 2005

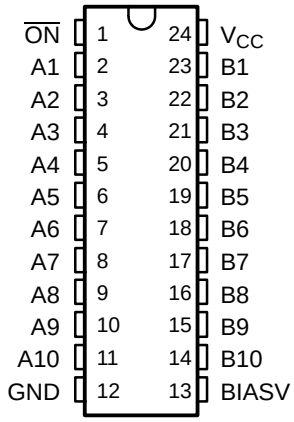
## FEATURES

- **High-Bandwidth Data Path (Up To 500 MHz (1))**
- **5-V Tolerant I/Os With Device Powered Up or Powered Down**
- **Low and Flat ON-State Resistance ($r_{on}$) Characteristics Over Operating Range ($r_{on}$ = 4.5 Ω Typ)**
- **Rail-to-Rail Switching on Data I/O Ports**
  - **– 0- to 5-V Switching With 3.3-V $V_{CC}$**
  - **– 0- to 3.3-V Switching With 2.5-V $V_{CC}$**
- **B-Port Outputs Are Precharged by Bias Voltage (BIASV) to Minimize Signal Distortion During Live Insertion and Hot Plugging**
- **Supports PCI Hot Plug**
- **Bidirectional Data Flow With Near-Zero Propagation Delay**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 3.5 pF Typ)**

(1) For additional information regarding the performance characteristics of the CB3Q family, refer to the TI application report, *CBT-C, CB3T, and CB3Q Signal-Switch Families*, literature number SCDA008.

- **Fast Switching Frequency ($f_{\overline{ON}}$= 20 MHz Max)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption ($I_{CC}$ = 0.75 mA Typ)**
- **$V_{CC}$ Operating Range From 2.3 V to 3.6 V**
- **Data I/Os Support 0- to 5-V Signaling Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)**
- **Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **$I_{off}$ Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **– 2000-V Human-Body Model (A114-B, Class II)**
  - **– 1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications: PCI Interface, Differential Signal Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating**

**DBQ, DGV, OR PW PACKAGE**
**(TOP VIEW)**

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## DESCRIPTION/ORDERING INFORMATION

The SN74CB3Q6800 is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance ($r_{on}$). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q6800 provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

The SN74CB3Q6800 is a 10-bit bus switch with a single output-enable ($\overline{ON}$) input. When $\overline{ON}$ is low, the 10-bit bus switch is ON and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{ON}$ is high, the 10-bit bus switch is OFF and a high-impedance state exists between the A and B ports. The B port is precharged to bias voltage (BIASV) through the equivalent of a 10-kΩ resistor when $\overline{ON}$ is high, or if the device is powered down ($V_{CC}$ = 0 V).

During insertion (or removal) of a card into (or from) an active bus, the card's output voltage may be close to GND. When the connector pins make contact, the card's parasitic capacitance tries to force the bus signal to GND, creating a possible glitch on the active bus. This glitching effect can be reduced by using a bus switch with precharged bias voltage (BIASV) of the bus switch equal to the input threshold voltage level of the receivers on the active bus. This method ensures that any glitch produced by insertion (or removal) of the card does not cross the input threshold region of the receivers on the active bus, minimizing the effects of live-insertion noise.

This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{ON}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### ORDERING INFORMATION

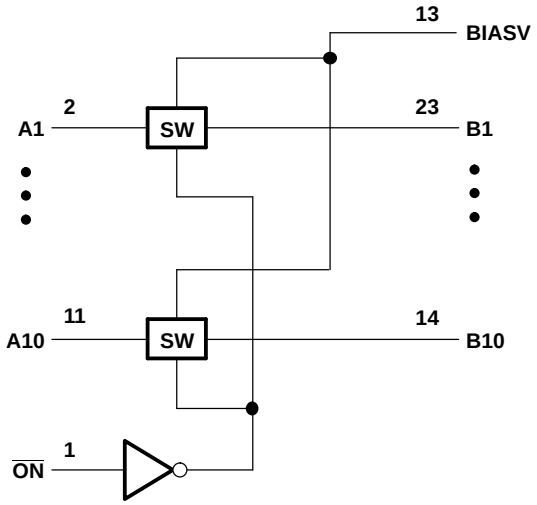
| $T_A$ | PACKAGE(1) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –40°C to 85°C | SSOP (QSOP) – DBQ | Tape and reel | SN74CB3Q6800DBQR | CB3Q6800 |
| | TSSOP – PW | Tube | SN74CB3Q6800PW | BY800 |
| | | Tape and reel | SN74CB3Q6800PWR | |
| | TVSOP – DGV | Tape and reel | SN74CB3Q6800DGVR | BY800 |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

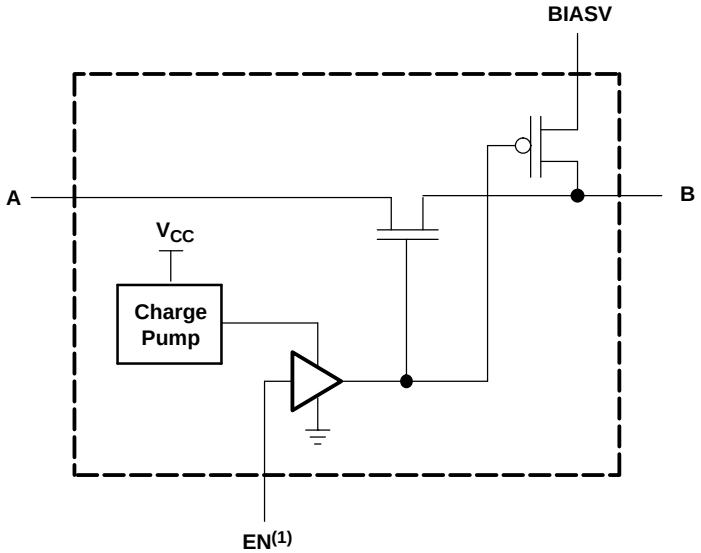
### FUNCTION TABLE

| INPUT $\overline{ON}$ | INPUT/OUTPUT A | FUNCTION |
|---|---|---|
| L | B | A port = B port |
| H | Z | Disconnect<br>B port = BIASV |

## LOGIC DIAGRAM (POSITIVE LOGIC)




## SIMPLIFIED SCHEMATIC, EACH FET SWITCH (SW)




(1) EN is the internal enable signal applied to the switch.

## Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | –0.5 | 4.6 | V |
| BIASV | BIAS supply voltage range | | –0.5 | 7 | V |
| $V_{IN}$ | Control input voltage range[2][3] | | –0.5 | 7 | V |
| $V_{I/O}$ | Switch I/O voltage range[2][3][4] | | –0.5 | 7 | V |
| $I_{IK}$ | Control input clamp current | $V_{IN} < 0$ | | –50 | mA |
| $I_{I/OK}$ | I/O port clamp current | $V_{I/O} < 0$ | | –50 | mA |
| $I_{I/O}$ | ON-state switch current[5] | | | ±64 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±100 | mA |
| $\theta_{JA}$ | Package thermal impedance[6] | DBG package | | 61 | °C/W |
| | | DGV package | | 86 | |
| | | PW package | | 88 | |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) $V_I$ and $V_O$ are used to denote specific conditions for $V_{I/O}$.
(5) $I_I$ and $I_O$ are used to denote specific conditions for $I_{I/O}$.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

## Recommended Operating Conditions[1]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2.3 | 3.6 | V |
| BIASV | Bias supply voltage | | 0 | 5 | V |
| $V_{IH}$ | High-level control input voltage | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | 5.5 | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2 | 5.5 | |
| $V_{IL}$ | Low-level control input voltage | $V_{CC}$ = 2.3 V to 2.7 V | 0 | 0.7 | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 0 | 0.8 | |
| $V_{I/O}$ | Data input/output voltage | | 0 | 5.5 | V |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |

(1) All unused control inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004. BIASV is a supply voltage, not a control input.

## Electrical Characteristics(1)

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP(2) | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 3.6 V, | $I_I$ = –18 mA | | | | –1.8 | V |
| $I_{IN}$ | Control inputs | $V_{CC}$ = 3.6 V, | $V_{IN}$ = 0 to 5.5 V | | | | ±1 | µA |
| $I_O$ | B port | $V_{CC}$ = 3.V, | BIASV = 2.4 V, $V_O$ = 0, | Switch OFF, $V_{IN}$ = $V_{CC}$ or GND | | 0.2 | | mA |
| $I_{OZ}$(3) | | $V_{CC}$ = 3.6 V, | $V_O$ = 0 to 5.5 V, $V_I$ = 0, | Switch OFF, $V_{IN}$ = $V_{CC}$ or GND | | | ±1 | µA |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_O$ = 0 to 5.5 V, | $V_I$ = 0 | | | 1 | µA |
| $I_{CC}$ | | $V_{CC}$ = 3.6 V, | $I_{I/O}$ = 0, Switch ON or OFF, | $V_{IN}$ = $V_{CC}$ or GND | | 0.75 | 2 | mA |
| $\Delta I_{CC}$(4) | Control inputs | $V_{CC}$ = 3.6 V, | One input at 3 V, | Other inputs at $V_{CC}$ or GND | | | 30 | µA |
| $I_{CCD}$(5) | Per control input | $V_{CC}$ = 3.6 V, Control input switching at 50% duty cycle | A and B ports open, | | | 0.38 | 0.45 | mA/MHz |
| $C_{in}$ | Control inputs | $V_{CC}$ = 3.3 V, | $V_{IN}$ = 5.5 V, 3.3 V, or 0 | | | 2.5 | 3.5 | pF |
| $C_{io(OFF)}$ | A port | $V_{CC}$ = 3.3 V, | Switch OFF, $V_{IN}$ = $V_{CC}$ or GND, | $V_{I/O}$ = 5.5 V, 3.3 V, or 0 | | 3.5 | 5 | pF |
| $C_{io(ON)}$ | | $V_{CC}$ = 3.3 V, | Switch ON, $V_{IN}$ = $V_{CC}$ or GND, | $V_{I/O}$ = 5.5 V, 3.3 V, or 0 | | 9 | 11 | pF |
| $r_{on}$(6) | | $V_{CC}$ = 2.3 V, TYP at $V_{CC}$ = 2.5 V | $V_I$ = 0, | $I_O$ = 30 mA | | 4.5 | 8 | Ω |
| | | | $V_I$ = 1.7 V, | $I_O$ = –15 mA | | 4.8 | 9 | |
| | | $V_{CC}$ = 3 V | $V_I$ = 0, | $I_O$ = 30 mA | | 4.5 | 6 | |
| | | | $V_I$ = 2.4 V, | $I_O$ = –15 mA | | 4.6 | 8 | |

(1) $V_{IN}$ and $I_{IN}$ refer to control inputs. $V_I$, $V_O$, $I_I$, and $I_O$ refer to data pins.
(2) All typical values are at $V_{CC}$ = 3.3 V (unless otherwise noted), $T_A$ = 25°C.
(3) For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.
(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than $V_{CC}$ or GND.
(5) This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 2).
(6) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

## Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

| PARAMETER | TEST CONDITIONS | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| $f_{\overline{ON}}$(1) | | $\overline{ON}$ | A or B | | 10 | | 20 | MHz |
| $t_{pd}$(2) | | A or B | B or A | | 0.135 | | 0.225 | ns |
| $t_{PZH}$ | BIASV = GND | $\overline{ON}$ | A or B | 1.5 | 8.5 | 1.5 | 6.7 | ns |
| $t_{PZL}$ | BIASV = 3 V | | | 1.5 | 8.5 | 1.5 | 6.7 | |
| $t_{PHZ}$ | BIASV = GND | $\overline{ON}$ | A or B | 1 | 5 | 1 | 5 | ns |
| $t_{PLZ}$ | BIASV = 3 V | | | 1 | 6.9 | 1 | 6.9 | |

(1) Maximum switching frequency for control input ($V_O$ > $V_{CC}$, $V_I$ = 5 V, $R_L$ ≥ 1 MΩ, $C_L$ = 0).
(2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

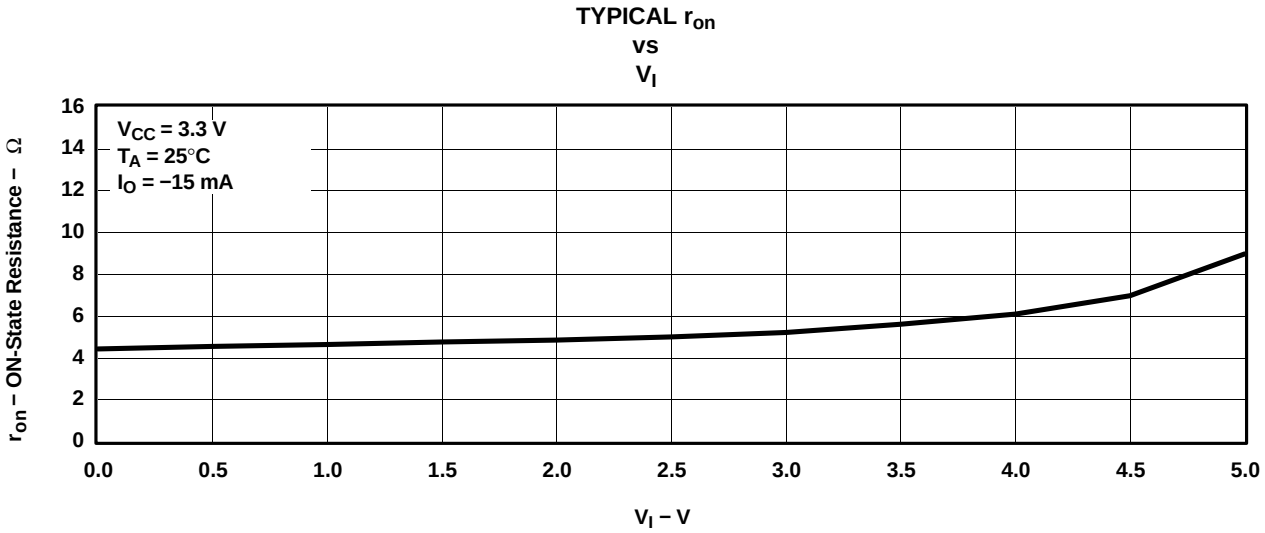



**Figure 1. Typical $r_{on}$ vs $V_I$**

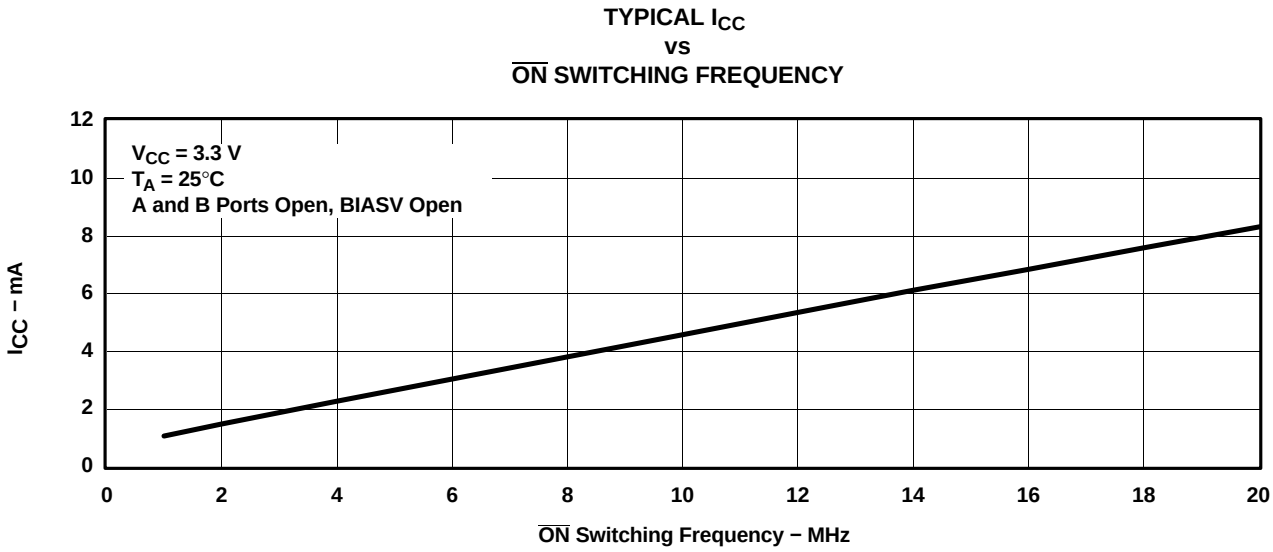
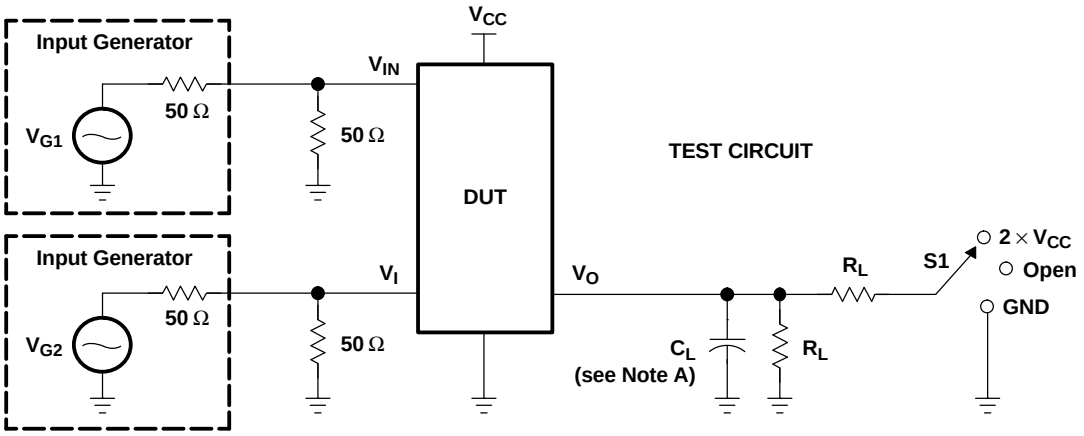
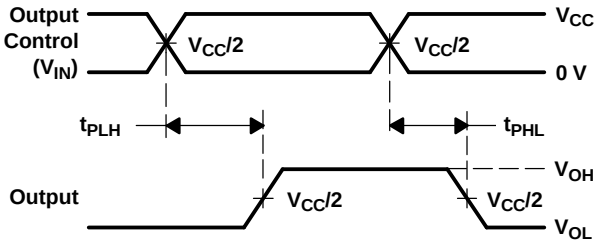



**Figure 2. Typical $I_{CC}$ vs $\overline{ON}$ Switching Frequency**

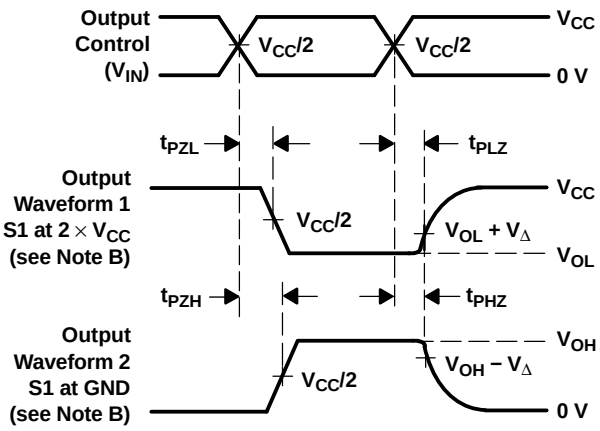
## PARAMETER MEASUREMENT INFORMATION




| TEST | $V_{CC}$ | S1 | $R_L$ | $V_I$ | $C_L$ | $V_\Delta$ |
|---|---|---|---|---|---|---|
| $t_{pd(s)}$ | 2.5 V ± 0.2 V<br>3.3 V ± 0.3 V | Open<br>Open | 500 Ω<br>500 Ω | $V_{CC}$ or GND<br>$V_{CC}$ or GND | 30 pF<br>50 pF | |
| $t_{PLZ}/t_{PZL}$ | 2.5 V ± 0.2 V<br>3.3 V ± 0.3 V | 2 × $V_{CC}$<br>2 × $V_{CC}$ | 500 Ω<br>500 Ω | GND<br>GND | 30 pF<br>50 pF | 0.15 V<br>0.3 V |
| $t_{PHZ}/t_{PZH}$ | 2.5 V ± 0.2 V<br>3.3 V ± 0.3 V | GND<br>GND | 500 Ω<br>500 Ω | $V_{CC}$<br>$V_{CC}$ | 30 pF<br>50 pF | 0.15 V<br>0.3 V |




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

**Figure 3. Test Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN74CB3Q6800DBQR | Active | Production | SSOP (DBQ) \| 24 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | CB3Q6800 |
| SN74CB3Q6800DBQR.B | Active | Production | SSOP (DBQ) \| 24 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | CB3Q6800 |
| SN74CB3Q6800DBQRG4 | Active | Production | SSOP (DBQ) \| 24 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | CB3Q6800 |
| SN74CB3Q6800DBQRG4.B | Active | Production | SSOP (DBQ) \| 24 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | CB3Q6800 |
| SN74CB3Q6800DGVR | Active | Production | TVSOP (DGV) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | BY800 |
| SN74CB3Q6800DGVR.B | Active | Production | TVSOP (DGV) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | BY800 |
| SN74CB3Q6800PW | Active | Production | TSSOP (PW) \| 24 | 60 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | BY800 |
| SN74CB3Q6800PW.B | Active | Production | TSSOP (PW) \| 24 | 60 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | BY800 |
| SN74CB3Q6800PWR | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | BY800 |
| SN74CB3Q6800PWR.B | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | BY800 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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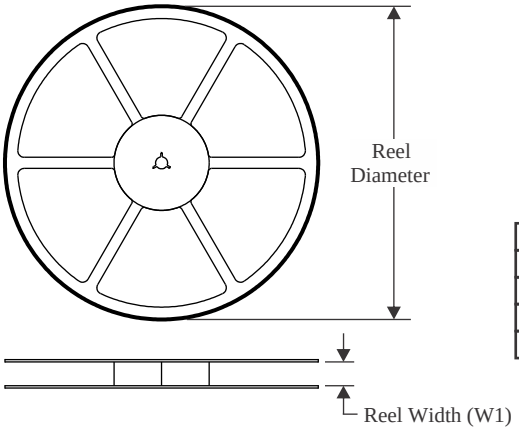
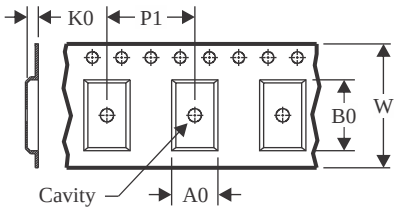
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

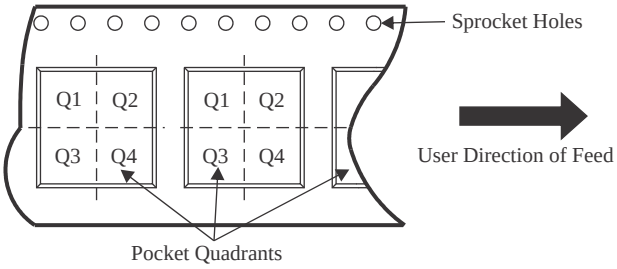



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

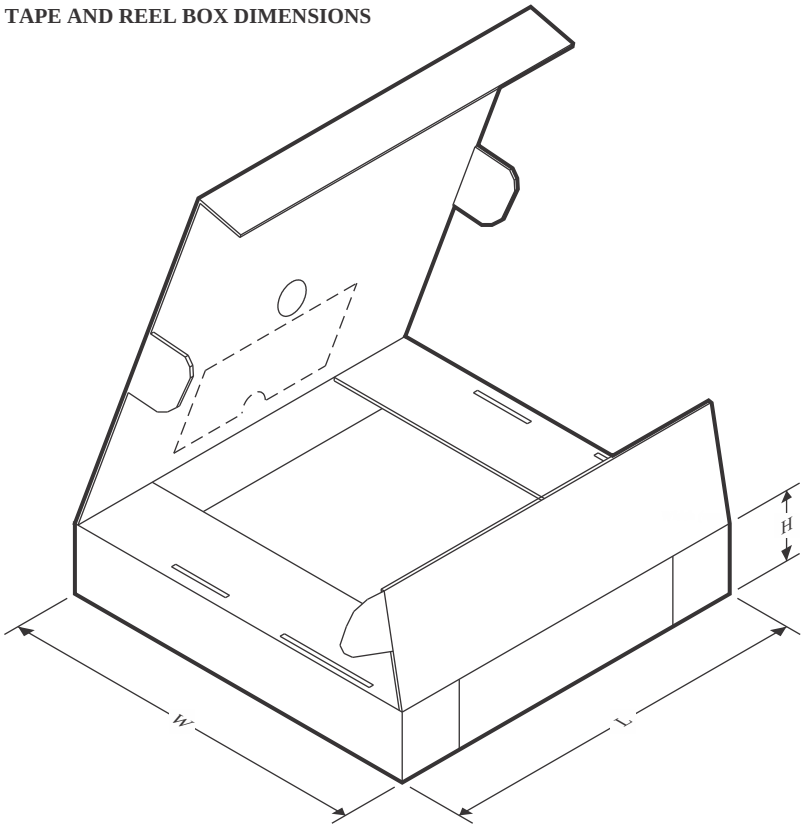
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74CB3Q6800DBQR | SSOP | DBQ | 24 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74CB3Q6800DBQRG4 | SSOP | DBQ | 24 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74CB3Q6800DGVR | TVSOP | DGV | 24 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74CB3Q6800PWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |

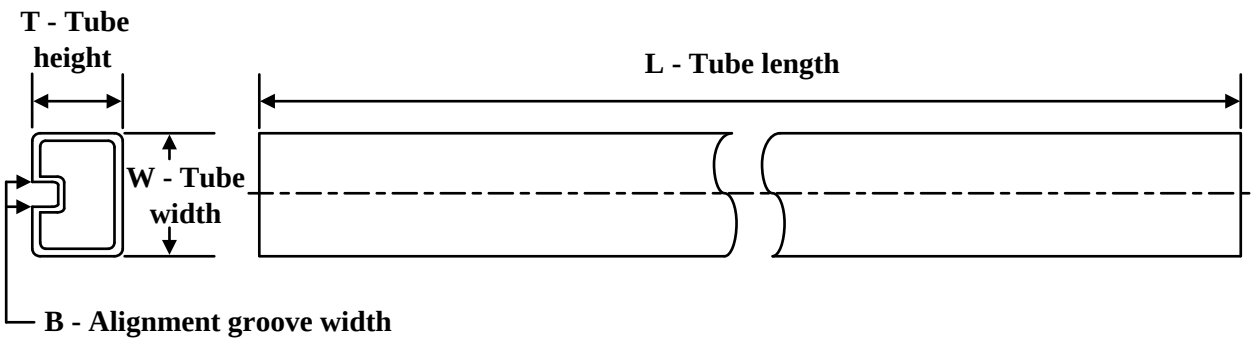
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

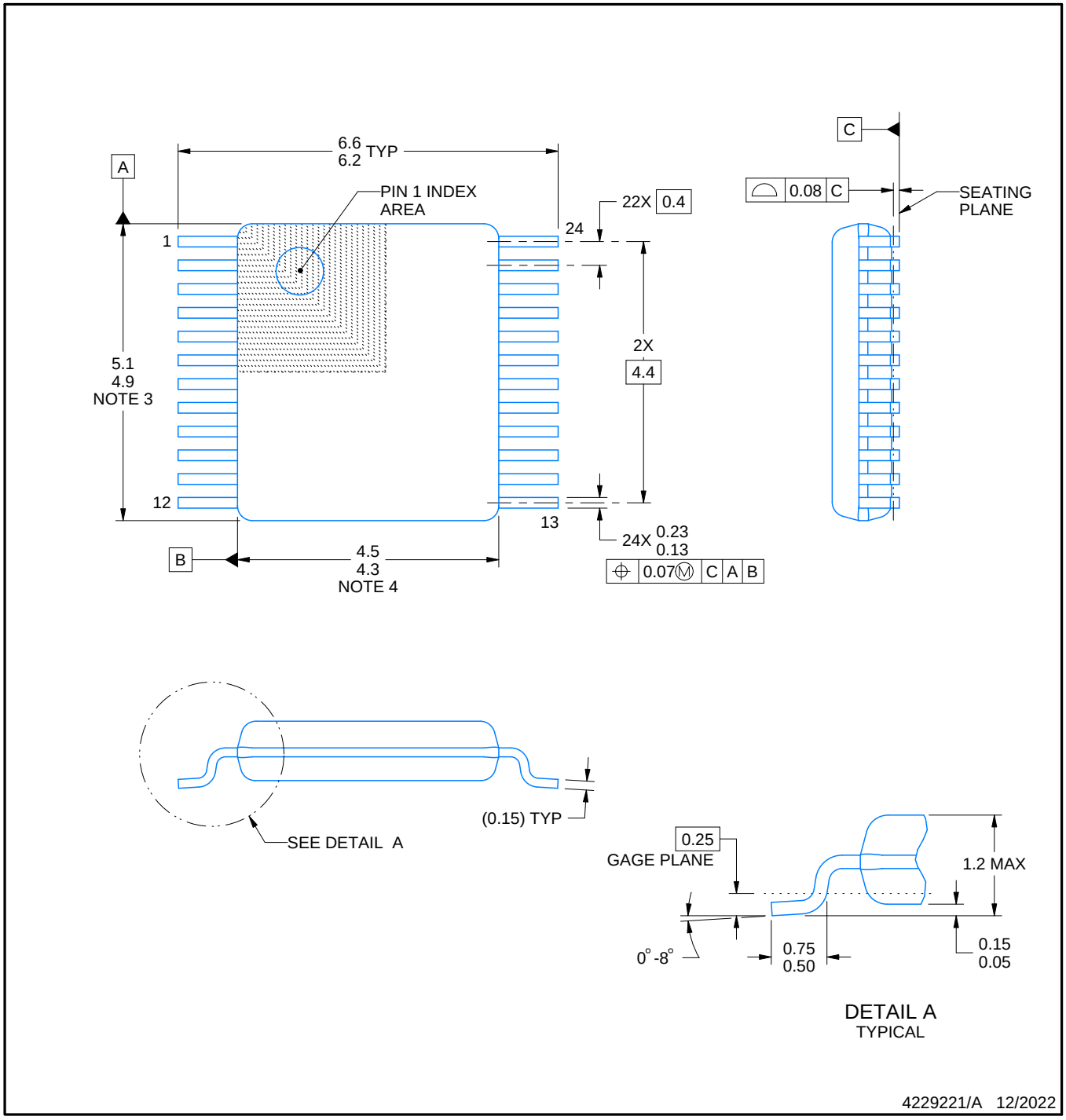
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74CB3Q6800DBQR | SSOP | DBQ | 24 | 2500 | 356.0 | 356.0 | 35.0 |
| SN74CB3Q6800DBQRG4 | SSOP | DBQ | 24 | 2500 | 356.0 | 356.0 | 35.0 |
| SN74CB3Q6800DGVR | TVSOP | DGV | 24 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74CB3Q6800PWR | TSSOP | PW | 24 | 2000 | 356.0 | 356.0 | 35.0 |

## TUBE



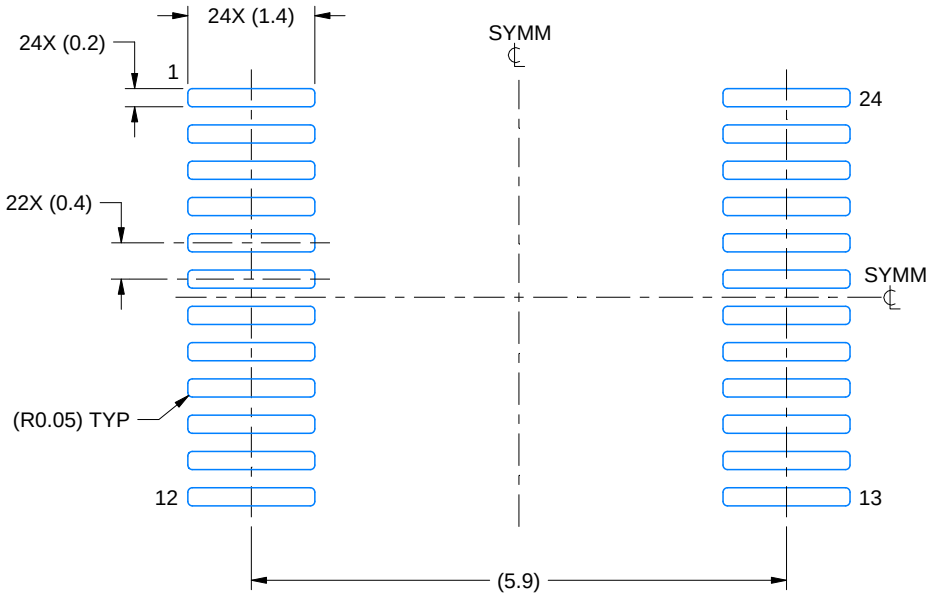

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| SN74CB3Q6800PW | PW | TSSOP | 24 | 60 | 530 | 10.2 | 3600 | 3.5 |
| SN74CB3Q6800PW.B | PW | TSSOP | 24 | 60 | 530 | 10.2 | 3600 | 3.5 |

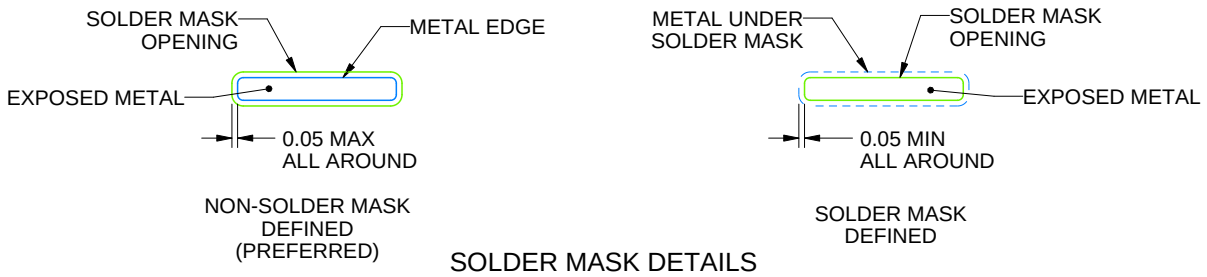



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X

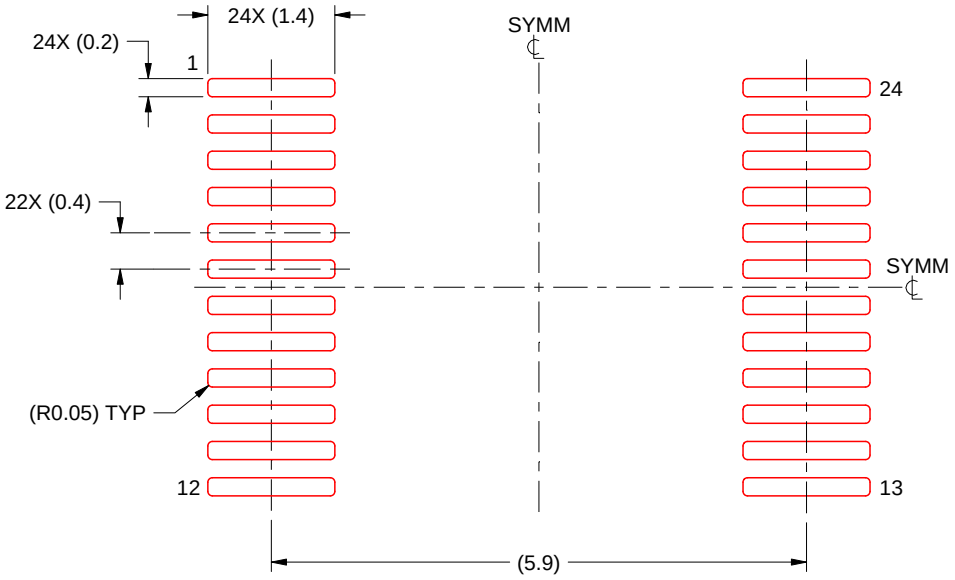



SOLDER MASK DETAILS

4229221/A 12/2022

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



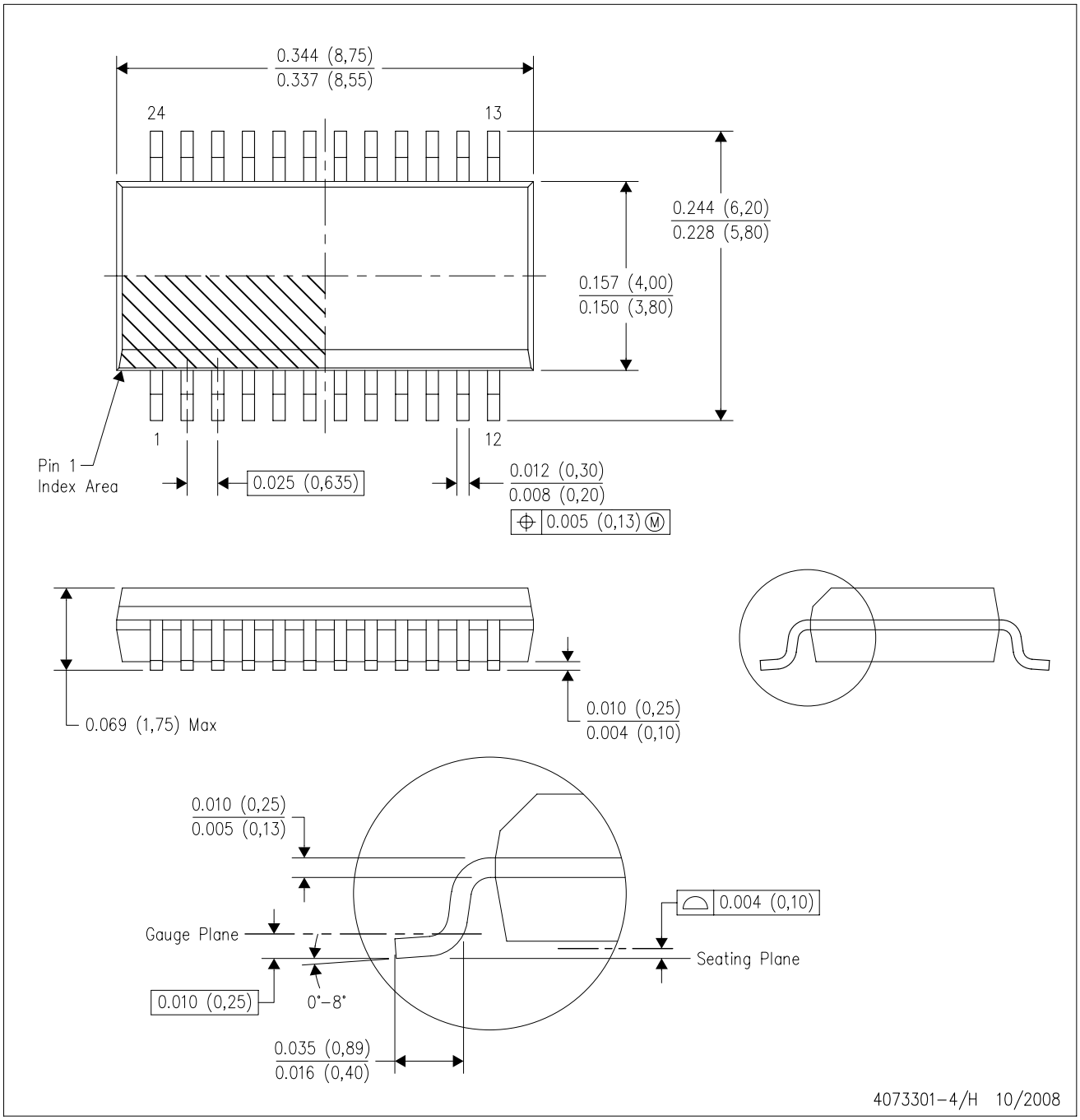

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

4229221/A 12/2022

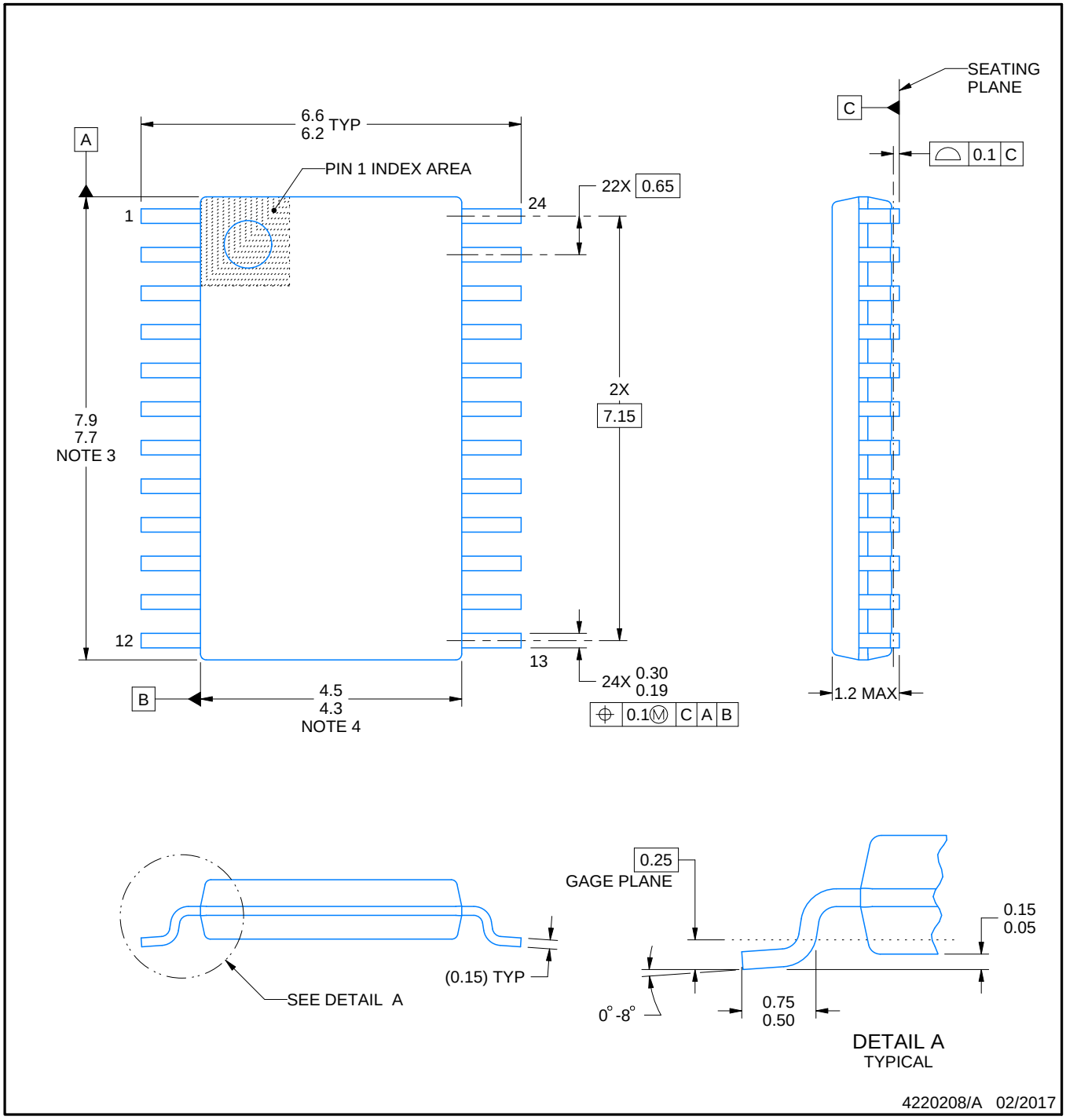
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DBQ (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE

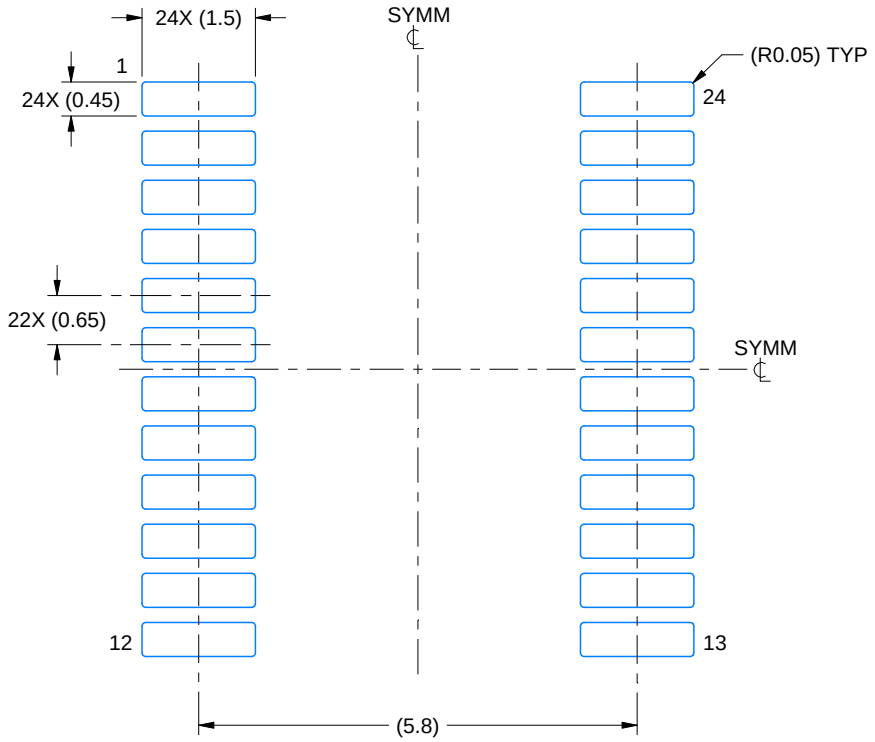



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AE.

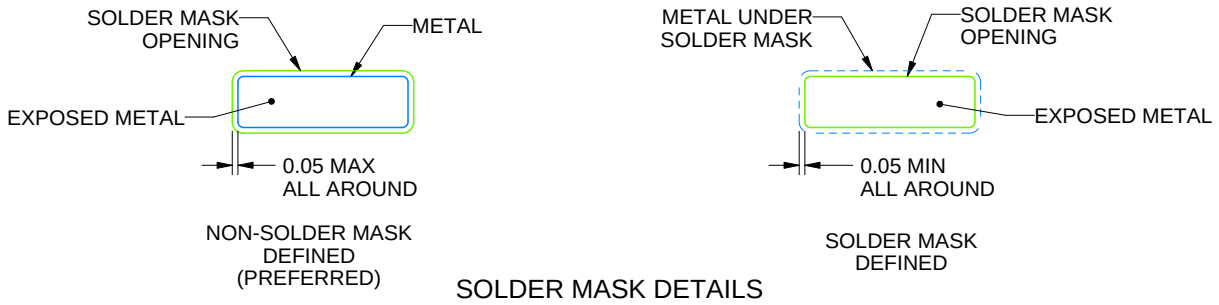



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

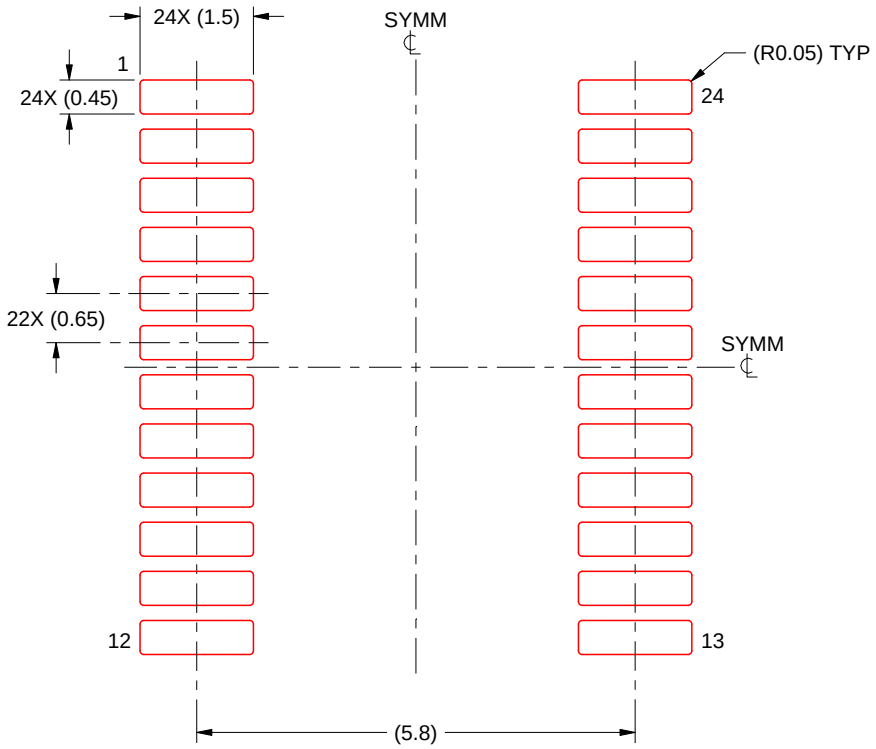



SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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