4-Channel Video Amplifier with One SD and Three HD 8th-Order Filters with 6-dB Gain

Check for Samples: THS7376

FEATURES

- **One SD Video Amplifier for CVBS Video :**
  - **Sixth-Order Low-Pass Filter: –3 dB at 10 MHz**
  - **Low Differential Gain and Phase: 0.2% and 0.3°**
- **Three HD Video Amplifiers for Y'P'$_B$P'$_R$, 720p, 1080i, 1080p24, and 1080p30 Filters or G'B'R' (R'G'B') Outputs:**
  - **8th-Order Low-Pass Filter:**
    - **–1 dB at 39 MHz**
    - **–3 dB at 42 MHz**
  - **Bypassable Filters: –3 dB at 300 MHz**
- **Versatile Input Biasing:**
  - **DC-Coupled with 210-mV Output Shift**
  - **AC-Coupled with Sync-Tip Clamp or Bias**
- **Built-In 6-dB Gain (2 V/V)**
- **+3-V to +5-V Single-Supply Operation**
- **Rail-to-Rail Output:**
  - **Allows AC or DC Output Coupling**
  - **Supports Driving Two Video Lines per Channel**
- **Low Total Quiescent Current: 30.9 mA at 3.3 V**
- **Disabled Supply Current Function: 0.1 µA**
- **Robust, 10-kV ESD Protection on Outputs**
- **Pin-Compatible with the THS7373 and THS7374**

APPLICATIONS

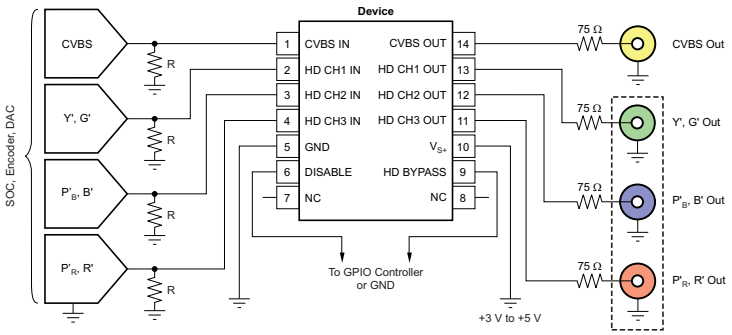
- **Set-Top Box Output Video Buffering**
- **PVR, DVDR, and BluRay™ Output Buffering**
- **Media Centers and Players**

DESCRIPTION

The THS7376 is a low-power, 3-V to 5-V single-supply, four-channel, integrated video amplifier. The device incorporates one standard definition (SD) filter channel for CVBS video and three high-definition (HD) filter channels. The CVBS filter features a sixth-order filter and the HD channels feature eighth-order filters. These filters are useful as digital-to-analog converter (DAC) reconstruction filters or as analog-to-digital converter (ADC) antialiasing filters. The HD filters can be bypassed to support 1080p60 video or up to super extended graphics array (SXGA) RGB video.

The device has flexible input coupling capabilities, and can be configured for either ac- or dc-coupled inputs. The 210-mV output level shift allows for a full sync dynamic range at the output with a 0-V input. The device's rail-to-rail output stage with 6-dB gain allows for both ac and dc line driving. The ability to drive two lines, or 75-Ω loads, allows for maximum flexibility as a video line driver. The 30.9-mA total quiescent current at 3.3 V and 0.1-µA disable mode makes the THS7376 an excellent choice for high-performance video applications.

The THS7376 is available in a small TSSOP-14 package that is RoHS compliant. The device is pin-compatible with the THS7373 and THS7374 video filter amplifiers from Texas Instruments.



Single-Supply, DC Input and DC Output Coupled Video Line Driver

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		VALUE	UNIT
Voltage	Supply, V_{S+} to GND	5.5	V
	Input, V_I	–0.4 to V_{S+}	V
Continuous Output current, I_O		±75	mA
Continuous power dissipation		See Thermal Information Table	
Temperature	Maximum junction, any condition(2), T_J	+150	°C
	Maximum junction, continuous operation, long-term reliability(3), T_J	+125	°C
	Storage range, T_{stg}	–60 to +150	°C
Electrostatic discharge (ESD) ratings (output pins)	Human body model (HBM)	±10	kV
	Charge device model (CDM)	±2	kV
Electrostatic discharge (ESD) ratings (all other pins)	Human body model (HBM)	±8	kV
	Charge device model (CDM)	±1	kV

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The absolute maximum junction temperature under any condition is limited by the constraints of the silicon process.
(3) The absolute maximum junction temperature for continuous operation is limited by the package constraints. Operation above this temperature may result in reduced reliability and lifetime of the device.

THERMAL INFORMATION

THERMAL METRIC(1)		THS7376 PW (TSSOP) 14 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	124.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	52.9	
θ_{JB}	Junction-to-board thermal resistance	66.0	
ψ_{JT}	Junction-to-top characterization parameter	7.3	
ψ_{JB}	Junction-to-board characterization parameter	65.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage, V_{S+}	3		5.25	V
Ambient temperature, T_A	–40	+25	+85	°C

ELECTRICAL CHARACTERISTICS: V_{S+} = +3.3 V

At T_A = +25°C, R_L = 150 Ω to GND, C_{LOAD} = 5 pF, filter mode, and dc-coupled input and output, unless otherwise noted. See Figure 123 and Figure 124.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS	TEST LEVEL (1)
AC PERFORMANCE: SD (CVBS) CHANNEL							
$BW_{(PB)}$	Passband bandwidth	–1 dB, V_O = 0.2 V_{PP} and 2 V_{PP}	7.5	9	11.5	MHz	B
	Small- and large-signal bandwidth	–3 dB, V_O = 0.2 V_{PP} and 2 V_{PP}	8.2	10	12	MHz	B
	Attenuation	With respect to 500 kHz (2), f = 6.75 MHz	–1	–0.1	0.9	dB	B
		With respect to 500 kHz (2), f = 27 MHz	38	46		dB	B
	Group delay	f = 100 kHz		68		ns	C
	Group delay variation	f = 5.1 MHz with respect to 100 kHz		10		ns	C
	Differential gain	NTSC		0.2%			C
		PAL		0.2%			C
	Differential phase	NTSC		0.3		Degrees	C
		PAL		0.3		Degrees	C
THD	Total harmonic distortion	f = 1 MHz, V_O = 1.4 V_{PP}		–70		dB	C
		f = 6 MHz, V_O = 1.4 V_{PP}		–62		dB	C
SNR	Signal-to-noise ratio	100 kHz to 6 MHz, non-weighted		70		dB	C
		100 kHz to 6 MHz, unified weighting		78		dB	C
G	Gain	All channels, T_A = +25°C	5.7	6	6.3	dB	A
		All channels, T_A = –40°C to +85°C	5.65		6.35	dB	B
	Output impedance	f = 6.75 MHz		0.7		Ω	C
		Disabled		20 || 3		kΩ || pF	C
	Return loss (3)	f = 6.75 MHz		46		dB	C
	Crosstalk	f = 1 MHz, SD channel to HD channels		–90		dB	C

(1) Test levels: **(A)** 100% tested at +25°C. Over temperature limits set by characterization and simulation. **(B)** Limits set by characterization and simulation only. **(C)** Typical value only for information.
(2) 3.3-V supply filter specifications are ensured by 100% testing at a 5-V supply with design and characterization.
(3) Return loss is calculated assuming an ideal 75-Ω external series resistor along with the THS7376 channel output impedance into an ideal 75-Ω end-termination resistance.

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ELECTRICAL CHARACTERISTICS: V_{S+} = +3.3 V (continued)

At T_A = +25°C, R_L = 150 Ω to GND, C_{LOAD} = 5 pF, filter mode, and dc-coupled input and output, unless otherwise noted. See Figure 123 and Figure 124.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS	TEST LEVEL (1)
AC PERFORMANCE: HD CHANNELS							
	Passband bandwidth	–1 dB, V_O = 0.2 V_{PP} and 2 V_{PP}	32	39	46.5	MHz	B
	Small- and large-signal bandwidth	–3 dB, V_O = 0.2 V_{PP} and 2 V_{PP}	35.5	42	49.5	MHz	B
	HD bypass mode bandwidth	–3 dB, V_O = 0.2 V_{PP}	200	300		MHz	B
SR	Slew rate	HD bypass mode	300	375		V/µs	B
	Attenuation	With respect to 500 kHz (4), f = 30 MHz	–1	–0.2	0.9	dB	B
		With respect to 500 kHz (4), f = 74 MHz	26	40		dB	B
	Group delay	f = 100 kHz		23		ns	C
	Group delay variation	f = 27 MHz with respect to 100 kHz		5.5		ns	C
	Channel-to-channel delay			0.3		ns	C
THD	Total harmonic distortion	f = 10 MHz, V_O = 1.4 V_{PP}		–57		dB	C
		f = 30 MHz, V_O = 1.4 V_{PP}		–60		dB	C
SNR	Signal-to-noise ratio	100 kHz to 30 MHz, non-weighted		63		dB	C
		100 kHz to 30 MHz, unified weighting		73		dB	C
G	Gain	All channels, T_A = +25°C	5.7	6	6.3	dB	A
		All channels, T_A = –40°C to +85°C	5.65		6.35	dB	B
	Output impedance	f = 30 MHz, filter mode		1.3		Ω	C
		f = 30 MHz, HD bypass mode		1.4		Ω	C
		Disabled		1.8 || 3		kΩ || pF	C
	Return loss (5)	f = 30 MHz, filter mode		41		dB	C
	Crosstalk	f = 1 MHz, HD channels to SD channel		–85		dB	C
		f = 1 MHz, HD to HD channels		–85		dB	C
DC PERFORMANCE							
$V_{O(Bias)}$	Biased output voltage	V_{IN} = 0 V, SD channel	100	210	300	mV	A
		V_{IN} = 0 V, HD channels	100	210	300	mV	A
V_I	Input voltage range	DC linear input, limited by output		–0.05 / 1.5		V	C
	Sync-tip clamp charge current	V_{IN} = –0.1 V, SD channel	140	200		µA	A
		V_{IN} = –0.1 V, HD channels	260	360		µA	A
	Input impedance			800 || 2		kΩ || pF	C

(4) 3.3-V supply filter specifications are ensured by 100% testing at a 5-V supply with design and characterization.
(5) Return loss is calculated assuming an ideal 75-Ω external series resistor along with the THS7376 channel output impedance into an ideal 75-Ω end-termination resistance.

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ELECTRICAL CHARACTERISTICS: V_{S+} = +3.3 V (continued)

At T_A = +25°C, R_L = 150 Ω to GND, C_{LOAD} = 5 pF, filter mode, and dc-coupled input and output, unless otherwise noted. See Figure 123 and Figure 124.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS	TEST LEVEL (1)
OUTPUT CHARACTERISTICS							
	High output voltage swing	R_L = 150 Ω to +1.65 V		3.2		V	C
		R_L = 150 Ω to GND	2.85	3.1		V	A
		R_L = 75 Ω to +1.65 V		3.1		V	C
		R_L = 75 Ω to GND		3		V	C
	Low output voltage swing	R_L = 150 Ω to +1.65 V (V_{IN} = –0.2 V)		0.07		V	C
		R_L = 150 Ω to GND (V_{IN} = –0.2 V)		0.06	0.1	V	A
		R_L = 75 Ω to +1.65 V (V_{IN} = –0.2 V)		0.1		V	C
		R_L = 75 Ω to GND (V_{IN} = –0.2 V)		0.05		V	C
	Output current (sourcing)	R_L = 10 Ω to +1.65 V		100		mA	C
	Output current (sinking)	R_L = 10 Ω to +1.65 V		110		mA	C
POWER SUPPLY							
	Operating voltage		2.85	3.3	5.5	V	B
	Total quiescent current, no load	V_{IN} = 0 V, enabled, $V_{DISABLE}$ = 0 V	25.8	30.9	37	mA	A
		V_{IN} = 0 V, disabled, $V_{DISABLE}$ = 3 V		0.1	10	µA	A
PSRR	Power-supply rejection ratio	At dc		50		dB	C
LOGIC CHARACTERISTICS (6)							
V_{IH}	High-level input voltage	Disabled or HD bypass engaged	2	1.8		V	A
V_{IL}	Low-level input voltage	Enabled or HD bypass disengaged		0.7	0.65	V	A
I_{IH}	High-level input current	Applied voltage = 3 V		1		µA	C
I_{IL}	Low-level input current	Applied voltage = 0 V		0.1		µA	C
t_{dis}	Disable time	Disable pin transitions from low to high		125		ns	C
t_{en}	Enable time	Disable pin transitions from high to low		200		ns	C
	HD bypass and filter switch time			10		ns	C

(6) The logic input pins default to a logic '0' condition when left floating.

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ELECTRICAL CHARACTERISTICS: V_{S+} = +5 V

At T_A = +25°C, R_L = 150 Ω to GND, C_{LOAD} = 5 pF, filter mode, and dc-coupled input and output, unless otherwise noted. See Figure 123 and Figure 124.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS	TEST LEVEL (1)
AC PERFORMANCE: SD (CVBS) CHANNEL							
$BW_{(PB)}$	Passband bandwidth	–1 dB, V_O = 0.2 V_{PP} and 2 V_{PP}	7.5	9	11.5	MHz	B
	Small- and large-signal bandwidth	–3 dB, V_O = 0.2 V_{PP} and 2 V_{PP}	8.2	10	12	MHz	B
	Attenuation	With respect to 500 kHz (2), f = 6.75 MHz	–1	–0.1	0.9	dB	B
		With respect to 500 kHz (2), f = 27 MHz	38	46		dB	B
	Group delay	f = 100 kHz		68		ns	C
	Group delay variation	f = 5.1 MHz with respect to 100 kHz		9.5		ns	C
	Differential gain	NTSC		0.4%			C
		PAL		0.4%			C
	Differential phase	NTSC		0.2		Degrees	C
		PAL		0.3		Degrees	C
THD	Total harmonic distortion	f = 1 MHz, V_O = 1.4 V_{PP}		–70		dB	C
		f = 6 MHz, V_O = 1.4 V_{PP}		–63		dB	C
SNR	Signal-to-noise ratio	100 kHz to 6 MHz, non-weighted		70		dB	C
		100 kHz to 6 MHz, unified weighting		78		dB	C
G	Gain	All channels, T_A = +25°C	5.7	6	6.3	dB	A
		All channels, T_A = –40°C to +85°C	5.65		6.35	dB	B
	Output impedance	f = 6.75 MHz		0.6		Ω	C
		Disabled		20 || 3		kΩ || pF	C
	Return loss (3)	f = 6.75 MHz		48		dB	C
	Crosstalk	f = 1 MHz, SD channel to HD channels		–88		dB	C

(1) Test levels: **(A)** 100% tested at +25°C. Over temperature limits set by characterization and simulation. **(B)** Limits set by characterization and simulation only. **(C)** Typical value only for information.
(2) 3.3-V supply filter specifications are ensured by 100% testing at a 5-V supply with design and characterization.
(3) Return loss is calculated assuming an ideal 75-Ω external series resistor along with the THS7376 channel output impedance into an ideal 75-Ω end-termination resistance.

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ELECTRICAL CHARACTERISTICS: V_{S+} = +5 V (continued)

At T_A = +25°C, R_L = 150 Ω to GND, C_{LOAD} = 5 pF, filter mode, and dc-coupled input and output, unless otherwise noted. See Figure 123 and Figure 124.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS	TEST LEVEL (1)
AC PERFORMANCE: HD CHANNELS							
	Passband bandwidth	–1 dB, V_O = 0.2 V_{PP} and 2 V_{PP}	32	39	46.5	MHz	B
	Small- and large-signal bandwidth	–3 dB, V_O = 0.2 V_{PP} and 2 V_{PP}	35.5	42	49.5	MHz	B
	HD bypass mode bandwidth	–3 dB, V_O = 0.2 V_{PP}	200	300		MHz	B
SR	Slew rate	HD bypass mode	300	375		V/µs	B
	Attenuation	With respect to 500 kHz (4), f = 30 MHz	–1	–0.2	0.9	dB	B
		With respect to 500 kHz (4), f = 74 MHz	26	40		dB	B
	Group delay	f = 100 kHz		23		ns	C
	Group delay variation	f = 27 MHz with respect to 100 kHz		5.5		ns	C
	Channel-to-channel delay			0.3		ns	C
THD	Total harmonic distortion	f = 10 MHz, V_O = 1.4 V_{PP}		–59		dB	C
		f = 30 MHz, V_O = 1.4 V_{PP}		–62		dB	C
SNR	Signal-to-noise ratio	100 kHz to 30 MHz, non-weighted		63		dB	C
		100 kHz to 30 MHz, unified weighting		73		dB	C
G	Gain	All channels, T_A = +25°C	5.7	6	6.3	dB	A
		All channels, T_A = –40°C to +85°C	5.65		6.35	dB	B
	Output impedance	f = 30 MHz, filter mode		1.3		Ω	C
		f = 30 MHz, HD bypass mode		1.4		Ω	C
		Disabled		1.8 || 3		kΩ || pF	C
	Return loss (5)	f = 30 MHz, filter mode		41		dB	C
	Crosstalk	f = 1 MHz, HD channels to SD channel		–85		dB	C
		f = 1 MHz, HD to HD channels		–85		dB	C
DC PERFORMANCE							
	Biased output voltage	V_{IN} = 0 V, SD channel	100	210	300	mV	A
		V_{IN} = 0 V, HD channels	100	210	300	mV	A
	Input voltage range	DC linear input, limited by output		–0.05 / 2.3		V	C
	Sync-tip clamp charge current	V_{IN} = –0.1 V, SD channel	140	200		µA	A
		V_{IN} = –0.1 V, HD channels	270	370		µA	A
	Input impedance			800 || 2		kΩ || pF	C

(4) 3.3-V supply filter specifications are ensured by 100% testing at a 5-V supply with design and characterization.
(5) Return loss is calculated assuming an ideal 75-Ω external series resistor along with the THS7376 channel output impedance into an ideal 75-Ω end-termination resistance.

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ELECTRICAL CHARACTERISTICS: V_{S+} = +5 V (continued)

At T_A = +25°C, R_L = 150 Ω to GND, C_{LOAD} = 5 pF, filter mode, and dc-coupled input and output, unless otherwise noted. See Figure 123 and Figure 124.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS	TEST LEVEL (1)
OUTPUT CHARACTERISTICS							
	High output voltage swing	R_L = 150 Ω to +2.5 V		4.85		V	C
		R_L = 150 Ω to GND	4.4	4.75		V	A
		R_L = 75 Ω to +2.5 V		4.75		V	C
		R_L = 75 Ω to GND		4.5		V	C
	Low output voltage swing	R_L = 150 Ω to +2.5 V (V_{IN} = –0.2 V)		0.09		V	C
		R_L = 150 Ω to GND (V_{IN} = –0.2 V)		0.05	0.1	V	A
		R_L = 75 Ω to +2.5 V (V_{IN} = –0.2 V)		0.15		V	C
		R_L = 75 Ω to GND (V_{IN} = –0.2 V)		0.05		V	C
	Output current (sourcing)	R_L = 10 Ω to +2.5 V		150		mA	C
	Output current (sinking)	R_L = 10 Ω to +2.5 V		140		mA	C
POWER SUPPLY							
	Operating voltage		2.85	5	5.5	V	B
	Total quiescent current, no load	V_{IN} = 0 V, enabled, $V_{DISABLE}$ = 0 V	27.2	32.6	39	mA	A
		V_{IN} = 0 V, disabled, $V_{DISABLE}$ = 3 V		0.1	10	µA	A
PSRR	Power-supply rejection ratio	At dc		53		dB	C
LOGIC CHARACTERISTICS (6)							
V_{IH}	High-level input voltage	Disabled or HD bypass engaged	2.2	2.1		V	A
V_{IL}	Low-level input voltage	Enabled or HD bypass disengaged		0.8	0.75	V	A
I_{IH}	High-level input current	Applied voltage = 3 V		1		µA	C
I_{IL}	Low-level input current	Applied voltage = 0 V		0.1		µA	C
t_{dis}	Disable time	Disable pin transitions from low to high		100		ns	C
t_{en}	Enable time	Disable pin transitions from high to low		200		ns	C
	HD bypass and filter switch time			10		ns	C

(6) The logic input pins default to a logic '0' condition when left floating.

Table 1. Logic Table

PIN NAME	INPUT, OUTPUT	DEFAULT LOGIC STATE	LOGIC STATES	DESCRIPTION
Disable	Input	0	0	All channels enabled
		0	1	All channels disabled
HD bypass	Input	0	0	HD channels use 8th-order low-pass filters
		0	1	HD channels bypass low-pass filters

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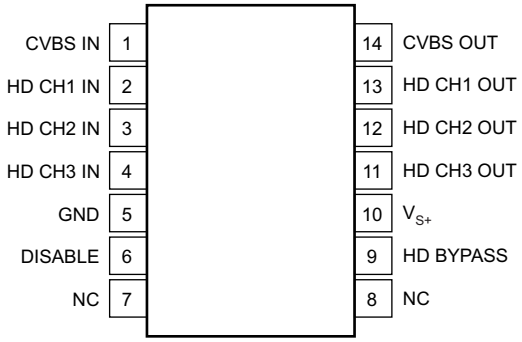
PIN CONFIGURATION

PW PACKAGE
TSSOP-14
(TOP VIEW)



NC = No connection.

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
CVBS IN	1	I	CVBS filter video input
CVBS OUT	14	O	CVBS filter video output
DISABLE	6	I	Disable pin. Logic high disables the device; logic low enables the device. This pin defaults to logic low (enabled) if left floating.
GND	5	I	Ground pin for all internal circuitry
HD BYPASS	9	I	Internal HD filter bypass. Logic high bypasses the internal HD low-pass filters; logic low uses the HD internal filters. This pin defaults to logic '0' (filter mode) if left floating. Note that the SD filter is never bypassed.
HD CH1 IN	2	I	HD channel 1 video input
HD CH1 OUT	13	O	HD channel 1 video output
HD CH2 IN	3	I	HD channel 2 video input
HD CH2 OUT	12	O	HD channel 2 video output
HD CH3 IN	4	I	HD channel 3 video input
HD CH3 OUT	11	O	HD channel 3 video output
NC	7, 8	—	No internal connection
V_{S+}	10	I	Positive power-supply pin; connect to +3 V to +5 V

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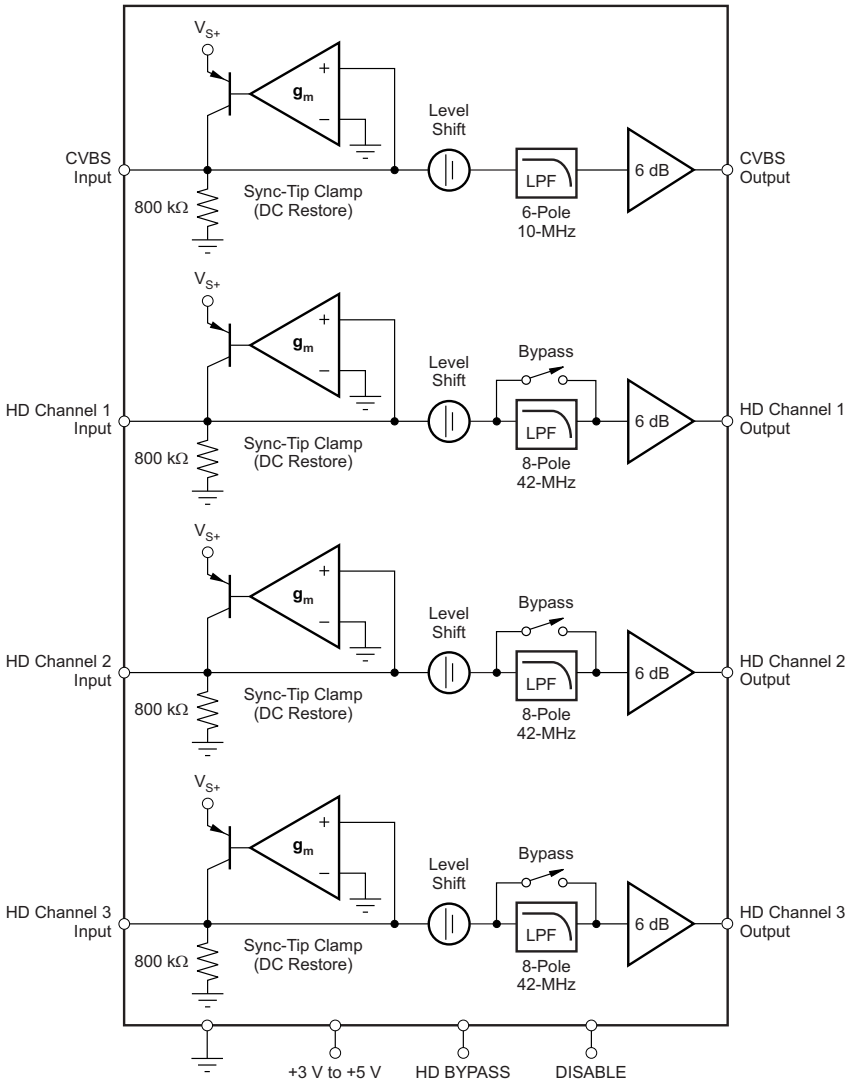
FUNCTIONAL BLOCK DIAGRAM



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TYPICAL CHARACTERISTICS: 3.3-V Standard-Definition (SD) Channel

At load = 150 Ω || 5 pF and dc-coupled input and output, unless otherwise noted.

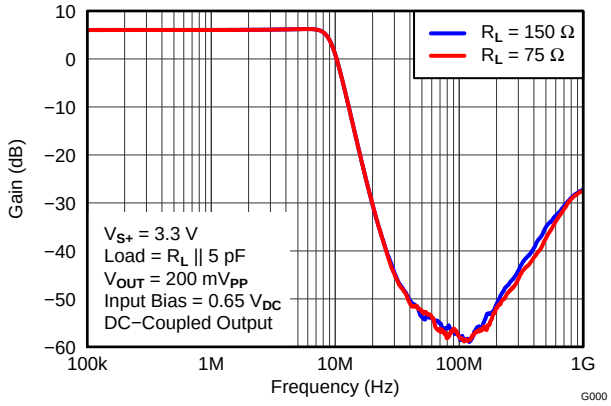

Figure 1. SD SMALL-SIGNAL GAIN vs FREQUENCY

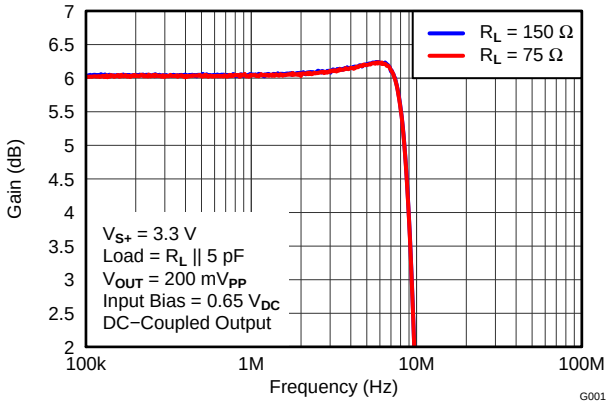

Figure 2. SD SMALL-SIGNAL GAIN vs FREQUENCY

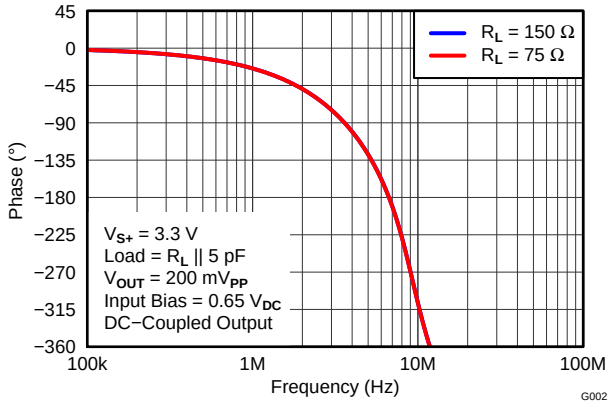

Figure 3. SD PHASE vs FREQUENCY

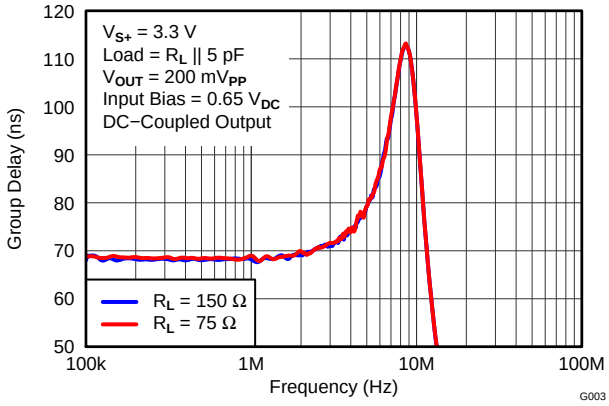

Figure 4. SD GROUP DELAY vs FREQUENCY

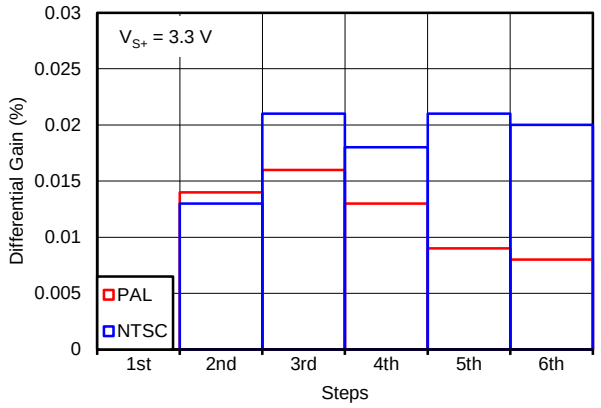

Figure 5. SD DIFFERENTIAL GAIN

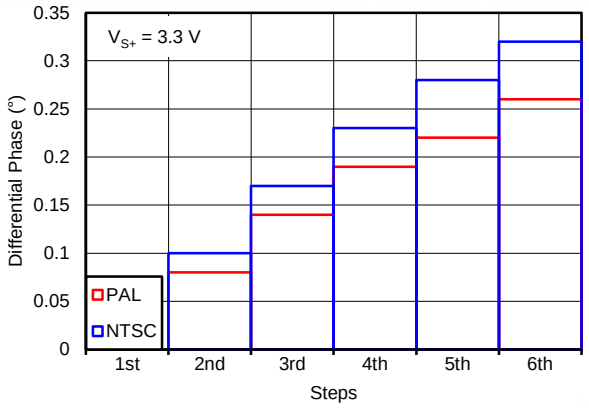

Figure 6. SD DIFFERENTIAL PHASE

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TYPICAL CHARACTERISTICS: 3.3-V Standard-Definition (SD) Channel (continued)

At load = 150 Ω || 5 pF and dc-coupled input and output, unless otherwise noted.

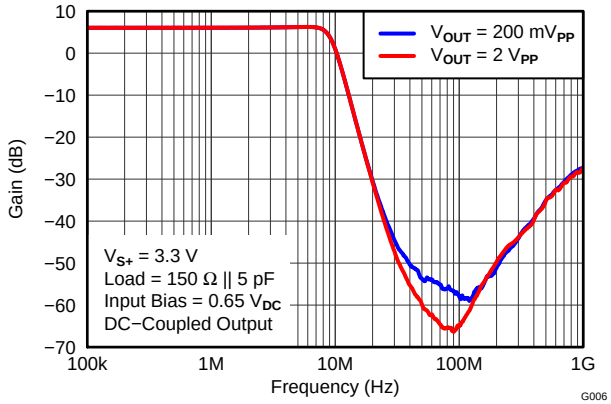

Figure 7. SD LARGE-SIGNAL GAIN vs FREQUENCY

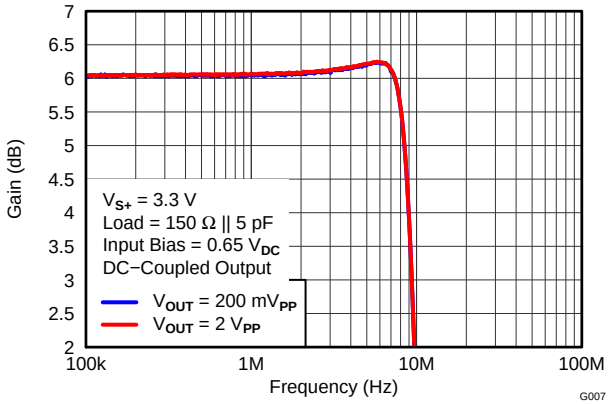

Figure 8. SD LARGE-SIGNAL GAIN vs FREQUENCY

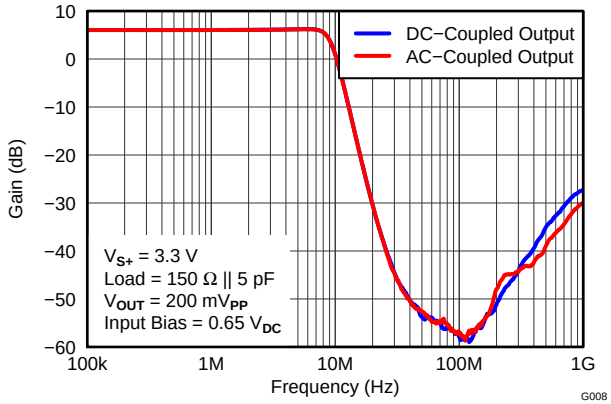

Figure 9. SD SMALL-SIGNAL GAIN vs FREQUENCY

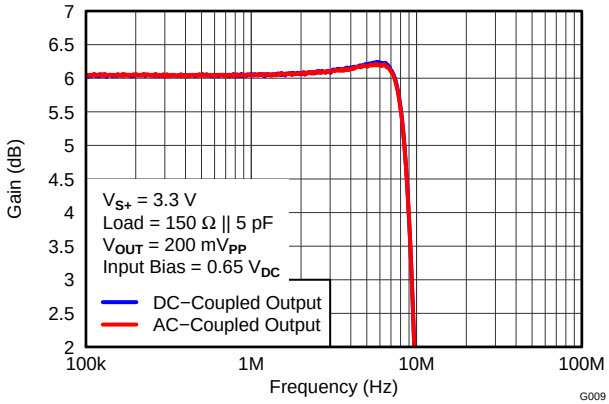

Figure 10. SD SMALL-SIGNAL GAIN vs FREQUENCY

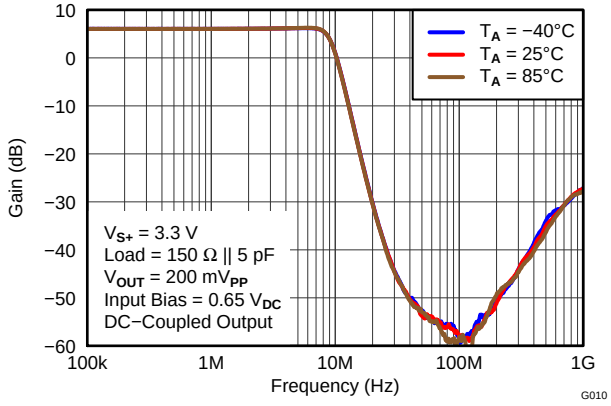

Figure 11. SD SMALL-SIGNAL GAIN vs FREQUENCY

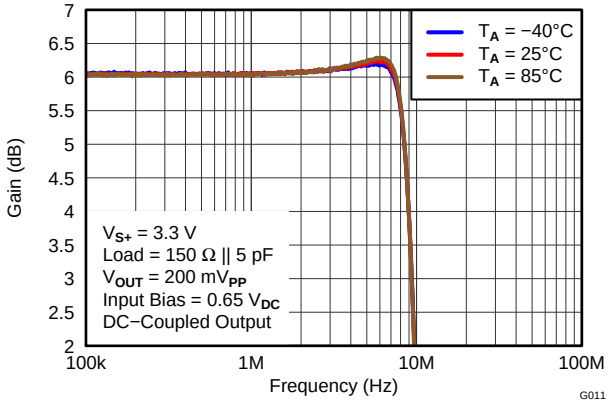

Figure 12. SD SMALL-SIGNAL GAIN vs FREQUENCY

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TYPICAL CHARACTERISTICS: 3.3-V Standard-Definition (SD) Channel (continued)

At load = 150 Ω || 5 pF and dc-coupled input and output, unless otherwise noted.

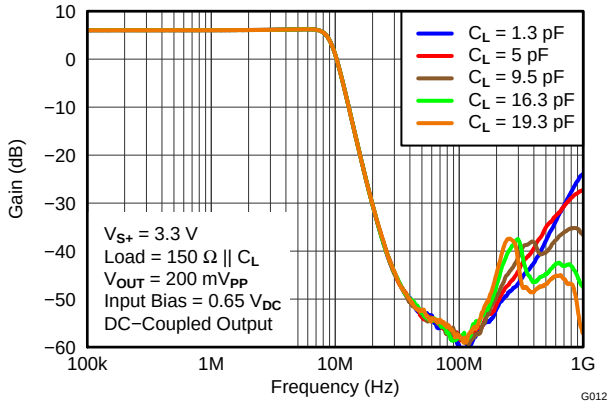

Figure 13. SD SMALL-SIGNAL GAIN vs FREQUENCY

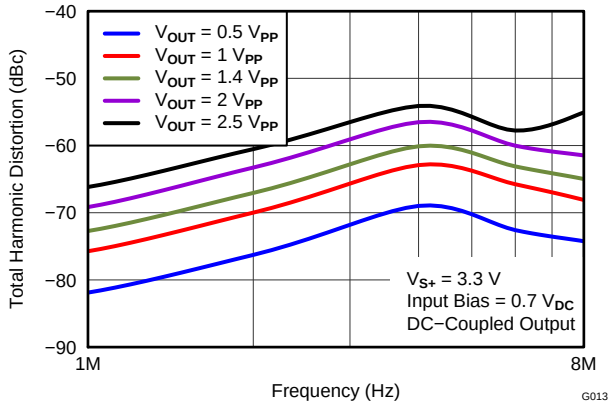

Figure 14. SD THD vs FREQUENCY

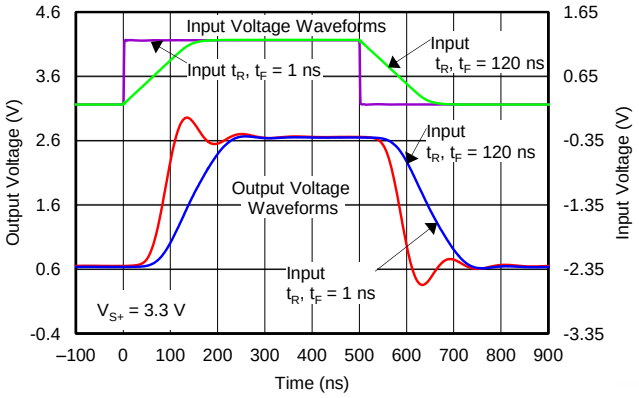

Figure 15. SD LARGE-SIGNAL PULSE RESPONSE vs TIME

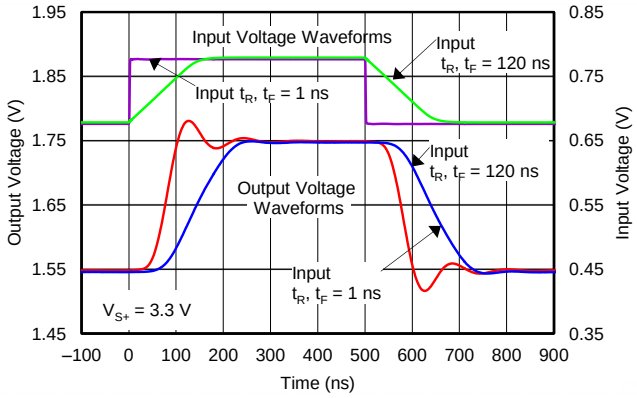

Figure 16. SD SMALL-SIGNAL PULSE RESPONSE vs TIME

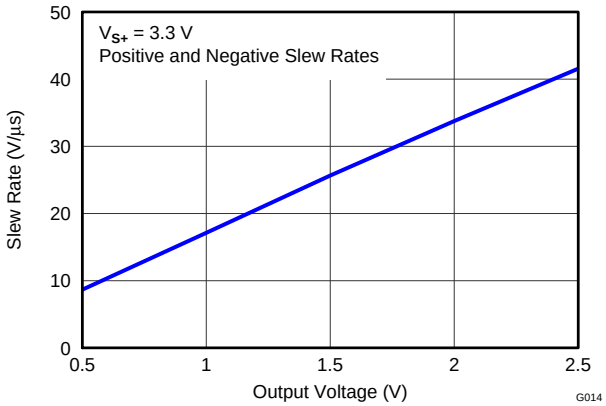

Figure 17. SD SLEW RATE vs OUTPUT VOLTAGE

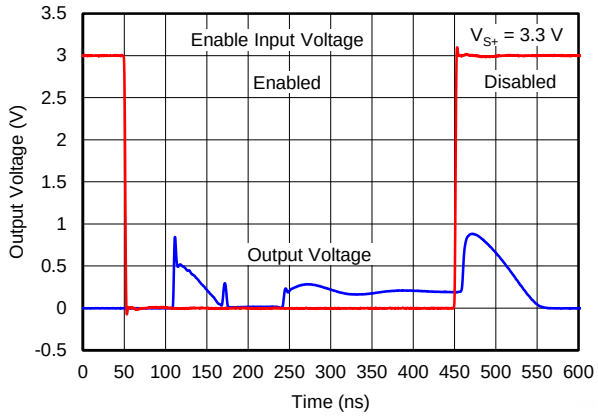

Figure 18. SD ENABLE AND DISABLE RESPONSE vs TIME

TYPICAL CHARACTERISTICS: 3.3-V Standard-Definition (SD) Channel (continued)

At load = 150 Ω || 5 pF and dc-coupled input and output, unless otherwise noted.

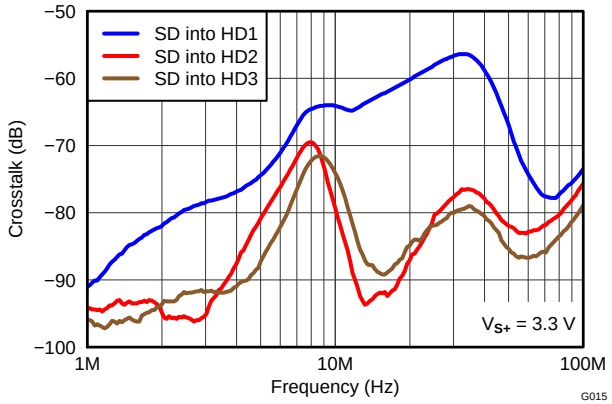

Figure 19. SD-TO-HD CROSSTALK vs FREQUENCY

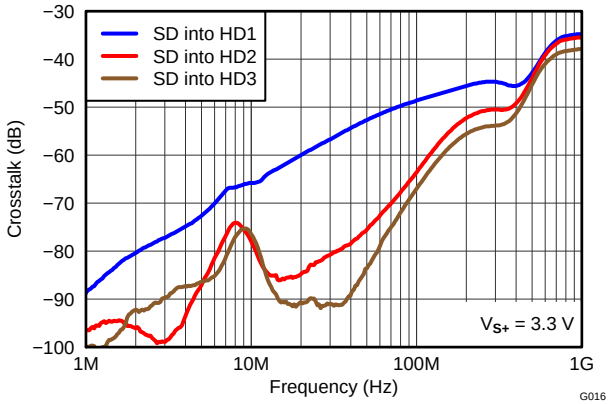

Figure 20. SD-TO-HD BYPASS CROSSTALK vs FREQUENCY

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TYPICAL CHARACTERISTICS: 3.3-V High-Definition (HD) Channels

At load = 150 Ω || 5 pF and dc-coupled input and output, unless otherwise noted.

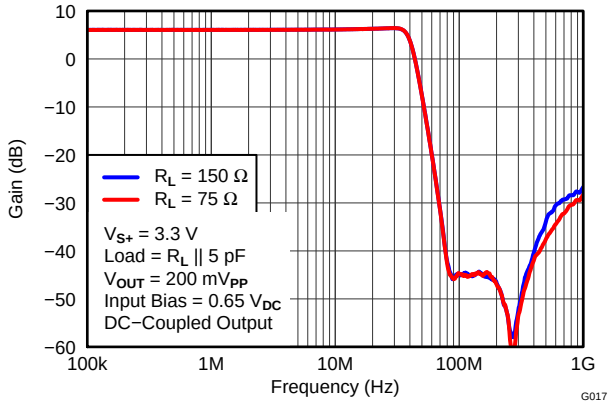

Figure 21. HD SMALL-SIGNAL GAIN vs FREQUENCY

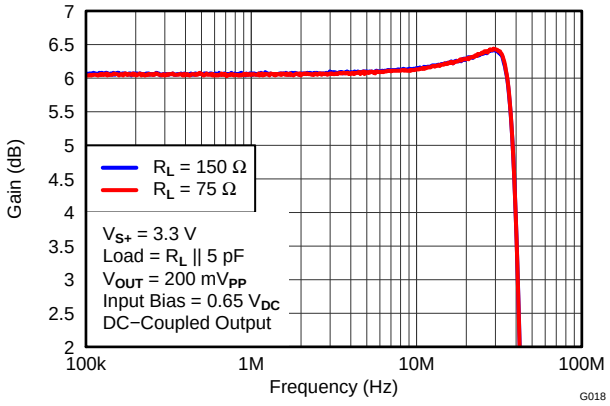

Figure 22. HD SMALL-SIGNAL GAIN vs FREQUENCY

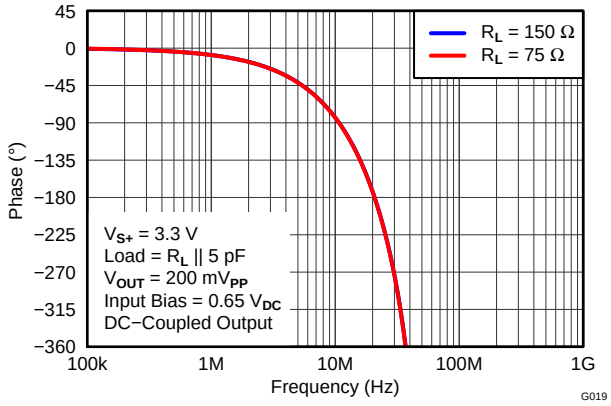

Figure 23. HD PHASE vs FREQUENCY

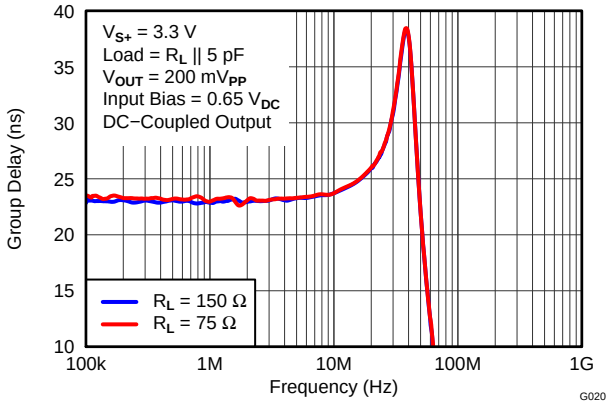

Figure 24. HD GROUP DELAY vs FREQUENCY

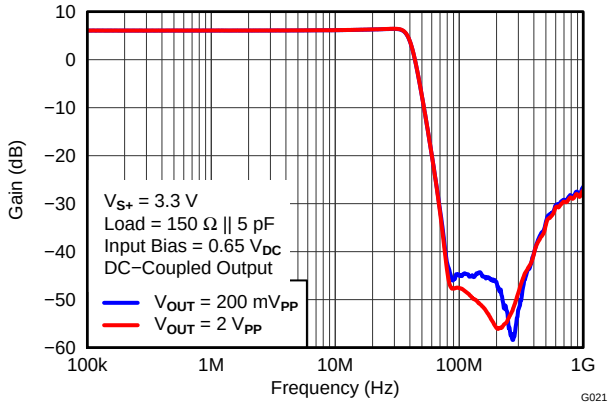

Figure 25. HD LARGE-SIGNAL GAIN vs FREQUENCY

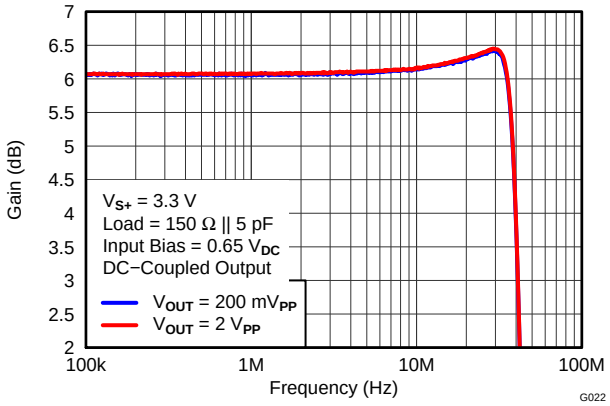

Figure 26. HD LARGE-SIGNAL GAIN vs FREQUENCY

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TYPICAL CHARACTERISTICS: 3.3-V High-Definition (HD) Channels (continued)

At load = 150 Ω || 5 pF and dc-coupled input and output, unless otherwise noted.

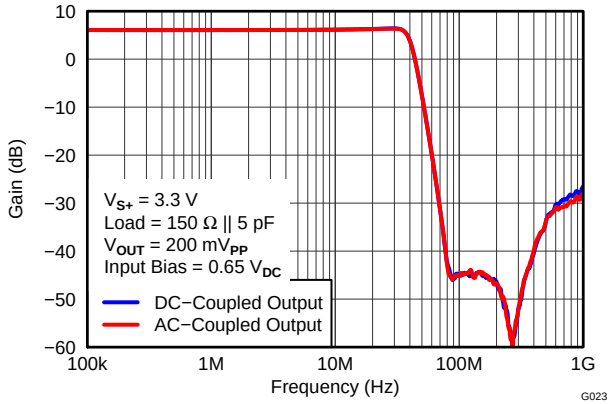

Figure 27. HD SMALL-SIGNAL GAIN vs FREQUENCY

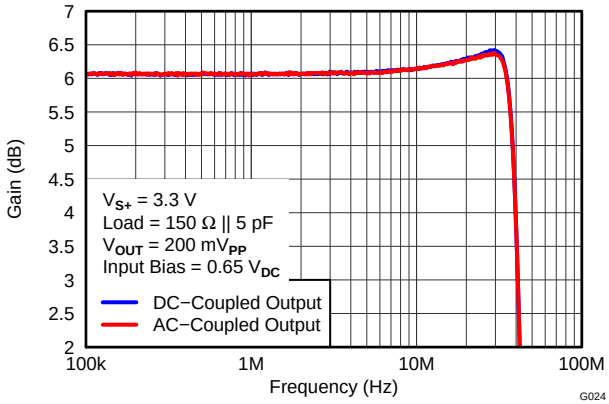

Figure 28. HD SMALL-SIGNAL GAIN vs FREQUENCY

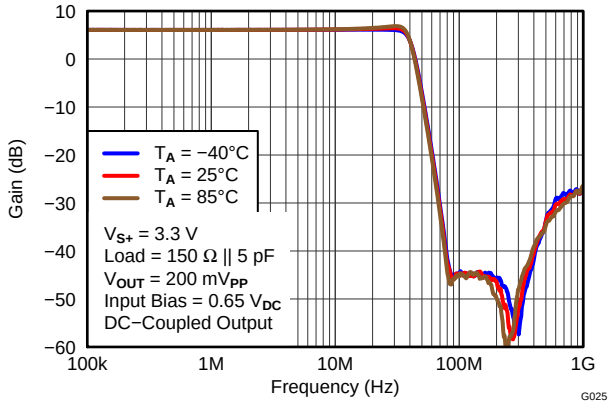

Figure 29. HD SMALL-SIGNAL GAIN vs FREQUENCY

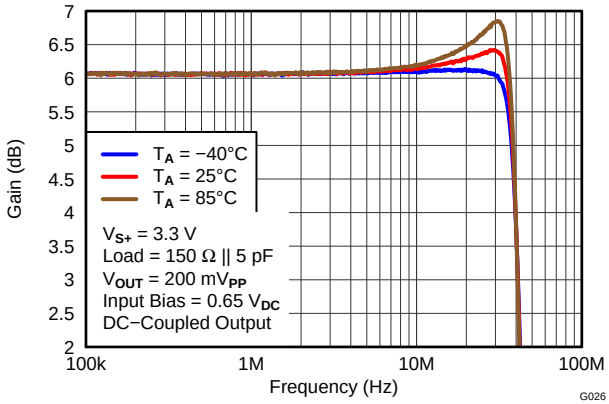

Figure 30. HD SMALL-SIGNAL GAIN vs FREQUENCY

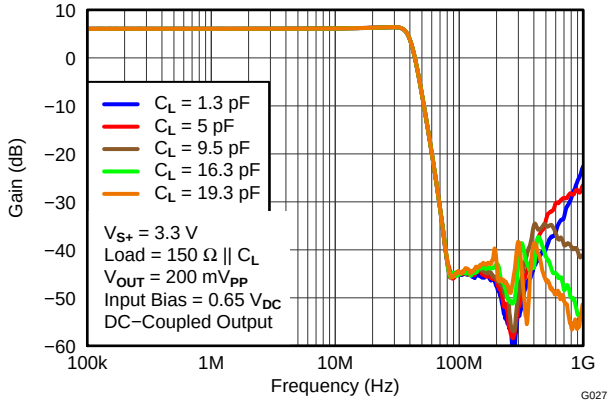

Figure 31. HD SMALL-SIGNAL GAIN vs FREQUENCY

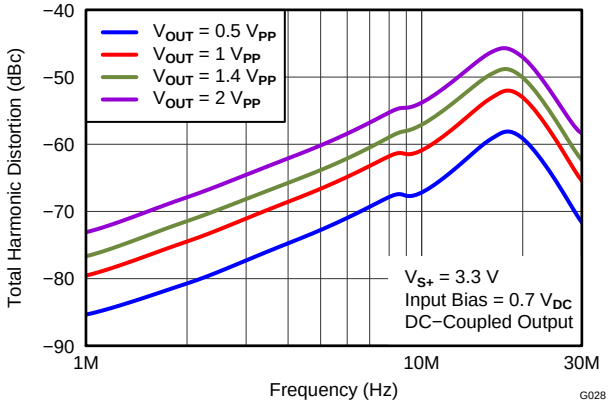

Figure 32. HD THD vs FREQUENCY

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TYPICAL CHARACTERISTICS: 3.3-V High-Definition (HD) Channels (continued)

At load = 150 Ω || 5 pF and dc-coupled input and output, unless otherwise noted.

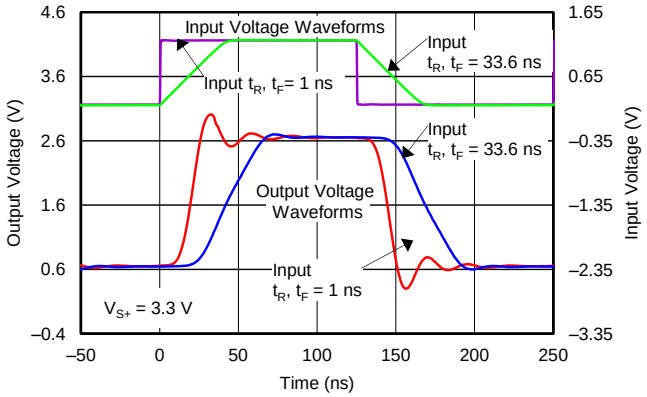

Figure 33. HD LARGE-SIGNAL PULSE RESPONSE vs TIME

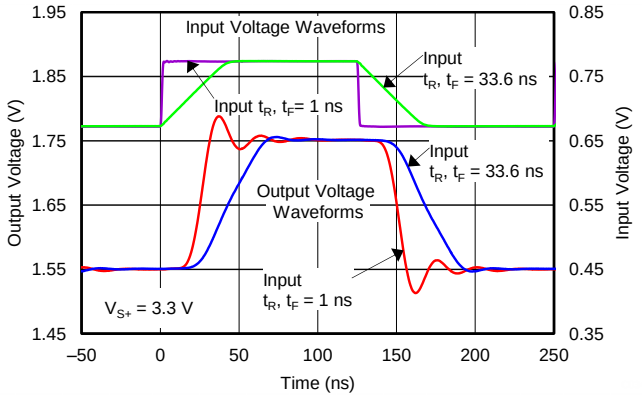

Figure 34. HD SMALL-SIGNAL PULSE RESPONSE vs TIME

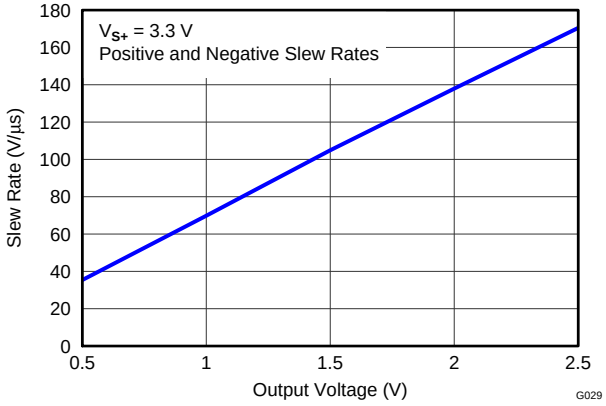

Figure 35. HD SLEW RATE vs OUTPUT VOLTAGE

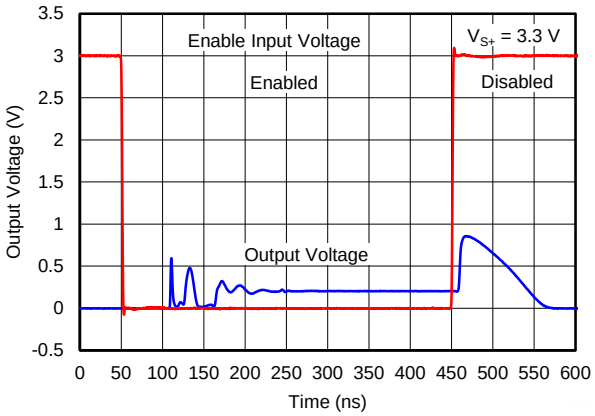

Figure 36. HD ENABLE AND DISABLE RESPONSE vs TIME

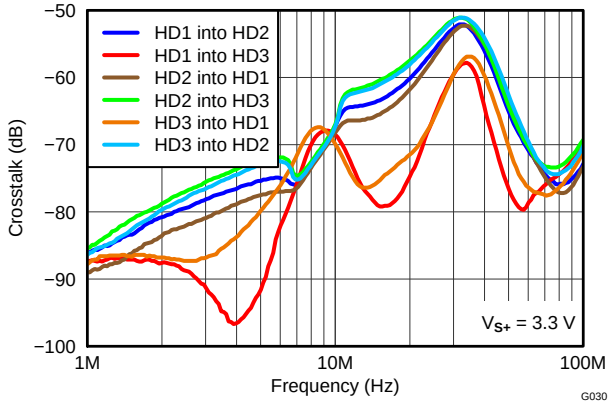

Figure 37. HD-TO-HD CROSSTALK vs FREQUENCY

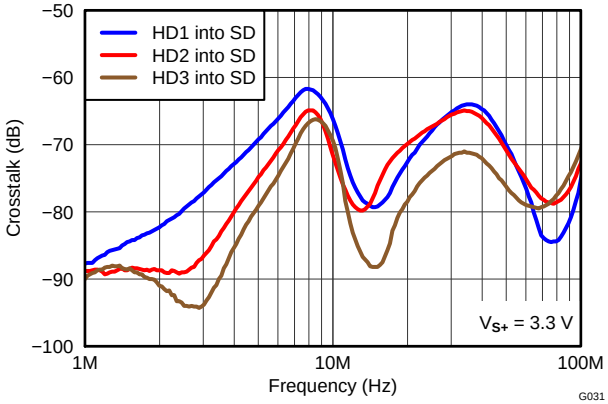

Figure 38. HD-TO-SD CROSSTALK vs FREQUENCY

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TYPICAL CHARACTERISTICS: 3.3-V High-Definition (HD) Bypass Channels

At load = 150 Ω || 5 pF and dc-coupled input and output, unless otherwise noted.

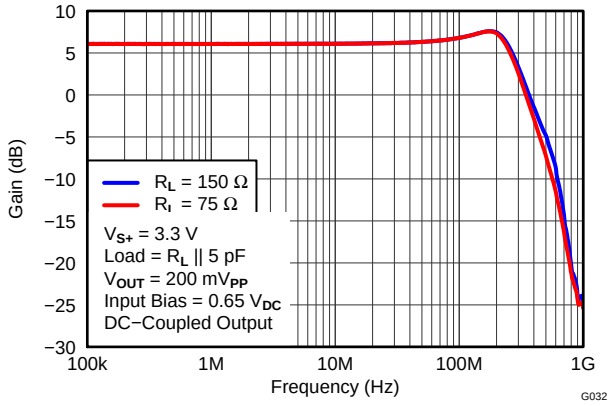

Figure 39. HD BYPASS SMALL-SIGNAL GAIN vs FREQUENCY

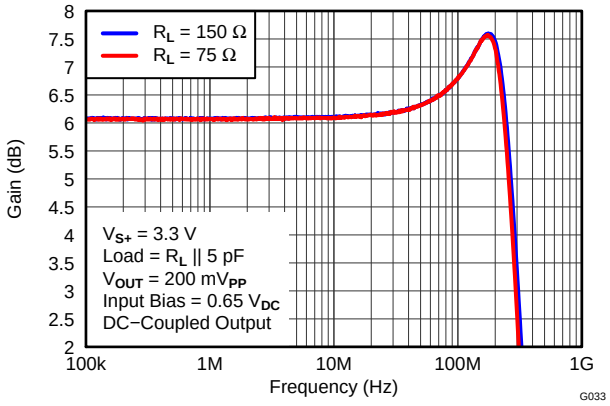

Figure 40. HD BYPASS SMALL-SIGNAL GAIN vs FREQUENCY

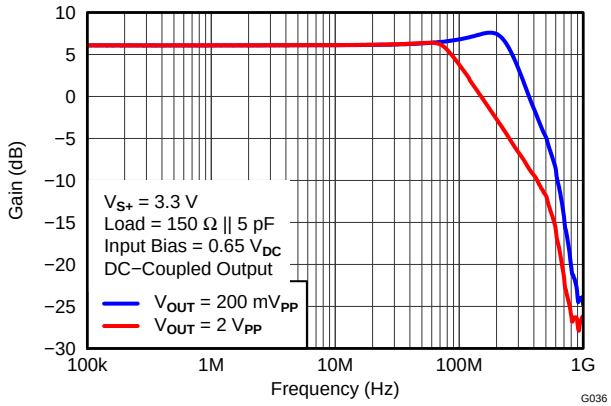

Figure 41. HD BYPASS LARGE-SIGNAL GAIN vs FREQUENCY

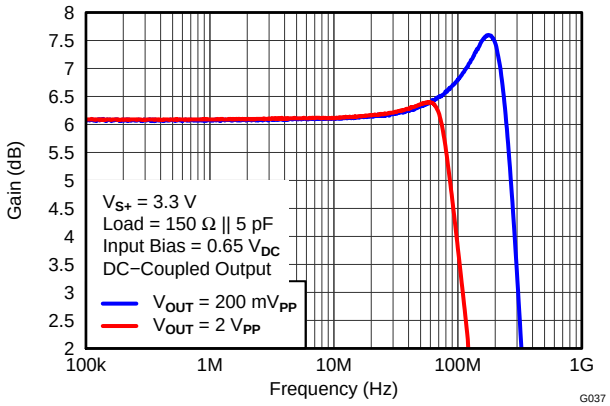

Figure 42. HD BYPASS LARGE-SIGNAL GAIN vs FREQUENCY

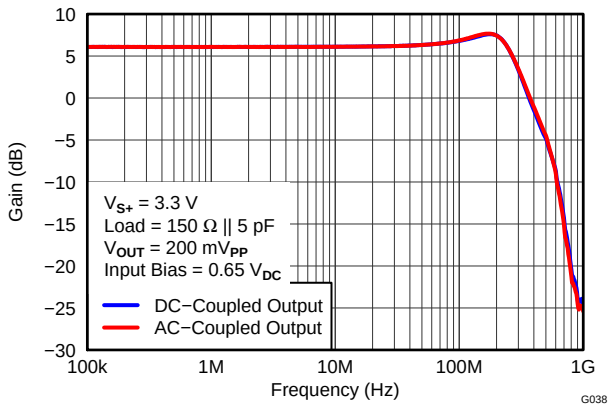

Figure 43. HD BYPASS SMALL-SIGNAL GAIN vs FREQUENCY

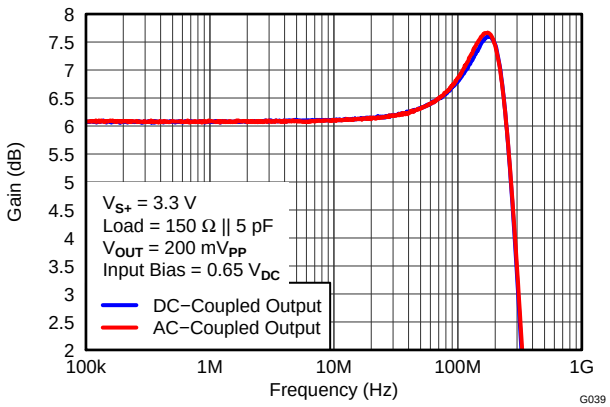

Figure 44. HD BYPASS SMALL-SIGNAL GAIN vs FREQUENCY

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TYPICAL CHARACTERISTICS: 3.3-V High-Definition (HD) Bypass Channels (continued)

At load = 150 Ω || 5 pF and dc-coupled input and output, unless otherwise noted.

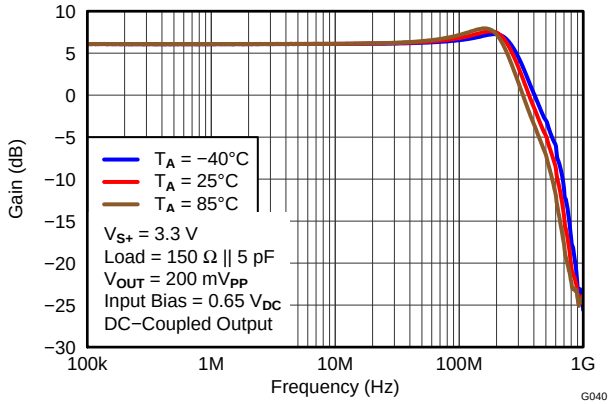

Figure 45. HD BYPASS SMALL-SIGNAL GAIN vs FREQUENCY

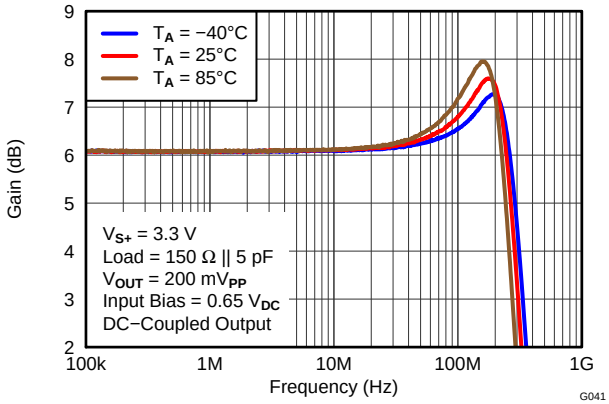

Figure 46. HD BYPASS SMALL-SIGNAL GAIN vs FREQUENCY

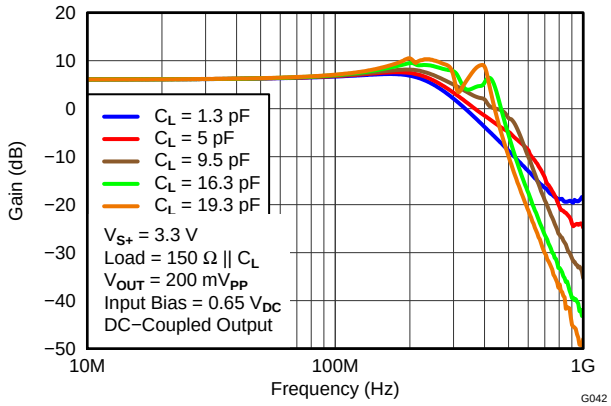

Figure 47. HD BYPASS SMALL-SIGNAL GAIN vs FREQUENCY

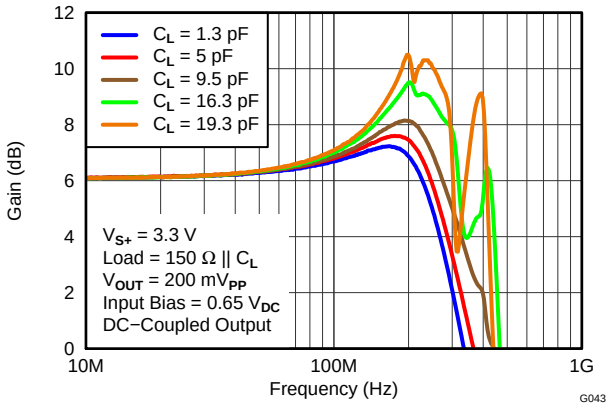

Figure 48. HD BYPASS SMALL-SIGNAL GAIN vs FREQUENCY

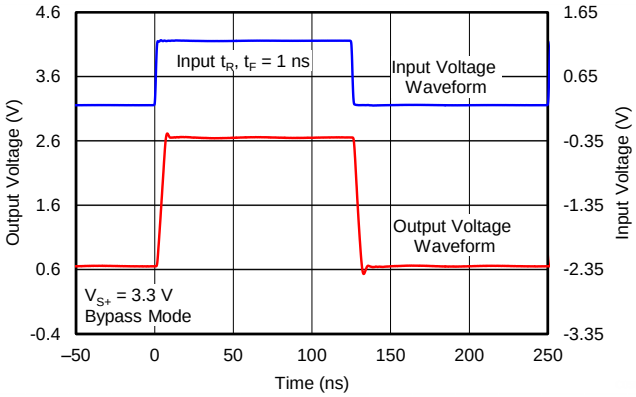

Figure 49. HD BYPASS LARGE-SIGNAL PULSE RESPONSE vs TIME

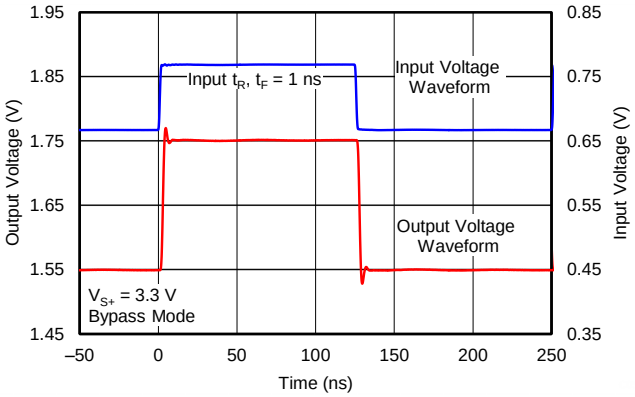

Figure 50. HD BYPASS SMALL-SIGNAL PULSE RESPONSE vs TIME

TYPICAL CHARACTERISTICS: 3.3-V High-Definition (HD) Bypass Channels (continued)

At load = 150 Ω || 5 pF and dc-coupled input and output, unless otherwise noted.

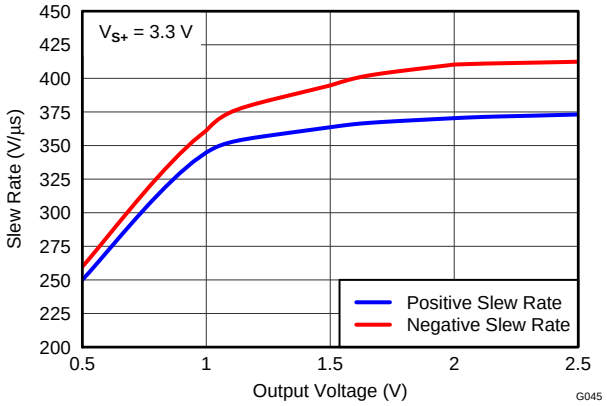

Figure 51. HD BYPASS SLEW RATE vs OUTPUT VOLTAGE

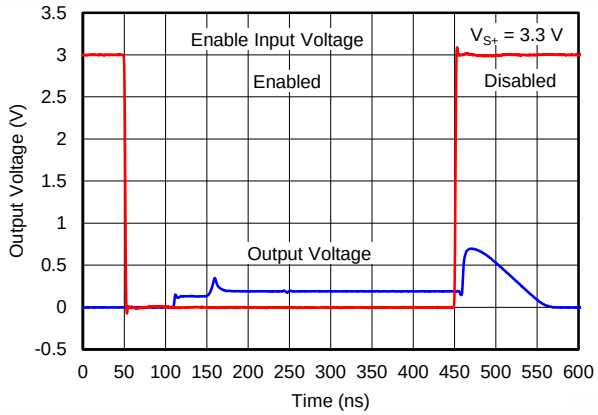

Figure 52. HD ENABLE AND DISABLE RESPONSE vs TIME

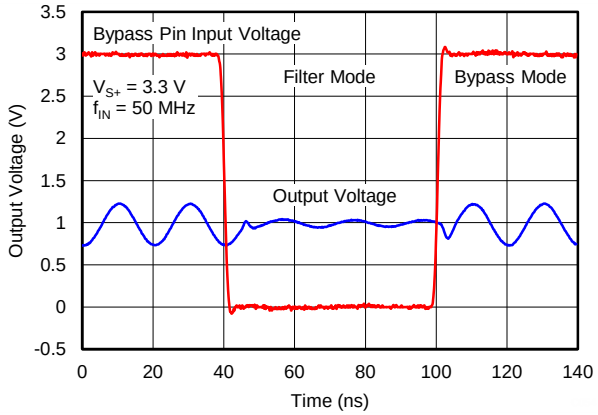

Figure 53. HD FILTER AND BYPASS RESPONSE vs TIME

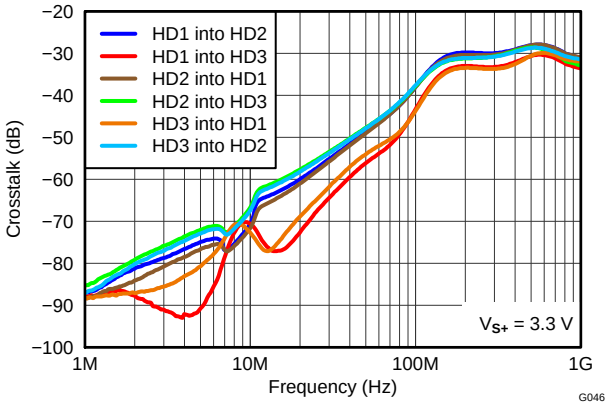

Figure 54. HD BYPASS TO HD BYPASS CROSSTALK vs FREQUENCY

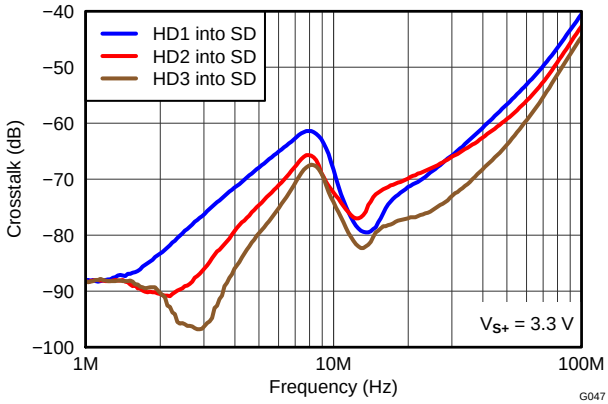

Figure 55. HD BYPASS TO SD CROSSTALK vs FREQUENCY

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TYPICAL CHARACTERISTICS: 5-V Standard-Definition (SD) Channel

At load = 150 Ω || 5 pF and dc-coupled input and output, unless otherwise noted.

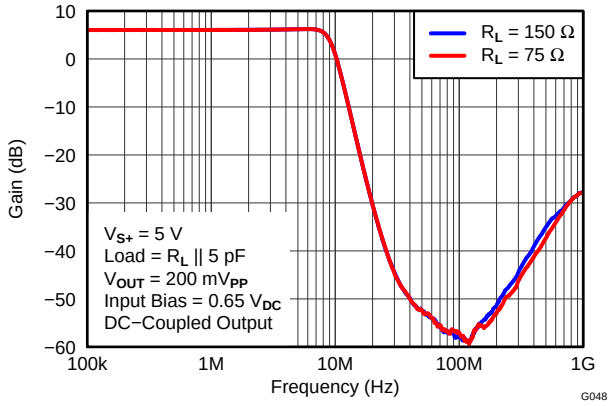

Figure 56. SD SMALL-SIGNAL GAIN vs FREQUENCY

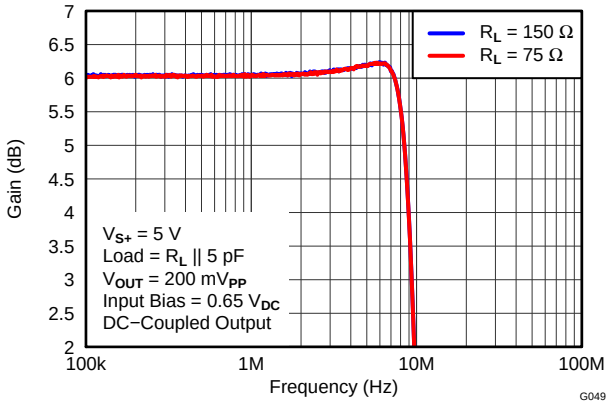

Figure 57. SD SMALL-SIGNAL GAIN vs FREQUENCY

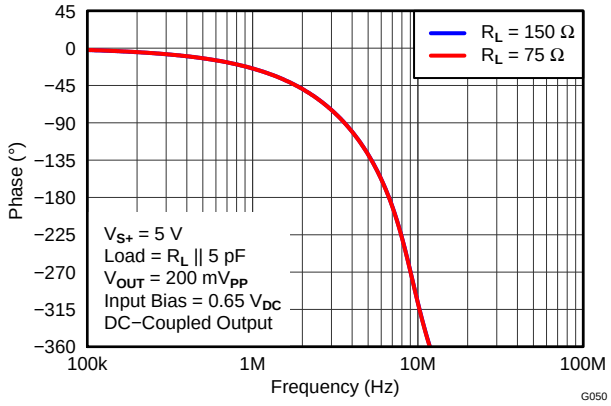

Figure 58. SD PHASE vs FREQUENCY

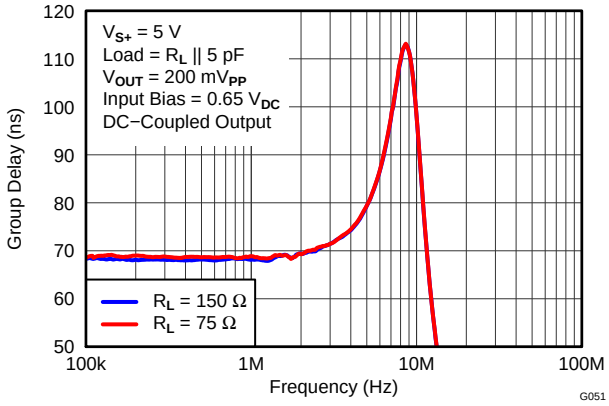

Figure 59. SD GROUP DELAY vs FREQUENCY

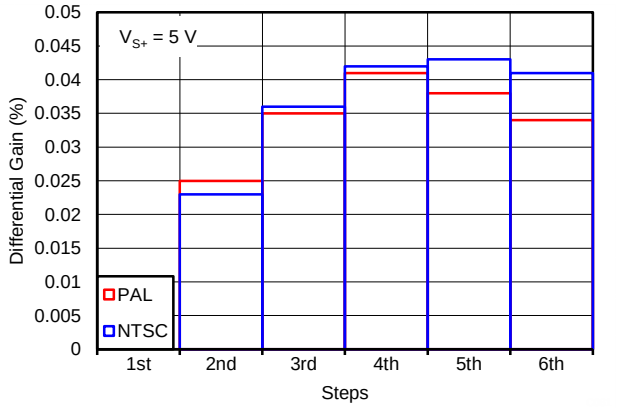

Figure 60. SD DIFFERENTIAL GAIN

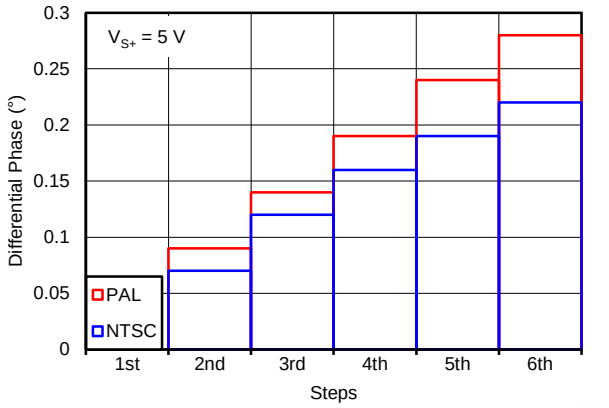

Figure 61. SD DIFFERENTIAL PHASE

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TYPICAL CHARACTERISTICS: 5-V Standard-Definition (SD) Channel (continued)

At load = 150 Ω || 5 pF and dc-coupled input and output, unless otherwise noted.

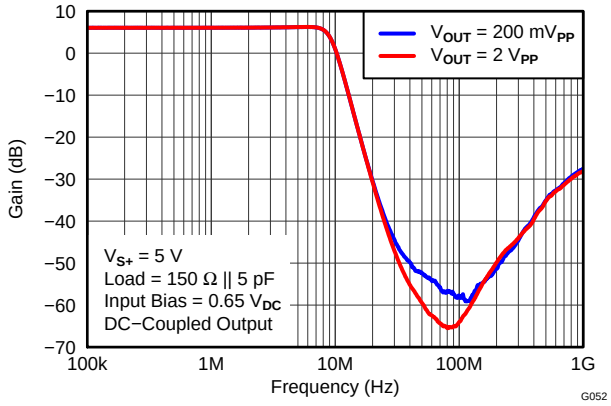

Figure 62. SD LARGE-SIGNAL GAIN vs FREQUENCY

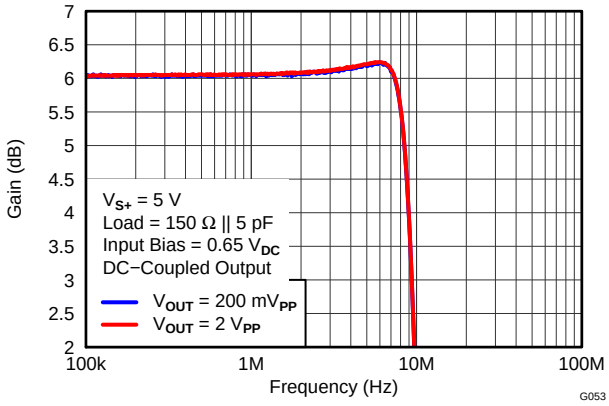

Figure 63. SD LARGE-SIGNAL GAIN vs FREQUENCY

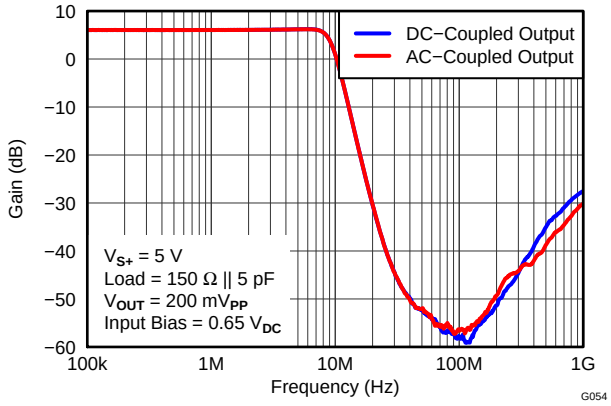

Figure 64. SD SMALL-SIGNAL GAIN vs FREQUENCY

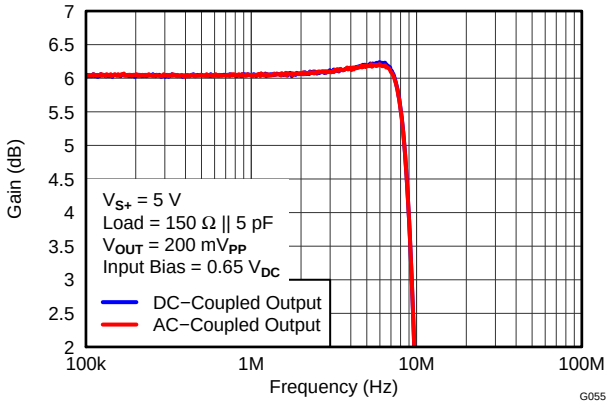

Figure 65. SD SMALL-SIGNAL GAIN vs FREQUENCY

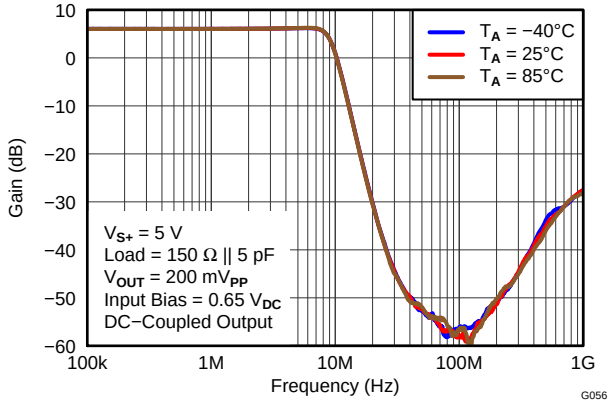

Figure 66. SD SMALL-SIGNAL GAIN vs FREQUENCY

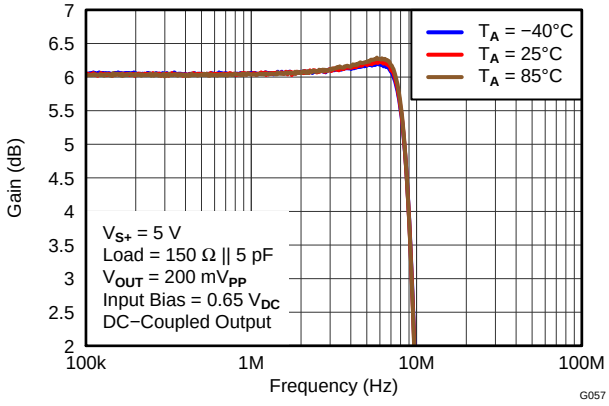

Figure 67. SD SMALL-SIGNAL GAIN vs FREQUENCY

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TYPICAL CHARACTERISTICS: 5-V Standard-Definition (SD) Channel (continued)

At load = 150 Ω || 5 pF and dc-coupled input and output, unless otherwise noted.

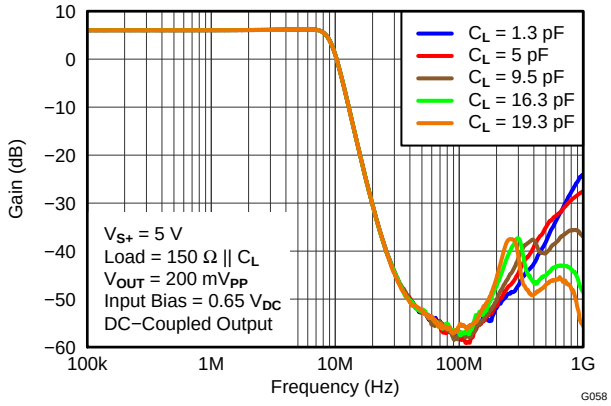

Figure 68. SD SMALL-SIGNAL GAIN vs FREQUENCY

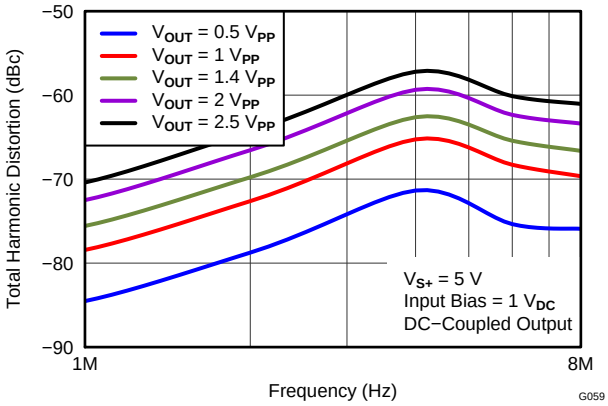

Figure 69. SD THD vs FREQUENCY

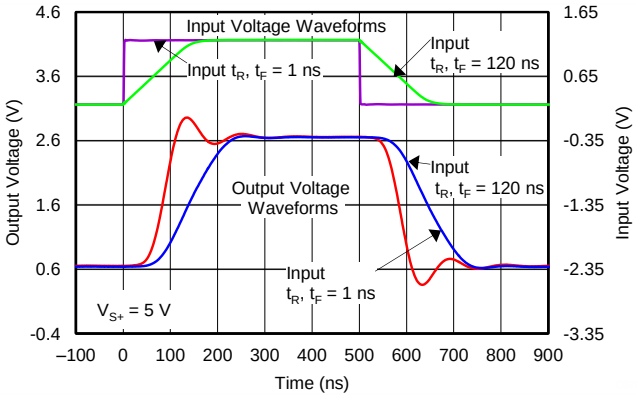

Figure 70. SD LARGE-SIGNAL PULSE RESPONSE vs TIME

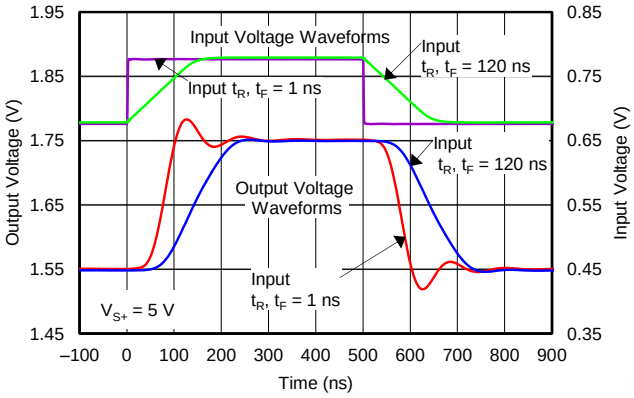

Figure 71. SD SMALL-SIGNAL PULSE RESPONSE vs TIME

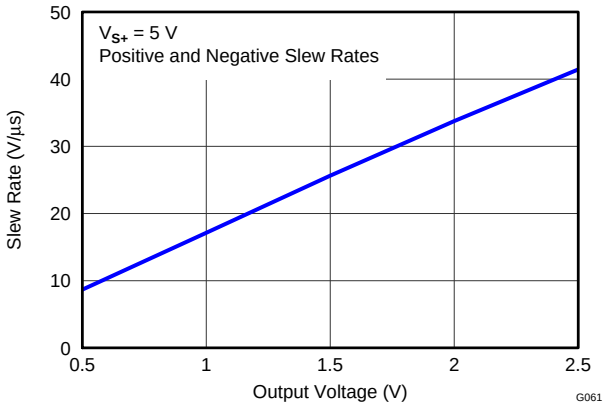

Figure 72. SD SLEW RATE vs OUTPUT VOLTAGE

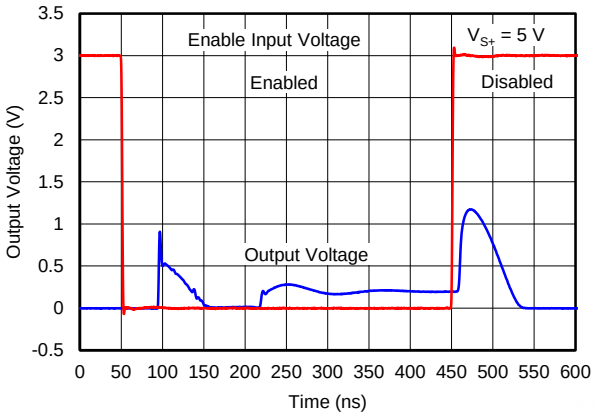

Figure 73. SD ENABLE AND DISABLE RESPONSE vs TIME

TYPICAL CHARACTERISTICS: 5-V Standard-Definition (SD) Channel (continued)

At load = 150 Ω || 5 pF and dc-coupled input and output, unless otherwise noted.

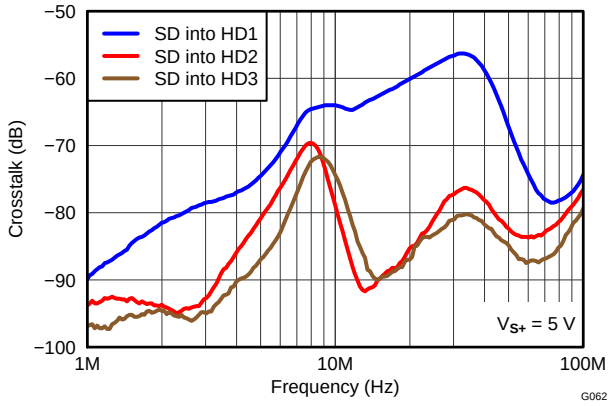

Figure 74. SD-TO-HD CROSSTALK vs FREQUENCY

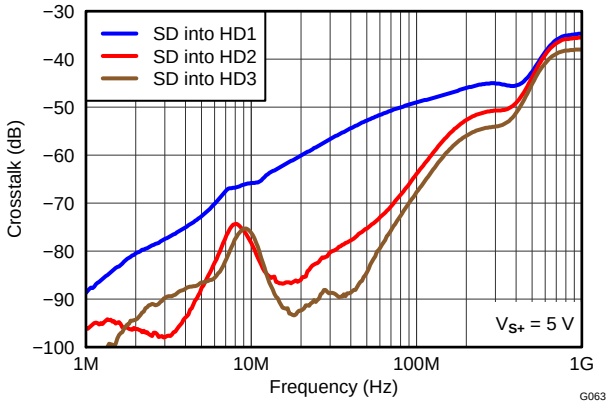

Figure 75. SD-TO-HD BYPASS CROSSTALK vs FREQUENCY

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TYPICAL CHARACTERISTICS: 5-V High-Definition (HD) Channels

At load = 150 Ω || 5 pF and dc-coupled input and output, unless otherwise noted.

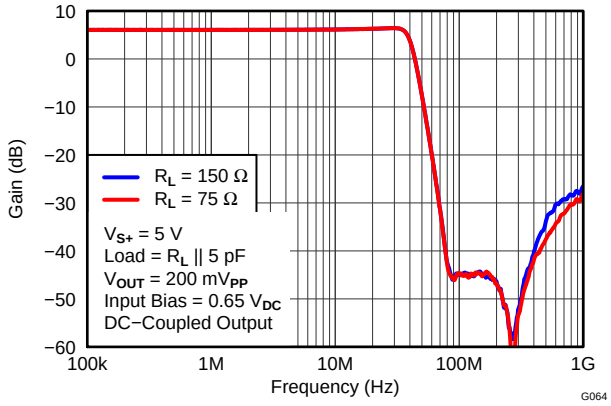

Figure 76. HD SMALL-SIGNAL GAIN vs FREQUENCY

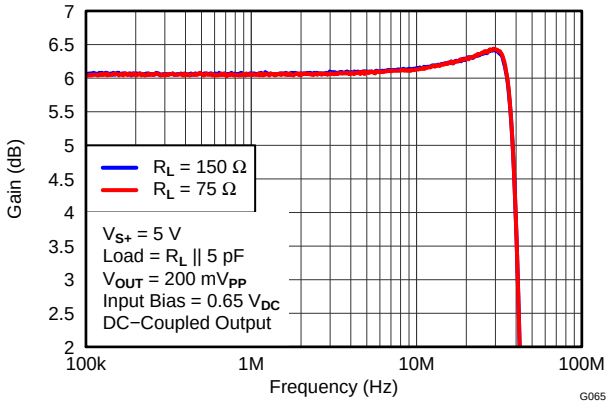

Figure 77. HD SMALL-SIGNAL GAIN vs FREQUENCY

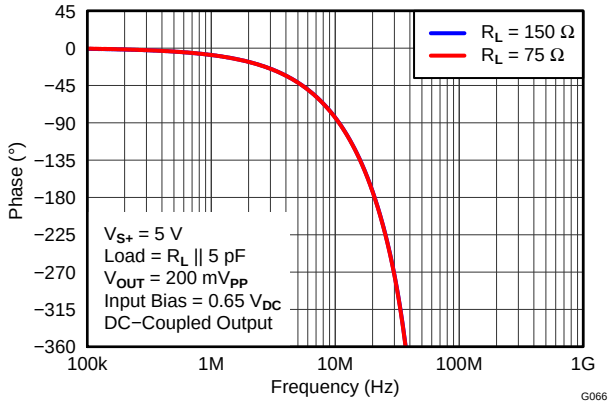

Figure 78. HD PHASE vs FREQUENCY

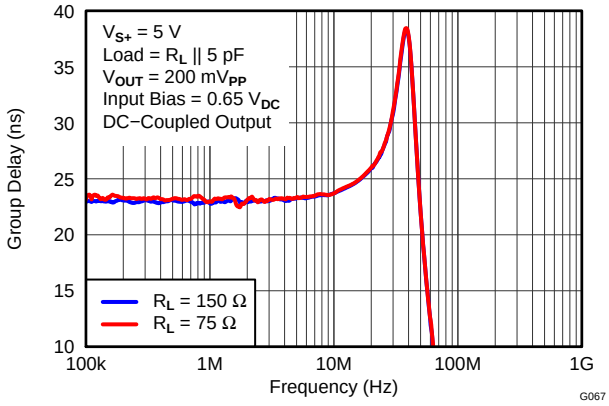

Figure 79. HD GROUP DELAY vs FREQUENCY

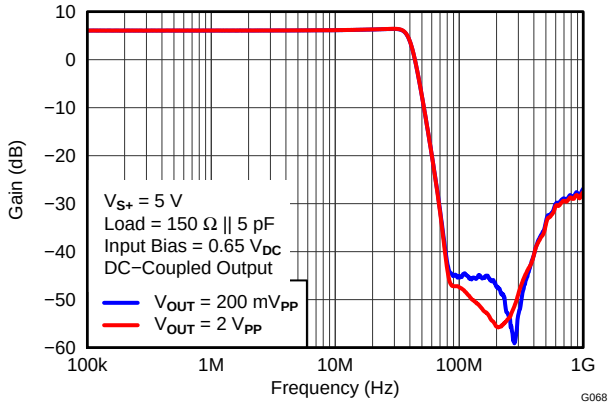

Figure 80. HD LARGE-SIGNAL GAIN vs FREQUENCY

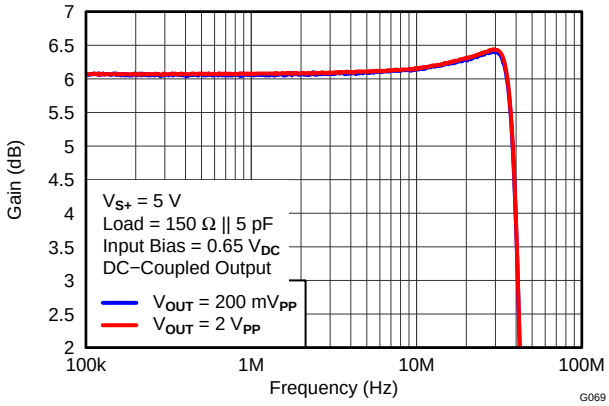

Figure 81. HD LARGE-SIGNAL GAIN vs FREQUENCY

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TYPICAL CHARACTERISTICS: 5-V High-Definition (HD) Channels (continued)

At load = 150 Ω || 5 pF and dc-coupled input and output, unless otherwise noted.

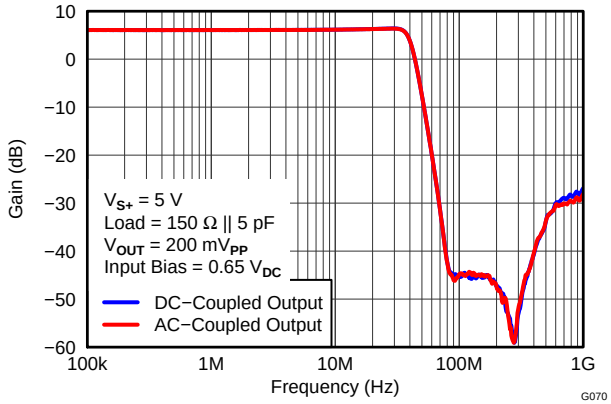

Figure 82. HD SMALL-SIGNAL GAIN vs FREQUENCY

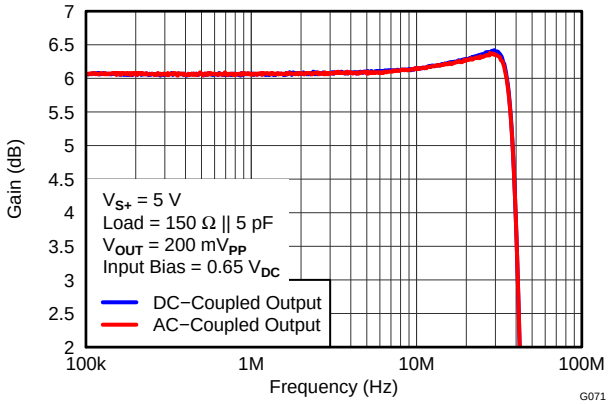

Figure 83. HD SMALL-SIGNAL GAIN vs FREQUENCY

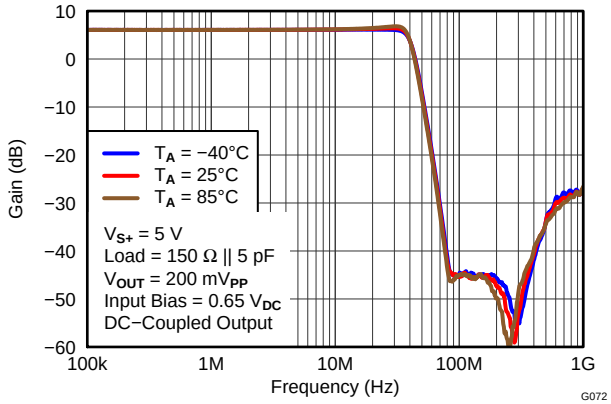

Figure 84. HD SMALL-SIGNAL GAIN vs FREQUENCY

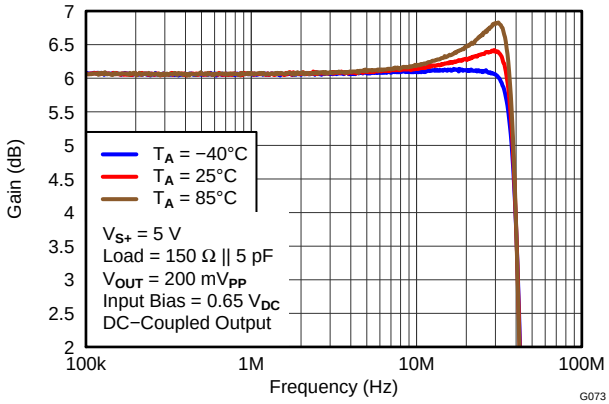

Figure 85. HD SMALL-SIGNAL GAIN vs FREQUENCY

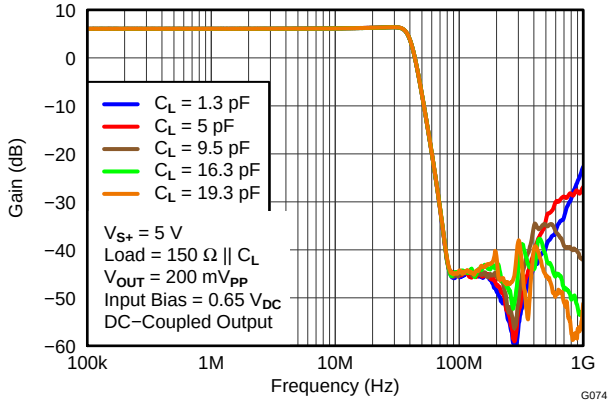

Figure 86. HD SMALL-SIGNAL GAIN vs FREQUENCY

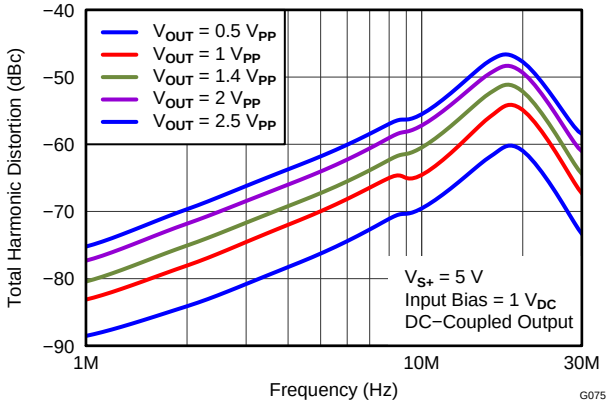

Figure 87. HD THD vs FREQUENCY

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TYPICAL CHARACTERISTICS: 5-V High-Definition (HD) Channels (continued)

At load = 150 Ω || 5 pF and dc-coupled input and output, unless otherwise noted.

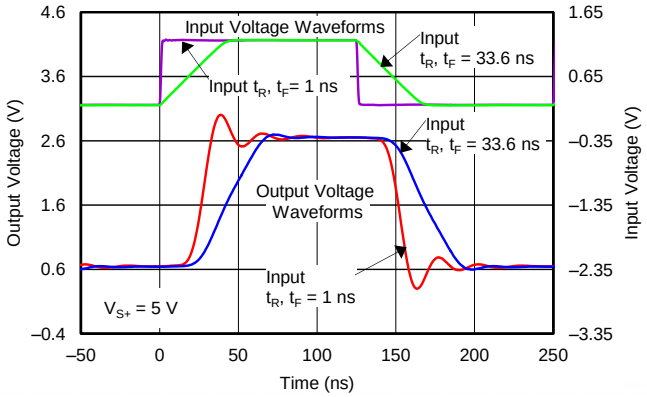

Figure 88. HD LARGE-SIGNAL PULSE RESPONSE vs TIME

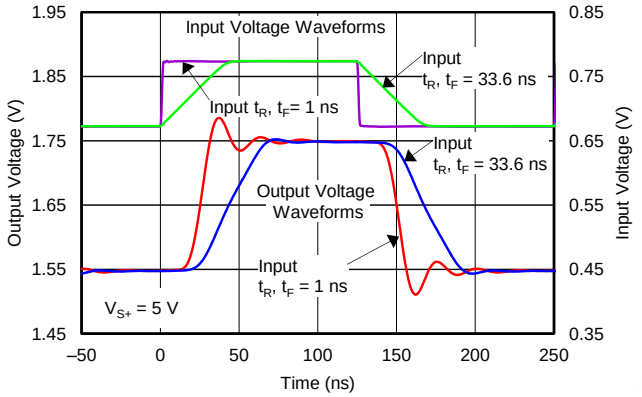

Figure 89. HD SMALL-SIGNAL PULSE RESPONSE vs TIME

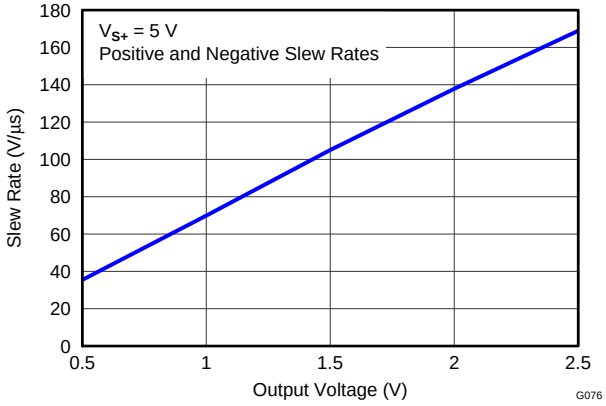

Figure 90. HD SLEW RATE vs OUTPUT VOLTAGE

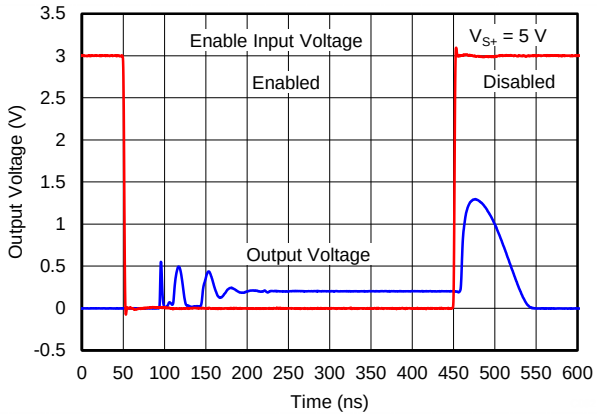

Figure 91. HD ENABLE AND DISABLE RESPONSE vs TIME

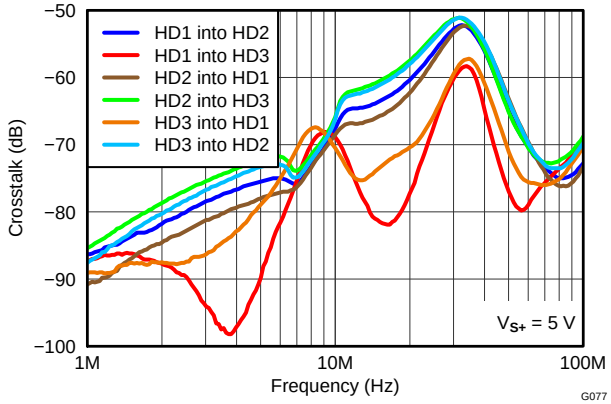

Figure 92. HD-TO-HD CROSSTALK vs FREQUENCY

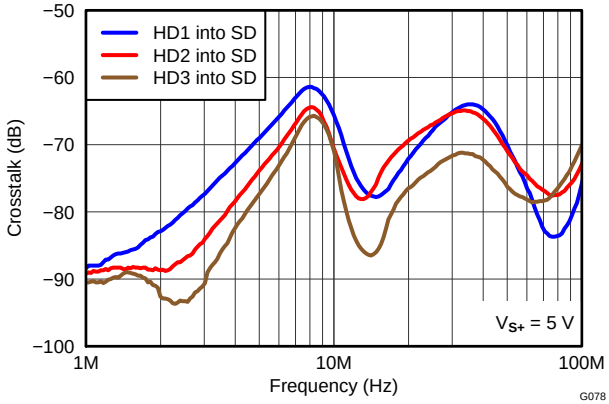

Figure 93. HD-TO-SD CROSSTALK vs FREQUENCY

TYPICAL CHARACTERISTICS: 5-V High-Definition (HD) Bypass Channels

At load = 150 Ω || 5 pF and dc-coupled input and output, unless otherwise noted.

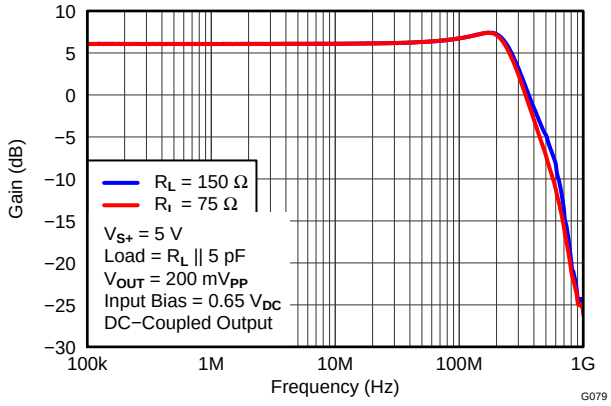

Figure 94. HD BYPASS SMALL-SIGNAL GAIN vs FREQUENCY

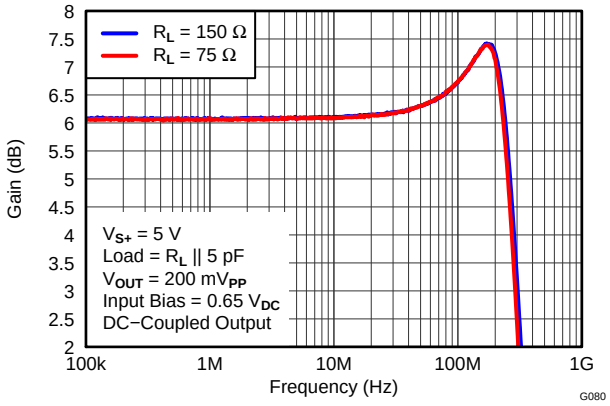

Figure 95. HD BYPASS SMALL-SIGNAL GAIN vs FREQUENCY

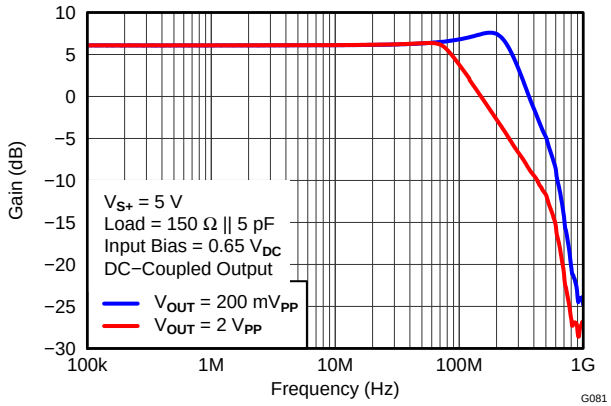

Figure 96. HD BYPASS LARGE-SIGNAL GAIN vs FREQUENCY

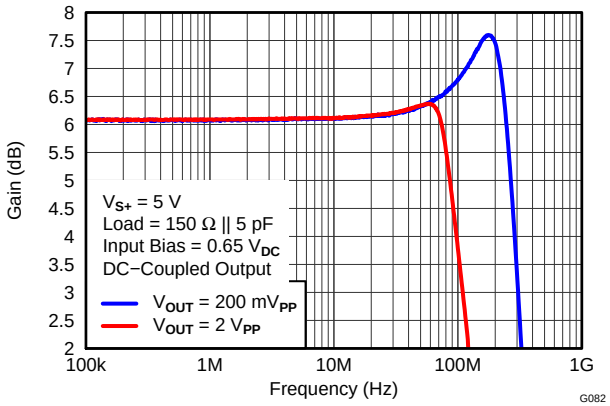

Figure 97. HD BYPASS LARGE-SIGNAL GAIN vs FREQUENCY

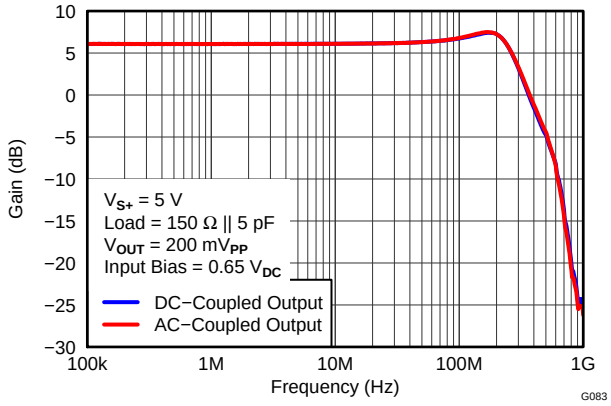

Figure 98. HD BYPASS SMALL-SIGNAL GAIN vs FREQUENCY

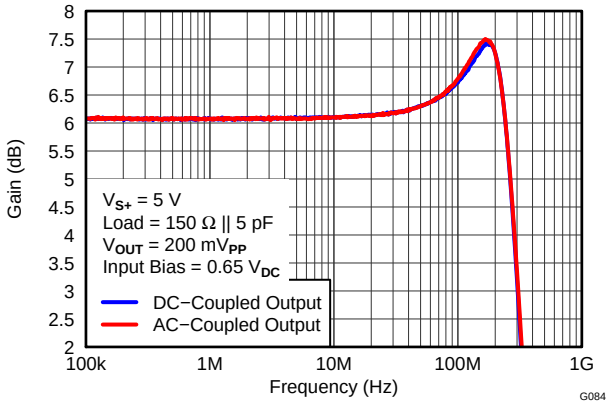

Figure 99. HD BYPASS SMALL-SIGNAL GAIN vs FREQUENCY

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TYPICAL CHARACTERISTICS: 5-V High-Definition (HD) Bypass Channels (continued)

At load = 150 Ω || 5 pF and dc-coupled input and output, unless otherwise noted.

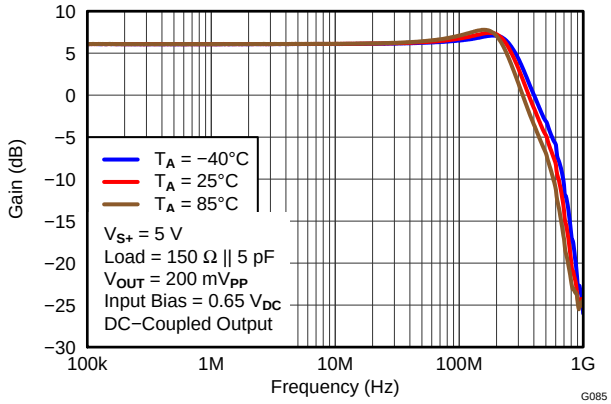

Figure 100. HD BYPASS SMALL-SIGNAL GAIN vs FREQUENCY

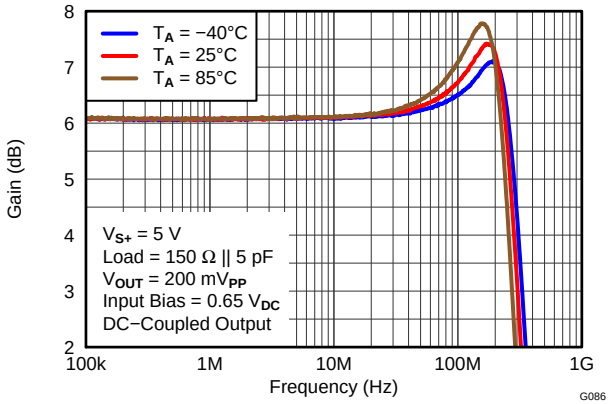

Figure 101. HD BYPASS SMALL-SIGNAL GAIN vs FREQUENCY

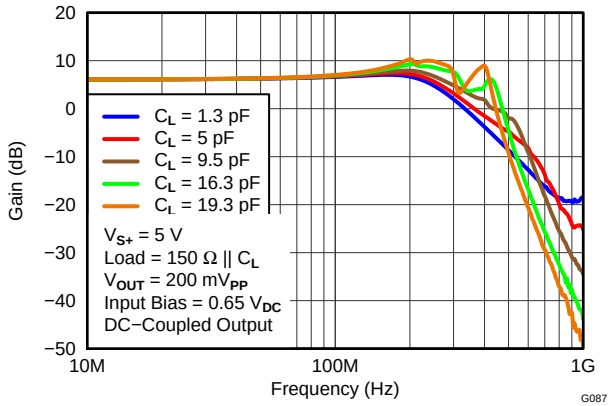

Figure 102. HD BYPASS SMALL-SIGNAL GAIN vs FREQUENCY

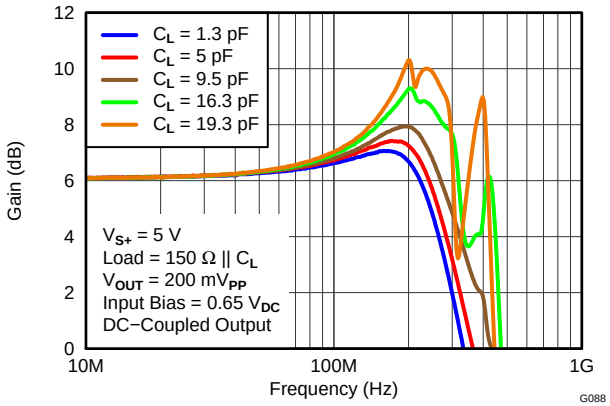

Figure 103. HD BYPASS SMALL-SIGNAL GAIN vs FREQUENCY

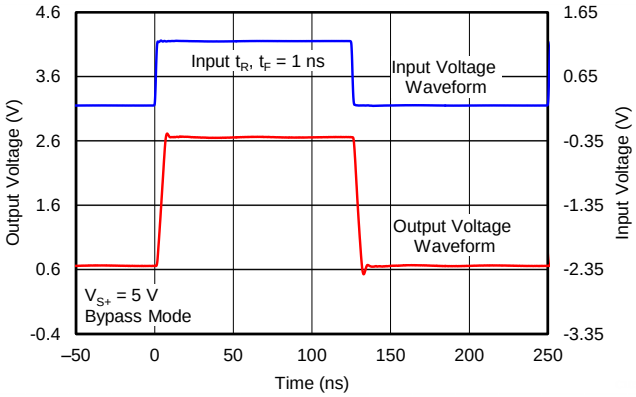

Figure 104. HD BYPASS LARGE-SIGNAL PULSE RESPONSE vs TIME

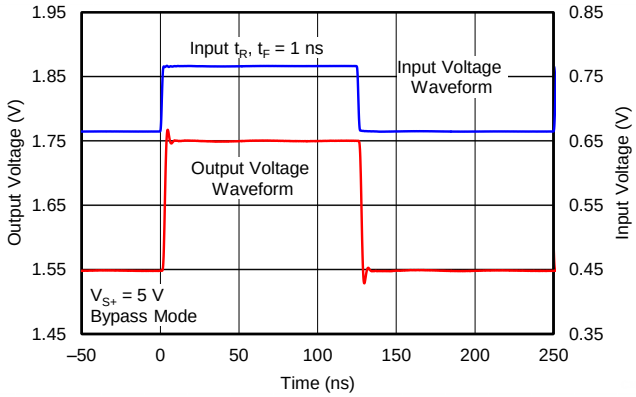

Figure 105. HD BYPASS SMALL-SIGNAL PULSE RESPONSE vs TIME

TYPICAL CHARACTERISTICS: 5-V High-Definition (HD) Bypass Channels (continued)

At load = 150 Ω || 5 pF and dc-coupled input and output, unless otherwise noted.

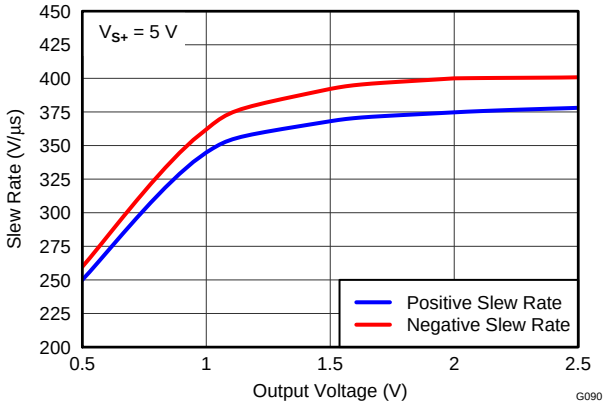

Figure 106. HD BYPASS SLEW RATE vs OUTPUT VOLTAGE

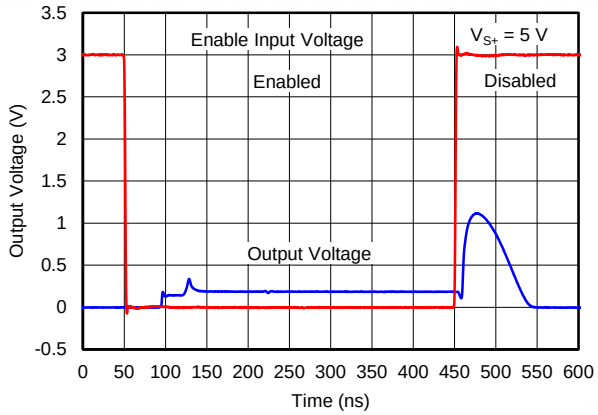

Figure 107. HD ENABLE AND DISABLE RESPONSE vs TIME

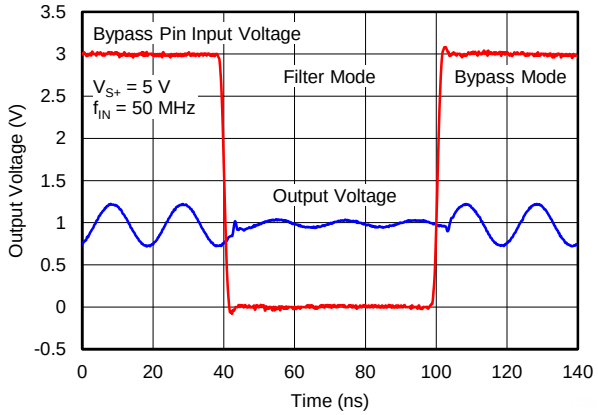

Figure 108. HD FILTER AND BYPASS RESPONSE vs TIME

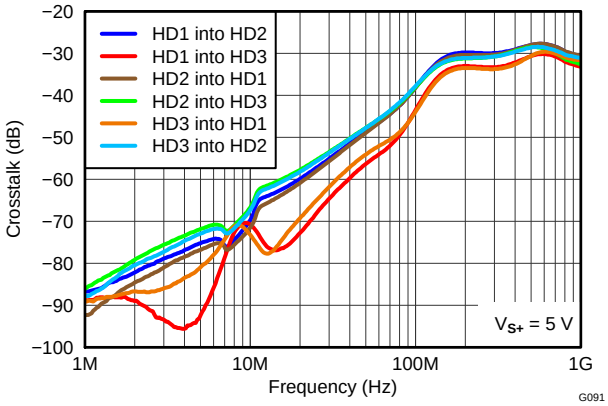

Figure 109. HD BYPASS TO HD BYPASS CROSSTALK vs FREQUENCY

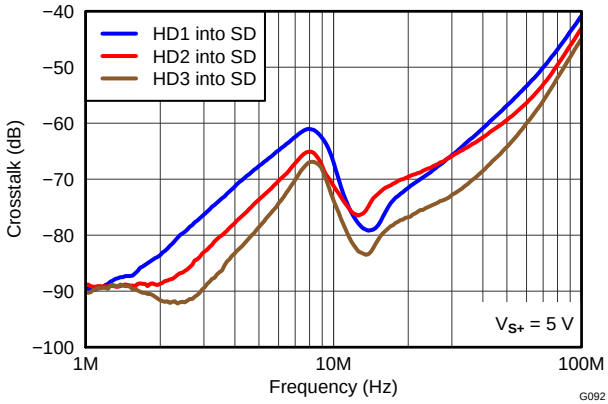

Figure 110. HD BYPASS TO SD CROSSTALK vs FREQUENCY

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TYPICAL CHARACTERISTICS: General Standard-Definition (SD) Channel

At load = 150 Ω || 5 pF and dc-coupled input and output, unless otherwise noted.

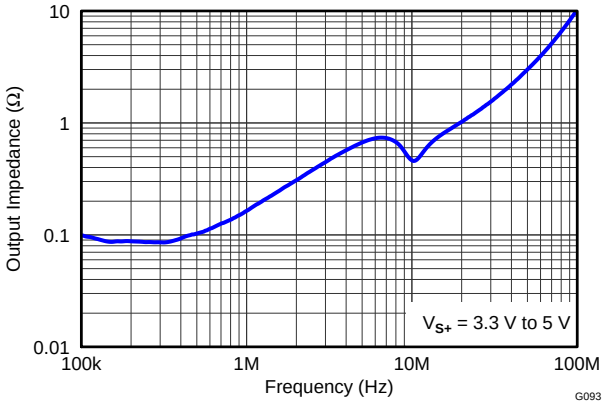

Figure 111. SD OUTPUT IMPEDANCE vs FREQUENCY

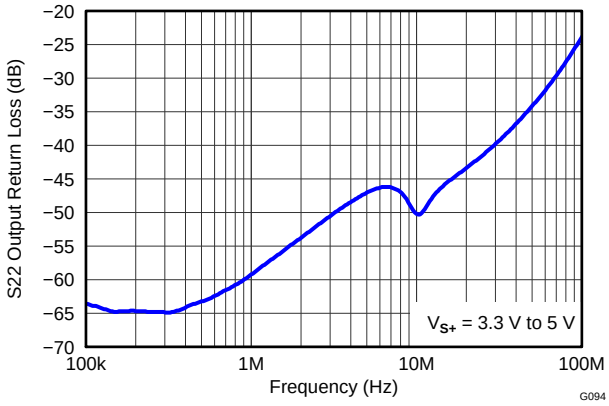

Figure 112. SD S22 OUTPUT RETURN LOSS vs FREQUENCY

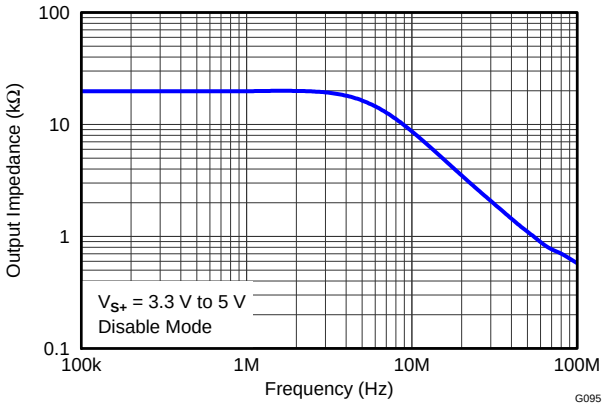

Figure 113. SD DISABLED OUTPUT IMPEDANCE vs FREQUENCY

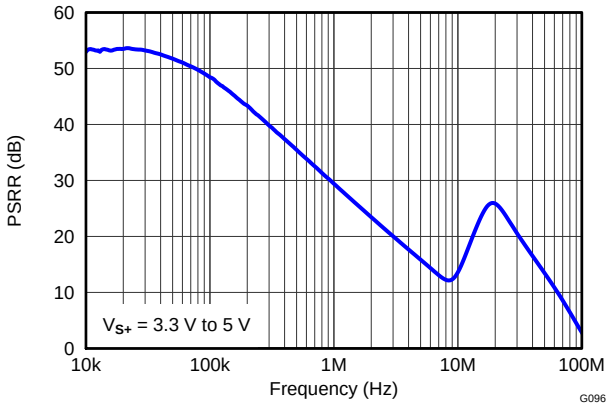

Figure 114. SD PSRR vs FREQUENCY

TYPICAL CHARACTERISTICS: General High-Definition (HD) Channels

At load = 150 Ω || 5 pF and dc-coupled input and output, unless otherwise noted.

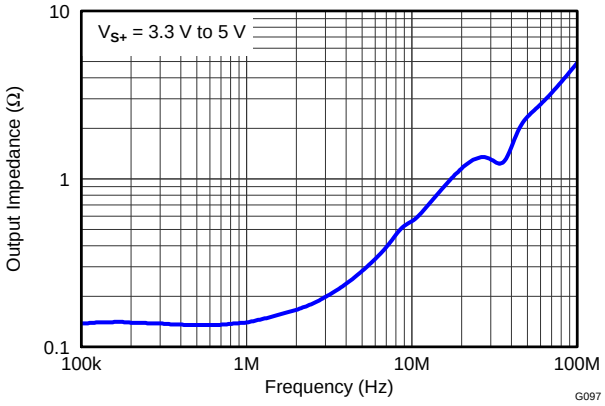

Figure 115. HD OUTPUT IMPEDANCE vs FREQUENCY

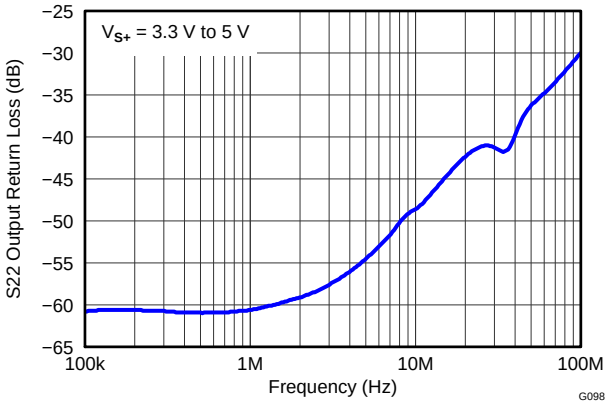

Figure 116. HD S22 OUTPUT RETURN LOSS vs FREQUENCY

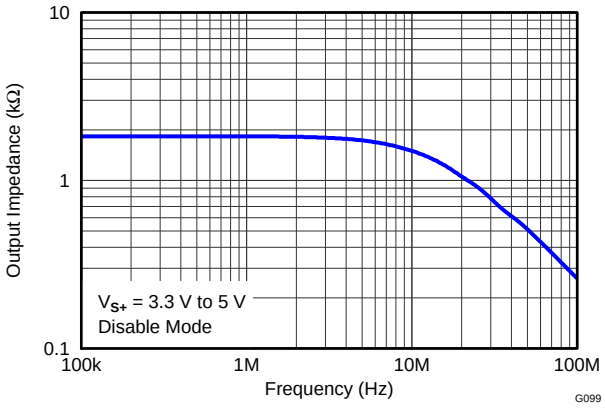

Figure 117. HD DISABLED OUTPUT IMPEDANCE vs FREQUENCY

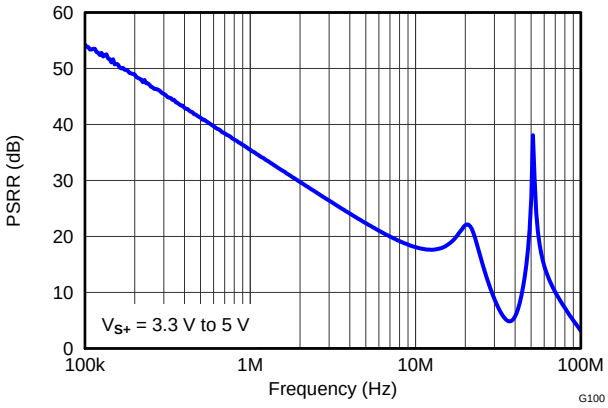

Figure 118. HD PSRR vs FREQUENCY

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TYPICAL CHARACTERISTICS: General High-Definition (HD) Bypass Channels

At load = 150 Ω || 5 pF and dc-coupled input and output, unless otherwise noted.

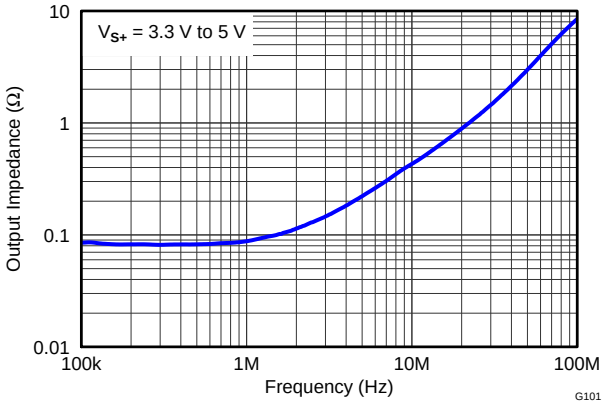

Figure 119. HD BYPASS OUTPUT IMPEDANCE vs FREQUENCY

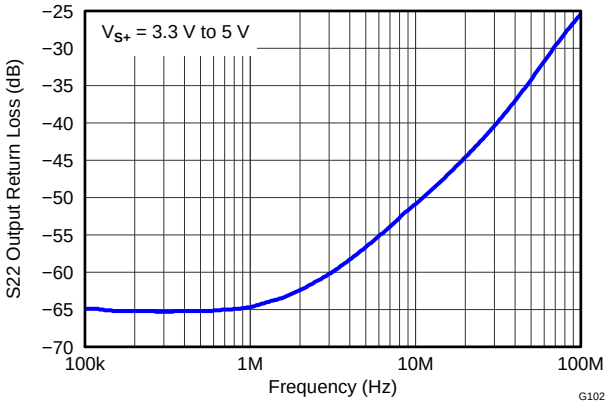

Figure 120. HD BYPASS S22 OUTPUT RETURN LOSS vs FREQUENCY

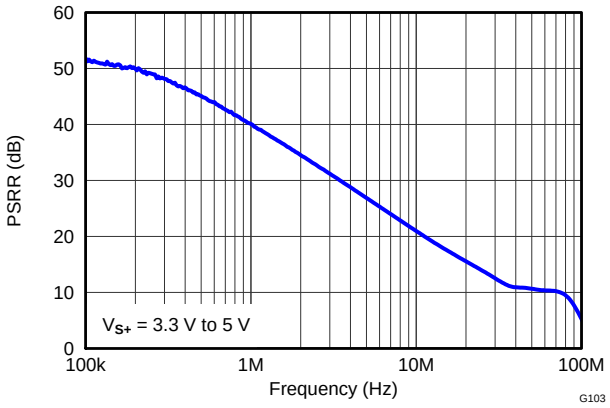

Figure 121. HD BYPASS PSRR vs FREQUENCY

APPLICATION INFORMATION

The THS7376 is targeted for applications that require one standard-definition (SD) video output buffer for CVBS video support along with three full high definition (HD) video output buffers. Although the video signal can be used for numerous other applications, the needs and requirements of the video signal are the most important design parameters of the THS7376. Built on the revolutionary, complementary Silicon Germanium (SiGe) BiCom3X process, the THS7376 incorporates many features not typically found in integrated video devices while consuming very low power. The THS7376 includes the following features:

- 3-V to 5-V, single-supply operation with a low total quiescent current of 30.9 mA at 3.3 V and 32.6 mA at 5 V.
- Disable mode enables shutting down the device to save system power in power-sensitive applications. This mode reduces quiescent current to as low as 0.1 µA.
- Flexible input configurations accept dc + level shift, ac sync-tip clamp, or ac-bias. AC-biasing is configured by using external pull-up resistors to the positive power supply.
- A low-pass filter for DAC reconstruction or ADC image rejection provides:
  - A 6th-order, 10-MHz filter for NTSC, PAL, SECAM, and composite video (CVBS) baseband signals, and
  - Three 8th-order, 42-MHz filters for 720p, 1080i, or up to 1080p30 Y', P'_B, P'_R, or G'B'R' signals. These filters also support 480i and 576i or 480p and 576p component video signals.
- HD bypass mode bypasses the HD low-pass filters for all three channels. The HD channels can support a 1080p60 full-HD component video or SXGA RGB video with 300-MHz and 375-V/µs performance.
  –
- Internally-fixed gain of 2-V/V (+6-dB).
- Supports driving two video lines per channel with dc-coupling or traditional ac-coupling.
- Robust 10-kV ESD protection on video output pins and 8-kV ESD protection on all other pins
- Flow-through configuration using a TSSOP-14 package that complies with the latest lead-free (RoHS-compatible) and green manufacturing requirements.
- The THS7373 and THS7374 from TI are drop-in compatible devices.

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TEST CIRCUITS

Figure 122 shows the default test condition for the THS7376. R_{LOAD} is nominally 150 Ω and C_{LOAD} is nominally 5 pF to account for traditional printed circuit board (PCB) layout parasitics. The input typically comes from either a video generator (such as a TEK TG700) or other sources (such as a network analyzer, pulse generator, or a sine-wave generator). Inputs originating from a video generator require a 75-Ω input termination and a dc offset. Inputs from other sources require a 50-Ω termination and a dc offset (approximately 0.6 VDC). Figure 122 is the preferred configuration for most testing.

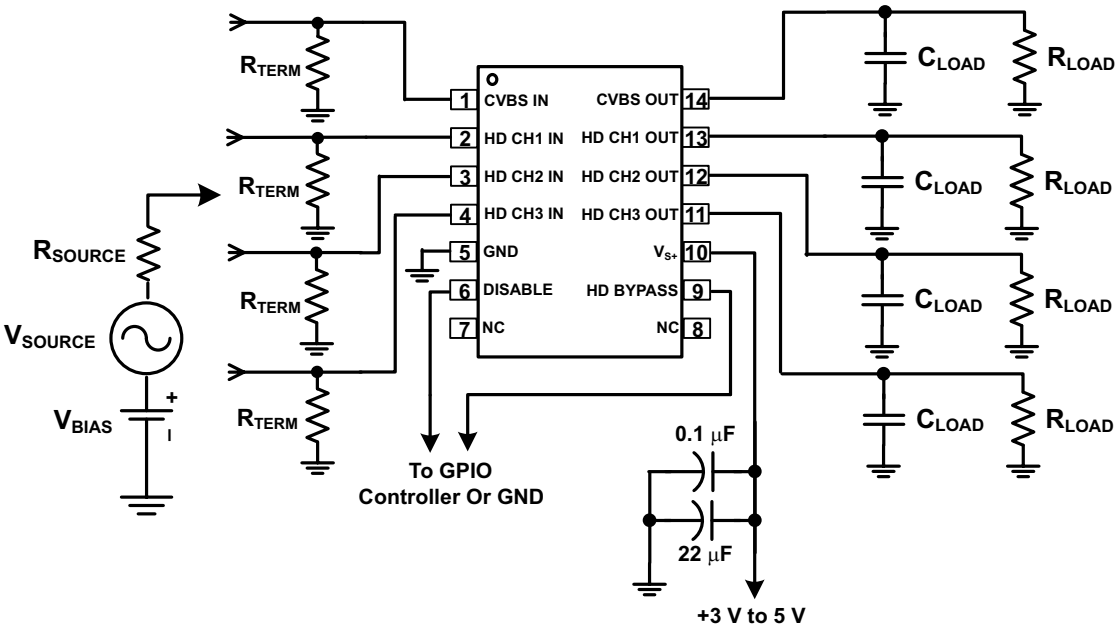

Figure 122. Default Test Configuration

Figure 123 shows the typical system configuration where long PCB traces between the system-on-a-chip (SOC) DAC output and the THS7376 are common. On the output, long PCB traces and small capacitors placed near the connector are common components, and are normally used for electromagnetic interference (EMI) considerations. These capacitors combine with the device filter response and can help attenuate very high frequencies. This circuit is useful in understanding the high-frequency roll-off effects resulting from actual system parasitics typically found in end applications.

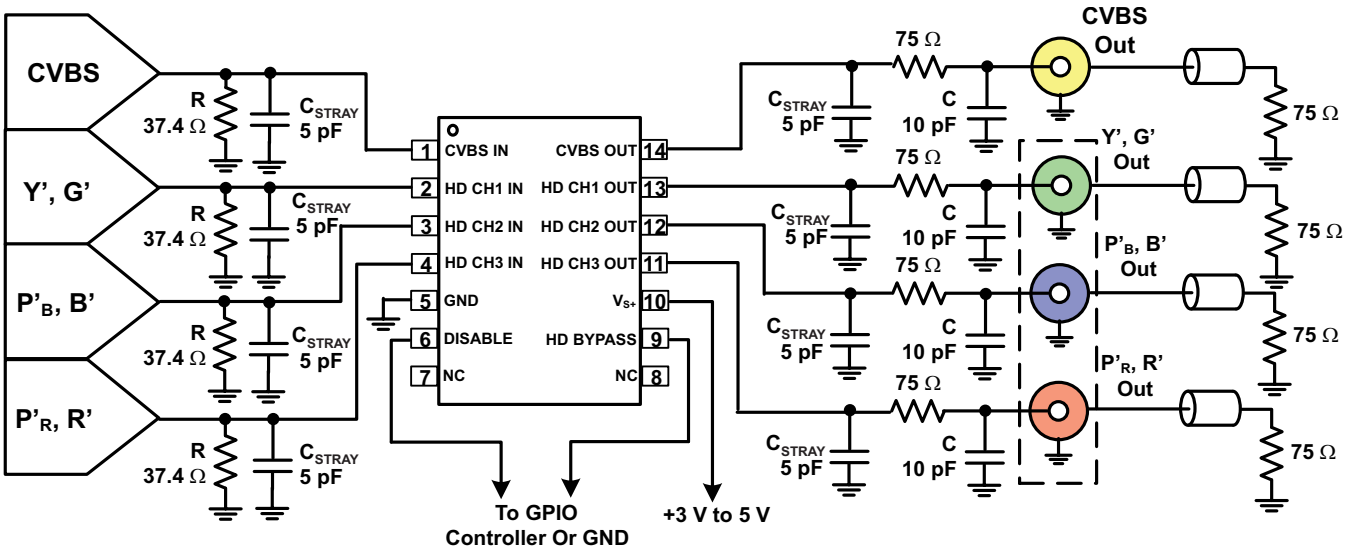

Figure 123. Typical System Configuration

For ac-coupled input testing, use the circuit shown in Figure 124. This circuit allows virtually any signal to be applied to the THS7376 while still biased properly on the input and output.

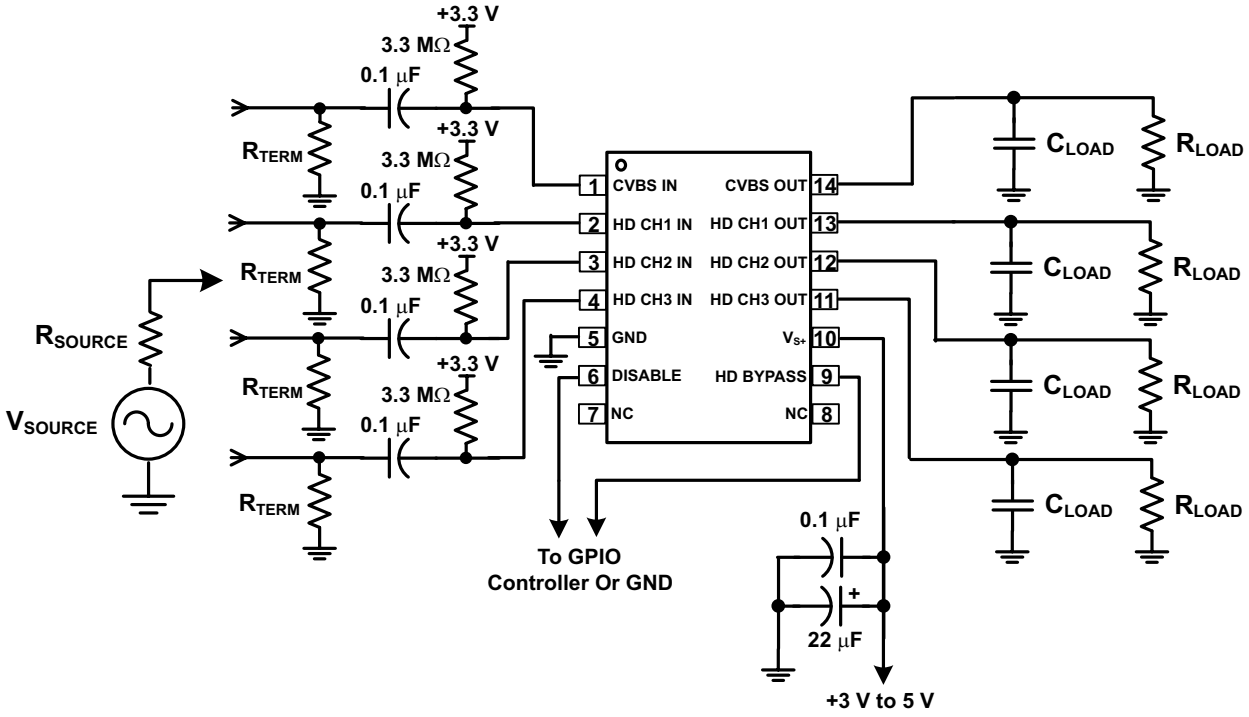

Figure 124. AC Input Test Configuration

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Sometimes the input must be ac-coupled to the THS7376 with current-sinking video DACs. The configuration shown in Figure 125 allows for these DACs to interface properly with the device. The CVBS channel and the component Y channel have bottom-level syncs that function perfectly with the device built-in sync-tip clamps. The component P'_B and P'_R channel syncs are not the lowest voltage because the active video is allowed to be below the sync voltage. Under some video frames and signals, this voltage can cause issues when trying to use the sync-tip clamp function. The bias coupling mode shown in Figure 125 is preferable for these signals. Note that the RGB signals can be coupled using the sync-tip clamp function without issue, even if sync is not present.

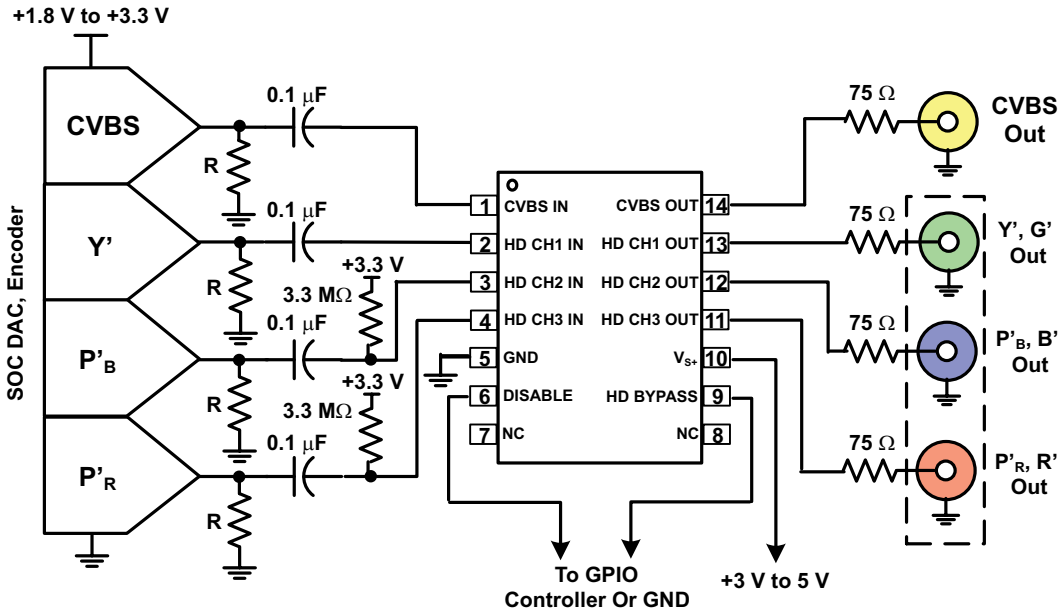

Figure 125. Typical CVBS, Y, P'_B, P'_R AC Input Coupled System Configuration for a DAC Input

Figure 126 shows a similar configuration to Figure 125, except that the inputs come from an external source. The same information for Figure 125 applies to Figure 126 as well.

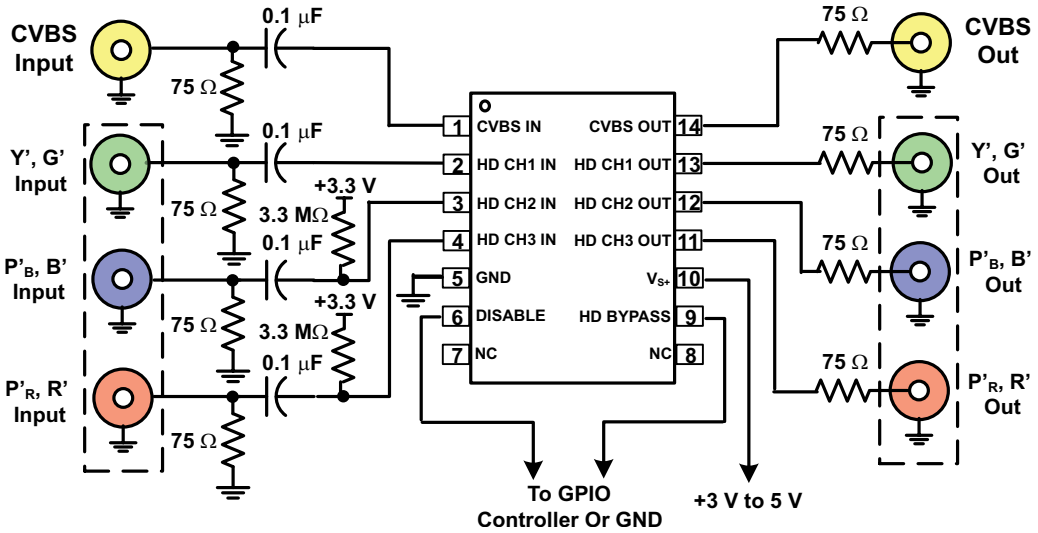

Figure 126. Typical CVBS, Y, P_B, P_R AC Input Coupled System Configuration for External Source Inputs

Figure 127 shows the THS7376 driving two dc-coupled video loads on each output with dc-coupled inputs. Parasitic capacitances are not shown for simplification purposes. Note that ac-coupling on the inputs is also fully applicable if desired.

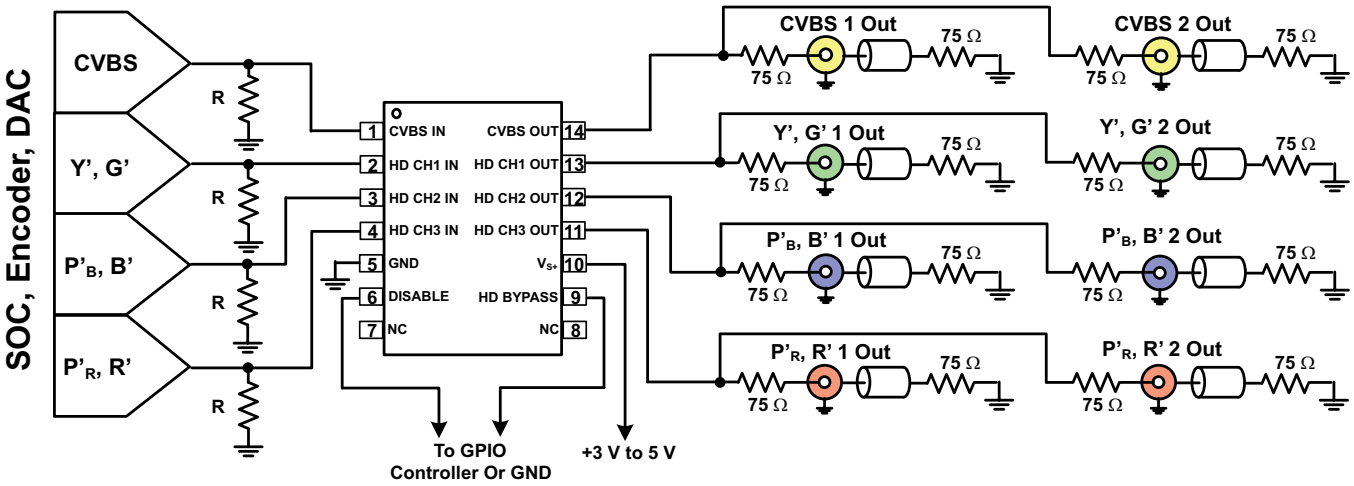

Figure 127. Typical DC-Coupled Input System Configuration Driving Two DC-Coupled Loads per Channel

Figure 128 shows the THS7376 driving two ac-coupled video loads on each output with dc-coupled inputs. Parasitic capacitances are not shown for simplification purposes. Note that ac-coupling on the inputs is also fully applicable if desired. Also note that the large coupling capacitors should be placed after the 75-Ω resistor and not before them. This configuration isolates the parasitic capacitance of the capacitors from appearing on the device output, thus creating a very stable system.

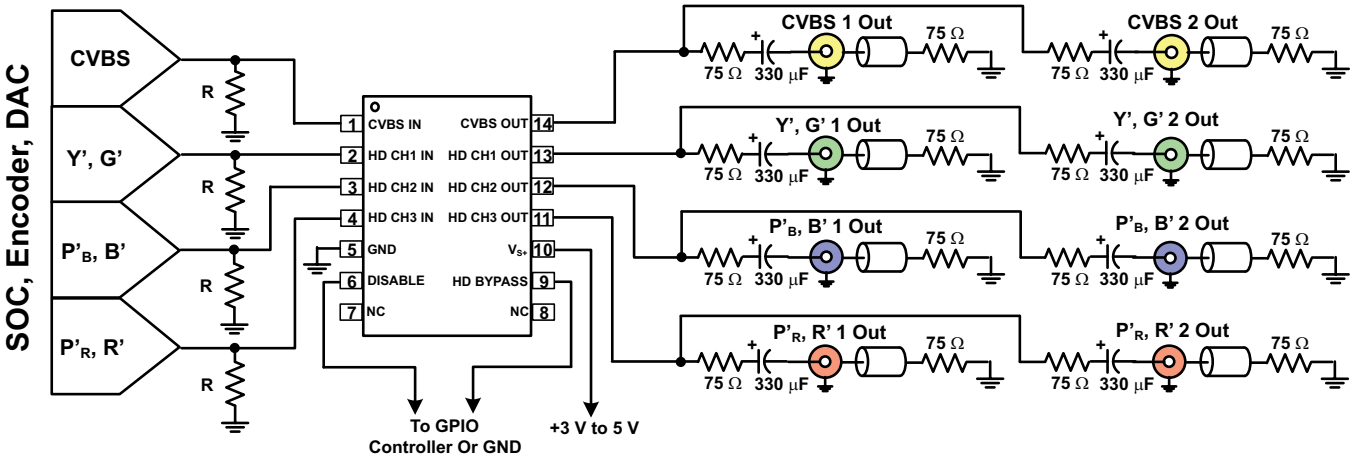

Figure 128. Typical DC-Coupled Input System Configuration Driving Two AC-Coupled Loads per Channel

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OPERATING VOLTAGE

The THS7376 is designed to operate from 3 V to 5 V over the –40°C to +85°C temperature range. The impact on performance over the entire temperature range is negligible as a result of the implementation of thin film resistors and high-quality, low-temperature coefficient capacitors. The design of the THS7376 allows operation down to 2.85 V, but TI recommends using at least a 3-V supply to ensure that no issues arise with headroom or clipping with 100% color-saturated CVBS signals. If only 75% color-saturated CVBS is supported, then the output voltage requirements are reduced to 2 V_{PP} on the output, allowing a 2.85-V supply to be used without issue.

A 0.1-µF to 0.01-µF capacitor should be placed as close as possible to the power-supply pins. Failure to do so may result in the THS7376 outputs ringing or oscillating. Additionally, a large capacitor (such as 22 µF to 100 µF) should be placed on the power-supply line to minimize interference with 50- and 60-Hz line frequencies.

INPUT VOLTAGE

The device input range allows for an input signal range from –0.05 V to approximately (V_{S+} – 1.5 V). However, because of the internal fixed gain of 2 V/V (+6 dB) and the internal input level shift of 105 mV (typical), the output is generally the limiting factor for the allowable linear input range. For example, with a 5-V supply, the linear input range is from –0.05 V to 3.5 V. However, because of the gain and level shift, the linear output range limits the allowable linear input range to approximately –0.05 V to 2.3 V.

INPUT OVERVOLTAGE PROTECTION

The device is built using a very high-speed, complementary, BiCMOS process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All input and output device pins are protected with internal ESD protection diodes to the power supplies, as shown in Figure 129.

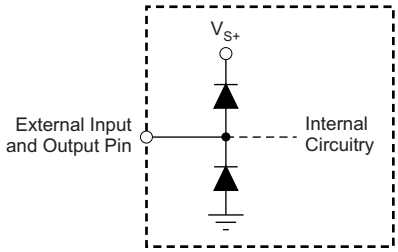

Figure 129. Internal ESD Protection

These diodes provide moderate protection to input overdrive voltages above and below the supplies as well. The protection diodes can typically support 30 mA of continuous current when overdriven.

TYPICAL CONFIGURATION AND VIDEO TERMINOLOGY

A typical application circuit using the THS7376 as a video buffer is shown in Figure 130. Figure 130 shows a DAC or encoder driving the device input channels. The SD channel (CVBS IN pin) can be used for NTSC, PAL, or SECAM signals. The other three channels are the component video Y', P'_B, P'_R (sometimes labeled Y'U'V' or incorrectly labeled Y', C'_B, C'_R) signals. These signals are typically 480i, 576i, 480p, 576p, 720p, 1080i, 1080p24, 1080p30, or up to 1080p60 signals.

Note that the *Y'* term is used for the luma channels throughout this document rather than the more common luminance (*Y*) term. This usage accounts for the definition of luminance as stipulated by the International Commission on Illumination (CIE). Video departs from true luminance because a nonlinear term, *gamma*, is added to the true RGB signals to form R'G'B' signals. These R'G'B' signals are then used to mathematically create luma (Y'). Thus, luminance (Y) is not maintained, providing a difference in terminology.

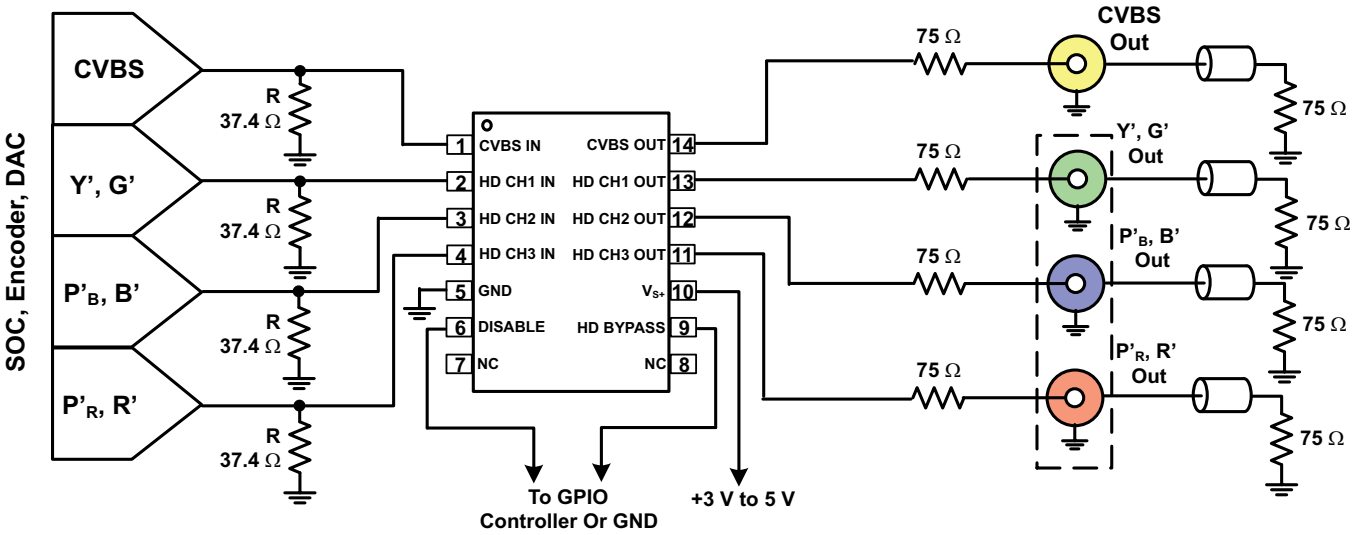

Figure 130. Typical Four-Channel System Inputs from a DC-Coupled Encoder and DAC with DC-Coupled Line Driving

R'G'B' (commonly mislabeled *RGB*) is also called G'B'R' (again commonly mislabeled as *GBR*) in professional video systems. The Society of Motion Picture and Television Engineers (SMPTE) component standard stipulates that the luma information is placed on the first channel, the blue color difference is placed on the second channel, and the red color difference signal is placed on the third channel. This practice is consistent with the Y', P'_B, P'_R nomenclature. Placing the green channel (G') first in the system makes logical sense because the luma channel (Y') carries the sync information and the green channel (G') also carries sync information. Likewise, because the blue color difference channel (P'_B) is next and the red color difference channel (P'_R) is last, placing the B' signal on the second channel and the R' signal on the third channel (respectfully) also makes logical sense. Thus, hardware compatibility is better achieved when using G'B'R' rather than R'G'B'. Note that for many G'B'R' systems, sync is embedded on all three channels, but this configuration may not always be the case in all systems.

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INPUT MODE OF OPERATION: DC

The device inputs allow for both ac- and dc-coupled inputs. Many DACs or video encoders can be dc-connected to the THS7376. One of the drawbacks to dc-coupling arises when 0 V is applied to the input. Although the device input allows for a 0-V input signal without issue, the output swing of a traditional amplifier cannot yield a 0-V signal, resulting in possible clipping. This limitation is true for any single-supply amplifier because of the characteristics of the output transistors. Neither CMOS nor bipolar transistors can achieve 0 V while sinking current. This transistor characteristic is also the same reason why the highest output voltage is always less than the power-supply voltage when sourcing current.

This output clipping can reduce sync amplitudes (both horizontal and vertical sync) on the video signal. A problem occurs if the video signal receiver uses an automatic gain control (AGC) loop to account for losses in the transmission line. Some video AGC circuits derive gain from horizontal sync amplitude. If clipping occurs on the sync amplitude, then the AGC circuit can increase the gain too much—resulting in too much luma and chroma amplitude gain correction. This correction may result in a picture with an overly bright display with too much color saturation.

Other AGC circuits use the chroma burst amplitude for amplitude control; reduction in the sync signals does not alter the proper gain setting. However, good engineering design practice is to ensure that neither saturation nor clipping takes place. Transistors always take a finite amount of time to come out of saturation. This saturation could possibly result in timing delays or other aberrations on the signals.

To eliminate saturation or clipping problems, the THS7376 has a 105-mV input level shift feature. This feature takes the input voltage and adds an internal +105-mV shift to the signal. Because the device also has a gain of 6 dB (2 V/V), the resulting output with a 0-V applied input signal is approximately 210 mV. The THS7376 rail-to-rail output stage can create this output level while connected to a typical video load. This configuration ensures that no saturation or clipping of the sync signals occur. This shift is constant, regardless of the input signal. For example, if a 1-V input is applied, the output is 2.21 V.

Because the internal gain is fixed at +6 dB, the gain dictates what the allowable linear input voltage range can be without clipping concerns. For example, if the power supply is set to 3 V, the maximum output is approximately 2.9 V while driving a significant amount of current. Thus, to avoid clipping, the allowable input is ([2.9 V / 2] – 0.105 V) = 1.345 V. This range is valid up to the maximum recommended 5-V power supply that allows approximately a ([4.9 V / 2] – 0.105 V) = 2.345 V input range while avoiding clipping on the output.

The device input impedance in this mode of operation is dictated by the internal, 800-kΩ pull-down resistor, as shown in Figure 131. Note that the internal voltage shift only appears at the output pin, not at the input pin.

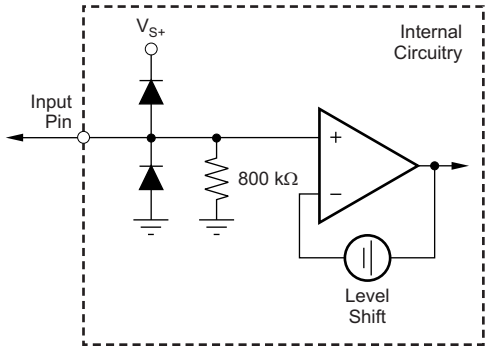

Figure 131. Equivalent DC Input Mode Circuit

INPUT MODE OF OPERATION: AC SYNC TIP CLAMP

Some video DACs or encoders are not referenced to ground but rather to the positive power supply. The resulting video signals are generally at too great a voltage for a dc-coupled video buffer to function properly. To account for this scenario, the device incorporates a sync-tip clamp (STC) circuit. This function requires a capacitor (nominally 0.1 µF) to be in series with the input. Although the term *sync-tip-clamp* is used throughout this document, note that the device is probably better termed as a *dc restoration circuit* based on how this function is performed. This circuit is an active clamp circuit and not a passive diode clamp function.

The input to the THS7376 has an internal control loop that sets the lowest input applied voltage to clamp at ground (0 V). By setting the reference at 0 V, the device allows a dc-coupled input to also function. Therefore, the STC is considered transparent because it does not operate unless the input signal goes below ground. The signal then goes through the same 105-mV level shifter, resulting in an output voltage low level of 210 mV. If the input signal tries to go below 0 V, the THS7376 internal control loop sources up to 6 mA of current to increase the input voltage level on the device input side of the coupling capacitor. As soon as the voltage goes above the 0-V level, the loop stops sourcing current and becomes very high impedance.

One of the concerns about the sync-tip-clamp level is how the clamp reacts to a sync edge that has overshoot—common in VCR signals, noise, DAC overshoot, or reflections found in poor printed circuit board (PCB) layouts. Ideally, the STC should not react to the overshoot voltage of the input signal. Otherwise, this response could result in clipping on the rest of the video signal because the response may raise the bias voltage too much.

To help minimize this input signal overshoot problem, the control loop in the THS7376 has an internal low-pass filter (LPF), as shown in Figure 132. This filter reduces the response time of the STC circuit. This delay is a function of how far the voltage is below ground, but in general there is approximately a 400-ns delay for the SD channel filters and approximately a 150-ns delay for the HD filters. The effect of this filter is to slow down the response of the control loop so as not to clamp on the input overshoot voltage but rather on the flat portion of the sync signal.

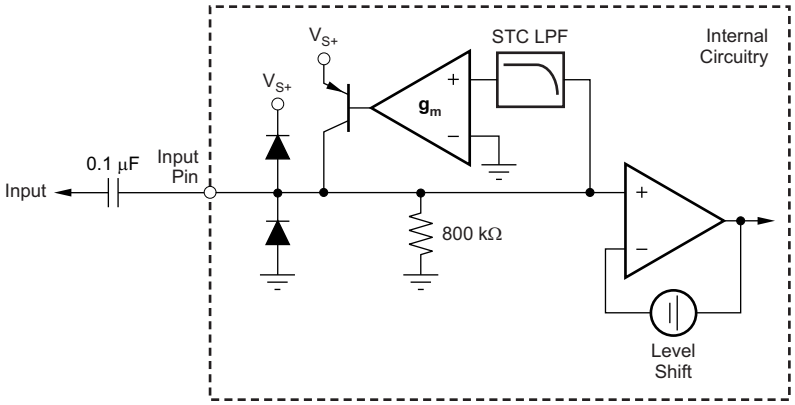

Figure 132. Equivalent AC Sync-Tip-Clamp Input Circuit

As a result of this delay, the sync signal may have an apparent voltage shift. The amount of shift depends on the amount of droop in the signal as dictated by the input capacitor and the STC current flow. Because sync is used primarily for timing purposes with syncing occurring on the edge of the sync signal, this shift is transparent in most systems.

While this feature may not fully eliminate overshoot issues on the input signal, in cases of extreme overshoot or ringing, the STC system should help minimize improper clamping levels. As an additional method to help minimize this issue, an external capacitor (for example, 10 pF to 47 pF) to ground in parallel with the external termination resistors can help filter overshoot problems.

Note that this STC system is dynamic and does not rely upon timing in any way. The system only depends on the voltage that appears at the input pin at any given point in time. STC filtering helps minimize level shift problems associated with switching noises or very short spikes on the signal line. This architecture helps ensure a very robust STC system.

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When the ac STC operation is used, there must also be some finite amount of discharge bias current. As previously described, if the input signal goes below the 0-V clamp level, the internal loop of the THS7376 sources current to increase the voltage appearing at the input pin. As the difference between the signal level and the 0-V reference level increases, the amount of source current increases proportionally, thus supplying up to 6 mA of current. Therefore, the time to re-establish the proper STC voltage can be very fast. If the difference is very small, then the source current is also very small to account for minor voltage droop.

However, what happens if the input signal goes above the 0-V input level? The problem is that the video signal is always above this level and must not be altered in any way. Thus, if the sync level of the input signal is above this 0-V level, then the internal discharge (sink) current reduces the ac-coupled bias signal to the proper 0-V level.

This discharge current must not be large enough to alter the video signal appreciably or picture quality issues may arise. This effect is often seen by comparing the tilt (droop) of a constant luma signal being applied and the resulting output level. The associated change in luma level from the beginning and end of the video line is the amount of line tilt (droop).

If the discharge current is very small, the amount of tilt is very low, which is a generally a good thing. However, the amount of time for the system to capture the sync signal could be too long. This effect is also termed *hum rejection*. Hum arises from the ac line voltage frequency of 50 Hz or 60 Hz. The value of the discharge current and the ac-coupling capacitor combine to dictate the hum rejection and the amount of line tilt.

To allow for both dc- and ac-coupling in the same device, the THS7376 incorporates an 800-kΩ resistor to ground. Although a true constant-current sink is preferred over a resistor, there can be issues when the voltage is near ground. This configuration can cause the current sink transistor to saturate and cause potential problems with the signal. The 800-kΩ resistor is large enough to not impact a dc-coupled DAC termination. For discharging an ac-coupled source, Ohm's Law is used. If the video signal is 1 V, then there is (1 V / 800 kΩ = 1.25-μA) of discharge current. If more hum rejection is desired or there is a loss of sync occurring, then simply decrease the 0.1-μF input coupling capacitor. A decrease from 0.1 μF to 0.047 μF increases the hum rejection by a factor of 2.1. Alternatively, an external pull-down resistor to ground may be added that decreases the overall resistance and ultimately increases the discharge current.

To ensure proper stability of the ac STC control loop, the source impedance must be less than 1 kΩ with the input capacitor in place. Otherwise, there is a possibility of the control loop ringing, which may appear on the device output. Because most DACs or encoders use resistors (typically less than 300 Ω) to establish the voltage, meeting the less than 1-kΩ requirement is easily done. However, if the source impedance is very high, then simply adding a 1-kΩ resistor to GND ensures proper device operation.

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INPUT MODE OF OPERATION: AC BIAS

Sync-tip clamps work very well for signals that have horizontal or vertical syncs associated with them; however, some video signals do not have a sync embedded within the signal. If ac-coupling of these signals is desired, then using a dc bias is desired to properly set the dc operating point within the device. This function is easily accomplished with the THS7376 by simply adding an external pull-up resistor to the positive power supply, as shown in Figure 133.

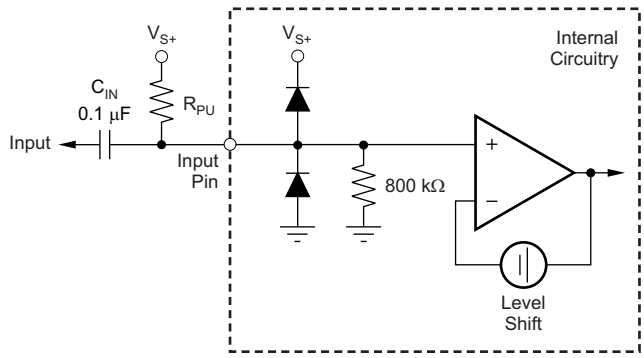

Figure 133. AC-Bias Input Mode Circuit Configuration

The dc voltage appearing at the input pin is equal to Equation 1:

$$V_{DC} = V_S \left(\frac{800\ k\Omega}{800\ k\Omega + R_{PU}} \right) \tag{1}$$

The device allowable input range is approximately 0 V to (V_{S+} – 1.5 V), allowing for a very wide input voltage range. As such, the input dc bias point is very flexible, with the output dc bias point being the primary factor. For example, if the output dc bias point is desired to be 1.6 V on a 3.3-V supply, then the input dc bias point should be (1.6 V – 210 mV) / 2 = 0.695 V. Thus, the pull-up resistor calculates to approximately 3 MΩ, resulting in 0.694 V. If the output dc-bias point is desired to be 1.6 V with a 5-V power supply, then the pull-up resistor calculates to approximately 4.99 MΩ.

Keep in mind that the internal 800-kΩ resistor has approximately a ±20% variance. As such, the calculations should take this variance into account. For the 0.644-V example above, using an ideal 3.3-MΩ resistor, the input dc bias voltage is approximately 0.694 V ±0.1 V.

The value of the output bias voltage is very flexible and is left to each individual design. The signal must not clip or saturate the video signal. Thus, TI recommends ensuring the output bias voltage is between 0.9 V and (V_{S+} – 1 V). For 100% color-saturated CVBS or signals with Macrovision®, the CVBS signal can reach up to 1.23 V_{PP} at the input, or 2.46 V_{PP} at the device output. In contrast, other signals are typically 1 V_{PP} or 0.7 V_{PP} at the input (which translates to an output voltage of 2 V_{PP} or 1.4 V_{PP}). The output bias voltage must account for a worst-case situation, depending on the signals involved.

One other issue that must be taken into account is that the dc-bias point is a function of the power supply. As such, there is an impact on system PSRR. To help reduce this impact, the input capacitor combines with the pull-up resistance to function as a low-pass filter. Additionally, the time to charge the capacitor to the final dc bias point is a function of the pull-up resistor and the input capacitor size. Lastly, the input capacitor forms a high-pass filter with the parallel impedance of the pull-up resistor and the 800-kΩ resistor. In general, keep this high-pass filter at approximately 3 Hz to minimize any potential droop on a P'_B or P'_R signal. A 0.1-µF input capacitor with a 3-MΩ pull-up resistor equates to approximately a 2.5-Hz high-pass corner frequency.

This mode of operation is recommended for use with chroma (C'), P'_B, P'_R, U', and V' signals. This method can also be used with sync signals if desired. The benefit of using the STC function over the ac-bias configuration on embedded sync signals is that the STC maintains a constant *back-porch* voltage as opposed to a back-porch voltage that fluctuates depending on the video content. Because the high-pass corner frequency is a very low 2.5 Hz, the impact on the video signal is negligible relative to the STC configuration.

One question may arise over the P'_B and P'_R channels. For 480i, 576i, 480p, and 576p signals, a sync may or may not be present. If no sync exists within the signal, then ac-bias is the preferred method to ac-couple the signal.

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For 720p, 1080i, and 1080p signals, or for the 480i, 576i, 480p, and 576p signals with sync present on the P'_B and P'_R channels, the lowest voltage of the sync is –300 mV below the midpoint reference voltage of 0 V. The P'_B and P'_R signals allow a signal to be as low as –350 mV below the midpoint reference voltage of 0 V. This allowance corresponds to 100% yellow for the P'_B signal or 100% cyan for the P'_R signal . Because the P'_B and P'_R signal voltage can be lower than the sync voltage, there is a potential for clipping the signal over a short period of time if the signals drop below the sync voltage.

The THS7376 includes a 105-mV input level shift, or 210 mV at the output, that should mitigate any clipping issues. For example, if an STC is used, then the bottom of the sync is 210 mV at the output. If the signal does go the lowest level, or 50 mV lower than the sync at the input, then the instantaneous output is [(–50 mV + 105 mV) × 2 = 110 mV] at the output.

Another potential risk is that if this signal (100% yellow for P'_B or 100% cyan for P'_R) exists for several pixels, then the STC circuit engages to raise the voltage back to 0 V at the input. This function can cause a 50-mV level shift at the input midway through the active video signal. This effect is undesirable and can cause errors in the decoding of the signal. Therefore, TI recommends using ac-bias mode for component P'_B and P'_R signals when ac-coupling is desired.

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OUTPUT MODE OF OPERATION: DC-COUPLED

The device incorporates a rail-to-rail output stage that can be used to drive the line directly without the need for large ac-coupling capacitors. This design offers the best line tilt and field tilt (droop) performance because no ac-coupling occurs. Keep in mind that if the input is ac-coupled, then the resulting tilt as a result of the input ac-coupling continues to be seen on the output, regardless of the output coupling. The 100-mA output current drive capability of the device is designed to drive two video lines simultaneously (essentially a 75-Ω load) while keeping the output dynamic range as wide as possible. Figure 134 shows the device driving two video lines while keeping the output dc-coupled.

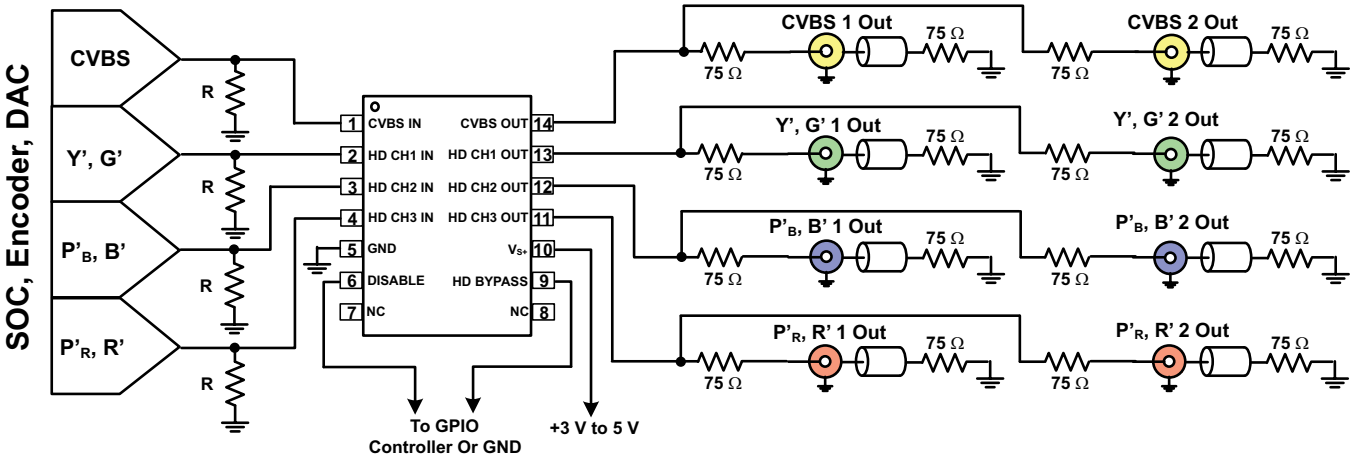

Figure 134. Typical Four-Channel System with DC-Coupled Line Driving and Two Outputs Per Channel

One concern of dc-coupling, however, arises if the line is terminated to ground. If the ac-bias input configuration is used, the device output has a dc bias on the output, such as 1.6 V. With two lines terminated to ground, this configuration allows a dc current path to flow, such as 1.6 V / 75-Ω = 21.3 mA. The result of this configuration is a slightly decreased high output voltage swing and an increase in device power dissipation. Although the device was designed to operate with a junction temperature of up to +125°C, care must be taken to ensure that the junction temperature does not exceed this level or else long-term reliability could suffer. Using a 5-V supply, this configuration can result in an additional dc power dissipation of (5 V – 1.6 V) × 21.3 mA = 72.5 mW per channel. With a 3.3-V supply, this dissipation reduces to 36.2 mW per channel. The overall low quiescent current of the device design minimizes potential thermal issues even when using the TSSOP package at high ambient temperatures, but power and thermal analysis should always be examined in any system to ensure that no issues arise. Be sure to use RMS power and not instantaneous power when evaluating the thermal performance.

Note that the device can drive the line with dc-coupling regardless of the input mode of operation. The only requirement is to make sure the video line has proper termination in series with the output (typically 75 Ω). This requirement helps isolate capacitive loading effects from the device output. Failure to isolate capacitive loads may result in instabilities with the output buffer, potentially causing ringing or oscillations to appear. The stray capacitance appearing directly at the device output pins should be kept below 20 pF for the fixed SD filter channels and below 15 pF for the HD filter channels. One way to verify this condition is satisfied is to ensure the 75-Ω source resistor is placed within 0.5 inches, or 12.7 mm, of the device output pin. If a large ac-coupling capacitor is used, the capacitor should be placed after this resistor.

There are many reasons why dc-coupling is desirable, including reduced costs, printed circuit board (PCB) area, and no line tilt. A common question is whether or not there are any drawbacks to using dc-coupling. There are some potential issues that must be examined, such as the dc current bias as discussed above. Another potential risk is whether this configuration meets industry standards. EIA/CEA-770 stipulates that the back-porch shall be 0 V ± 1 V as measured at the receiver. With a double-terminated load system, this requirement implies a 0-V ± 2-V level at the video amplifier output. The THS7376 can easily meet this requirement without issue. However, in Japan, the EIAJ CP-1203 specification stipulates a 0-V ± 0.1-V level with no signal. This requirement can be met with the THS7376 in shutdown mode, but while active the device cannot meet this specification without output ac-coupling. AC-coupling the output essentially ensures that the video signal functions with any system and any specification. For many modern systems, however, dc-coupling can satisfy most needs.

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OUTPUT MODE OF OPERATION: AC-COUPLED

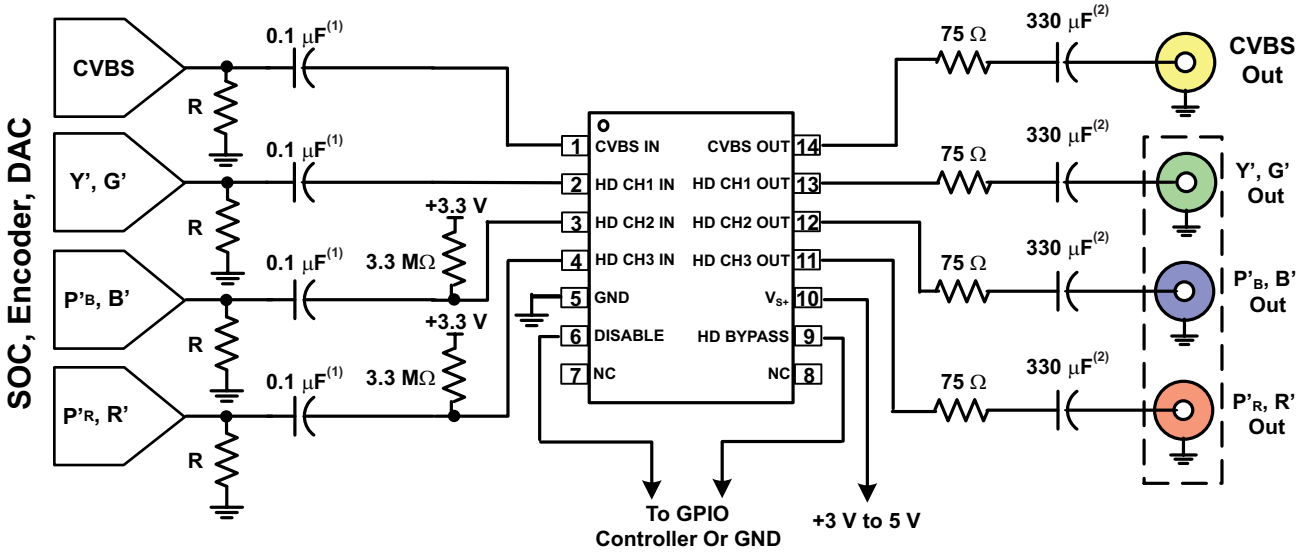
A very common method of coupling the video signal to the line is with a large capacitor. This capacitor is typically between 220 µF and 1000 µF, although 470 µF is very typical. The value of this capacitor must be large enough to minimize the line tilt (droop) and field tilt associated with ac-coupling as described previously. AC-coupling is performed for several reasons, but the most common reason is to ensure full interoperability with the receiving video system. This approach ensures that regardless of the reference dc voltage used on the transmitting side, the receiving side re-establishes the dc reference voltage to its own requirements.

In the same way as in the *DC-Coupled Output Mode of Operation* , each line should have a 75-Ω source termination resistor in series with the ac-coupling capacitor. This 75-Ω resistor should be placed next to the device output to minimize capacitive loading effects. If two lines are to be driven, having each line use its own capacitor and resistor rather than sharing these components is best. This configuration helps ensure line-to-line dc isolation and eliminates the potential problems as described previously. Using a single, 1000-µF capacitor for two lines is permissible, but there is a chance for interference between the two receivers.

Lastly, because of the edge rates and frequencies of operation, TI recommends (but does not require) placing a 0.1-µF to 0.01-µF capacitor in parallel with the large 220-µF to 1000-µF capacitor. These large value capacitors are most commonly aluminum electrolytic. These capacitors have significantly large equivalent series resistance (ESR), and the impedance at high frequencies is rather large as a result of the associated inductances involved with the leads and construction. The small 0.1-µF to 0.01-µF capacitors help pass these high-frequency signals (greater than 1 MHz) with much lower impedance than the large capacitors.

Although using the same capacitor values for all video lines is a common practice, the frequency bandwidth of the chroma signal in a S-Video system is not required to go as low (or as high of a frequency) as the luma channels. Thus, the capacitor values of the chroma line can be smaller, such as 0.1 µF.

Figure 135 shows a typical configuration where the input is ac-coupled and the output is also ac-coupled. AC-coupled inputs are generally required when current-sink DACs are used or the input is connected to an unknown source, such as when the device is used as an input device.



(1) An ac-coupled input is shown in this example. DC-coupling is also allowed as long as the DAC output voltage is within the allowable linear input and output voltage range of the device. To apply dc-coupling, remove the 0.1-µF input capacitors and the R_{PU} pull-up resistors.

(2) This example shows an ac-coupled output. DC-coupling is also allowed by simply removing these capacitors.

Figure 135. Typical AC Input System Driving AC-Coupled Video Lines

LOW-PASS FILTER (LPF)

Each channel of the THS7376 incorporates a sixth-order or eighth-order, low-pass filter. These video reconstruction filters minimize DAC images from being passed onto the video receiver. Depending on the receiver design, failure to eliminate these DAC images can cause picture quality problems because of aliasing of the ADC in the receiver. If the DAC sampling freqeuncy is different than the ADC sampling frequency, then the images will not fold properly back into the base-band and picture quality may suffer. Another benefit of the filter is to smooth out aberrations in the signal that some DACs can have if the internal filtering is not very good. This benefit helps with picture quality and ensures that the signal meets video bandwidth requirements.

Each filter has an associated Butterworth characteristic. The benefit of the Butterworth response is that the frequency response is flat with a relatively steep initial attenuation at the corner frequency. The problem with this characteristic is that the group delay rises near the corner frequency. Group delay is defined as the change in phase (radians per second) divided by a change in frequency. An increase in group delay corresponds to a time domain pulse response that has overshoot and some possible ringing associated with the overshoot.

The use of other type of filters, such as elliptic or chebyshev, are not recommended for video applications because of the very large group delay variations near the corner frequency resulting in significant overshoot and ringing. Although these filters may help meet the video standard specifications with respect to amplitude attenuation, the group delay is well beyond standard specifications. Considering this delay with the fact that video can go from a white pixel to a black pixel over and over again, ringing can easily occur. Ringing typically causes a display to have ghosting or fuzziness appear on the edges of a sharp transition. On the other hand, a Bessel filter has an ideal group delay response, but the rate of attenuation is typically too low for acceptable image rejection. Thus, the Butterworth filter is an acceptable compromise for both attenuation and group delay.

The THS7376 SD filter has a nominal corner (–3-dB) frequency at 10 MHz and a –1-dB passband typically at 9 MHz. This 10-MHz filter is ideal for SD NTSC, PAL, and SECAM composite video (CVBS) signals. The 10-MHz, –3-dB corner frequency is designed to achieve 46 dB of attenuation at 27 MHz—a common sampling frequency between the DAC and ADC second and third Nyquist zones found in many video systems. This consideration is important because any signal that appears around this frequency can also appear in the baseband as a result of aliasing effects of an ADC found in a receiver.

The device HD filters have a nominal corner (–3-dB) frequency at 42 MHz and a –1-dB passband typically at 39 MHz. This 42-MHz filter is ideal for 720p, 1080i, 1080p24, or 1080p30 component video. This filter is also ideal for oversampling systems where the video DAC upsamples the video signal (such as 480i or 480p upsampled to >74MHz). The benefit is an extremely flat passband response along with almost no group delay within the HD video passband.

Keep in mind that images do not stop at the DAC sampling frequency, f_S (for example, 27 MHz for traditional SD DACs); they continue around the sampling frequencies of 2x f_S, 3x f_S, 4x f_S, and so on (that is, 54 MHz, 81 MHz, 108 MHz, and so forth). An ADC will fold down these images into the baseband signal which meanis that the low-pass filter must eliminate these higher-order images. The device filters are Butterworth filters and, as such, do not *bounce* at higher frequencies, thus maintaining good attenuation performance.

The filter frequencies are chosen to account for process variations in the device. To ensure the required video frequencies are effectively passed, the filter corner frequency must be high enough to allow component variations. The other consideration is that the attenuation must be large enough to ensure the antialiasing and reconstruction filtering is sufficient to meet system demands. Thus, selection of the filter frequencies is not arbitrarily selected and is a good compromise that should meet the demands of most systems.

BENEFITS OVER PASSIVE FILTERING

Two key benefits of using an integrated filter system, such as the THS7376, over a passive system are PCB area and filter variations. The small TSSOP-14 package for four video channels is much smaller over a passive RLC network, especially a seventh-order passive network. Additionally, consider that inductors have ±5% up to ±20% tolerances and capacitors typically have ±5% up to ±10% tolerances. Using a Monte Carlo analysis shows that the filter corner frequency (–3 dB), flatness (–1 dB), Q factor (or peaking), and channel-to-channel delay have wide variations. These variances can lead to potential performance and quality issues in mass-production environments. The THS7376 solves most of these problems with the corner frequency being essentially the only variable.

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Another concern about passive filters is the use of inductors. Inductors are magnetic components, and are therefore susceptible to electromagnetic coupling and interference (EMC/EMI). Coupling can occur because of other video channels nearby using inductors for filtering, or coupling can come from nearby switched-mode power supplies. Some other forms of coupling could be from outside sources with strong EMI radiation and can cause failure in EMC testing such as required for CE compliance.

One concern about an active filter in an integrated circuit is the variation of the filter characteristics when the ambient temperature and the subsequent die temperature changes. To minimize temperature effects, the THS7376 uses low-temperature coefficient resistors and high-quality, low-temperature coefficient capacitors found in the BiCom3X process. These filters are specified by design to account for process variations and temperature variations to maintain proper filter characteristics. This approach maintains a low channel-to-channel time delay that is required for proper video signal performance.

Another benefit of the THS7376 over a passive RLC filter is the input and output impedance. The input impedance presented to the DAC from passive filters varies significantly, from 35 Ω to over 1.5 kΩ, and may cause voltage variations over frequency. The THS7376 input impedance is 800 kΩ, and only the 2-pF input capacitance plus the PCB trace capacitance impacts the input impedance. As such, the voltage variation appearing at the DAC output is better controlled with a fixed termination resistor and the high input impedance buffer of the THS7376.

On the output side of the filter, a passive filter again has a large impedance variation over frequency. The EIA/CEA-770 specifications require the return loss to be at least 25 dB over the video frequency range of usage. For a video system, this requirement implies the source impedance (which includes the source, series resistor, and filter) must be better than 75 Ω, ±9 Ω. The THS7376 is an operational amplifier that approximates an ideal voltage source, which is desirable because the output impedance is very low and can source and sink current. To properly match the transmission line characteristic impedance of a video line, a 75-Ω series resistor is placed on the output. To minimize reflections and to maintain a good return loss meeting EIA/CEA specifications, this output impedance must maintain a 75-Ω impedance. A wide impedance variation of a passive filter cannot ensure this level of performance. On the other hand, the THS7376 has approximately 0.7 Ω of output impedance (or a return loss of 46 dB, at 6.75 MHz for the SD filter) and approximately 1.3 Ω of output impedance (or a return loss of 41 dB, at 30 MHz for the HD filters). Thus, the system is matched significantly better with a THS7376 compared to a passive filter.

One final benefit of the THS7376 over a passive filter is power dissipation. A DAC driving a video line must be able to drive a 37.5-Ω load: the receiver 75-Ω resistor and the 75-Ω impedance matching resistor next to the DAC to maintain the source impedance requirement. This requirement forces the DAC to drive at least 1.25 V_P (100% saturation CVBS) / 37.5 Ω = 33.3 mA. A DAC is a current-steering element, and this amount of current flows internally to the DAC even if the output is 0 V. Thus, power dissipation in the DAC may be very high, especially when four channels are being driven. Using the THS7376 with a high input impedance and the capability to drive up to two video lines per channel can reduce DAC power dissipation significantly. This outcome is possible because the resistance that the DAC drives can be substantially increased. Setting this resistance in a DAC by a current-setting resistor on the DAC itself is a common practice. Thus, the resistance can be 300 Ω or more, substantially reducing the current drive demands from the DAC and saving significant amounts of power. For example, a 3.3-V, four-channel DAC dissipates 440 mW alone for the steering current capability (four channels × 33.3 mA × 3.3 V) if the DAC must drive a 37.5-Ω load. With a 300-Ω load, the DAC power dissipation as a result of current steering current would only be 55 mW (four channels × 4.16 mA × 3.3 V).

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EVALUATION MODULE

To evaluate the THS7376, an evaluation module (EVM) is available. The THS7376EVM allows for testing the device in many different configurations. Inputs and outputs include BNC connectors commonly found in video systems, along with 75-Ω input termination resistors, 75-Ω series source-termination resistors, and 75-Ω characteristic impedance traces. Several unpopulated component pads are found on the EVM to allow for different input and output configurations as dictated by the user. This EVM is designed to be used with a single supply from 2.85 V up to 5.5 V maximum.

The EVM default input configuration sets all channels for dc input coupling. The input signal must be within 0 V to approximately 1.4 V for proper operation. Failure to be within this range saturates and clips the output signal. If the input range is beyond this range, or if the signal voltage is unknown, or if coming from a current-sink DAC, then ac input configuration is desired. This option is easily accomplished with the EVM by simply replacing the Z_1 through Z_4 0-Ω resistors with 0.1-µF capacitors.

For an ac-coupled input and sync-tip clamp (STC) functionality commonly used for CVBS, s-video Y', component Y' signals, and R'G'B' signals, no other changes are needed. However, if a bias voltage is desired after the input capacitor which is commonly needed for s-video C', component P'_B and P'_R signals, then a pull-up resistor should be added to the signal on the EVM. This configuration is easily achieved by simply adding a resistor to any of the following resistor pads: RX1, RX3, RX5, or RX7. A common value to use is 3 MΩ. Note that even signals with an embedded sync can also use bias mode if desired.

The THS7376EVM default output configuration sets all channels for dc-output coupling. This configuration is commonly used for most modern systems today. However, if ac-coupling is desired, then replacing the 0-Ω resistors at C12, C14, C16, and C17 with 0.1-µF capacitors works well along with the existing 470-µF capacitors already populated. Removing the 470-µF capacitors is optional when dc-coupling is used. Removing these capacitors eliminates a few picofarads of stray capacitance on each signal path, which may be desirable for improved high-frequency response.

The THS7376 incorporates an easy method to configure the bypass and disable mode. The use of JP1 controls the disable feature and JP4 controls the HD channels filter and bypass mode. While there is a space on the EVM for JP2 and JP3, these components are not used for the THS7376.

Connecting JP1 to GND applies 0 V to the disable pin and the THS7376 operates normally. Moving JP1 to $+V_S$ causes all channels of the THS7376 to be in disable mode. If left open, the THS7376 defaults to 0 V and is fully functional.

Connecting JP4 to GND places the THS7376 HD channels in filter mode; moving JP4 to $+V_S$ places the THS7376 HD channels in bypass mode. If left open, the THS7376 defaults to 0 V and is in filter mode operation.

The THS7376 has improved ESD performance on all video input and output pins. Refer to the Absolute Maximum Ratings table for specific tested values of the device. When tested with the THS7376EVM, the THS7376 has passed the IEC ±8-kV contact surge testing through the RCA connections. Note that every complete system may not pass IEC testing because IEC is a system-level test and not a device-level test. However, when a very small EVM with minimal parasitics is used, the THS7376 has been shown to pass IEC surge testing. If further protection is desired, the EVM incorporates pads that can be populated with standard dual-diode packaged parts (such as the BAV99 or BAT54S).

Figure 136 shows the THS7376EVM schematic. Figure 137 and Figure 138 illustrate the two layers of the EVM PCB, incorporating standard high-speed layout practices. Table 2 lists the bill of materials as the board comes supplied from Texas Instruments.

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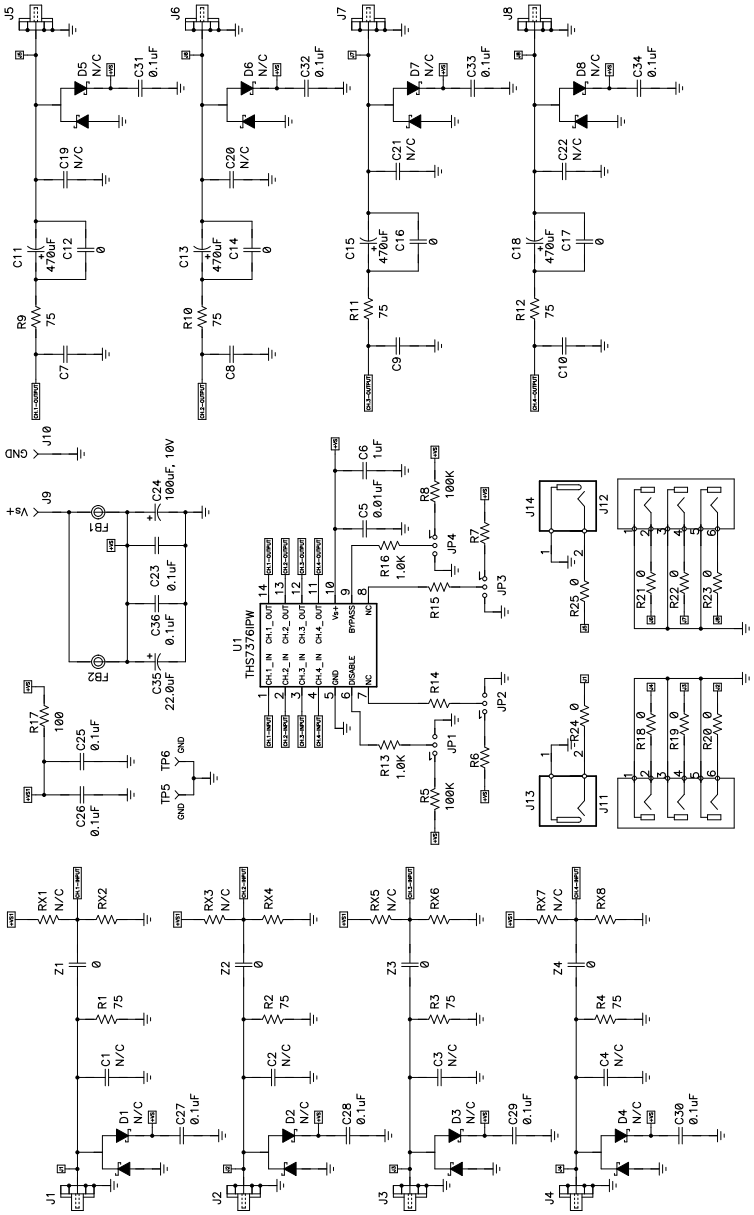

Figure 136. THS7376EVM Schematic

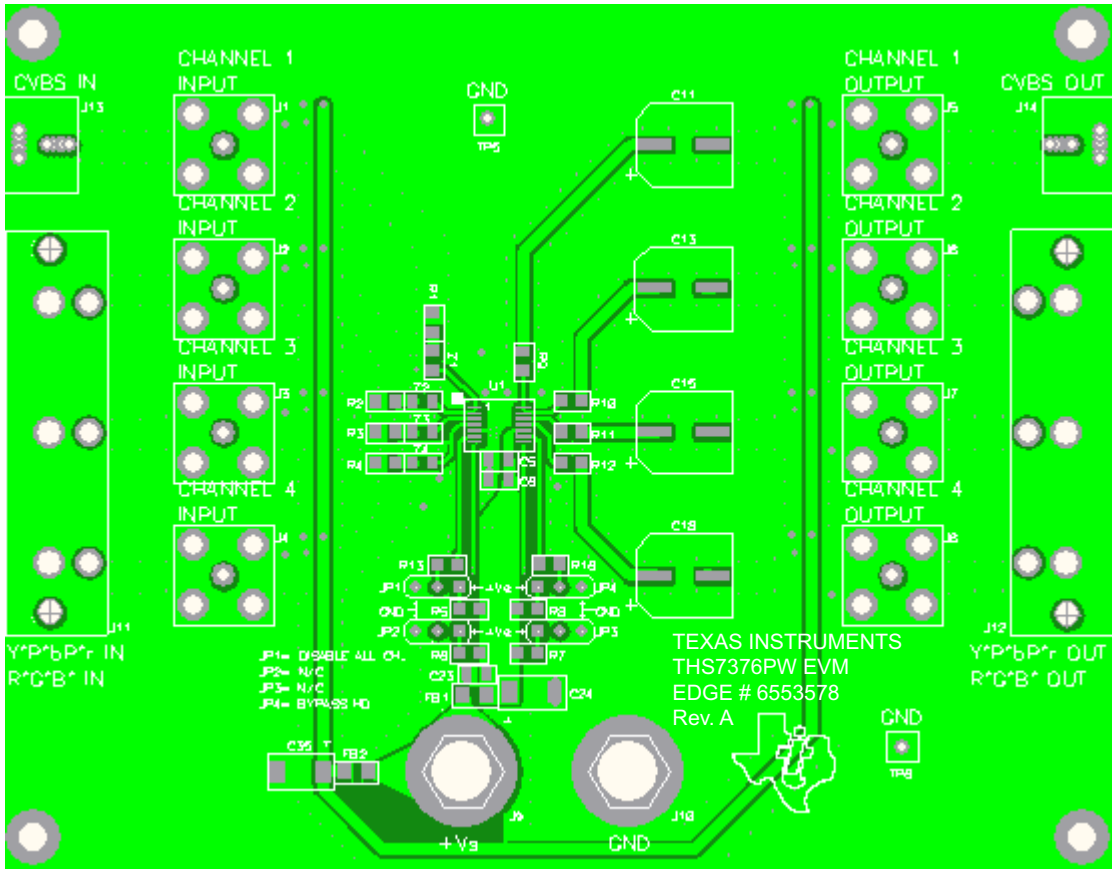

Figure 137. THS7376EVM PCB Top Layer

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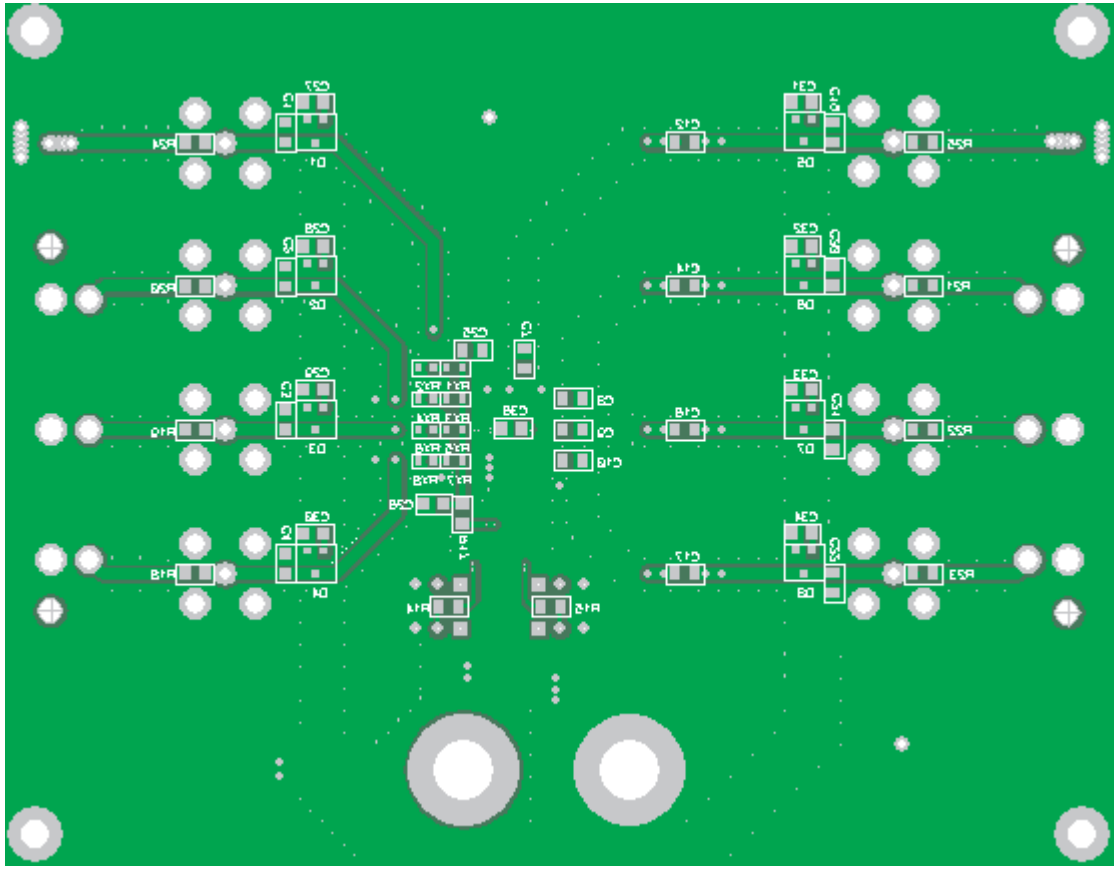

Figure 138. THS7376EVM PCB Bottom Layer

THS7376EVM Bill of Materials

Table 2. THS7376EVM

ITEM	REF DES	QTY	DESCRIPTION	SMD SIZE	MANUFACTURER PART NUMBER	DISTRIBUTOR PART NUMBER
1	FB1, FB2	2	Bead, ferrite, 2.5A, 330 Ω	0805	(TDK) MPZ2012S331A	(DIGI-KEY) 445-1569-1-ND
2	C24	1	Capacitor, 100 µF, tantalum, 10V, 10%, low ESR	C	(AVX) TPSC107K010R0100	(DIGI-KEY) 478-1765-1-ND
3	C35	1	Capacitor, 22 µF, tantalum, 16V, 10%, low ESR	C	(AVX) TPSC226K016R0375	(DIGI-KEY) 478-1767-1-ND
4	C1-C4, C7-C10, C19-C22	12	Open	0805		
5	C5	1	Capacitor, 0.01 µF, ceramic, 100V, X7R	0805	(AVX) 08051C103KAT2A	(DIGI-KEY) 478-1358-1-ND
6	C23, C25-C34, C36	12	Capacitor, 0.1 µF, ceramic, 50V, X7R	0805	(AVX) 08055C104KAT2A	(DIGI-KEY) 478-1395-1-ND
7	C6	1	Capacitor, 1 µF, ceramic, 16V, X7R	0805	(TDK) C2012X7R1C105K	(DIGI-KEY) 445-1358-1-ND
8	C11, C13, C15, C18	4	Capacitor, aluminum, 470 µF, 10V, 20%	F	(PANASONIC) EEE-FP1A471AP	(DIGI-KEY) PCE4526CT-ND
9	RX1-RX8	8	Open	0603		
10	R6, R7, R14, R15	4	Open	0805		
11	Z1-Z4, R18-R25, C12, C14, C16, C17	16	Resistor, 0 Ω	0805	(ROHM) MCR10EZHJ000	(DIGI-KEY) RHM0.0ACT-ND
12	R1-R4, R9-R12	8	Resistor, 75 Ω, 1/8W, 1%	0805	(ROHM) MCR10EZHF75.0	(DIGI-KEY) RHM75.0CCT-ND
13	R17	1	Resistor, 100 Ω, 1/8W, 1%	0805	(ROHM) MCR10EZHF1000	(DIGI-KEY) RHM100CCT-ND
14	R13, R16	2	Resistor, 1k Ω, 1/8W, 1%	0805	(ROHM) MCR10EZHF1001	(DIGI-KEY) RHM1.00KCCT-ND
15	R5, R8	2	Resistor, 100k Ω, 1/8W, 1%	0805	(ROHM) MCR10EZHF1003	(DIGI-KEY) RHM100KCCT-ND
16	D1-D8	8	Open, ultrafast		(FAIRCHILD) BAV99	(DIGI-KEY) BAV99FSCT-ND
17	J9, J10	2	Jack, banana receptance, 0.25" diameter hole		(SPC) 813	(NEWARK) 39N867
18	J1-J8	8	Connector, BNC, jack, 75 Ω		(AMPHENOL) 31-5329-72RFX	(NEWARK) 93F7554
19	J13, J14	2	Connector, RCA jack, yellow		(CUI) RCJ-044	(DIGI-KEY) CP-1421-ND
20	J11, J12	2	Connector, RCA, jack, R/A		(CUI) RCJ-32265	(DIGI-KEY) CP-1446-ND
21	TP5, TP6	2	Test point, black		(KEYSTONE) 5001	(DIGI-KEY) 5001K-ND
22	JP2, JP3	2	Open	3 pos.		
23	JP1, JP4	2	Header, 0.1" CTRS, 0.025" square pins	3 pos.	(SULLINS) PBC36SAAN	(DIGI-KEY) S1011E-36-ND
24	JP1, JP4	2	Shunts		(SULLINS) SSC02SYAN	(DIGI-KEY) S9002-ND
25	U1	1	IC, THS7376	PW	(TI) THS7376IPW	
26	—	4	Standoff, 4-40 hex, 0.625" length		(KEYSTONE) 1808	(DIGI-KEY) 1808K-ND
27	—	4	Screw, Phillips, 4-40, 0.250"		(BF) PMS 440 0031 PH	(DIGI-KEY) H343-ND
28	—	1	Board, printed circuit		EDGE # 6553578 REV. A	

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It is important to operate this EVM within the input voltage range of and the output voltage range of .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than . The EVM is designed to operate properly with certain components above as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THS7376IPW	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS7376
THS7376IPW.B	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS7376
THS7376IPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS7376
THS7376IPWR.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS7376

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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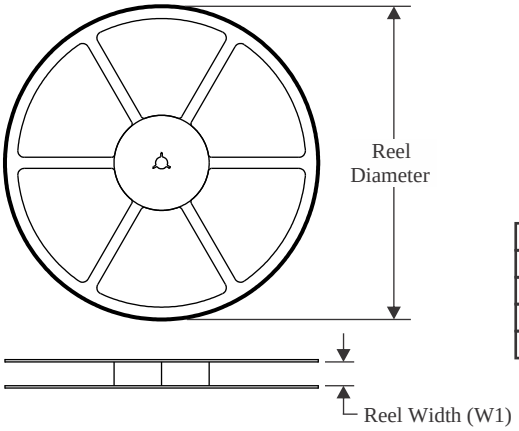
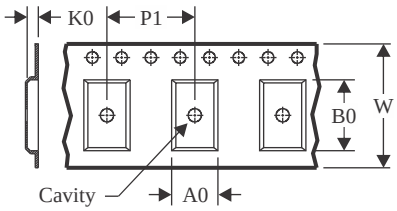
TAPE AND REEL INFORMATION

REEL DIMENSIONS

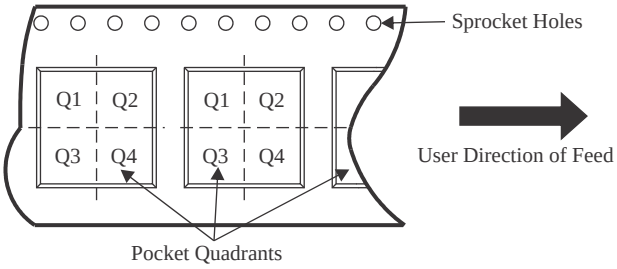


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

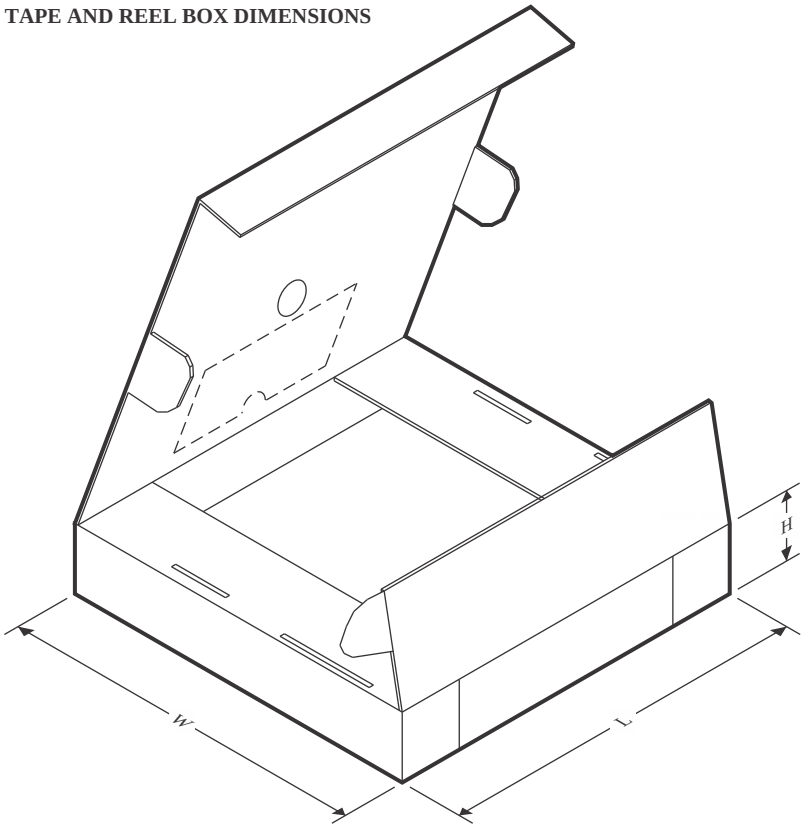
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS7376IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

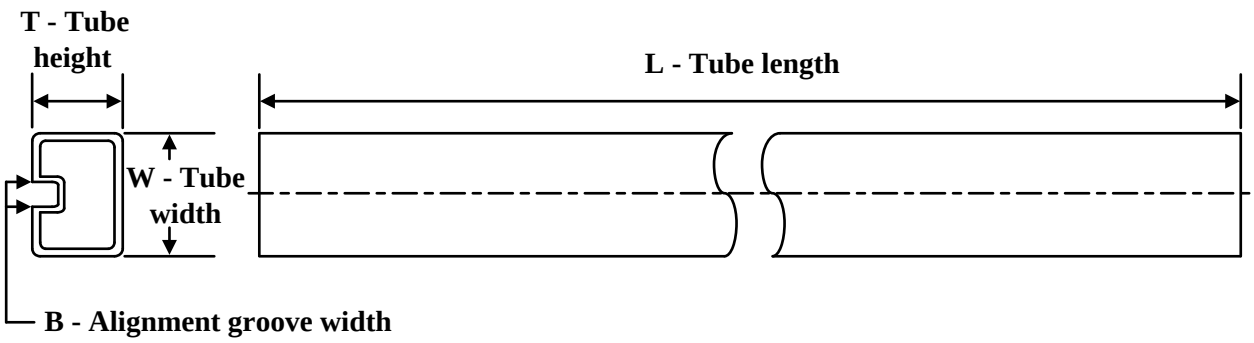
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS7376IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0

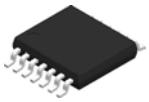
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
THS7376IPW	PW	TSSOP	14	90	530	10.2	3600	3.5
THS7376IPW.B	PW	TSSOP	14	90	530	10.2	3600	3.5

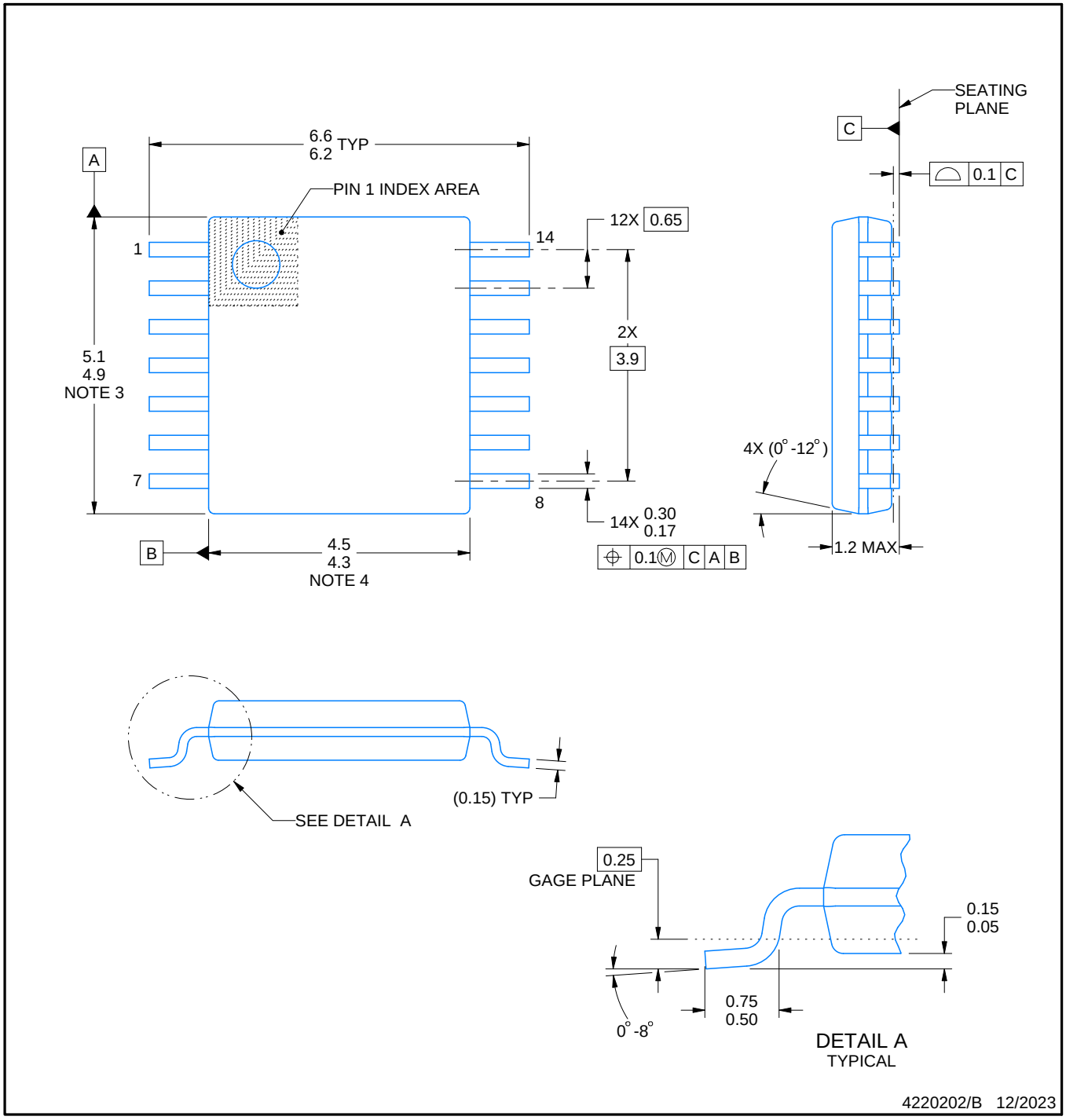
PW0014A



PACKAGE OUTLINE

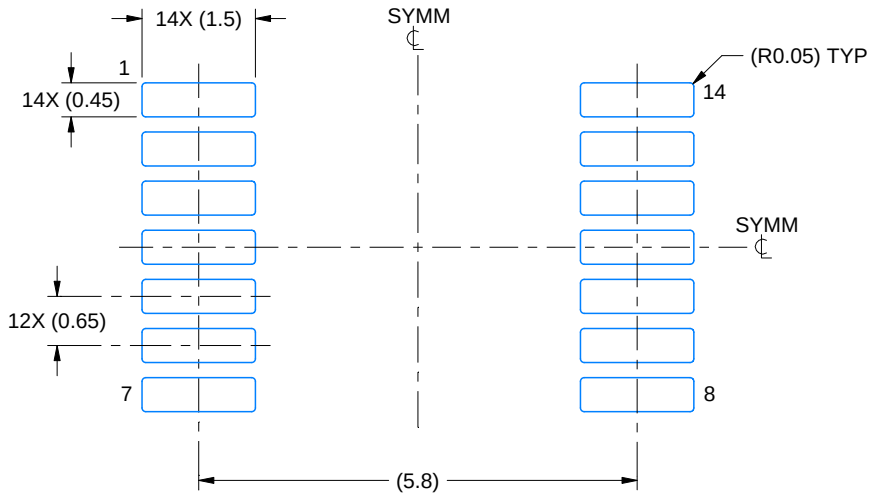
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

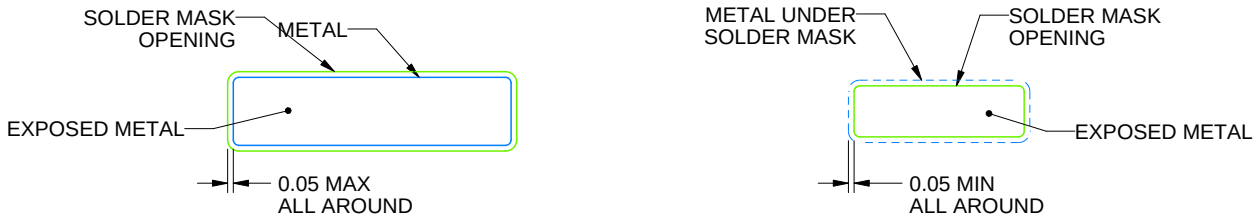


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON-SOLDER MASK DEFINED (PREFERRED)

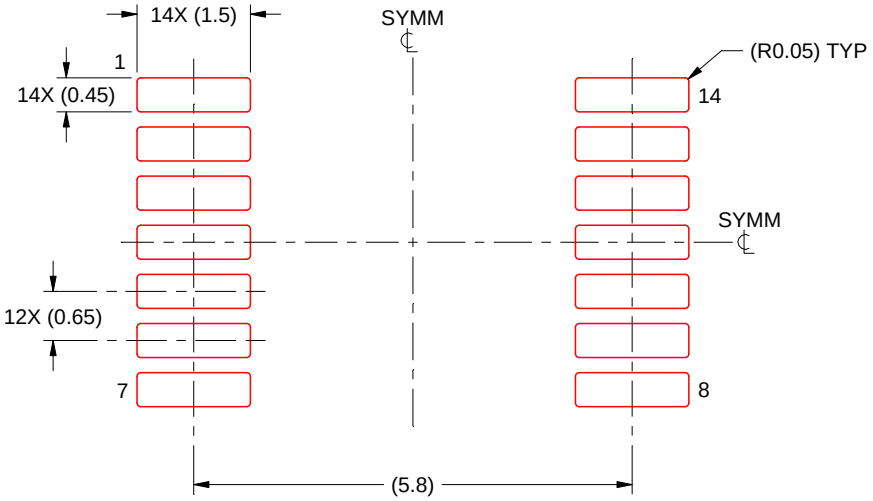
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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