TPS61289 23V_{LOW} , 25V_{HIGH}, 20A Bidirectional BUCK/BOOST Converter

1 Features

- VLOW voltage range: 0.5V to 23V
  - The minimum VLOW voltage is determined by the VLOW/VHIGH ratio and frequency
- VHIGH voltage range: 4.5V to 25V
- Pin selectable bidirectional buck or boost mode
- Buck/boost forced PWM mode operation
- High efficiency and power capability
  - Programmable current limit: 5A to 20A
  - Integrated 8.5mΩ high-side MOSFET
- Switching frequency
  - F_{SW} 250kHz when VLOW > 1.7V
  - F_{SW} down to 100kHz when VLOW < 1.5V
  - F_{SW} down to 50kHz when VLOW < 0.5V
  - 200mV hysteresis prevents frequency jitter
- Synchronization capability to external clock
- Rich protection
  - VHIGH overvoltage protection at 27V
  - VHIGH undervoltage protection at 3.1V
  - VCC undervoltage protection at 2.15V
  - Precise EN/UVLO threshold
  - Cycle-by-cycle overcurrent protection
  - Thermal shutdown
- 2.5mm × 3.0mm VQFN 14 HotRod™ Lite package

2 Applications

- Battery Testing System (BTS)
- Super-cap or battery backup power converter
- USB Type-C® power delivery

3 Description

The TPS61289 is a bidirectional buck/boost synchronous converter that integrates the high-side synchronous rectifier MOSFET and uses an external low side MOSFET. The TPS61289 can be configured as a buck or boost converter using the MODE pin. The TPS61289 can support 20A switching current and the VHIGH voltage supports up to 25V. The minimum VLOW voltage is determined by the VLOW/VHIGH ratio and frequency, for example, the VLOW voltage can support as low as 0.5V at the VHIGH = 15V condition. The device provides an excellent balance of efficiency, thermal dissipation and solution size for high power bidirectional conversion.

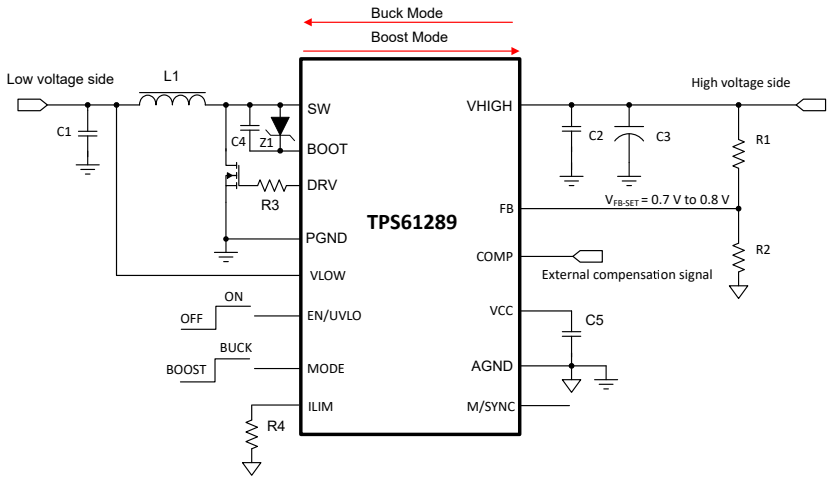
The TPS61289 offers adjustable switching current limit function. In addition, the device provides VHIGH overvoltage and undervoltage protection, cycle-by-cycle overcurrent protection, and thermal shutdown protection.

The TPS61289 offers a very small solution size with 2.5mm x 3.0mm VQFN HotRod™ Lite package with minimal external components.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS61289	VQFN (14)	2.5mm × 3.0mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Circuit

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4 Pin Configuration and Functions

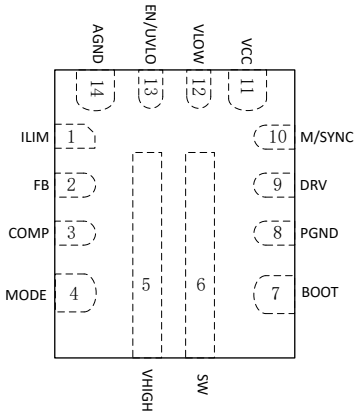

Figure 4-1. 14-Pin RZP VQFN Package (Top View)

Table 4-1. Pin Functions

PIN		TYPE[(1)]	DESCRIPTION
NAME	NUMBER		
ILIM	1	I	Programmable switching peak/valley current limit. An external resistor must be connected between this pin and the AGND pin.
FB	2	I	For bidirectional operation, connect to the center tap of a resistor divider to make the VFB = 0.7V to 0.8V.
COMP	3	I	External loop compensation signal input pin.
MODE	4	I	Mode selection pin, this pin must not be floating. MODE = logic high, buck mode. MODE = logic low, boost mode.
VHIGH	5	P	High voltage side pin.
SW	6	P	The switching node pin. This pin is connected to the drain of the external low-side MOSFET and the source of the internal high-side MOSFET.
BOOT	7	O	Power supply for the high-side MOSFET gate driver. A ceramic capacitor of 0.1μF to 1.0μF and a 5.6V Zener diode must be connected between this pin and the SW pin.
PGND	8	G	Power ground of external low side MOSFET. Source of external low side MOSFET must be connected to this pin.
DRV	9	O	Gate driver output for external low-side MOSFET.
M/SYNC	10	I	When the M/SYNC pin is short to ground or floating, the device works with internal configured switching frequency. When a valid clock signal is applied to this pin, the switching frequency of the device is forced to the external clock.
VCC	11	O	Output of the internal regulator. A ceramic capacitor of more than 1.0μF is required between this pin and AGND.
VLOW	12	P	Low voltage side pin.
EN/UVLO	13	I	Enable logic input and programmable input voltage undervoltage lockout (UVLO) input. Logic high level enables the device. Logic low level disables the device and puts the device into shutdown mode. The converter start-up and shutdown levels can be programmed by connecting this pin to the supply voltage through a resistor divider. This pin must not be left floating and must be terminated.
AGND	14	G	Analog signal ground.

(1) I = Input, O = Output, G = Ground, P = Power.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Voltage	VLOW, EN/UVLO	–0.3	30	V
Voltage	SW, VHIGH	–0.3	32	V
Voltage	BOOT	SW–0.3	SW+6	V
Voltage	M/SYNC, MODE, VCC, COMP, FB, DRV, ILIM	–0.3	7	V
T_J	Operating Junction Temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JS-002, all pins[2]	±500	

(1) HBM: JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process
(2) CDM: JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process

5.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{LOW}	V_{LOW} voltage range			23	V
V_{HIGH}	V_{VHIGH} voltage range	4.5		25	V
L	Effective inductance range		3.3		µH
T_J	Operating junction temperature	-40		125	°C

5.4 Thermal Information

THERMAL METRIC[1]		TPS61289 RZP (VQFN) - 14 PINS Standard	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	64.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	41.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	18.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	18.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

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5.5 Electrical Characteristics

T_J = –40°C to 125°C, V_{LOW} = 3.6V and V_{HIGH} = 18V. Typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{LOW}	V_{LOW} voltage range				23	V
V_{VHIGH}	V_{HIGH} voltage range		4.5		25	V
V_{HIGH_UVLO}	Under voltage lockout threshold	V_{HIGH_UVLO} rising	3.2	3.4	3.6	V
V_{HIGH_UVLO}	Under voltage lockout threshold	V_{HIGH_UVLO} falling	2.9	3.1	3.3	V
V_{CC}	Internal regulator output	I_{VCC} = 15mA		5.1		V
V_{CC_UVLO}	VCC UVLO threshold	VCC rising		2.3		V
V_{CC_UVLO}	VCC UVLO threshold	VCC falling		2.15		V
V_{CC_HYS}	VCC UVLO hysteresis	VCC hysteresis		0.15		V
I_{SD_VLOW}	Shutdown current into VLOW pin	IC disabled, V_{LOW} = SW = 2.3V to 23V, T_J up to 85°C		1.5	6	µA
I_{SD_SW}	Shutdown current into SW pin	IC disabled, V_{LOW} = SW = 2.3V to 23V, T_J up to 85°C		0.2	4	µA
I_{FB_LKG}	Leakage current into FB pin				50	nA
LOGIC INTERFACE						
V_{EN_H}	EN high-level voltage threshold	VCC = 5.0V			1.15	V
V_{EN_L}	EN low-level voltage threshold	VCC = 5.0V	0.4			V
$V_{EN/UVLO_RISE}$	UVLO rising threshold at the EN/UVLO	VCC = 5.0V	1.20	1.23	1.27	V
$I_{EN/UVLO}$	Sourcing current at the EN/UVLO pin	$V_{EN/UVLO}$ = 1.3V	4.4	5	5.6	µA
V_{MODE_H}	MODE high-level voltage threshold	VCC = 5.0V			1.2	V
V_{MODE_L}	MODE low-level voltage threshold	VCC = 5.0V	0.4			V
OUTPUT						
V_{REF}	Reference voltage at the FB pin	PWM mode	0.985	1	1.015	V
V_{HIGH_OVP}	V_{HIGH} overvoltage protection threshold	V_{HIGH} OVP rising	26	27	28	V
$V_{HIGH_OVP_HYS}$	V_{HIGH} OVP protection hysteresis			1		V
POWER SWITCH						
$R_{DS(on)}$	High-side MOSFET on resistance	VCC = 5.0V		8.5		mΩ
F_{SW}	F_{SW} when VLOW > 1.7V	V_{LOW} = 3.6V		250		kHz
	F_{SW} when 0.5V < VLOW < 1.5V	V_{LOW} = 1.2V		100		kHz
	F_{SW} when VLOW < 0.5V	V_{LOW} = 0.3V		50		kHz
t_{OFF_min}	Minimum off time in boost mode			90	130	ns
t_{ON_min}	Minimum on time in buck mode			90	130	ns
t_{DLH}	LS-GATE off to HS-GATE on deadtime			35		ns
t_{DHL}	HS-GATE off to LS-GATE on deadtime			25		ns
I_{LIM}	High clamp valley current limit(boost mode)	R_{ILIM} = 20kΩ	17	20	23	A
	Low clamp valley current limit(boost mode)			-3.3		A
	High clamp peak current limit(buck mode)	R_{ILIM} = 20kΩ	17	20	23	A
	Low clamp peak current limit(buck mode)			-1.5		A

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T_J = –40°C to 125°C, V_{LOW} = 3.6V and V_{HIGH} = 18V. Typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SOFT START						
t_{SS}	Soft start time of internal reference			8		ms
ERROR AMPLIFIER						
I_{SINK}	COMP pin sink current	V_{FB} = V_{REF} + 400mV, V_{COMP} = 1.5V		20		µA
I_{SOURCE}	COMP pin source current	V_{FB} = V_{REF} - 400mV, V_{COMP} = 1.5V		20		µA
V_{COMPH}	High clamp voltage at the COMP pin	R_{ILIM} = 20kΩ , PWM mode		1.6		V
V_{COMPL}	Low clamp voltage at the COMP pin			0.6		V
G_{EA}	Error amplifier transconductance	VCC = 5.0V		180		µA/V
SYNCHRONOUS CLOCK						
R_{SYNC}	Internal pull down resistor from SYNC pin			800		kΩ
$V_{M/SYNC_H}$	M/SYNC high-level voltage threshold				1.2	V
$V_{M/SYNC_L}$	M/SYNC low-level voltage threshold		0.4			V
T_{SYNC_MIN}	Minimum sync clock pulse width		50			ns
PROTECTION						
T_{SD}	Thermal shutdown	Junction temperature rising		160		°C
T_{SD_HYS}	Thermal shutdown hysteresis			20		°C

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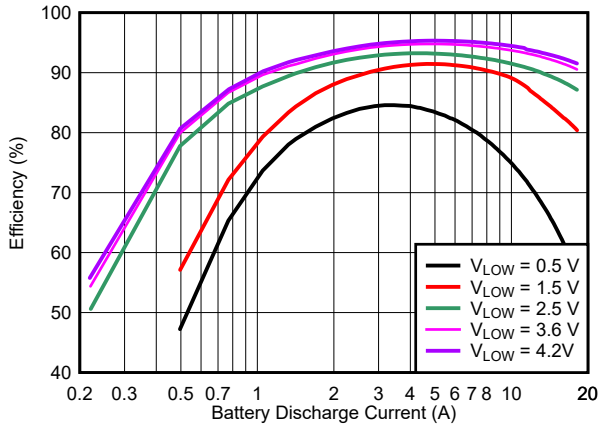
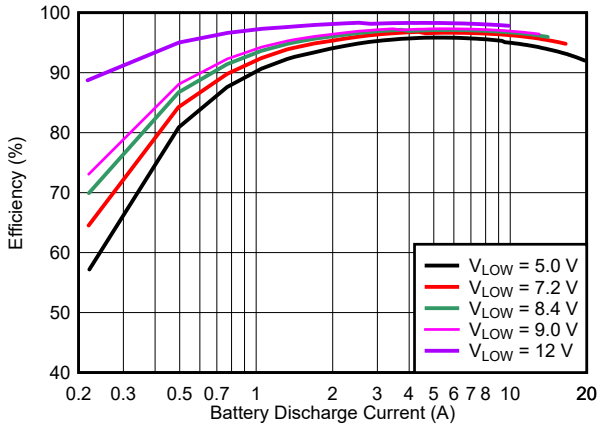
5.6 Typical Characteristics

T_A = 25°C, efficiency data based on EVM, unless otherwise noted.



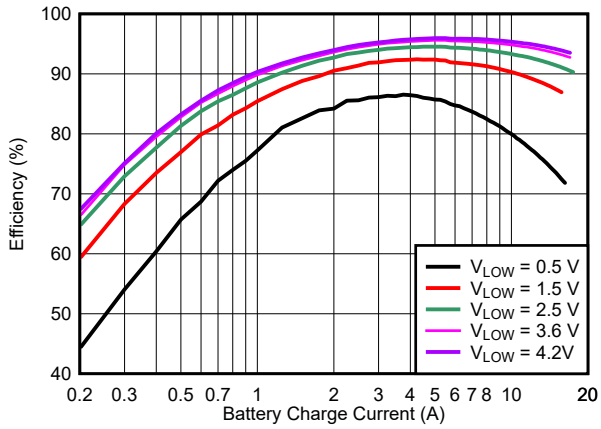
V_{LOW} = 0.5V; 1.5V; 2.5V; 3.6V; 4.2V

Figure 5-1. Efficiency V_{HIGH} = 15 V Boost Mode



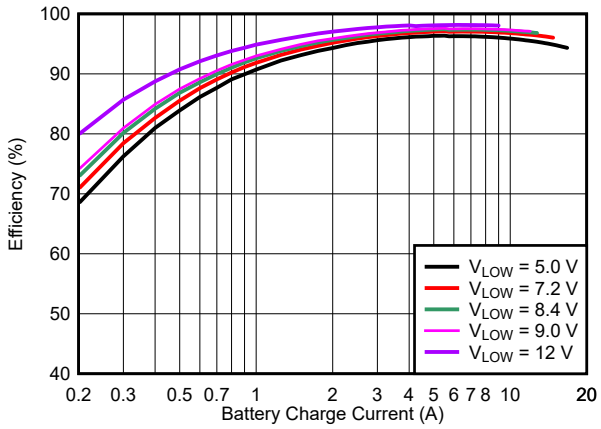
V_{LOW} = 5.0V; 7.2V; 8.4V; 9.0V; 12V

Figure 5-2. Efficiency V_{HIGH} = 15 V Boost Mode



V_{LOW} = 0.5V; 1.5V; 2.5V; 3.6V; 4.2V

Figure 5-3. Efficiency V_{HIGH} = 15 V Buck Mode



V_{LOW} = 5.0V; 7.2V; 8.4V; 9.0V; 12V

Figure 5-4. Efficiency V_{HIGH} = 15V Buck Mode

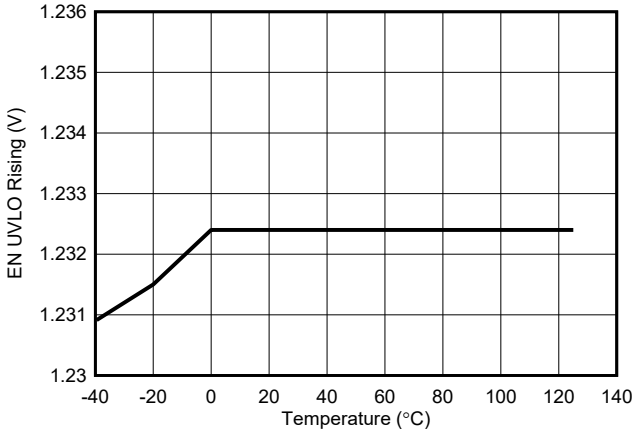


Figure 5-5. EN/UVLO Rising Voltage vs Temperature

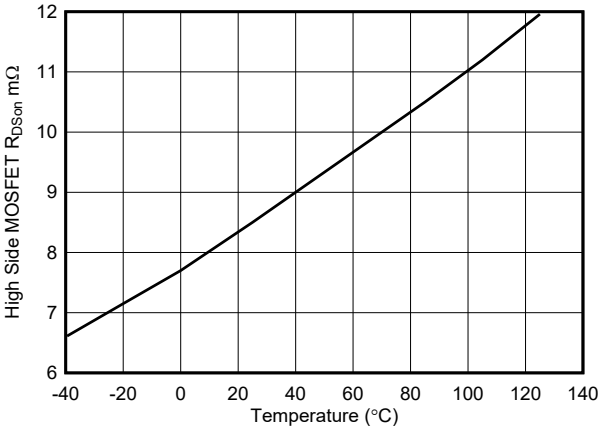


Figure 5-6. R_{DSON} vs Temperature

6 Detailed Description

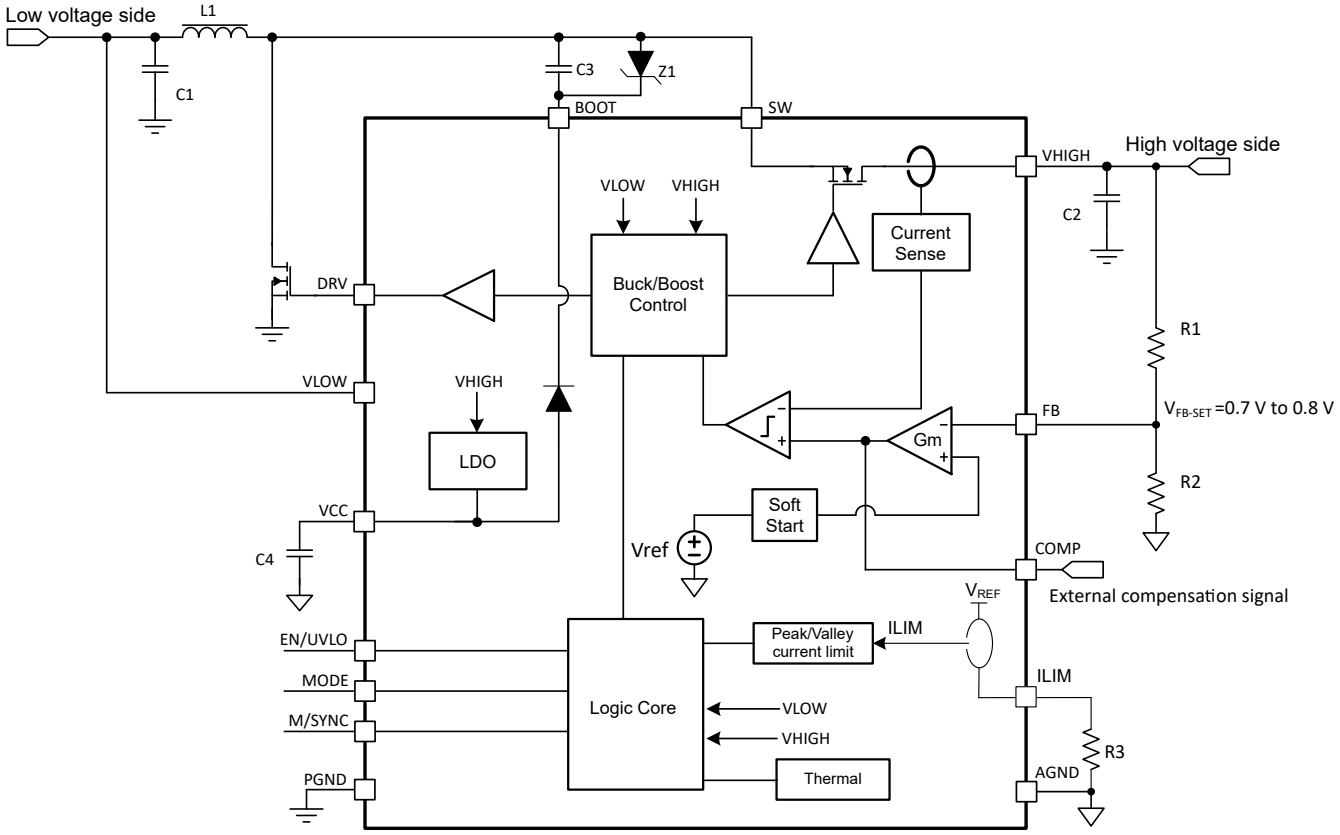
6.1 Overview

The TPS61289 is a bidirectional buck/boost synchronous converter that integrates the high-side synchronous rectifier MOSFET and uses an external low side MOSFET. The low-side gate driver of the TPS61289 has a 1.5A sourcing current and 2A sinking current capability. The TPS61289 can be configured as a buck or boost converter using the MODE pin. The TPS61289 can support 20A switching current and the VHIGH voltage supports up to 25V. The minimum VLOW voltage is determined by the VLOW/VHIGH ratio and frequency, for example, the VLOW voltage can support as low as 0.5V at the VHIGH = 15V condition. The device provides an excellent balance of efficiency, thermal dissipation and solution size for high power bidirectional conversion.

In boost converter mode, the TPS61289 uses an adaptive constant on time valley current control scheme. In buck converter mode, the TPS61289 uses an adaptive constant off time peak current control scheme. In buck or boost operation, the device operates in force PWM mode. The quasi-constant switching frequency is 250kHz when the VLOW pin voltage is greater than 1.7V. To extend the VLOW/VHIGH ratio, when the VLOW pin voltage is less than 1.5V, the frequency drops to 100kHz and the frequency is further reduced to 50kHz when the VLOW pin voltage is less than 0.5V. A hysteresis of 200mV prevents frequency jitter in the presence of VLOW pin voltage noise.

The TPS61289 offers adjustable switching current limit function. In addition, the device provides VHIGH overvoltage protection, cycle-by-cycle overcurrent protection, and thermal shutdown protection.The TPS61289 offers a very small solution size with 2.5mm x 3.0mm VQFN HotRod™ Lite package with minimal external components.

6.2 Functional Block Diagram



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6.3 Feature Description

6.3.1 Bidirectional Operation Configuration

When operating in bidirectional mode, the FB pin must be connected to the center tap of a resistor divider to make the VFB = 0.7V to 0.8V and the COMP pin is connected to an external compensation control signal to implement CC/CV control. To prevent the reverse current from the VHIGH side to the VLOW side, the device will not switch if the COMP pin voltage is below 0.65V. The MODE pin can be used to select the buck or boost mode, the VLOW must be connected to a sink/source power equipment, for example a Li-ion battery. The internal LDO of the TPS61289 is always powered by the VHIGH pin. A valid voltage above V_{HIGH_UVLO} must be applied to the VHIGH pin before the TPS61289 is enabled. Enable the TPS61289 after setting the VHIGH, FB, COMP, VLOW, and Mode pins.

6.3.2 VCC Power Supply

The internal LDO of the TPS61289 is always powered by VHIGH and outputs a regulated voltage of 5.1V with 15mA output current capability. A ceramic capacitor must be connected between the VCC pin and the GND pin to stabilize the VCC voltage and also to decouple the noise on the VCC pin. The value of this ceramic capacitor must be greater than 1µF. A ceramic capacitor with an X7R or X5R grade dielectric and a voltage rating higher than 10V is recommended.

6.3.3 VHIGH and VCC Undervoltage Lockout (UVLO)

The TPS61289 has both V_{HIGH_UVLO} and V_{CC_UVLO} functions. These lockout functions disable the device from switching when the falling voltage at the VHIGH pin triggers the falling threshold of V_{HIGH_UVLO} , which is typically 3.1V. These functions also disables the device when the falling voltage at the VCC pin triggers the threshold of V_{CC_UVLO}, which is typically 2.3V. The device can operate when the rising voltage at the VHIGH and VCC pins exceeds the rising thresholds of V_{HIGH_UVLO} and V_{CC_UVLO}.

6.3.4 Enable and Programmable EN/UVLO

The TPS61289 has a dual function enable and undervoltage lockout (UVLO) circuit. When the voltage at the VHIGH pin and VCC pin is above the rising threshold of UVLO and the EN/UVLO pin is pulled above 1.15V but below the enable EN/UVLO threshold of 1.23V, the TPS61289 is enabled but still in standby mode.

The EN/UVLO pin has an accurate UVLO voltage threshold to support programmable input undervoltage lockout with hysteresis. When the EN/UVLO pin voltage is greater than the UVLO threshold of 1.23V, the TPS61289 is enabled for switching operation. A hysteresis current, I_{UVLO_HYS}, is sourced out of the EN/UVLO pin to provide a hysteresis that prevents on or off chatter in the presence of noise with a slowly changing input voltage. The input voltage can be the voltage of the VLOW or VHIGH pin.

By using resistor divider as shown in Figure 6-1, the turn-on threshold is calculated using Equation 1.

$$V_{IN(UVLO_{ON})} = V_{UVLO} \times \left(1 + \frac{R1}{R2}\right) \tag{1}$$

where

- V_{UVLO} is the UVLO threshold of 1.23V at the EN/UVLO pin.
- V_{IN} can be the voltage of VLOW or VHIGH pin.

The hysteresis between the UVLO turn-on threshold and turn-off threshold is set by the upper resistor in the EN/UVLO resistor divider and is given by Equation 2.

$$\Delta V_{IN(UVLO)} = I_{UVLO_HYS} \times R1 \tag{2}$$

where

- I_{UVLO_HYS} is the sourcing current from the EN/UVLO pin when the voltage at the EN/UVLO pin is above V_{UVLO}.

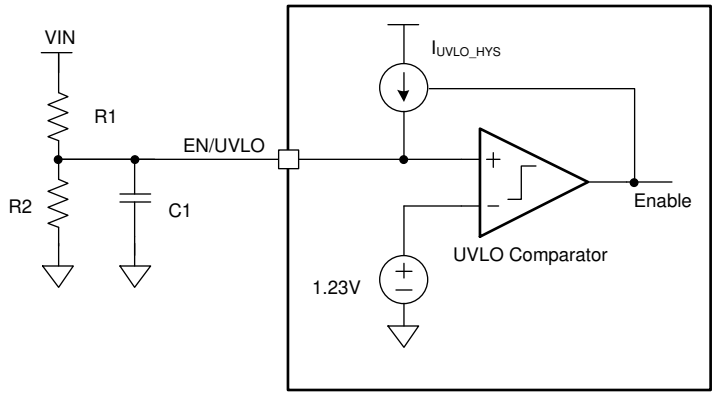

Figure 6-1. Programmable UVLO With Resistor Divider at the EN/UVLO Pin

By using an NMOSFET together with a resistor divider the user can implement both logic enable and programmable UVLO as shown in Figure 6-2. The EN logic high level must be greater than the enable threshold plus the V_{th} of the NMOSFET Q1. The Q1 also eliminates the leakage current from VIN to ground through the UVLO resistor divider during shutdown mode.

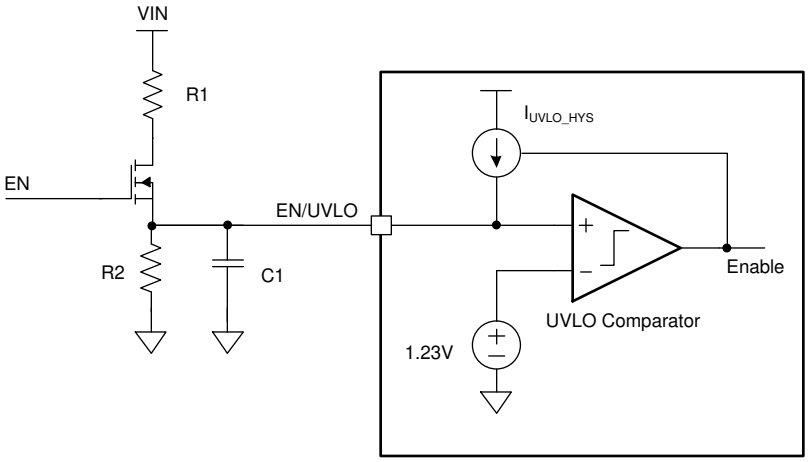

Figure 6-2. Logic Enable and Programmable UVLO

6.3.5 Switching Frequency

The TPS61289 operates at a quasi-constant frequency pulse width modulation (PWM) mode. Based on the ratio of the VLOW voltage to the VHIGH voltage, a circuit predicts the required on or off time of the switching cycle.

When the VLOW pin voltage is higher than 1.7V, the TPS61289 operates at 250kHz switching frequency. When VLOW voltage falls below 1.5V, the frequency changes from 250kHz to 100kHz, when VLOW voltage rises above 1.7V, the frequency changes from 100kHz to 250kHz. When the VLOW voltage falls below 0.5V, the frequency changes from 100kHz to 50kHz, when the VLOW voltage rises above 0.7V, the frequency changes from 50kHz to 100kHz to improve the efficiency and extend the buck/boost ratio. The 200mV hysteresis prevents frequency jitter in the presence of VLOW pin voltage noise.

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6.3.6 Programmable Switching Peak and Valley Current Limit

The TPS61289 has an internal cycle-by-cycle current limit to prevent the inadvertent application of a large switching current.

In boost mode, the TPS61289 adopts a cycle-by-cycle valley current limit method. Current limit detection occurs during the off-time by sensing of the voltage drop across the integrated high-side MOSFET. The high-side MOSFET is turned off immediately as soon as the switch valley current triggers the limit threshold. The switch valley current limit can be set by a resistor from the ILIM pin to ground. The relationship between the valley current limit and the resistor is shown in Equation 3.

$$I_{Valley}(A) = \frac{400k}{R_{LIM}(K)} \tag{3}$$

where

- R_{LIM} is the resistance between the ILIM pin and the AGND pin.
- I_{Valley} is the switch valley current limit.

For instance, the valley current limit in boost mode is 20A if the R_{LIM} is 20kΩ. ILIM pin can not be left floating or connected to VCC.

In buck mode, the TPS61289 adopts a cycle-by-cycle peak current limit method. Current limit detection occurs during the on-time by sensing of the voltage drop across the integrated high-side MOSFET. The high-side MOSFET is turned off immediately as soon as the switch peak current triggers the limit threshold. The switch peak current limit can be set by a resistor from the ILIM pin to ground. The relationship between the peak current limit and the resistor is shown in Equation 4.

$$I_{Peak}\left(A\right) = \frac{400k}{R_{LIM}(K)} \tag{4}$$

where

- R_{LIM} is the resistance between the ILIM pin and the AGND pin.
- I_{Peak} is the switch peak current limit.

For instance, the peak current limit in buck mode is 20A if the R_{LIM} is 20kΩ. ILIM pin can not be left floating or connected to VCC.

6.3.7 External Clock Synchronization

The TPS61289 can synchronize to an external clock signal applied to the M/SYNC pin for noise-sensitive or multiphase applications. When an external clock signal is applied to the M/SYNC pin, the device switching frequency is forced to the external clock. The external clock frequency must be within ±20% of 250kHz. The external clock on the M/SYNC pin must have a low-level voltage less than 0.4V and a high-level voltage greater than 1.2V. A valid synchronous clock signal must be greater than 50ns wide and have a minimum of 4 consecutive clocks prior to synchronization.

6.3.8 VHIGH Overvoltage Protection

The TPS61289 has a VHIGH overvoltage protection to protect the device in case that the external feedback resistor divider is wrongly populated. When the VHIGH voltage is above 27V typically, the device stops switching. Once the VHIGH voltage falls 1V below the OVP threshold, the device resumes operating again.

6.3.9 Thermal Shutdown

The thermal shutdown is implemented to prevent damage from excessive heat and power dissipation. Typically, the thermal shutdown occurs when junction temperatures exceeding 160°C (typical). If the thermal shutdown is triggered, the device stops switching and recovers when the junction temperature drops below 140°C (typical).

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TPS61289 is a bidirectional buck/boost synchronous converter that integrates the high side synchronous rectifier MOSFET and uses an external low side MOSFET. The TPS61289 can be configured as a buck or boost converter using the MODE pin. The TPS61289 can support 20A switching current and the VHIGH voltage supports up to 25V. The minimum VLOW voltage is determined by the VLOW/VHIGH ratio and frequency, for example, the VLOW voltage can support as low as 0.5V at the VHIGH = 15V condition.

The TPS61289 operates in buck mode when current is required to flow from the high voltage side to the low voltage side. Alternatively in boost mode when current is required to flow from the low voltage side to the high voltage side. This makes the TPS61289 applicable for high-current battery test systems that require battery charging and discharging under current and voltage loop control signals. And the use of rechargeable batteries in testing systems is becoming increasingly extensive. To initialize the rechargeable batteries, multiple charge and discharge cycles are required. In this process, the current and voltage of the battery must be accurately controlled. This design does not fully consider the accuracy requirements and focuses only on displaying the charge and discharge functions.

7.2 Typical Application

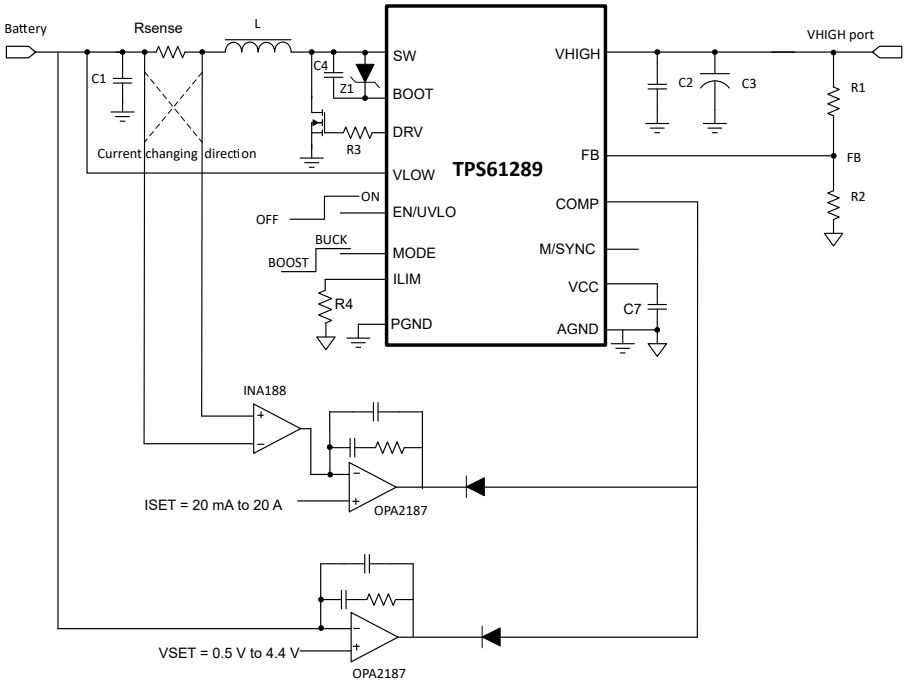

Figure 7-1. TPS61289 Battery Test System Simplified Schematic

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7.2.1 Design Requirements

Table 7-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
VLOW voltage range	0.5V to 4.4V
VHIGH voltage	15V
Max charge current	15A
Max discharge current	15A

7.2.2 Detailed Design Procedure

7.2.2.1 Bootstrap Capacitor Selection

The bootstrap capacitor between the BOOT and SW pin supplies the gate current to charge the high-side FET device gate during the turn on of each cycle. The gate current also supplies charge for the bootstrap capacitor. The recommended value of the bootstrap capacitor is 0.1µF to 1.0µF. C_{BOOT} must be a good quality, low-ESR ceramic capacitor located at the pins of the device to minimize potentially damaging voltage transients caused by trace inductance.

7.2.2.2 Inductor Selection

Since the selection of the inductor affects the steady state of the power supply operation, transient behavior, loop stability, and buck/boost converter efficiency, the inductor is the most important component in switching power regulator design. The three most important specifications to the performance of the inductor are the inductance value, DC resistance, and saturation current.

The TPS61289 is designed to work with inductor values between 2.2µH and 10µH. A 2.2µH inductor is typically available in a smaller or lower-profile package, while a 10µH inductor produces lower inductor current ripple.

Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, the inductance can decrease 20% to 35% from the value at 0A current, depending on how the inductor vendor defines saturation. When selecting an inductor, verify that the rated current of the inductor, especially the saturation current, is larger than the peak current during the operation.

Follow Equation 5 to Equation 7 to calculate the peak current of the inductor. To calculate the current in the worst case, use the minimum input voltage, maximum output voltage, and maximum load current of the application. To leave enough design margin, TI recommends using the minimum switching frequency, the inductor value with –30% tolerance, and a low-power conversion efficiency for the calculation.

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Calculate the inductor DC current as in Equation 5.

$$I_{DC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \tag{5}$$

where

- V_{OUT} is the voltage of VHIGH in boost mode or VLOW in buck mode.
- I_{OUT} is the output current of the converter.
- V_{IN} is the voltage of VHIGH in buck mode or VLOW in boost mode.
- η is the power conversion efficiency.

Calculate the inductor current peak-to-peak ripple as in Equation 6.

$$I_{PP} = \frac{1}{L \times \left(\frac{1}{V_{OUT} \times V_{IN}} + \frac{1}{V_{IN}}\right) \times f_{SW}} \tag{6}$$

where

- I_{PP} is the inductor peak-to-peak ripple.
- L is the inductor value.
- f_{SW} is the switching frequency.
- V_{OUT} is the voltage of VHIGH in boost mode or VLOW in buck mode.
- V_{IN} is the voltage of VHIGH in buck mode or VLOW in boost mode.

Therefore, the peak current, I_{Lpeak}, seen by the inductor is calculated with Equation 7.

$$I_{Lpeak} = I_{DC} + \frac{I_{PP}}{2} \tag{7}$$

Set the current limit of the TPS61289 higher than the peak current, I_{Lpeak}. Then select the inductor with saturation current higher than the setting current limit.

Buck or boost converter efficiency is dependent on the resistance of the current path, the switching loss associated with the switching MOSFETs, and the core loss of the inductor. The TPS61289 has optimized the internal low side switch resistance. However, the overall efficiency is affected significantly by the DC resistance (DCR) of the inductor, equivalent series resistance (ESR) at the switching frequency, and the core loss. Core loss is related to the core material and different inductors have different core loss. For a certain inductor, larger current ripple generates higher DCR and ESR conduction losses and higher core loss. Usually, a data sheet of an inductor does not provide the ESR and core loss information. If needed, consult the inductor vendor for detailed information. Generally, TI recommends an inductor with lower DCR and ESR. However, there is a tradeoff among the inductance of the inductor, DCR and ESR resistance, and the footprint. Furthermore, shielded inductors typically have higher DCR than unshielded inductors. Table 7-2 lists recommended inductors for the TPS61289. Verify whether the recommended inductor can support the user target application with the previous calculations and bench evaluation.

Table 7-2. Recommended Inductors

PART NUMBER	L (µH)	DCR MAX (mΩ)	SATURATION CURRENT(A)	SIZE (L × W × H mm)	VENDOR
XGL1060-332ME	3.3	5.7	26.0	10.0 x 11.3 x 6.0	Coilcraft
XAL1060-222ME	2.2	4.95	32.0	10.0 x 11.3 x 6.0	Coilcraft
CMLE105T-2R2MS-99	2.2	4.5	26.0	10.3 x 11.5 x 4.8	Cyntec

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7.2.2.3 MOSFET Selection

The external power MOSFETs must be selected with a VDS rating that can withstand the maximum VHIGH voltage plus transient spikes (ringing). Once the voltage rating is determined, select the MOSFETs by making tradeoffs between MOSFET $R_{DS(ON)}$ and total gate charge (Qg) to balance conduction and switching losses. Be aware of the deadtime limitation, verify that the low-side and high-side MOSFET are not turned on simultaneously. Be careful when adding series gate resistors, as this can decrease the effective deadtime. The MOSFET gate driver current of the device is supplied from VCC. The maximum gate charge is limited by the 15mA VCC sourcing current limit. A leadless package is preferred for this high switching-frequency designs.

7.2.2.4 VLOW/VHIGH Output Capacitor Selection

For small output voltage ripple, TI recommends a low-ESR output capacitor like a ceramic capacitor. Higher capacitor values or parallel with aluminum electrolytic capacitors can be used to improve the load transient response. Take care when evaluating the derating of the capacitor under DC bias. The bias can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to provide adequate effective capacitance. From the required output voltage ripple, use the following equations to calculate the minimum required effective capacitance C_{OUT}.

$$V_{ripple_dis} = \frac{(V_{OUT} - V_{IN_MIN}) \times I_{OUT}}{V_{OUT} \times f_{SW} \times C_{OUT}} \tag{8}$$

$$V_{ripple_ESR} = I_{Lpeak} \times R_{C_ESR} \tag{9}$$

where

- V_{ripple_dis} is output voltage ripple caused by charging and discharging of the output capacitor.
- V_{ripple_ESR} is output voltage ripple caused by ESR of the output capacitor.
- V_{IN_MIN} is the minimum input voltage.
- V_{OUT} is the output voltage.
- I_{OUT} is the output current.
- I_{Lpeak} is the peak current of the inductor.
- f_{SW} is the converter switching frequency.
- R_{C_ESR} is the ESR of the output capacitors.

Note

DC bias effect: High-capacitance ceramic capacitors have a DC bias effect, which has a strong influence on the final effective capacitance. Therefore, the right capacitor value must be chosen carefully. The differences between the rated capacitor value and the effective capacitance result from package size and voltage rating in combination with material. A 10V rated 0805 capacitor with 10µF can have an effective capacitance of less than 5µF at an output voltage of 5V.

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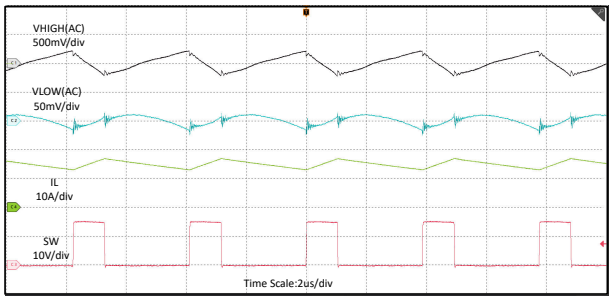
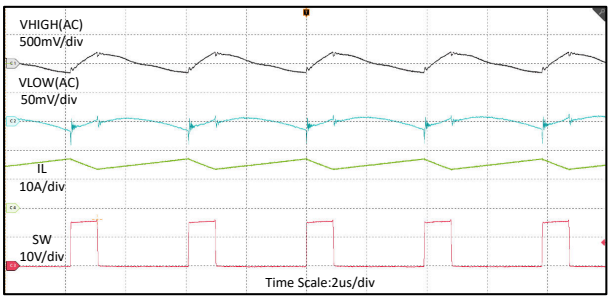
7.2.3 Application Curves



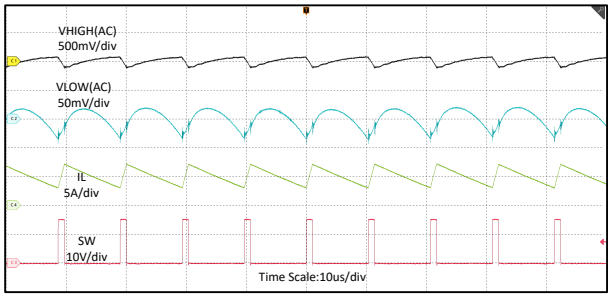
V_{LOW} = 3.6V V_{HIGH} = 15V I_{Charge} = 15A

Figure 7-2. Switching Waveforms in Buck Mode



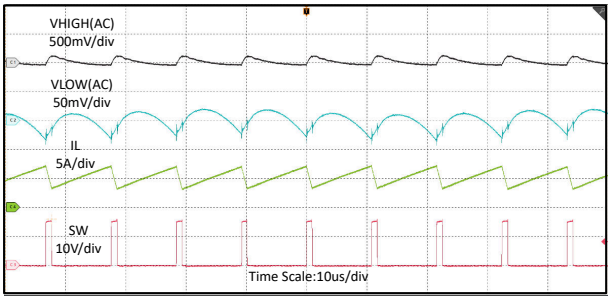
V_{LOW} = 3.6V V_{HIGH} = 15V $I_{Discharge}$ = 15A

Figure 7-3. Switching Waveforms in Boost Mode



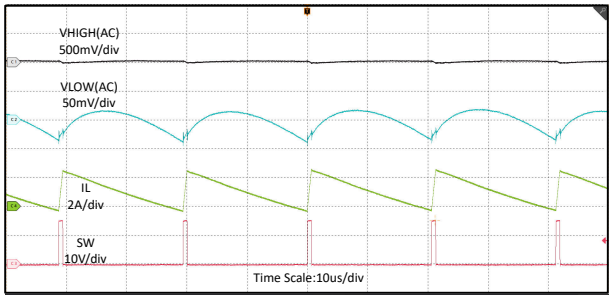
V_{LOW} = 1.5V V_{HIGH} = 15V I_{Charge} = 5A

Figure 7-4. Switching Waveforms in Buck Mode



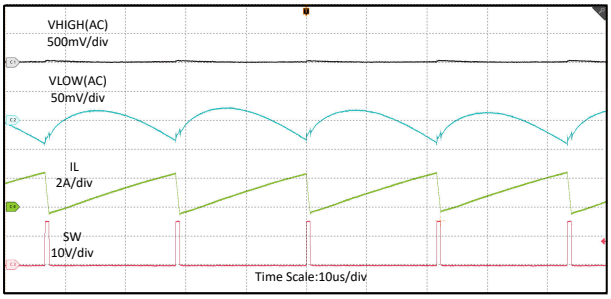
V_{LOW} = 1.5V V_{HIGH} = 15V $I_{Discharge}$ = 5A

Figure 7-5. Switching Waveforms in Boost Mode



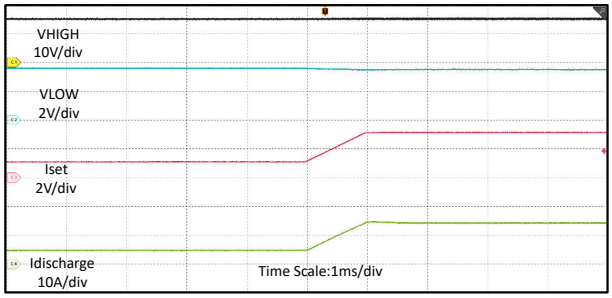
V_{LOW} = 0.5V V_{HIGH} = 15V I_{Charge} = 1.0A

Figure 7-6. Switching Waveforms in Buck Mode



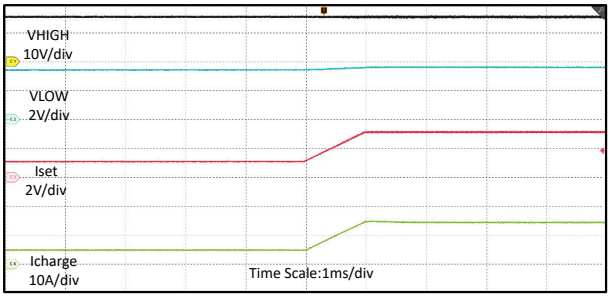
V_{LOW} = 0.5V V_{HIGH} = 15V $I_{Discharge}$ = 1.0A

Figure 7-7. Switching Waveforms in Boost Mode



V_{LOW} = 3.6V V_{HIGH} = 15V

Figure 7-8. Discharge current Transient (5A to 15A)



V_{LOW} = 3.6V V_{HIGH} = 15V

Figure 7-9. Charge current Transient (5A to 15A)

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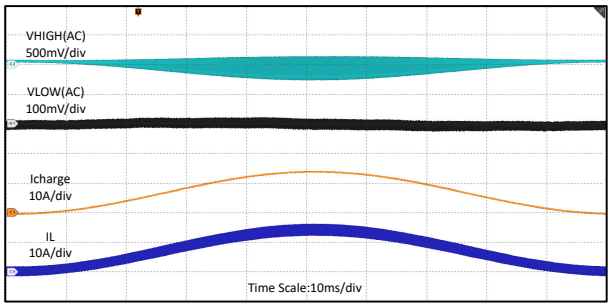
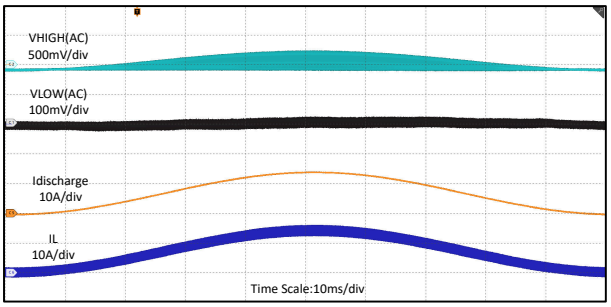


V_{LOW} = 3.6V V_{HIGH} = 15V

Figure 7-10. Buck Load Sweep (I_{Charge}= 0A to 15A)



V_{LOW} = 3.6V V_{HIGH} = 15V

Figure 7-11. Boost Load Sweep ($I_{Discharge}$= 0A to 15A)

7.3 Power Supply Recommendations

The VLOW and VHIHG power supply must be well regulated. If the power supply is located more than a few inches from the converter, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. A typical choice is an electrolytic or tantalum capacitor with a value of 47µF.

7.4 Layout

7.4.1 Layout Guidelines

For all switching power supplies, especially those running at high switching frequency and high currents, layout is an important design step. If layout is not carefully done, the regulator can suffer from instability and noise problems. To maximize efficiency, switch rise and fall times are very fast. To prevent radiation of high-frequency noise (for example, EMI), proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize interplane coupling.

The most critical current path for this bidirectional buck/boost converter is from the external low side MOSFET to the integrated high side MOSFET, then to the VHIGH side capacitors, and back to the source of the external low side MOSFET. This current path contains nanosecond rise and fall times and must be kept as short as possible to reduce the parasitic inductance. Therefore, the VHIGH side output capacitors must be close not only to the VHIGH pin, but also to the source pin of the external low side MOSFET to reduce the spike at the SW pin and the VHIGH pin.

The PGND plane and the AGND plane are connected at the terminal of the VCC capacitor. Thus the noise caused by the MOSFET driver and parasitic inductance does not interfere with the AGND and internal control circuit.

The layout must also be designed with consideration of the thermal as this is a high power density device. The VLOW, SW and VHIGH that improves the thermal capabilities of the package must be soldered with the large polygon. Using thermal vias underneath the nets can improve thermal performance.

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7.4.2 Layout Example

The bottom layer is a large ground plane GND.

VLOW- plane ,VHIGH- plane and PGND nets are all connected to the ground plane by vias on top layer .

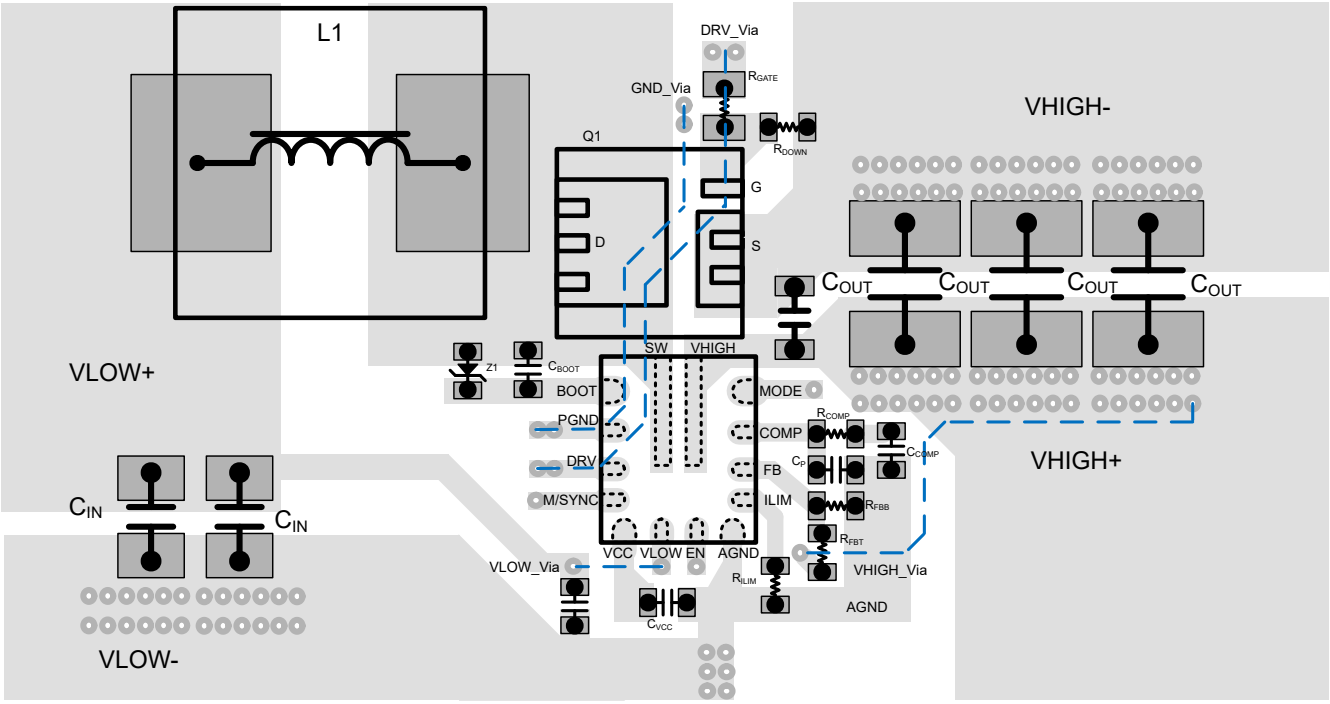

Figure 7-12. Layout Example

7.4.2.1 Thermal Considerations

The maximum IC junction temperature must be restricted to 125°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation 10.

$$P_{D(max)} = \frac{125 - T_A}{R_{\theta JA}} \tag{10}$$

where

- T_A is the maximum ambient temperature for the application.
- $R_{\theta JA}$ is the junction-to-ambient thermal resistance given in the *Thermal Information* table.

The TPS61289 is in a thermally-enhanced VQFN package. The real junction-to-ambient thermal resistance of the package greatly depends on the PCB type, layout, and thermal pad connection. Using thick PCB copper and soldering the thermal pad to a large ground plate enhance the thermal performance. Increasing the number of vias that connect the ground plate on both the top and bottom layers around the IC, without solder mask, can also enhance the thermal capability.

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8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2023) to Revision A (January 2024)	Page
• Changed device status from Advance Information to Production Data	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS61289RZPR	Active	Production	VQFN-HR (RZP) | 14	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	S61289
TPS61289RZPR.A	Active	Production	VQFN-HR (RZP) | 14	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	S61289

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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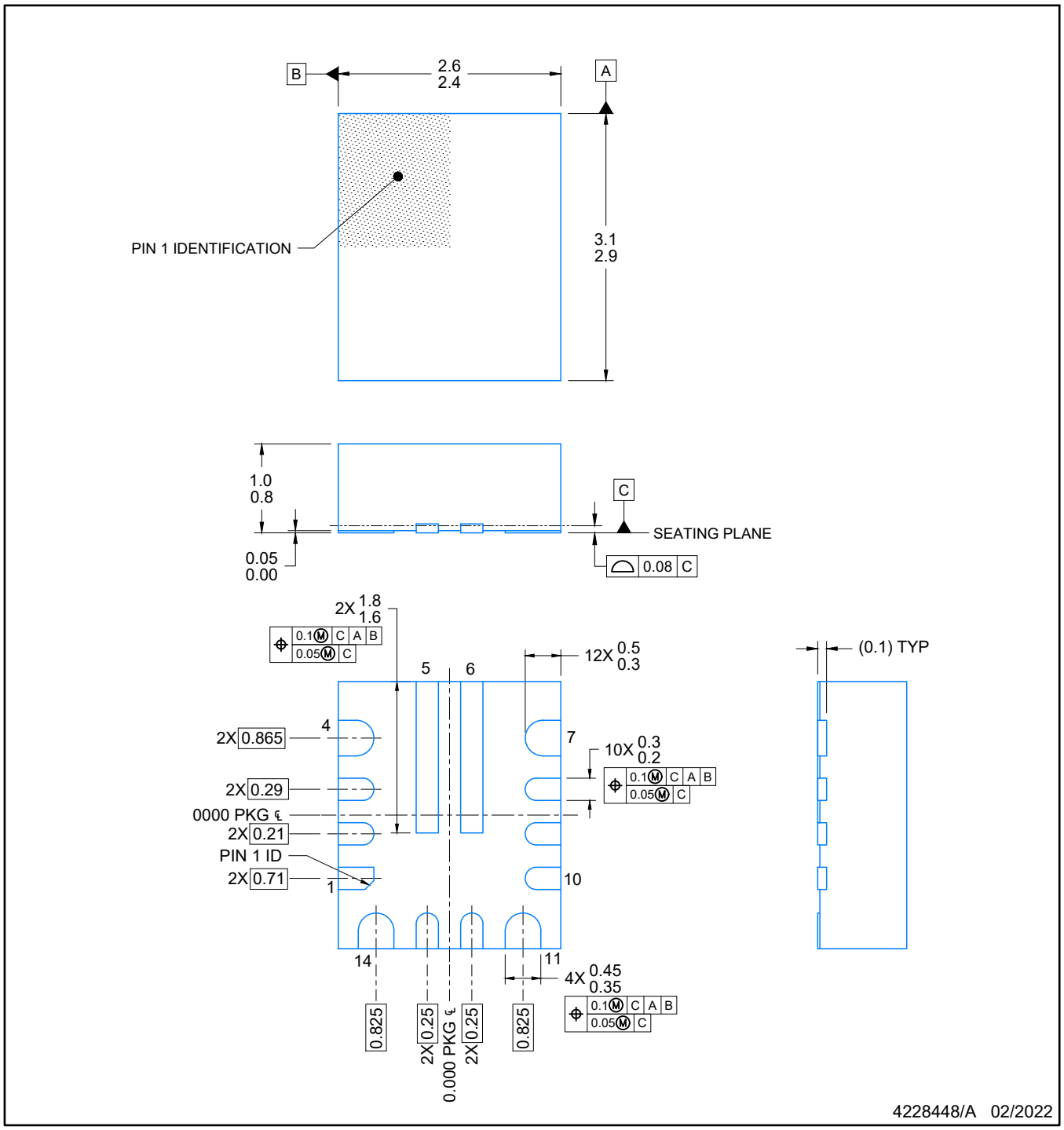
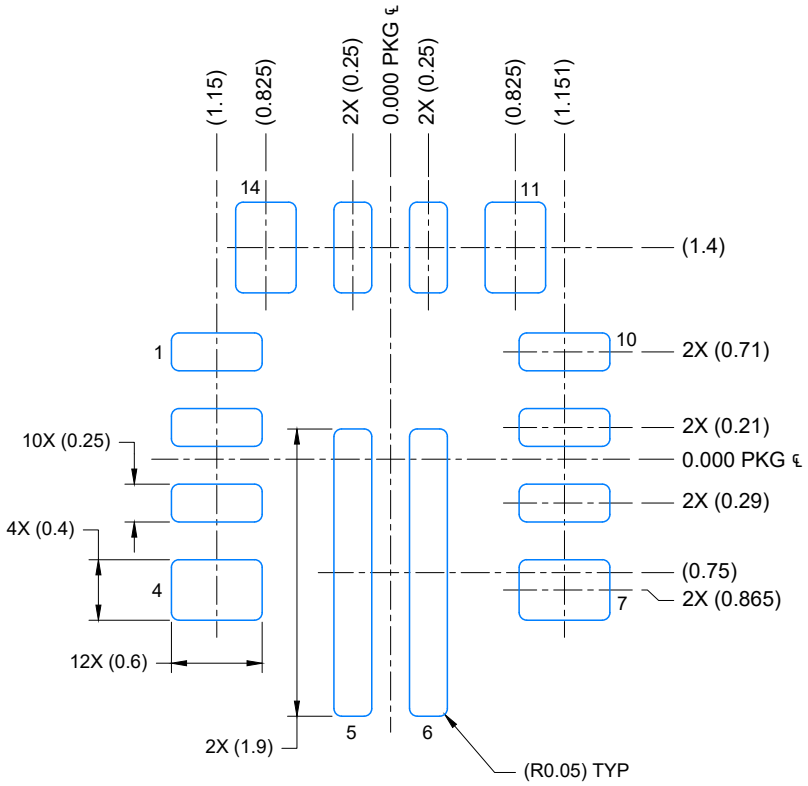
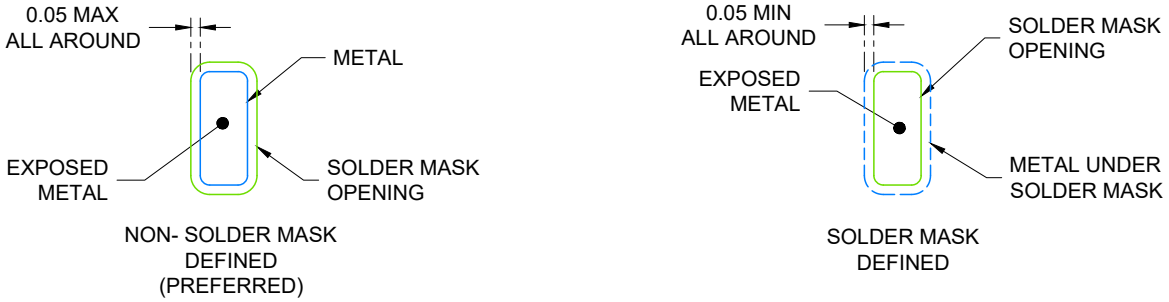


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

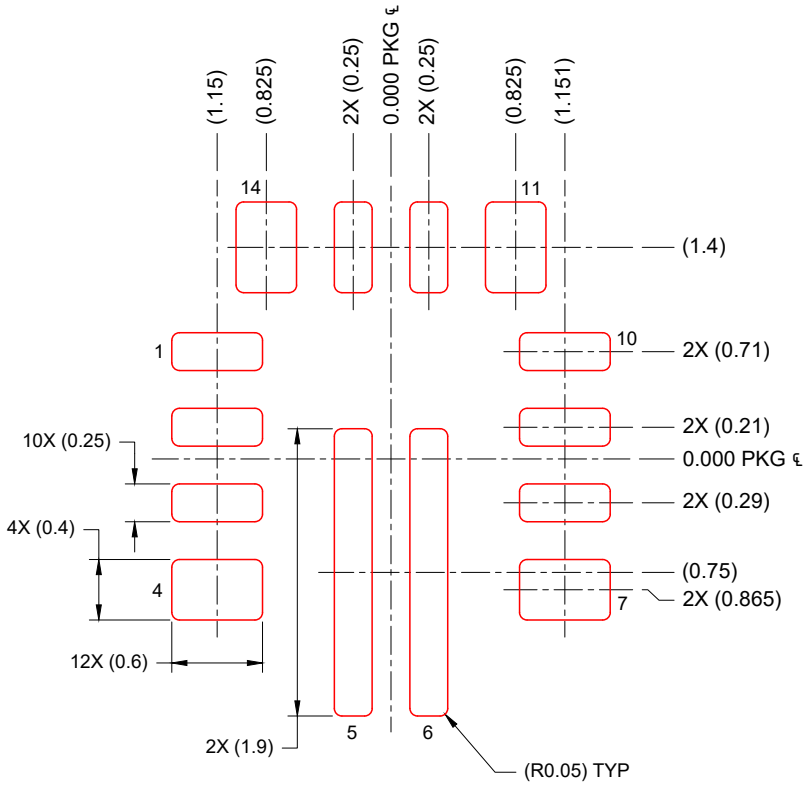


SOLDER MASK DETAILS
NOT TO SCALE

4228448/A 02/2022

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 20X

4228448/A 02/2022

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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