DS34RT5110 DVI, HDMI Retimer with Input Equalization and Output De-Emphasis

Check for Samples: DS34RT5110

FEATURES

- **Optimized for HDMI/DVI Repeater Applications**
- **TMDS compatible Inputs with Configurable Receive Equalization Supporting Data Rates up to 3.4 Gbps**
- **TMDS compatible Outputs with Configurable Transmit De-Emphasis**
- **Dedicated CDR on Each Data Channel Reduces Jitter Transfer, Enabling Multiple Devices to be Cascaded without Impairing Signal Fidelity**
- **Capable of Multi-Hop Extension of HDMI/DVI Applications at Data Rates between 250 Mbps and 3.4 Gbps**
- **Resistor Adjustable Differential Output Voltage for AC Coupled Cat5e and Cat6 Extension Applications**
- **2 Equalizer Settings for a Wide Range of Cable Reaches at Different Data Rates**
- **Total Output Jitter of 0.09 UI at 2.25 Gbps**
- **Total Output Jitter of 0.10 UI at 3.4 Gbps**
- **DVI 1.0 and HDMI v1.3a Compatible TMDS Source and Sink Interface**
- **7 mm x 7 mm 48 Pin WQFN Package**
- **>8 kV HBM ESD Protection**
- **0 °C to +70 °C Operating Temperature**

APPLICATIONS

- **Repeater Applications**
  - **Digital Routers**
  - **HDMI / DVI Extender Multi-Hops**
- **Source Applications**
  - **Video Cards**
  - **Blu-ray DVD Players**
  - **Game Consoles**
- **Sink Applications**
  - **High Definition Displays**
  - **Projectors**

DESCRIPTION

The DS34RT5110 is a 10.2 Gbps (3 x 3.4 Gbps) high performance re-clocking device that supports 3 Transition Minimized Differential Signaling (TMDS) data channels and a single clock channel over DVI™ v1.0, and HDMI™ v1.3a data rates up to 3.4 Gbps for each data channel. The device incorporates a configurable receive equalizer, a clock and data recovery (CDR) circuit and a de-emphasis driver on each data channel. The clock channel feeds a high-performance phase-locked loop (PLL) that regenerates a low jitter output clock for data recovery.

The DS34RT5110 equalizes and retimes greater than 25 meters 28 AWG of HDMI cable for 1080p resolution with 12 bit deep color depth (2.25 Gbps), to a low jitter version of the clock and data signal outputs, reducing both deterministic and random jitter. Several devices can be cascaded for long links without degrading signal fidelity. Obtaining total jitter is 0.09 UI or less over the supported data rates. This low level of output jitter provides system designers with extra margin and flexibility when working with stringent timing budgets.

The transmitter supports configurable transmit de-emphasis so the output can be optimized for driving additional lengths of cables or FR4 traces.

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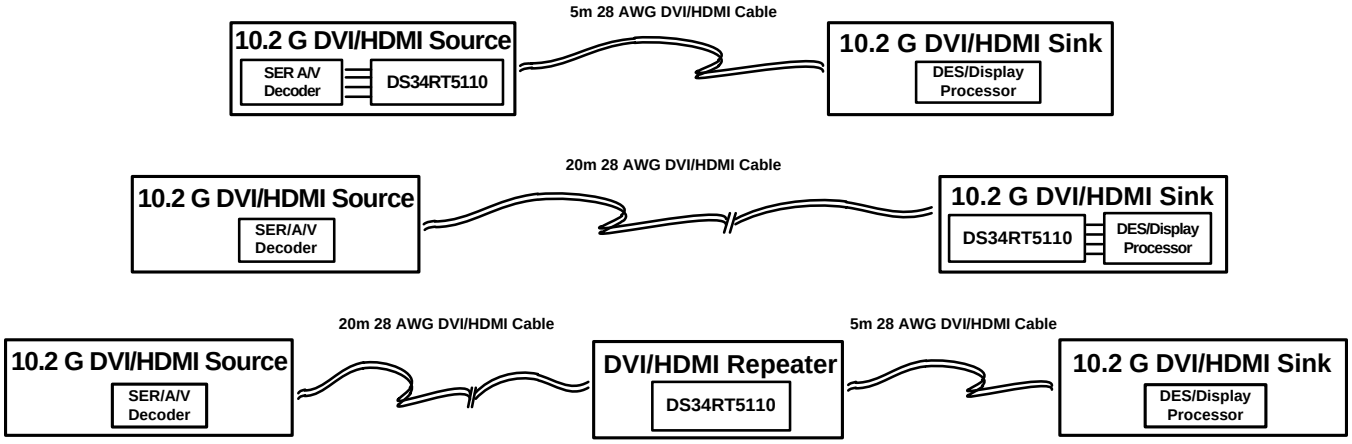
Application Diagram



PIN DESCRIPTIONS

Pin Name	Pin Number	I/O, Type	Description
High Speed Differential I/O			
C_IN− C_IN+	1 2	I, CML	Inverting and non-inverting TMDS Clock inputs to the equalizer. An on-chip 50 Ω terminating resistor connects C_IN+ to V_{DD} and C_IN- to V_{DD}.
D_IN0− D_IN0+	4 5	I, CML	Inverting and non-inverting TMDS Data inputs to the equalizer. An on-chip 50 Ω terminating resistor connects D_IN0+ to V_{DD} and D_IN0- to V_{DD}.
D_IN1− D_IN1+	8 9	I, CML	Inverting and non-inverting TMDS Data inputs to the equalizer. An on-chip 50 Ω terminating resistor connects D_IN1+ to V_{DD} and D_IN1- to V_{DD}.
D_IN2− D_IN2+	11 12	I, CML	Inverting and non-inverting TMDS Data inputs to the equalizer. An on-chip 50 Ω terminating resistor connects D_IN2+ to V_{DD} and D_IN2- to V_{DD}.
C_OUT- C_OUT+	36 35	O, CML	Inverting and non-inverting TMDS outputs from the equalizer. Open collector.
D_OUT0− D_OUT0+	33 32	O, CML	Inverting and non-inverting TMDS outputs from the equalizer. Open collector.
D_OUT1– D_OUT1+	29 28	O, CML	Inverting and non-inverting TMDS outputs from the equalizer. Open collector.
D_OUT2− D_OUT2+	26 25	O, CML	Inverting and non-inverting TMDS outputs from the equalizer. Open collector.
Equalization Control			
EQ2 EQ1 EQ0	37 38 39	I, LVCMOS	EQ2, EQ1 and EQ0 select the equalizer boost level for EQ channels. Internally pulled LOW as default. Refer to Table 1.
De-Emphasis Control			
DE1 DE0	42 43	I, LVCMOS	DE1, DE0 select the DE-emphasis level for output drivers. Internally pulled low as default. Refer to Table 2.
Device Control			
BYPASS	47	I, LVCMOS	Reclocker enable control. Internally pulled low as default. H = Reclock and De-Emphasis function is bypassed. L = Normal operation.
EN	44	I, LVCMOS	Enable Output Drivers. Internally pulled HIGH as default. H = normal operation (enabled). L = standby mode.
MODE	21	I, LVCMOS	Clock channel mode control. Internally pulled LOW as default. H = Clock channel is bypassed. L = Normal operation.
SD	45	O, LVCMOS	Signal Detect Output pin. H = signal detected on all channels. L = no signal detected on one or more channels.

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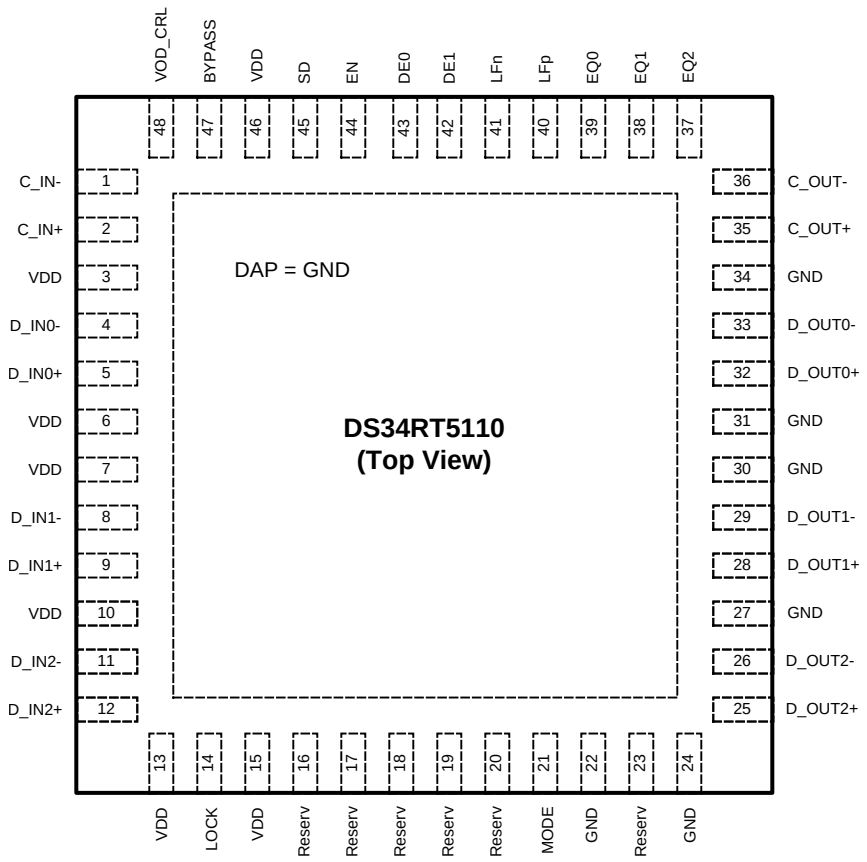
PIN DESCRIPTIONS (continued)

Pin Name	Pin Number	I/O, Type	Description
LOCK	14	O, LVCMOS	Lock Indicator Output pin. H = PLL is locked. L = PLL is not locked.
VOD_CRL	48	I, Analog	VOD control pin. Refer to Table 3. See Functional Description. External resistance = 24 kΩ to GND, Output DC Coupled Application. External resistance = 12 kΩ to GND, Output AC Coupled Application.
LFp LFn	40 41	I, Analog	Loop filter capacitor pins. See Functional Description.
Power			
V_{DD}	3, 6, 7, 10, 13, 15, 46	Power	V_{DD} = 3.3 V ±5%. V_{DD} pins should be tied to the V_{DD} plane through a low inductance path. A 0.1 µF bypass capacitor should be connected between each V_{DD} pin to the GND planes. See POWER SUPPLY BYPASSING for additional details.
GND	22, 24, 27, 30, 31, 34	GND	Ground reference. GND should be tied to a solid ground plane through a low impedance path.
Exposed DAP	DAP	GND	Ground reference. The exposed pad at the center of the package must be connected to the ground plane.
Other			
Reserv	16, 17, 18, 19, 20, 23		Reserved. Do not connect. Leave open.

Connection Diagram



TOP VIEW — Not to Scale

48 Pin WQFN Package
See Package Number RHS0048A

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

Supply Voltage (V_{DD})		-0.5V to 4.0 V
LVCMOS Input Voltage		-0.5V to (V_{DD}+ 0.5) V
LVCMOS Output Voltage		-0.5V to (V_{DD}+ 0.5) V
CML Input/Output Voltage		-0.5V to (V_{DD}+ 0.5) V
Junction Temperature		+125°C
Storage Temperature		-65°C to +150°C
Lead Temp. (Soldering, 5 sec.)		+260°C
ESD Rating	HBM, 1.5 kΩ, 100 pF	>8 kV
Thermal Resistance θ_{JA}, No Airflow		33°C/W

(1) "Absolute Maximum Ratings" are the ratings beyond which the safety of the device cannot be ensured. They are not meant to imply that the device should be operated at these limits.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

Recommended Operating Conditions[1][2]

	Min	Typ	Max	Units
Supply Voltage (V_{DD} to GND)	3.135	3.3	3.465	V
Supply Noise Tolerance (100 Hz to 50 MHz)[3]		100		mVp-p
Ambient Temperature	0	25	+70	°C

(1) Typical parameters are measured at V_{DD} = 3.3 V, T_A = 25 °C. They are for reference purposes, and are not production-tested.
(2) Parameter is ensured by statistical analysis and/or design.
(3) Allowed supply noise (mVp-p sine wave) at typical condition.

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Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. All parameters are ensured by test, statistical analysis, or design unless otherwise specified(1).

Symbol	Parameter	Condition	Min	Typ	Max	Units
Power						
P	Power Supply Consumption	EN = H, Device Enabled PRBS15 pattern, fCLK=340 MHz RT= 50Ω to AV_{CC}, Figure 2		1100	1250	mW
		EN = L, Standby Mode PRBS15 pattern, fCLK=340 MHz RT= 50Ω to AV_{CC}, Figure 2		850	1000	mW
LVCMOS / LVTTL DC Specifications						
VIH	High Level Input Voltage		2		V_{DD}	V
VIL	Low Level Input Voltage		GND		0.8	V
VOH	High Level Output Voltage	IOH = -3 mA	2.4			V
VOL	Low Level Output Voltage	IOL = 3 mA			0.4	V
IIH	Input High Current	VIN = V_{DD}, EQ2, EQ1, EQ0, DE1, DE0, BYPASS, MODE pins (pull down)			60	µA
		VIN = V_{DD}, EN pin (pull up)	-15			µA
IIL	Input Low Current	VIN = 0 V, EQ2, EQ1, EQ0, DE1, DE0, BYPASS, MODE pins (pull down)			15	µA
		VIN = 0 V, EN pin (pull up)	-20			µA
Signal Detect						
SDH	Signal Detect High	Default Input signal level to assert SD pin		80		mVp-p
SDL	Signal Detect Low	Default Input signal level to deassert SD		20		mVp-p
CML Inputs						
VTX	Input Voltage Swing (Launch Amplitude)	Measured differentially at TPA, Figure 1(2)	800	1000	1560	mVp-p
VICMDC	Input Common-Mode Voltage	DC-Coupled requirement Measured at TPB, VINmin = 800mV, VINmax = 1200mV, Figure 1	V_{DD}-0.3		V_{DD}-0.2	V
VIN	Input Voltage Sensitivity	Measured differentially at TPB, Figure 1, 3.4 Gbps, Clock Pattern	150		1560	mVp-p
RIN	Input resistance	IN+ to V_{DD} and IN- to V_{DD}	40	50	60	Ohms
RLI	Differential output return loss	100 MHz – 1125 MHz		10		dB
CML Outputs						
VOFF	Standby Output Voltage	Measured DC outputs at TPC, RT = 50Ω when DUT V_{DD} is off with OUT+ and OUT- terminated by RT= 50Ω to AV_{CC}, Figure 2	AV_{CC} - 10		AV_{CC}+ 10	mV

(1) Typical parameters are measured at V_{DD} = 3.3 V, T_A = 25 °C. They are for reference purposes, and are not production-tested.
(2) Parameter is ensured by statistical analysis and/or design.

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Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified. All parameters are ensured by test, statistical analysis, or design unless otherwise specified(1).

Symbol	Parameter	Condition	Min	Typ	Max	Units
VO	Differential Output voltage swing	External resistor = 24 kΩ at VOD_CRL pin.Measured differentially with OUT+ and OUT- terminated by RT=50Ω to AV_{CC}, Figure 2	800		1200	mVp-p
VOCM	Output common-mode Voltage	Measured single-ended, >1.65 Gbps, Figure 2, Figure 3	AV_{CC}- 0.35		AV_{CC}- 0.20	V
tR, tF	Transition time	20% to 80% of differential output voltage, measured within 1" from output pins, Figure 3		80		ps
tCCSK	Inter Pair Data Channel-to-Channel Skew (all 3 data channels)	Difference in 50% crossing between channels 3.4 Gbps, Clock Pattern(2)		2	3	ps
tPPSK	Inter Pair Data Channels Part-toPart Skew	Difference in 50% crossing between channels of any two devices 3.4 Gbps, Clock Pattern		50		ps
tDD	Data Channels Latency	3.4 Gbps, Clock Pattern, Figure 4		520		ps
tCD	Clock Channel Latency	3.4 Gbps, Clock Pattern, Figure 4		600		ps
LVCMOS Outputs						
tSL	SD to LOCK time	Figure 4		10		ms
Bit Rate						
fCLK	Clock Frequency	Clock Path(3)	25		340	MHz
bR	Bit Rate	Data Paths(3)	0.25		3.4	Gbps
Data Channel Random Jitter						
RJ	Random Jitter	See(3)(4)(5)(6)		3		psrms
Data Channel CDR Jitter Generation						
TROJ1	Total Output Jitter 0.25 Gbps	Data Paths, measured at TPC PRBS7, EQ [2:0] = 000 Figure 1(3)(4)(5)		0.03	0.05	UIp-p
TROJ2	Total Output Jitter 1.65 Gbps	Data Paths, measured at TPC PRBS7, EQ [2:0] = 000 Figure 1(3)(4)(5)		0.08	0.14	UIp-p
TROJ3	Total Output Jitter 2.25 Gbps	Data Paths, measured at TPC PRBS7, EQ [2:0] = 000 Figure 1(3)(4)(5)		0.09	0.16	UIp-p
TROJ4	Total Output Jitter 3.4 Gbps	Data Paths, measured at TPC PRBS7, EQ [2:0] = 000 Figure 1(3)(4)(5)		0.10	0.17	UIp-p
BWLOOP	CDR Loop Bandwidth	0.25 Gbps data rate		0.25		MHz
		1.65 Gbps data rate		1.65		MHz
		2.25 Gbps data rate		2.25		MHz
		3.4 Gbps data rate		2.25		MHz

(3) Parameter is ensured by statistical analysis and/or design.
(4) Deterministic jitter is measured at the differential outputs (TPC of Figure 1), minus the deterministic jitter before the test channel (TPA of Figure 1). Random jitter is removed through the use of averaging or similar means.
(5) Total Jitter is defined as peak-to-peak deterministic jitter from + 12 times random jitter (ps).
(6) Random jitter contributed by the equalizer is defined as sq rt ($J_{OUT}^2 - J_{IN}^2$). J_{OUT} is the random jitter at equalizer outputs in ps-rms, see TPC of Figure 1; J_{IN} is the random jitter at the input of the equalizer in ps-rms, see TPA of Figure 1.

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Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified. All parameters are ensured by test, statistical analysis, or design unless otherwise specified(1).

Symbol	Parameter	Condition	Min	Typ	Max	Units
Clock Channel PLL Jitter Generation						
TROJ5	Total Output Jitter 25 MHz	Clock Path, measured at TPC Figure 1 (7)(8)(9)		0.03	0.045	UIp-p
TROJ6	Total Output Jitter 165 MHz	Clock Path, measured at TPC Figure 1 (7)(8)(9)		0.07	0.13	UIp-p
TROJ7	Total Output Jitter 225 MHz	Clock Path, measured at TPC Figure 1 (7)(8)(9)		0.08	0.135	UIp-p
TROJ8	Total Output Jitter 340 MHz	Clock Path, measured at TPC Figure 1 (7)(8)(9)		0.09	0.14	UIp-p

(7) Parameter is ensured by statistical analysis and/or design.
(8) Deterministic jitter is measured at the differential outputs (TPC of Figure 1), minus the deterministic jitter before the test channel (TPA of Figure 1). Random jitter is removed through the use of averaging or similar means.
(9) Total Jitter is defined as peak-to-peak deterministic jitter from + 12 times random jitter (ps).

Setup and Timing Diagrams

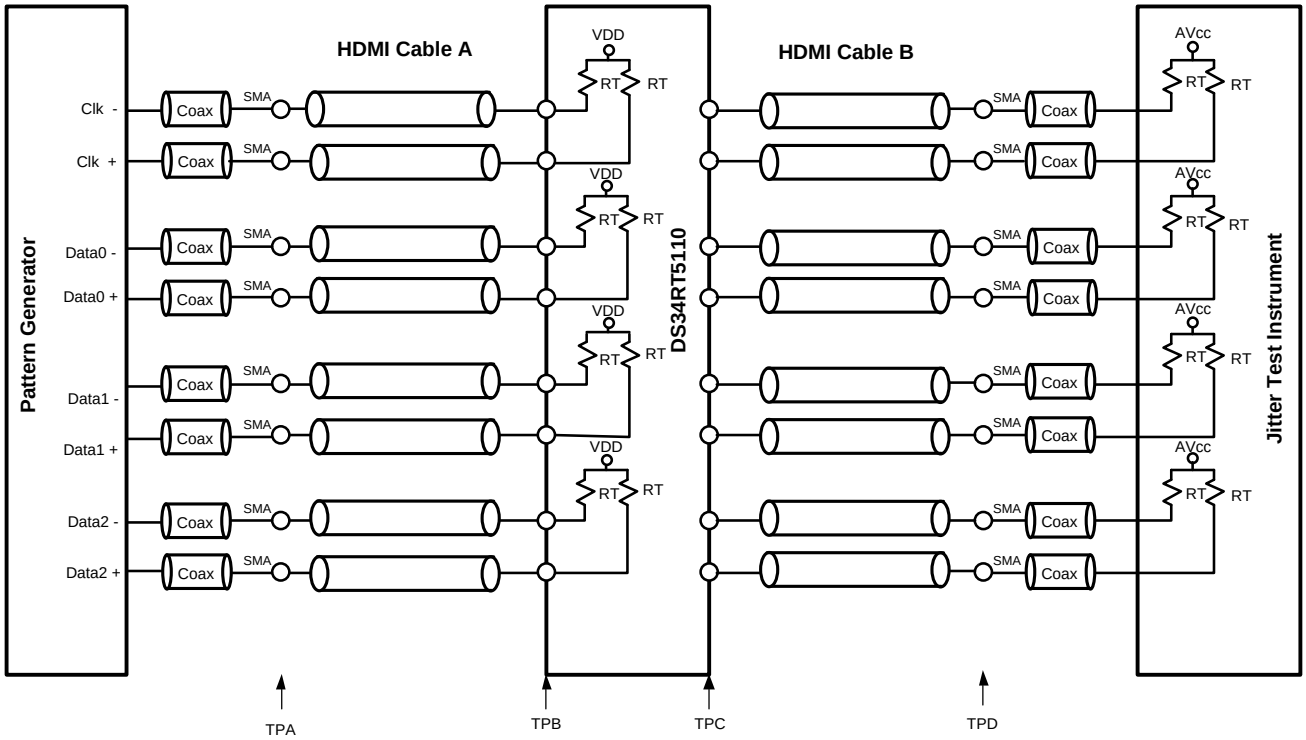

Figure 1. Test Setup Diagram

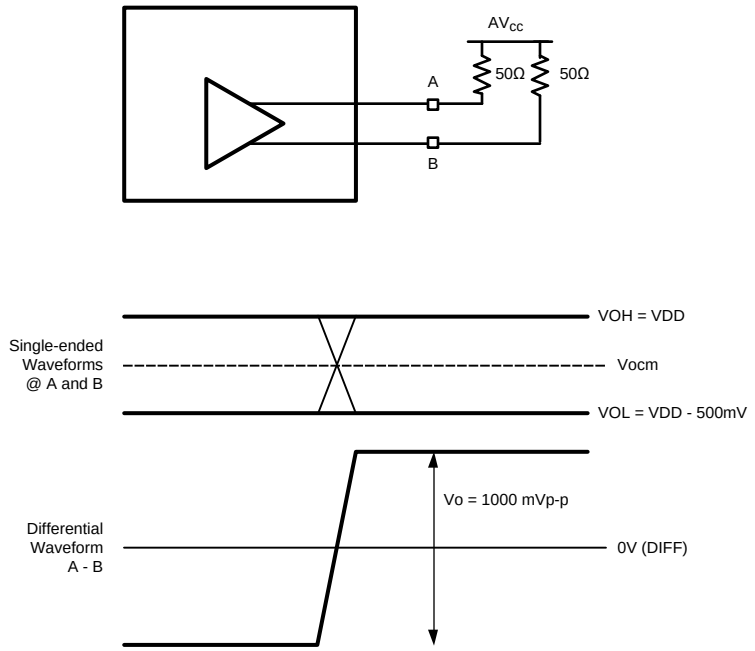

Figure 2. CML Output Swings at A/B (VOD_CRL = 24 kΩ)

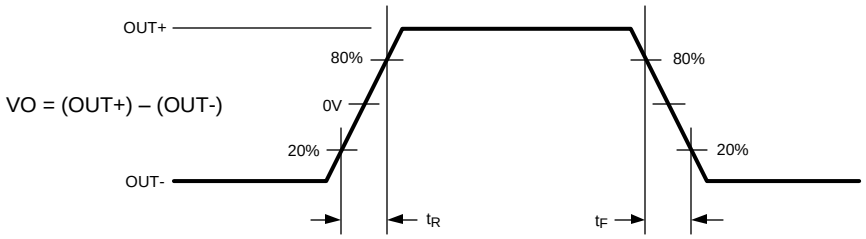

Figure 3. CML Output Transition Times

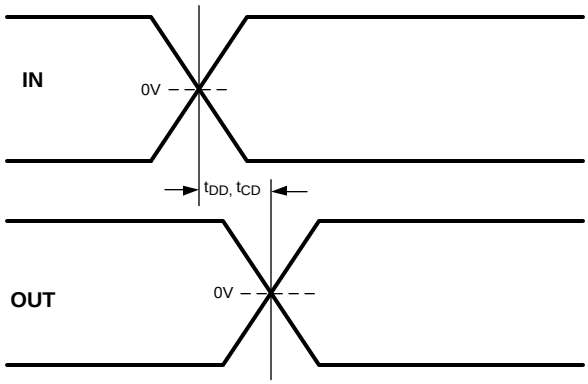

Figure 4. CML Latency Delay Time

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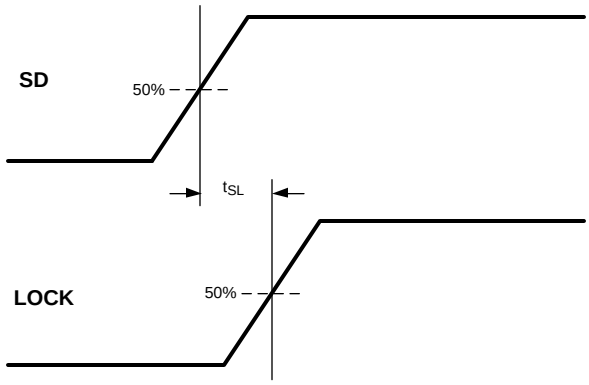

Figure 5. SD – LOCK Delay Time

Functional Description

The DS34RT5110 DVI, HDMI Retimer with Input Equalization and Output De-Emphasis consists of three data channels and a clock channel. Each data channel consists of a TMDS compatible receiver with a power efficient equalizer, a dedicated clock-data recovery (CDR) unit, and a TMDS compatible transmitter.

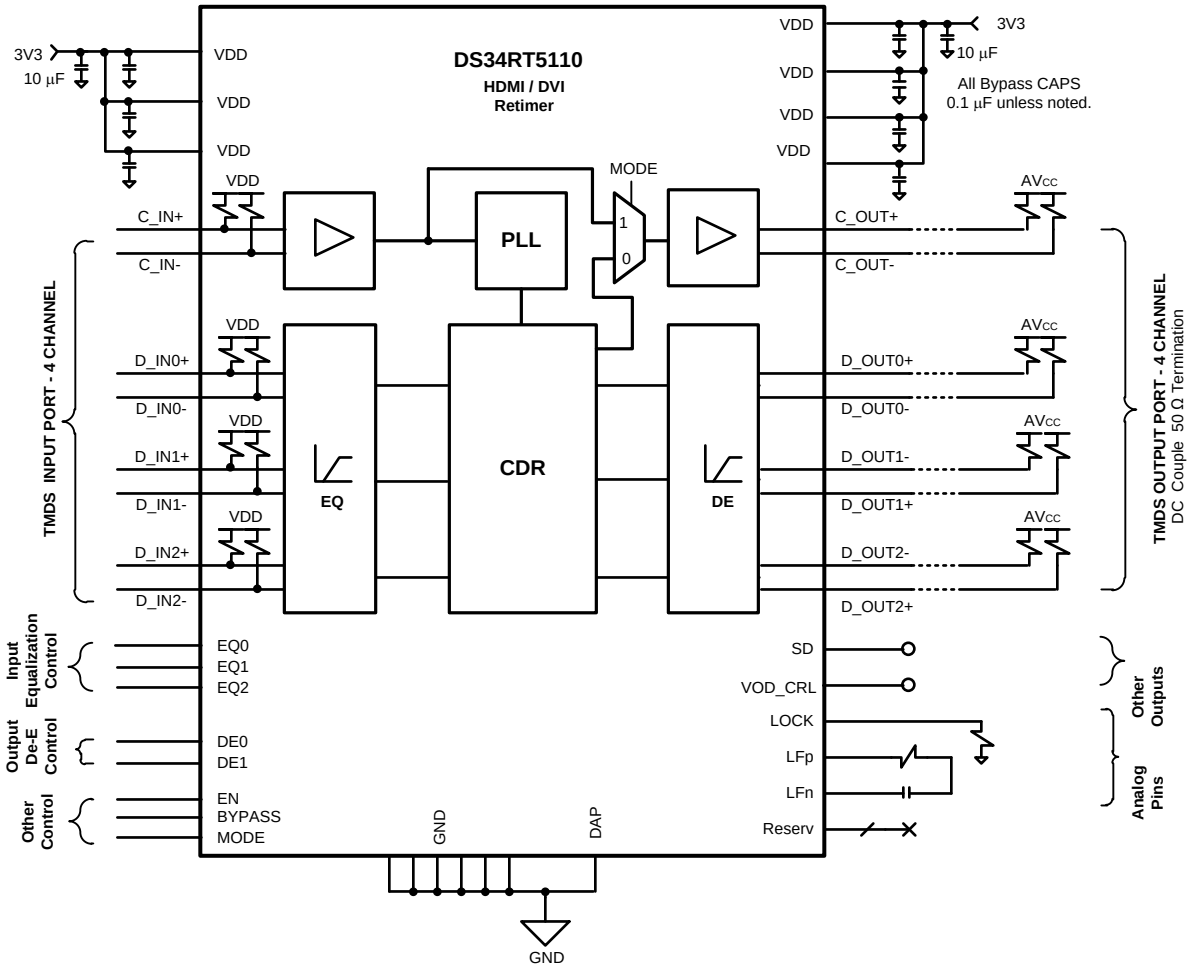

Figure 6. Block Diagram

PHASE-LOCKED-LOCKED LOOP (PLL)

The clock channel has a high-performance PLL that creates a low jitter sampling clock for the clock and data recovery units in the data channels. An external loop filter, composed of 2.2 nF (+ 5% tolerance) capacitor and a 3.3 kΩ (+ 5% tolerance) resistor in series, are required between the LFp and the LFn pins.

CLOCK-DATA RECOVERY UNIT (CDR)

Each TMDS data channel has a CDR that operates independently from other TMDS data channels. Each CDR aligns the sampling clock edges by digitally interpolating the clock from PLL of the TMDS clock channel. The device is designed to connect to DVI/HDMI compatible transmitter and receiver at any data rate between 250 Mbps to 3.4 Gbps. The loop bandwidth of the CDR is approximately baud_rate/1000, i.e. 2.25 MHz for 2.25 Gbps data.

INPUT EQUALIZATION

The input data channel equalizers support eight programmable levels of equalization boost Table 1 by the EQ pins (EQ [2:0]). The range of boost settings provided enables the DS34RT5110 to address a wide range of transmission line path loss scenarios, enabling support for a variety of data rates and formats. See Application Information for recommended EQ settings.

OUTPUT DE-EMPHASIS

De-emphasis is the conditioning function for use in compensating against backplane and cable transmission loss. The DS34RT5110 provides four steps of de-emphasis ranging from 0, 3, 6 and 9 dB, user-selectable dependent on the loss profile of output channels. Table 2 shows the De-emphasis control with default VO = 1000 mVp-p, and Figure 7 shows a driver de-emphasis waveform.

OUTPUT VO CONTROL

Output differential voltage (VO) is controlled through VOD_CRL pin ties an external resistor to the ground as shown in Table 3. Users should restrict the external resistor values used to be 12 kΩ to 24 kΩ. +5% tolerance is recommended.

Table 1. Equalization Control

INPUTS			RESULT
EQ2	EQ1	EQ0	Equalization in dB (1.7 GHz)
0	0	0	0 (default)
0	0	1	10
0	1	0	16
0	1	1	19
1	0	0	23
1	0	1	25
1	1	0	26
1	1	1	27

Table 2. De-Emphasis Control

INPUTS		RESULT	
DE1	DE0	VO De-Emphasis level in mVp-p (VODE w/VOD_CRL = 24 kΩ	VO De-Emphasis in dB
0	0	1000 (default)	0 (default)
0	1	710	-3
1	0	500	-6
1	1	355	-9

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Table 3. VO Control

External Resistor Value (VOD_CRL pin)	Applications	VO Level (mVp-p)
24 kΩ	DC Coupled	1000
12 kΩ	AC Coupled	1000

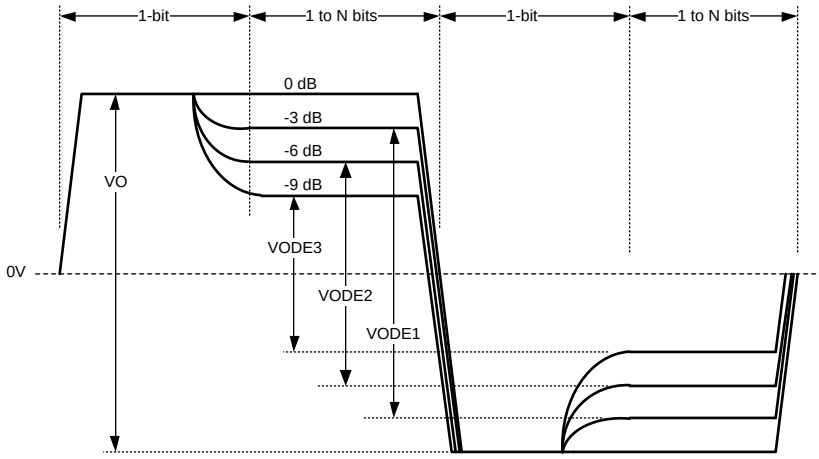

Figure 7. Output De-Emphasis Differential Waveform (showing all de-emphasis steps)

RETIMING AND DE-EMPHASIS BYPASS

The retiming and De-emphasis BYPASS pin provides the flexibility to configure the device to an equalizer only mode. The device is in normal operation, when holding a LOW state on the BYPASS pin. The retiming and De-emphasis features are disabled, when a HIGH state is applied.

CLOCK CHANNEL MODE CONTROL

During the normal operation mode, the clock channel signal is regenerated by the PLL and the CDR. Holding a LOW state (default) on the MODE pin places the DS34RT5110 in this normal operation mode. A HIGH state on the MODE pin bypasses the clock channel. This clock channel mode feature enables the multi-hop applications. (Refer to Multiple Hop Application for detailed information)

DEVICE STATE AND ENABLE CONTROL

The DS34RT5110 has an Enable feature which provides the ability to control device power consumption. This feature can be controlled via the Enable Pin (EN Pin). If Enable is activated, the data channels and clock channel are placed in the ACTIVE state and all device blocks function as described. The DS34RT5110 can also be placed in STANDBY mode to save power. In this mode, the output drivers of the device are disabled. The CML outputs are in the HIGH (AVCC) state. All LVCMOS outputs are in the HiZ state.

LOCK DETECT

When the PLL of the DS34RT5110 is locked, and the generated reference phases are successfully interpolated by the CDR, this status is indicated by a logic HIGH on the LOCK pin. The LOCK pin may be connected to the Enable (EN) pin input to disable the data channels and clock channel when no data signal is being received.

SIGNAL DETECT

The DS34RT5110 features a signal detect circuit on all channels. The status of the input signals can be determined by the state of the SD pin. A logic HIGH indicates the presence of signals that have exceeded a specified maximum threshold value (called SD_ON) on all channels. A logic LOW means that the signals have fallen below a minimum threshold value (called SD_OFF) on one or more channels.

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AUTOMATIC ENABLE FEATURE

During normal operation (i.e. BYPASS pin is LOW), the DS34RT5110 can be configured to automatically enter STANDBY mode, if the PLL of the DS34RT5110 is not locked. The STANDBY mode can be implemented by connecting the LOCK DETECT (LOCK) pin to the external (LVCMOS) Enable (EN) pin. If the LOCK pin is connected to the EN pin, a logic HIGH on the LOCK pin will enable the device; thus the DS34RT5110 will automatically enter the ACTIVE state. If the PLL is unlocked, then the LOCK pin will be asserted LOW, causing the aforementioned blocks to be placed in the STANDBY state.

APPLICATION INFORMATION

The DS34RT5110 is a DVI/HDMI video signal reconditioning device. The device conforms to DVI v1.0 and HDMI v1.3a standards supporting up to 10.2 Gbps total throughput TMDS data for 1080p with 48 bit deep color depth.

TYPICAL APPLICATION

In general, the DS34RT5110 in the default mode (MODE = L) is used as a DVI/HDMI source device, sink device, or a repeater device, see Figure 8. As the source device, the output de-emphasis setting should be configured based on the driving cable length. When used as the sink device, the levels of the equalization boost of the input data channels should be optimized based on the receiving cable length. The DS34RT5110 can also be used as a repeater in an external extender box with the equalization and de-emphasis level settings optimized to provide the maximum cable reach.

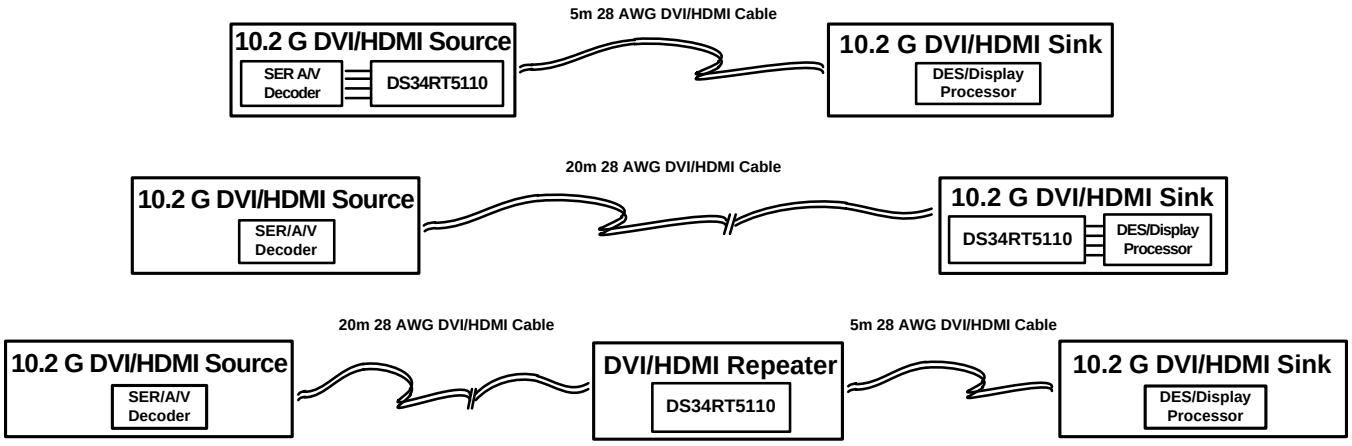

Figure 8. Typical Application Diagram

MULTIPLE HOP APPLICATION

For DVI/HDMI home theater and professional studio systems with extensive lengths of cable, multi-hops with 2 or more cascaded DS34RT5110 devices can be implemented as shown in Figure 9. In order to reach the maximum cable length, the levels of the equalization and de-emphasis should be optimized for each individual hop. The MODE pin(s) of the device at the first hop (using two hop application), or at the first and the second hops (using three hop application shown in Figure 9) is recommended to be set HIGH to minimize the jitter accumulation in multiple hops. The MODE pin of the device for the final hop should be set to a LOW state to clean up the clock jitter, in order to drive the maximum cable length to the Sink.

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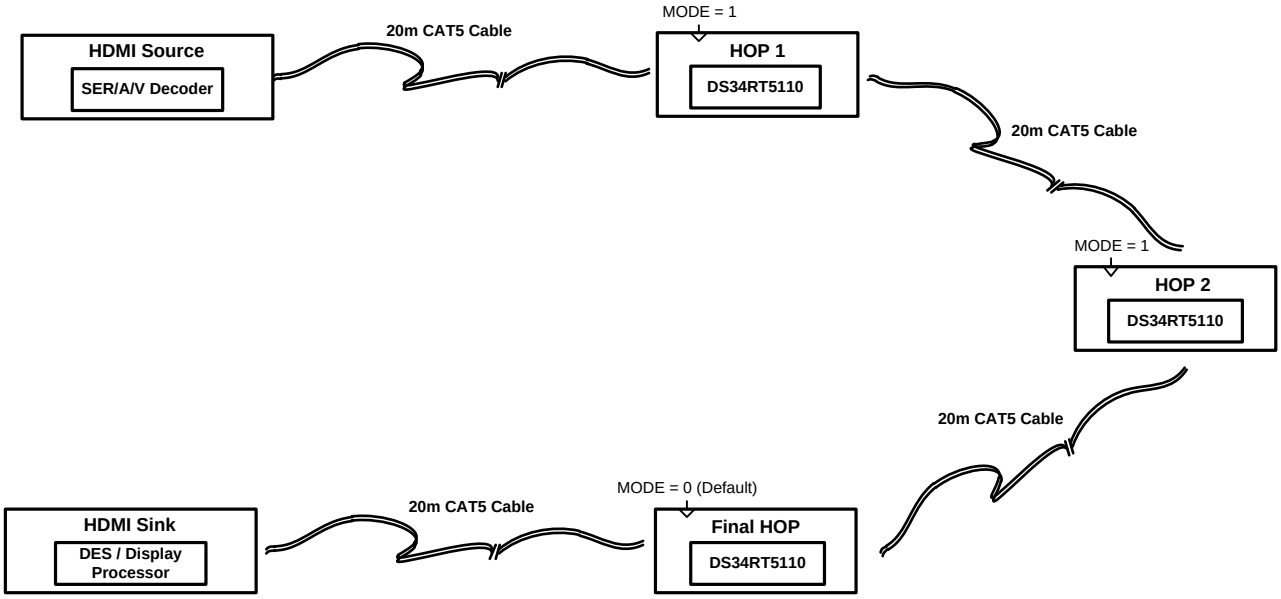

Figure 9. Multiple Hop Systems

MATRIX SWITCH APPLICATION

For the security system with matrix DVI/HDMI switches, the DS34RT5110 is ideal to equalize the long cable reach requirement from the Sources, clean the system jitter due to the complexity of PCB routings, and regenerate clean TMDS signals to the Sinks as shown in Figure 10.

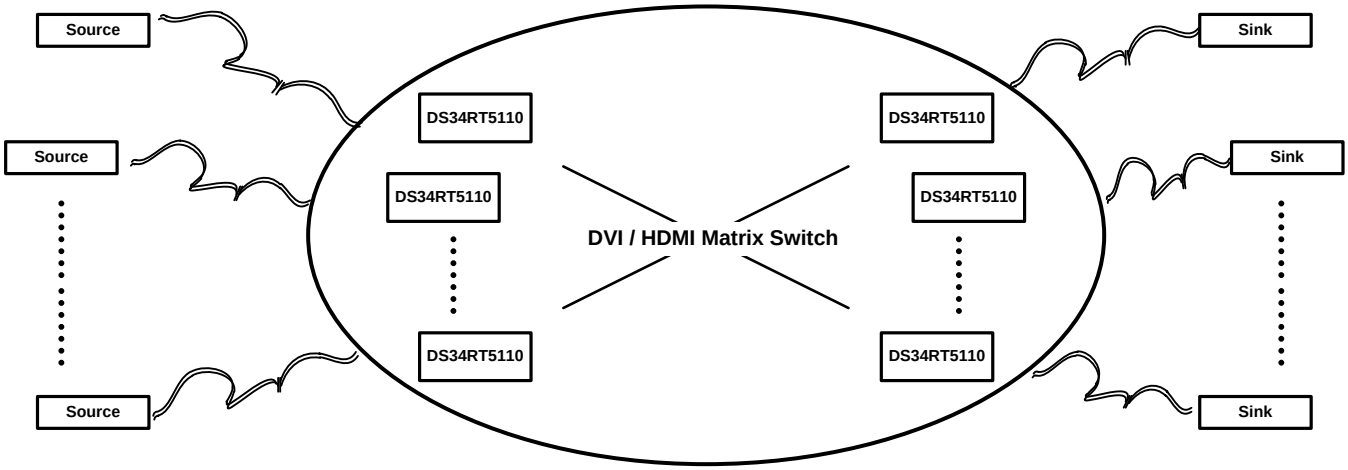

Figure 10. Matrix Switch Systems

DUAL LINK APPLICATION

The DS34RT5110 supports DVI dual link applications requiring ultra-high resolutions for QXGA and WQXGA. Two DS34RT5110 devices are configured as shown in Figure 11. This configuration is only recommended for a single dual link repeater application.

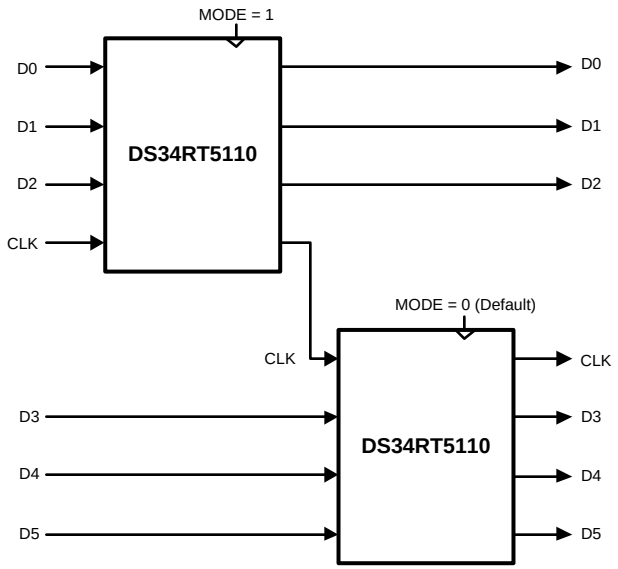

Figure 11. DVI/HDMI Dual Link Application

DC AND AC COUPLED APPLICATIONS

The DS34RT5110 is designed to support TMDS differential pairs with DC coupled transmission lines. It contains integrated termination resistors (50Ω), pulled up to VDD at the input stage, and open collector outputs for DVI / HDMI signaling. Figure 12 shows the DC coupled connection between the HDMI Source (ie. DS34RT5110) and HDMI Sink (ie. DS34RT5110) devices. In the DC coupled application, the external resistance of 24 kΩ at VOD_CRL pin is used at the Source to ensure the VO level of 1000 mVp-p. The AC coupled method connecting between the Source and the Sink devices may be preferred to eliminate the impact of the ground potential difference, or to use one CAT5/6 cable between two chassis. To optimize the DS34RT5110 performance, the external resistance of 12 kΩ at the VOD_CRL pin should be used on the Source DS34RT5110, and a pair of 50 Ω pull-up resistors should be placed close to the outputs of the Source DS34RT5110, in order to DC bias the output driver. Meanwhile, 622Ω pull-down resistors should be placed at the inputs of the Sink DS34RT5110 device, in order to set the input common mode to a 3.05 V. Note AC coupled configuration is not compliant to the HDMI specification of Source requirement (See Figure 13).

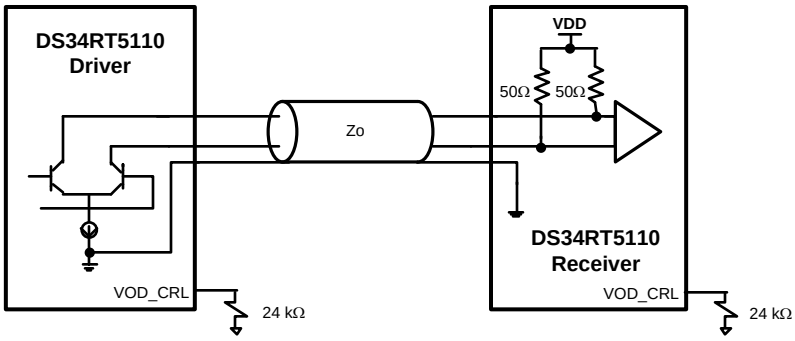

Figure 12. DC Coupled Application

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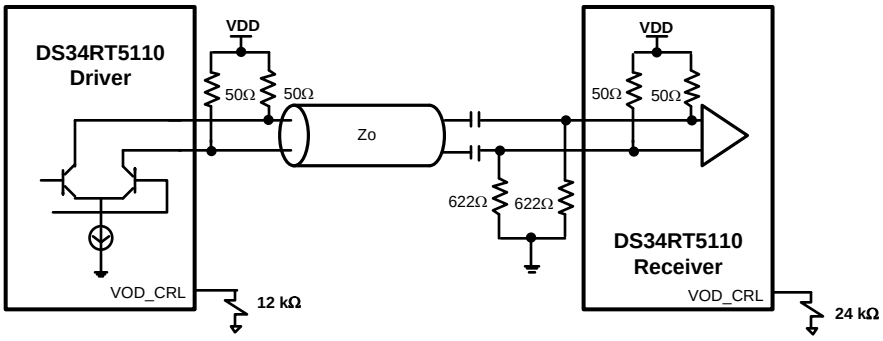

Figure 13. AC Coupled Application

CABLE SELECTION AND INTER-PAIR SKEW

DVI v1.0 and HDMI v1.3a specify Inter-Pair Skew requirements for the system. The DS34RT5110 intends to extend the longer cable reach with STP (DVI / HDMI) cable, or UTP (Cat5 / Cat5e / Cat6) cable, and it does not have a de-skew function to compensate any cable Inter-Pair Skews. Long cable with Inter-Pair Skew exceeding the DVI / HDMI standard limit tolerance could cause system distortion. Therefore, TI suggests the consideration of Inter-Pair Skew budget during the system design, and recommends Low-Skew Video grade cables for cable extending applications.

28 AWG STP (SHIELDED TWIST PAIRS) DVI / HDMI CABLES RECOMMENDED EQ SETTINGS

Table 4 provides the recommended EQ control settings for various data rates and cable lengths for 28 AWG DVI/HDMI compliant configurations. The EQ setting is made via three EQ [2:0] pins.

Table 4. EQ Control Setting for STP Cable

Format (Data Rate)	0 ~ 10m	> 10m
1080P 48-bit (3.4 Gbps)	Setting 0x01	Setting 0x06
1080P 36-bit (2.25 Gbps)	Setting 0x01	Setting 0x06
1080P (1.65 Gbps)	Setting 0x01	Setting 0x06
1080I (750 Mbps)	Setting 0x06	Setting 0x06

24 AWG UTP (LOW SKEW UNSHIELDED TWIST PAIRS) CABLES

The DS34RT5110 can be used to extend the length of low skew grade UTP cables, such as Cat5e and Cat6 to distances greater than 30 meters at 1.65 Gbps with < 0.20 UI of jitter. Note that for non-standard DVI/HDMI cables, the user must ensure the inter pair skew requirements are met. Table 5 shows the recommended EQ control settings for various data rates and cable lengths for UTP configurations.

Table 5. EQ Control Setting for UTP Cable

Format (Data Rate)	0 ~ 10m	> 10m
1080P 48-bit (3.4 Gbps)	Setting 0x01	Setting 0x05
1080P 36-bit (2.25 Gbps)	Setting 0x01	Setting 0x05
1080P (1.65 Gbps)	Setting 0x01	Setting 0x05
1080I (750 Mbps)	Setting 0x05	Setting 0x05

General Recommendations

The DS34RT5110 is a high performance circuit capable of delivering excellent performance. To achieve optimal performance, careful attention must be paid to the details associated with high-speed design as well as providing a clean power supply. Refer to the LVDS Owner's Manual for more detailed information on high-speed design tips as well as many other available resources addressing signal integrity design issues.

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PCB LAYOUT CONSIDERATIONS FOR DIFFERENTIAL PAIRS

The TMDS differential inputs and outputs must have a controlled differential impedance of 100 Ω. It is preferable to route TMDS lines exclusively on one layer of the board, particularly for the input traces. The use of vias should be avoided if possible. If vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair. Route the TMDS signals away from other signals and noise sources on the printed circuit board. All traces of TMDS differential inputs and outputs must be equal in length to minimize intra-pair skew.

WQFN FOOTPRINT RECOMMENDATIONS

See TI application note: AN-1187 *"Leadless Leadframe Package (LLP) Application Report"* (literature number SNOA401) for additional information on WQFN packages footprint and soldering information.

POWER SUPPLY BYPASSING

Two approaches are recommended to ensure the DS34RT5110 is provided with an adequate power supply. First, the supply (VDD) and ground (GND) pins should be connected to power planes routed on adjacent layers of the printed circuit board. The layer thickness of the dielectric should be minimized so the VDD and GND planes create a low inductance supply with distributed capacitance. Second, careful attention to supply bypassing through the proper use of bypass capacitors is required. A 0.1 µF bypass capacitor should be connected to each VDD pin such that the capacitor is placed as close as possible to the DS34RT5110. Smaller body size capacitors can help facilitate proper component placement. Additionally, two capacitors with capacitance in the range of 2.2 µF to 10 µF should be incorporated in the power supply bypassing design as well. These capacitors can be either tantalum or an ultra-low ESR ceramic and should be placed as close as possible to the DS34RT5110.

EQUIVALENT I/O STRUCTURES

Figure 14 shows the DS34RT5110 CML output structure and ESD protection circuitry.

Figure 15 shows the DS34RT5110 CML input structure and ESD protection circuitry.

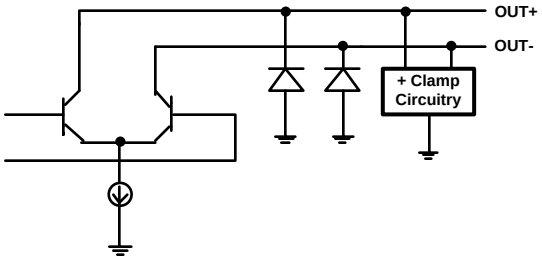

Figure 14. Equivalent Output Structure

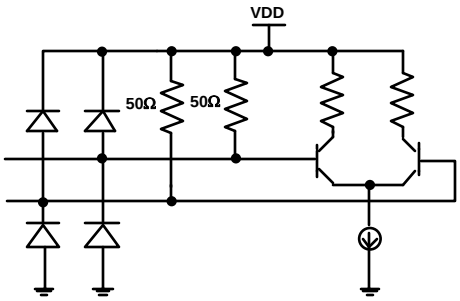

Figure 15. Equivalent Input Structure

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Typical Performance Characteristics as a Repeater

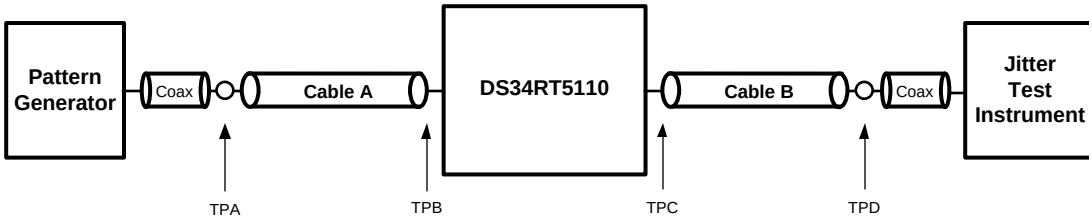

Figure 16. Simplified Test Setup as a Single Repeater

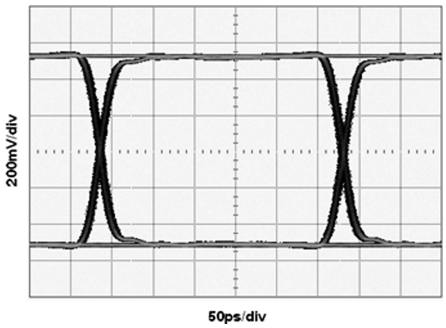

Figure 17. System Source Eye Diagram at TPA (3.4 Gbps)

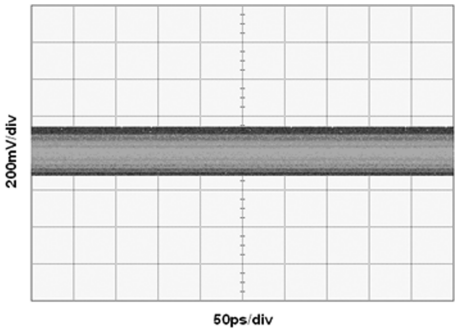

Figure 18. Device Sink Eye Diagram at TPB (3.4 Gbps, Cable A = 20m 28 AWG HDMI)

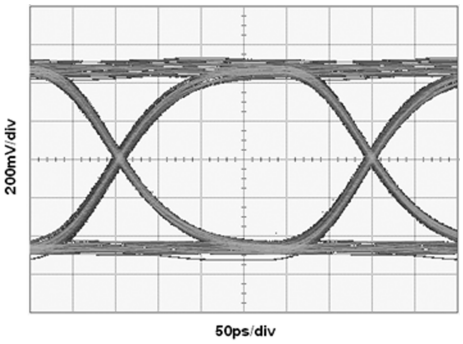

Figure 19. Device Source Eye Diagram at TPC (3.4 Gbps, Cable A = 20m 28 AWG HDMI, EQ = 0x05, BYPASS = 0, DE = 0dB)

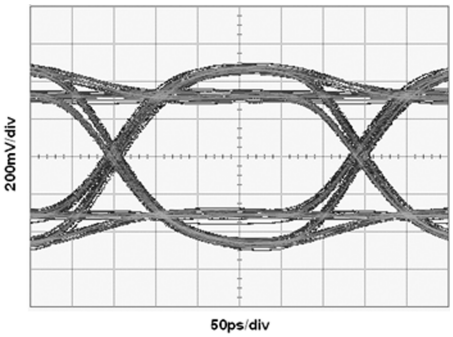

Figure 20. Device Source Eye Diagram at TPC (3.4 Gbps, Cable A = 20m 28 AWG HDMI, EQ = 0x05, BYPASS = 0, DE = -3dB)

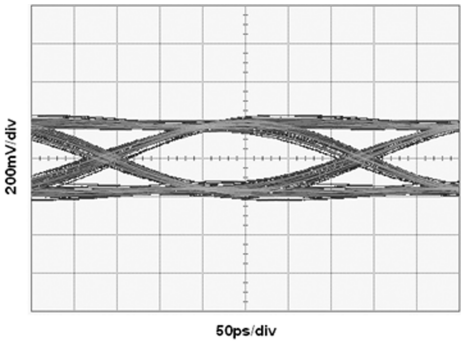

Figure 21. System Sink Eye Diagram at TPD (3.4 Gbps, Cable A = 20m 28 AWG HDMI, Cable B = 5m 28AWG HDMI, EQ = 0x05, BYPASS = 0, DE = -3dB)

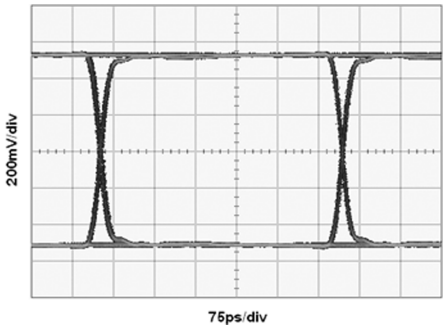

Figure 22. System Source Eye Diagram at TPA (2.25 Gbps)

Typical Performance Characteristics as a Repeater (continued)

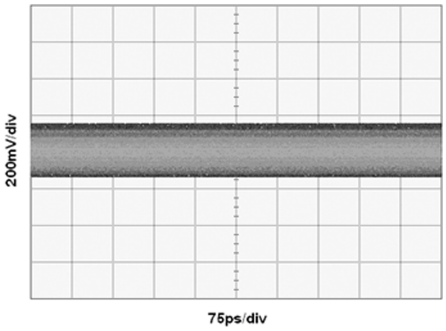

Figure 23. Device Sink Eye Diagram at TPB (2.25 Gbps, Cable A = 25m 28 AWG HDMI)

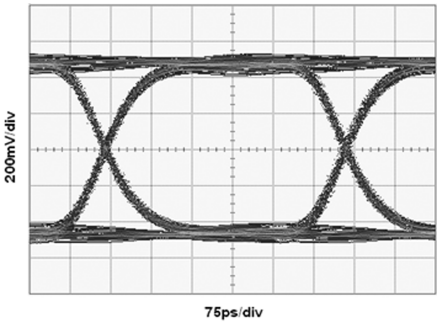

Figure 24. Device Source Eye Diagram at TPC (2.25 Gbps, Cable A = 25m 28 AWG HDMI, EQ = 0x05, BYPASS = 0, DE = 0dB)

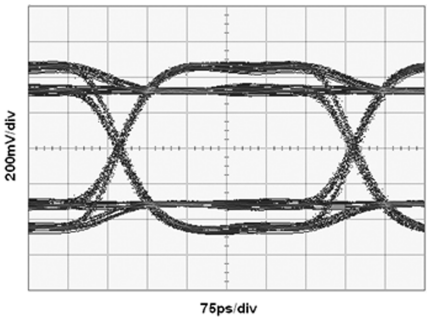

Figure 25. Device Source Eye Diagram at TPC (2.25 Gbps, Cable A = 25m 28 AWG HDMI, EQ = 0x05, BYPASS = 0, DE = -3dB)

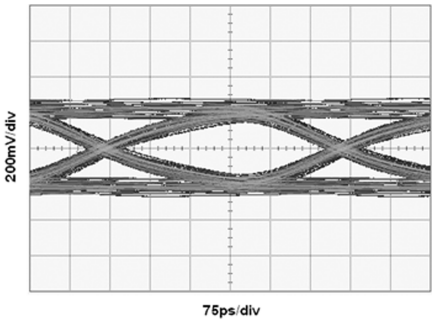

Figure 26. System Sink Eye Diagram at TPD (2.25 Gbps, Cable A = 25m 28 AWG HDMI, Cable B = 7.5m 28AWG HDMI, EQ = 0x05, BYPASS = 0, DE = -3dB)

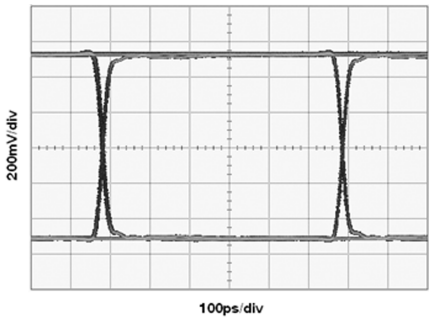

Figure 27. System Source Eye Diagram at TPA (1.65 Gbps)

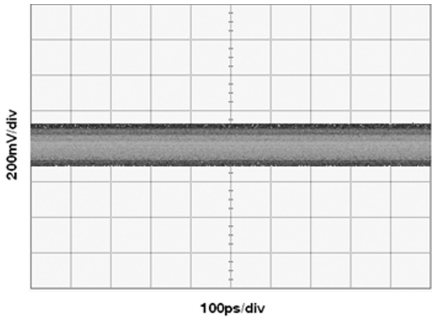

Figure 28. Device Sink Eye Diagram at TPB (1.65 Gbps, Cable A = 35m 28 AWG HDMI)

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Typical Performance Characteristics as a Repeater (continued)

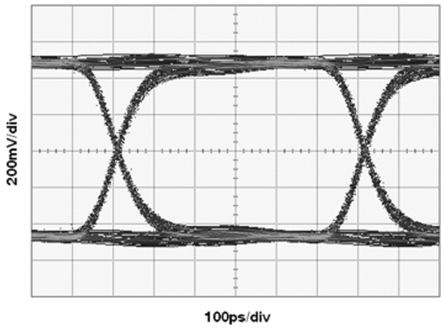

Figure 29. Device Source Eye Diagram at TPC (1.65 Gbps, Cable A = 35m 28 AWG HDMI, EQ = 0x05, BYPASS = 0, DE = 0dB)

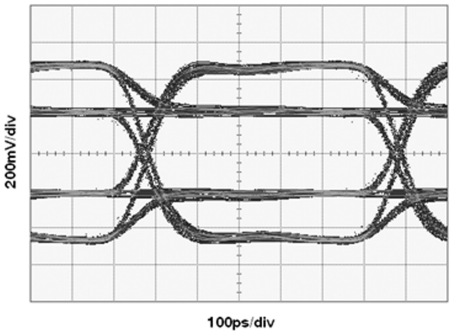

Figure 30. Device Source Eye Diagram at TPC (1.65 Gbps, Cable A = 35m 28 AWG HDMI, EQ = 0x05, BYPASS = 0, DE = -6dB)

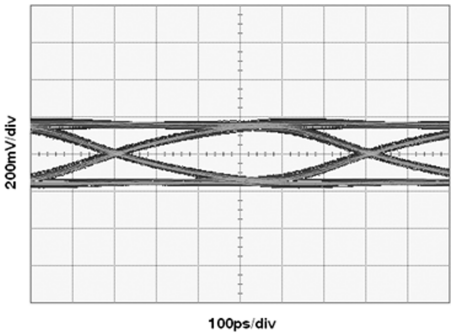

Figure 31. System Sink Eye Diagram at TPD (1.65 Gbps, Cable A = 35m 28 AWG HDMI, Cable B = 10m 28AWG HDMI, EQ = 0x05, BYPASS = 0, DE = -6dB)

REVISION HISTORY

Changes from Revision F (April 2013) to Revision G	Page
• Changed layout of National Data Sheet to TI format	19

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS34RT5110SQ/NOPB	NRND	Production	WQFN (RHS) | 48	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	0 to 70	34RT5110
DS34RT5110SQ/NOPB.A	NRND	Production	WQFN (RHS) | 48	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	0 to 70	34RT5110
DS34RT5110SQE/NOPB	NRND	Production	WQFN (RHS) | 48	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	0 to 70	34RT5110
DS34RT5110SQE/NOPB.A	NRND	Production	WQFN (RHS) | 48	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	0 to 70	34RT5110
DS34RT5110SQX/NOPB	NRND	Production	WQFN (RHS) | 48	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	0 to 70	34RT5110
DS34RT5110SQX/NOPB.A	NRND	Production	WQFN (RHS) | 48	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	0 to 70	34RT5110

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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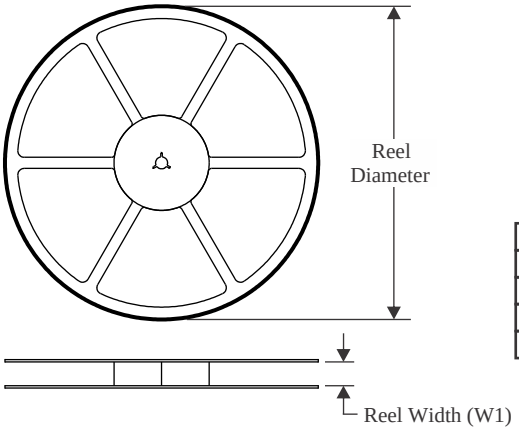
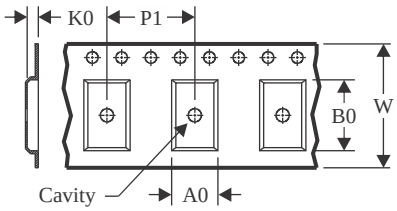
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

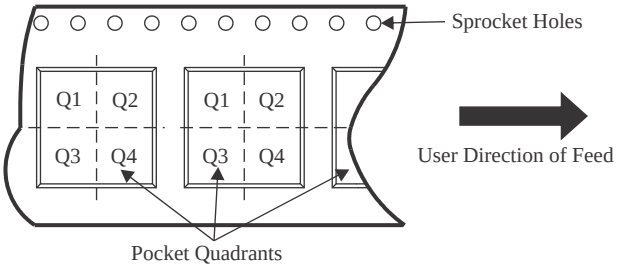


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

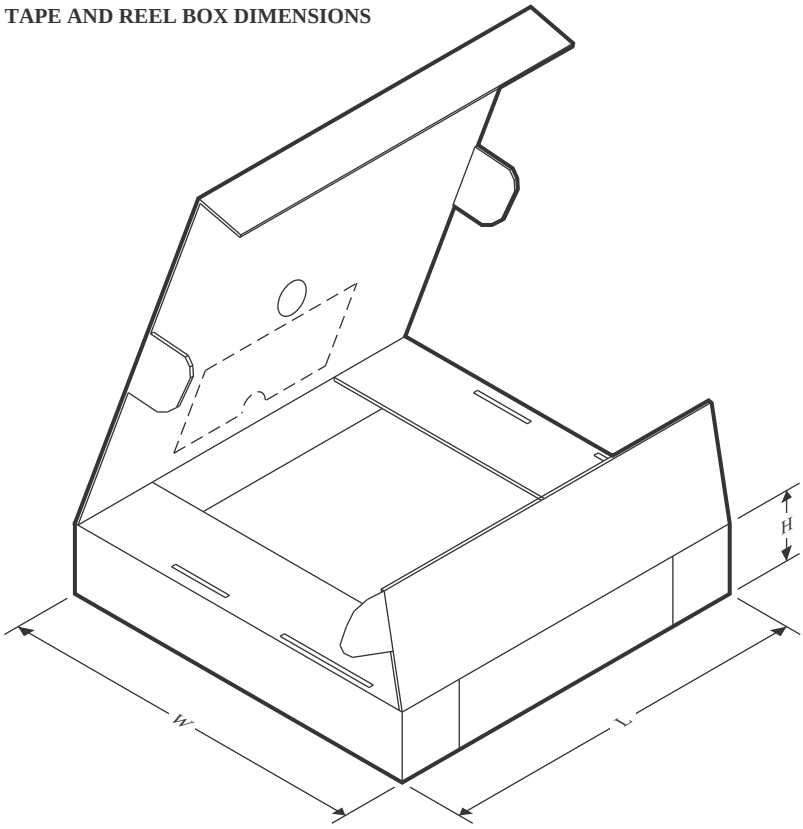
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

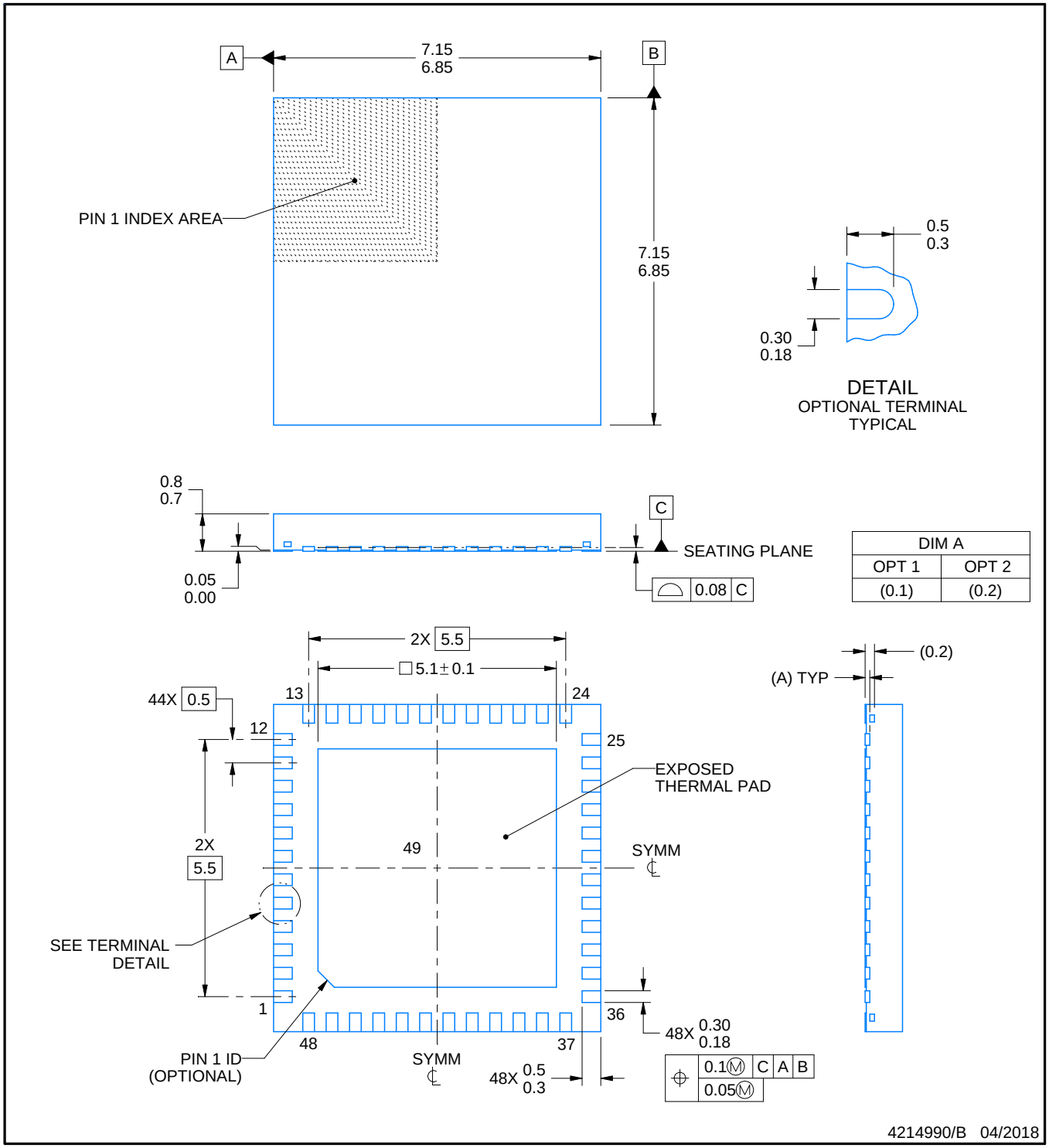
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS34RT5110SQ/NOPB	WQFN	RHS	48	1000	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
DS34RT5110SQE/NOPB	WQFN	RHS	48	250	178.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
DS34RT5110SQX/NOPB	WQFN	RHS	48	2500	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



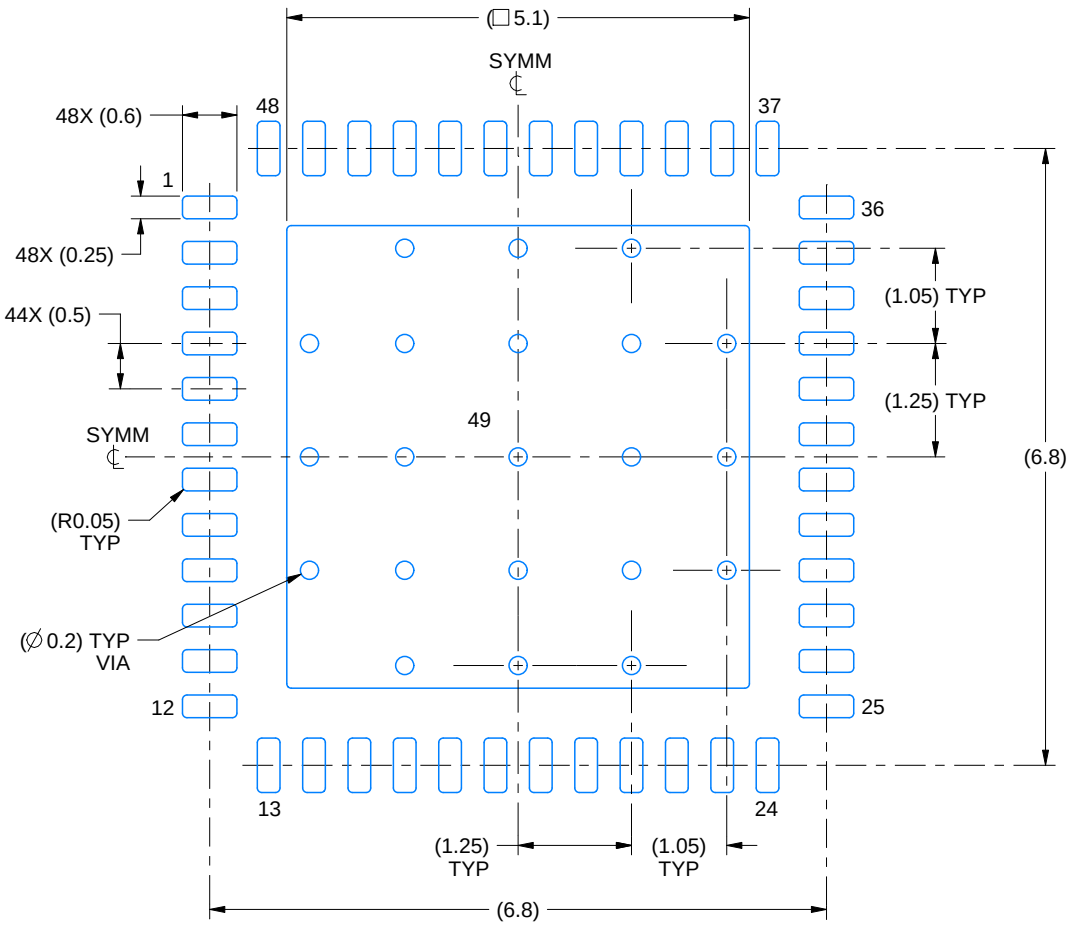
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS34RT5110SQ/NOPB	WQFN	RHS	48	1000	356.0	356.0	36.0
DS34RT5110SQE/NOPB	WQFN	RHS	48	250	208.0	191.0	35.0
DS34RT5110SQX/NOPB	WQFN	RHS	48	2500	356.0	356.0	36.0

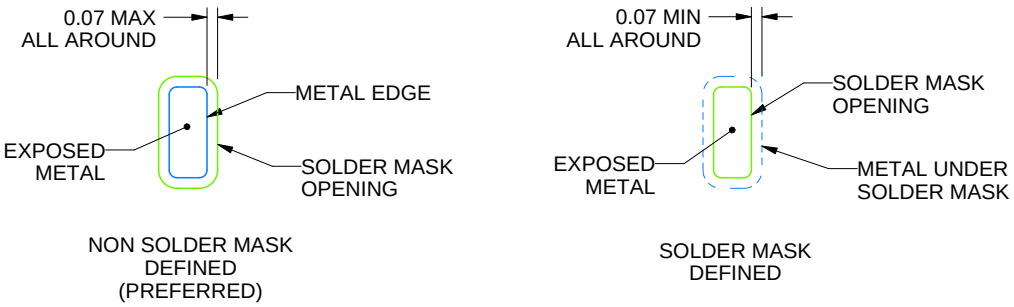


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X

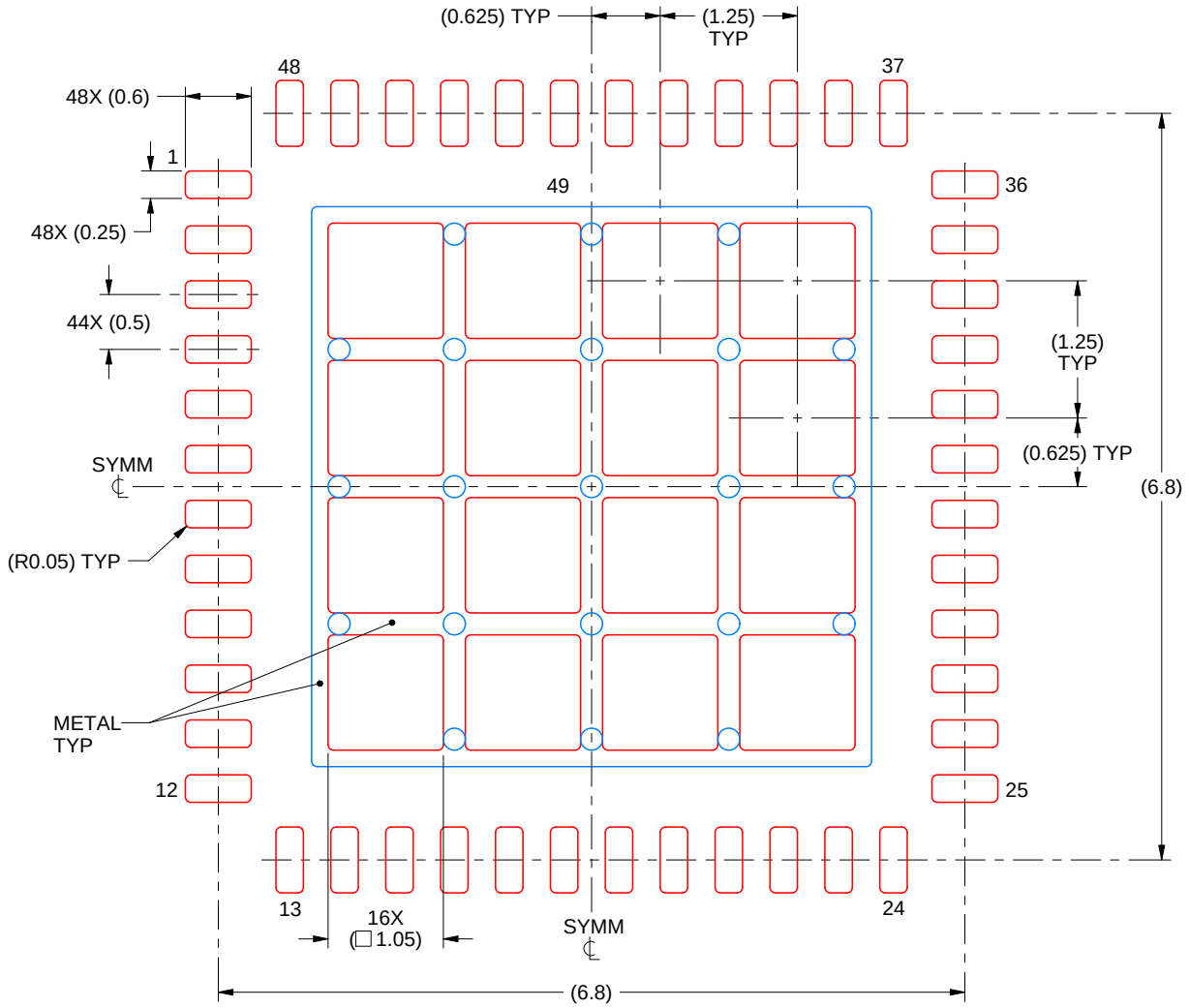


SOLDER MASK DETAILS

4214990/B 04/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
68% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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