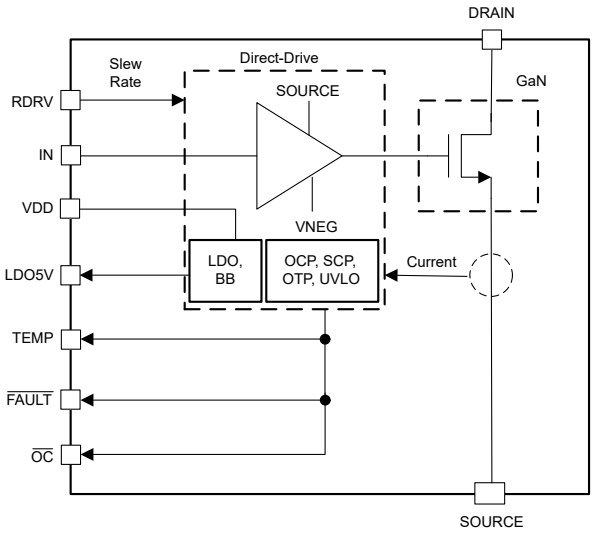
LMG3425R050 600V 50mΩ GaN FET With Integrated Driver, Protection, and Temperature Reporting

1 Features

- Qualified for JEDEC JEP180 for hard-switching topologies
- 600V GaN-on-Si FET with integrated gate driver
  - Integrated high precision gate bias voltage
  - 200V/ns FET hold-off
  - 3.6MHz switching frequency
  - 20V/ns to 150V/ns slew rate for optimization of switching performance and EMI mitigation
  - Operates from 7.5V to 18V supply
- Robust protection
  - Cycle-by-cycle overcurrent and latched short-circuit protection with < 100ns response
  - Withstands 720V surge while hard-switching
  - Self-protection from internal overtemperature and UVLO monitoring
- Advanced power management
  - Digital temperature PWM output
  - Ideal diode mode reduces third-quadrant losses

2 Applications

- Switch-mode power converters
- Merchant network and server PSU
- Merchant telecom rectifiers
- Solar inverters and industrial motor drives
- Uninterruptible power supplies



Simplified Block Diagram

3 Description

The LMG3425R050 GaN FET with integrated driver and protection is targeted at switch-mode power converters and enables designers to achieve new levels of power density and efficiency.

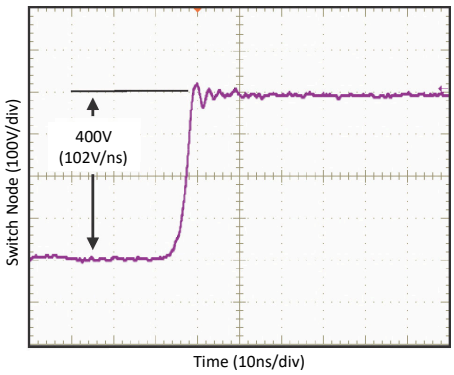
The LMG3425R050 integrates a silicon driver that enables switching speed up to 150V/ns. TI's integrated precision gate bias results in higher switching SOA compared to discrete silicon gate drivers. This integration, combined with TI's low-inductance package, delivers clean switching and minimal ringing in hard-switching power supply topologies. Adjustable gate drive strength allows control of the slew rate from 20V/ns to 150V/ns, which can be used to actively control EMI and optimize switching performance.

Advanced power management features include digital temperature reporting, fault detection, and ideal diode mode. The temperature of the GaN FET is reported through a variable duty cycle PWM output, which simplifies managing device loading. Faults reported include overcurrent, short-circuit, overtemperature, VDD UVLO, and high-impedance RDRV pin. Ideal diode mode reduces third-quadrant losses by enabling dead-time control.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LMG3425R050	RQZ (VQFN, 54)	12.00mm × 12.00mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information* section.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Switching Performance at > 100V/ns

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4 Pin Configuration and Functions

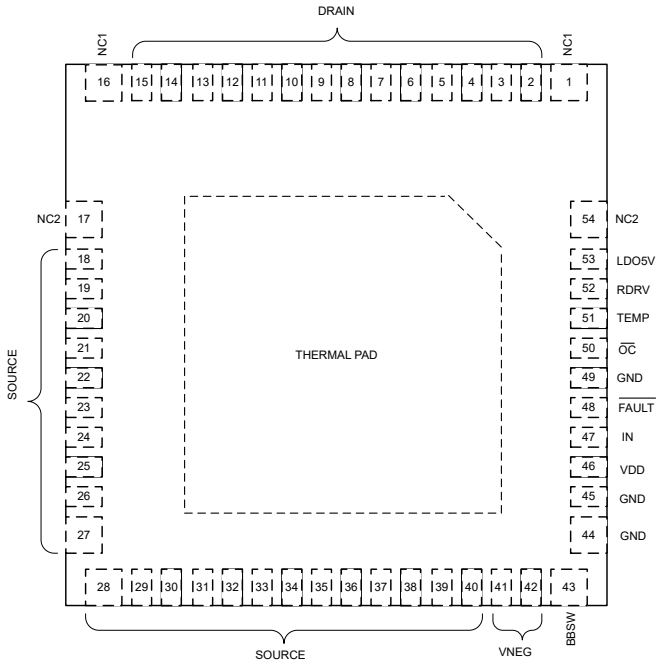

Figure 4-1. RQZ Package, 54-Pin VQFN (Top View)

Table 4-1. Pin Functions

PIN		TYPE[(1)]	DESCRIPTION
NAME	NO.		
NC1	1, 16	—	Used to anchor QFN package to PCB. Pins must be soldered to PCB landing pads. The PCB landing pads are non-solder mask defined pads and must not be physically connected to any other metal on the PCB. Internally connected to DRAIN.
DRAIN	2–15	P	GaN FET drain. Internally connected to NC1.
NC2	17, 54	—	Used to anchor QFN package to PCB. Pins must be soldered to PCB landing pads. The PCB landing pads are non-solder mask defined pads and must not be physically connected to any other metal on the PCB. Internally connected to SOURCE, GND, and THERMAL PAD.
SOURCE	18–40	P	GaN FET source. Internally connected to GND, NC2, and THERMAL PAD.
VNEG	41–42	P	Internal buck-boost converter negative output. Used as the negative supply to turn off the depletion mode GaN FET. Bypass to ground with a 2.2μF capacitor.
BBSW	43	P	Internal buck-boost converter switch pin. Connect an inductor from this point to ground.
GND	44, 45, 49	G	Signal ground. Internally connected to SOURCE, NC2, and THERMAL PAD.
VDD	46	P	Device input supply.
IN	47	I	CMOS-compatible non-inverting input used to turn the FET on and off.
$\overline{\text{FAULT}}$	48	O	Push-pull digital output that asserts low during a fault condition. Refer to *Fault Detection* for details.
$\overline{\text{OC}}$	50	O	Push-pull digital output that asserts low during overcurrent and short-circuit fault conditions. Refer to *Fault Detection* for details.
TEMP	51	O	Push-pull digital output that gives information about the GaN FET temperature. Outputs a fixed 9kHz pulsed waveform. The device temperature is encoded as the duty cycle of the waveform.
RDRV	52	I	Drive-strength selection pin. Connect a resistor from this pin to GND to set the turn-on drive strength to control slew rate. Tie the pin to GND to enable 150V/ns and tie the pin to LDO5V to enable 100V/ns.
LDO5V	53	P	5V LDO output for external digital isolator.
THERMAL PAD	—	—	Thermal pad. Internally connected to SOURCE, GND, and NC2. The thermal pad can be used to conduct rated device current.

(1) I = input, O = output, P = power, G = ground

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5 Specifications

5.1 Absolute Maximum Ratings

Unless otherwise noted: voltages are respect to GND[1]

			MIN	MAX	UNIT
V_{DS}	Drain-source voltage, FET off			600	V
$V_{DS(surge)}$	Drain-source voltage, FET switching, surge condition[2]			720	V
$V_{DS(tr)(surge)}$	Drain-source transient ringing peak voltage, FET off, surge condition[2] [3]			800	V
	Pin voltage	VDD	–0.3	20	V
		LDO5V	–0.3	5.5	V
		VNEG	–16	0.3	V
		BBSW	V_{VNEG}–1	V_{VDD}+0.5	V
		IN	–0.3	20	V
		$\overline{FAULT}$, $\overline{OC}$, TEMP	–0.3	V_{LDO5V}+0.3	V
		RDRV	–0.3	5.5	V
$I_{D(RMS)}$	Drain RMS current, FET on			44	A
$I_{D(pulse)}$	Drain pulsed current, FET on, tp < 10µs[4]		–96	Internally Limited	A
$I_{S(pulse)}$	Source pulsed current, FET off, tp < 1µs			60	A
T_J	Operating junction temperature[5]		–40	150	°C
T_{stg}	Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) See Section 7.3.3 for an explanation of the switching cycle drain-source voltage ratings.
(3) t1 < 200ns in Figure 7-1.
(4) The positive pulsed current must remain below the overcurrent threshold to avoid the FET being automatically shut off. The FET drain intrinsic positive pulsed current rating for t_p < 10µs is 96A.
(5) Refer to the Electrical and Switching Characteristics Tables for junction temperature test conditions.

5.2 ESD Ratings

PARAMETER			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Unless otherwise noted: voltages are respect to GND, SOURCE connected to GND

			MIN	NOM	MAX	UNIT
	Supply voltage	VDD (Maximum switching frequency derated for V_{VDD} < 9V)	7.5	12	18	V
	Input voltage	IN	0	5	18	V
$I_{D(RMS)}$	Drain RMS current				32	A
	Positive source current	LDO5V			25	mA
R_{RDRV}	RDRV to GND resistance from external slew-rate control resistor		0		500	kΩ
C_{VNEG}	VNEG to GND capacitance from external bypass capacitor		1		10	uF

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5.3 Recommended Operating Conditions (continued)

Unless otherwise noted: voltages are respect to GND, SOURCE connected to GND

		MIN	NOM	MAX	UNIT
L_{BBSW}	BBSW to GND inductance from external buck-boost inductor [(1)]	3	4.7	10	uH

(1) > 1A current rating is recommended.

5.4 Thermal Information

THERMAL METRIC[(1)]		LMG342xR050 RQZ (VQFN) 54 PINS	UNIT
$R_{\theta JC(bot,avg)}$	Junction-to-case (bottom) average thermal resistance	0.88	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

Unless otherwise noted: voltage, resistance, capacitance, and inductance are respect to GND; –40°C ≤ T_J ≤ 125°C; V_{DS} = 480V; 9V ≤ V_{VDD} ≤ 18V; V_{IN} = 0V; RDRV connected to LDO5V; L_{BBSW} = 4.7µH

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GAN POWER TRANSISTOR						
$R_{DS(on)}$	Drain-source on resistance	V_{IN} = 5V, T_J = 25°C		43	55	mΩ
		V_{IN} = 5V, T_J = 125°C		73		mΩ
V_{SD}	Third-quadrant mode source-drain voltage	I_S = 0.1A		3.8		V
		I_S = 15A	3	5.3		V
I_{DSS}	Drain leakage current	V_{DS} = 600V, T_J = 25°C		1		uA
		V_{DS} = 600V, T_J = 125°C		7		uA
C_{OSS}	Output capacitance	V_{DS} = 400V		110		pF
$C_{O(er)}$	Energy related effective output capacitance	V_{DS} = 0V to 400V		155		pF
$C_{O(tr)}$	Time related effective output capacitance			235		pF
Q_{OSS}	Output charge			100		nC
Q_{RR}	Reverse recovery charge			0		nC
VDD – SUPPLY CURRENTS						
	VDD quiescent current (LMG3422)	V_{VDD} = 12V, V_{IN} = 0V or 5V		700	1200	uA
	VDD quiescent current (LMG3425)	V_{VDD} = 12V, V_{IN} = 0V or 5V		780	1300	uA
	VDD operating current	V_{VDD} = 12V, f_{IN} = 140kHz, soft-switching		9	10.5	mA
BUCK BOOST CONVERTER						
	VNEG output voltage	VNEG sinking 40mA		–14		V
$I_{BBSW,PK(low)}$	Peak BBSW sourcing current at low peak current mode setting (Peak external buck-boost inductor current)		0.3	0.4	0.5	A
$I_{BBSW,PK(high)}$	Peak BBSW sourcing current at high peak current mode setting (Peak external buck-boost inductor current)		0.8	1	1.2	A
	High peak current mode setting enable – IN positive-going threshold frequency		280	420	515	kHz
LDO5V						

5.5 Electrical Characteristics (continued)

Unless otherwise noted: voltage, resistance, capacitance, and inductance are respect to GND; –40℃ ≤ T_J ≤ 125℃; V_{DS} = 480V; 9V ≤ V_{VDD} ≤ 18V; V_{IN} = 0V; RDRV connected to LDO5V; L_{BBSW} = 4.7µH

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Output voltage	LDO5V sourcing 25mA	4.75	5	5.25	V
	Short-circuit current		25	50	100	mA
IN						
$V_{IN,IT+}$	Positive-going input threshold voltage		1.7	1.9	2.45	V
$V_{IN,IT-}$	Negative-going input threshold voltage		0.7	1	1.3	V
	Input threshold hysteresis		0.7	0.9	1.3	V
	Input pulldown resistance	V_{IN} = 2V	100	150	200	kΩ
$\overline{FAULT}$, $\overline{OC}$, TEMP – OUPUT DRIVE						
	Low-level output voltage	Output sinking 8mA		0.16	0.4	V
	High-level output voltage	Output sourcing 8mA, Measured as $V_{LDO5V} – V_O$		0.2	0.45	V
VDD, VNEG – UNDER VOLTAGE LOCKOUT						
$V_{VDD,T+}$ (UVLO)	VDD UVLO – positive-going threshold voltage		6.5	7	7.5	V
	VDD UVLO – negative-going threshold voltage		6.1	6.5	7	V
	VDD UVLO – Input threshold voltage hysteresis			510		mV
	VNEG UVLO – negative-going threshold voltage		–13.6	–13.0	–12.3	V
	VNEG UVLO – positive-going threshold voltage		–13.2	–12.75	–12.1	V
GATE DRIVER						
	Turn-on slew rate	From V_{DS} < 320V to V_{DS} < 80V, RDRV disconnected from LDO5V, R_{RDRV} = 300kΩ, T_J = 25℃, V_{BUS} = 400V, L_{HB} current = 10A, see Figure 6-1		20		V/ns
		From V_{DS} < 320V to V_{DS} < 80V, RDRV tied to LDO5V, T_J = 25℃, V_{BUS} = 400V, L_{HB} current = 10A, see Figure 6-1		100		V/ns
		From V_{DS} < 320V to V_{DS} < 80V, RDRV disconnected from LDO5V, R_{RDRV} = 0Ω, T_J = 25℃, V_{BUS} = 400V, L_{HB} current = 10A, see Figure 6-1		150		V/ns
	Maximum GaN FET switching frequency.	V_{NEG} rising to > –13.25V, soft-switched, maximum switching frequency derated for V_{VDD} < 9V	3.6			MHz
FAULTS						
$I_{T(OC)}$	DRAIN overcurrent fault – threshold current		40	50	60	A
$I_{T(SC)}$	DRAIN short-circuit fault – threshold current		60	75	90	A
$di/dt_{T(SC)}$	di/dt threshold between overcurrent and short-circuit faults		150			A/µs
	GaN temperature fault – postive-going threshold temperature			175		°C
	GaN Temperature fault – threshold temperature hysteresis			30		°C
	Driver temperature fault – positive-going threshold temperature			185		°C

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5.5 Electrical Characteristics (continued)

Unless otherwise noted: voltage, resistance, capacitance, and inductance are respect to GND; –40°C ≤ T_J ≤ 125°C; V_{DS} = 480V; 9V ≤ V_{VDD} ≤ 18V; V_{IN} = 0V; RDRV connected to LDO5V; L_{BBSW} = 4.7µH

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Driver Temperature fault – threshold temperature hysteresis			20		°C
TEMP						
	Output Frequency		4.5	9	14	kHz
	Output PWM Duty Cycle	GaN T_J = 150°C		82		%
		GaN T_J = 125°C	58.5	64.6	70	%
		GaN T_J = 85°C	36.2	40	43.7	%
		GaN T_J = 25°C	0.3	3	6	%
IDEAL-DIODE MODE CONTROL						
$V_{T(3rd)}$	Drain-source third-quadrant detection – threshold voltage		–0.15	0	0.15	V
$I_{T(ZC)}$	Drain zero-current detection – threshold current	0°C ≤ T_J ≤ 125°C	–0.2	0	0.2	A
		–40°C ≤ T_J ≤ 0°C	–0.35	0	0.35	A

5.6 Switching Characteristics

Unless otherwise noted: voltage, resistance, capacitance, and inductance are respect to GND; –40°C ≤ T_J ≤ 125°C; V_{DS} = 480V; 9V ≤ V_{VDD} ≤ 18V; V_{IN} = 0V; RDRV connected to LDO5V; L_{BBSW} = 4.7µH

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SWITCHING TIMES						
$t_{d(on)}$ (Idrain)	Drain-current turn-on delay time	From V_{IN} > $V_{IN,IT+}$ to I_D > 1A, V_{BUS} = 400V, L_{HB} current = 10A, see Figure 6-1 and Figure 6-2		28	42	ns
$t_{d(on)}$	Turn-on delay time	From V_{IN} > $V_{IN,IT+}$ to V_{DS} < 320V, V_{BUS} = 400V, L_{HB} current = 10A, see Figure 6-1 and Figure 6-2		32	52	ns
$t_{r(on)}$	Turn-on rise time	From V_{DS} < 320V to V_{DS} < 80V, V_{BUS} = 400V, L_{HB} current = 10A, see Figure 6-1 and Figure 6-2		2.5	4	ns
$t_{d(off)}$	Turn-off delay time	From V_{IN} < $V_{IN\ ,IT-}$ to V_{DS} > 80V, V_{BUS} = 400V, L_{HB} current = 10A, see Figure 6-1 and Figure 6-2		44	65	ns
$t_{f(off)}$	Turn-off fall time[(1)]	From V_{DS} > 80V to V_{DS} > 320V, V_{BUS} = 400V, L_{HB} current = 10A, see Figure 6-1 and Figure 6-2			21	ns
	Minimum IN high pulse-width for FET turn-on	V_{IN} rise/fall times < 1ns, V_{DS} falls to < 200V, V_{BUS} = 400V, L_{HB} current = 10A, see Figure 6-1			24	ns
STARTUP TIMES						
$t_{(start)}$	Driver start-up time	From V_{VDD} > $V_{VDD,T+}$ (UVLO) to $\overline{FAULT}$ high, C_{LDO5V} = 100nF, C_{VNEG} = 2.2µF at 0V bias linearly decreasing to 1.5µF at 15V bias		310	470	us
FAULT TIMES						
$t_{off(OC)}$	Overcurrent fault FET turn-off time, FET on before overcurrent	V_{IN} = 5V, From I_D > $I_{T(OC)}$ to I_D < 50A, I_D di/dt = 100A/µs		110	145	ns
$t_{off(SC)}$	Short-circuit current fault FET turn-off time, FET on before short circuit	V_{IN} = 5V, From I_D > $I_{T(SC)}$ to I_D < 50A, I_D di/dt = 700A/µs		65	100	ns
	Overcurrent fault FET turn-off time, FET turning on into overcurrent	From I_D > $I_{T(OC)}$ to I_D < 50A		200	250	ns

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5.6 Switching Characteristics (continued)

Unless otherwise noted: voltage, resistance, capacitance, and inductance are respect to GND; –40℃ ≤ T_J ≤ 125℃; V_{DS} = 480V; 9V ≤ V_{VDD} ≤ 18V; V_{IN} = 0V; RDRV connected to LDO5V; L_{BBSW} = 4.7µH

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Short-circuit fault FET turn-off time, FET turning on into short circuit	From $I_D > I_{T(SC)}$ to I_D < 50A		100	180	ns
	IN reset time to clear $\overline{FAULT}$ latch	From $V_{IN} < V_{IN,IT-}$ to $\overline{FAULT}$ high	250	380	580	us
$t_{(window)(OC)}$	Overcurrent fault to short-circuit fault window time			50		ns
IDEAL-DIODE MODE CONTROL TIMES						
	Ideal-diode mode FET turn-on time	$V_{DS} < V_{T(3rd)}$ to FET turn-on, V_{DS} being discharged by half-bridge configuration inductor at 5A		50	65	ns
	Ideal-diode mode FET turn-off time	$I_D > I_{T(ZC)}$ to FET turn-off, I_D di/dt = 100A/µs created with a half-bridge configuration		50	76	ns
	Overtemperature-shutdown ideal-diode mode IN falling blanking time		150	230	360	ns

(1) During turn-off, V_{DS} rise time is the result of the resonance of C_{OSS} and loop inductance as well as load current.

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5.7 Typical Characteristics

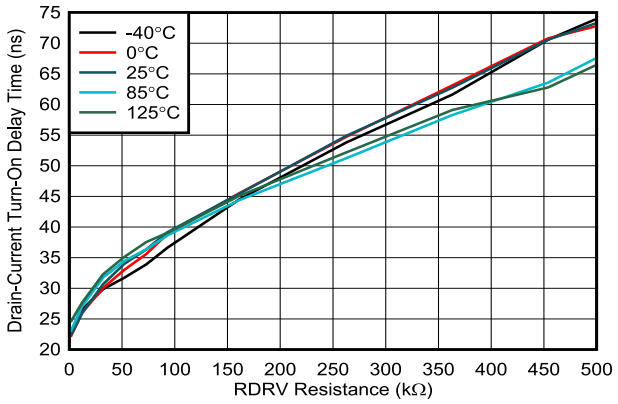

Figure 5-1. Drain-Current Turn-On Delay Time vs Drive-Strength Resistance

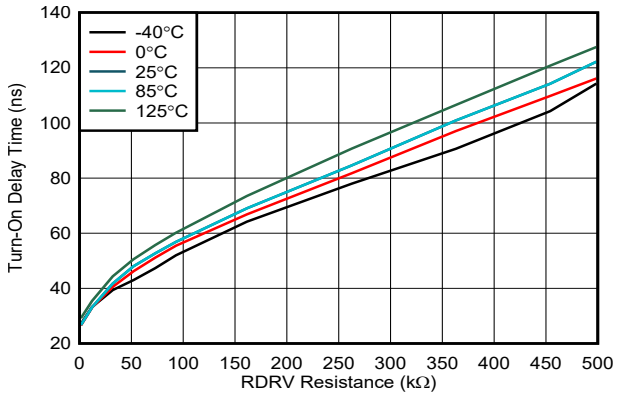

Figure 5-2. Turn-On Delay Time vs Drive-Strength Resistance

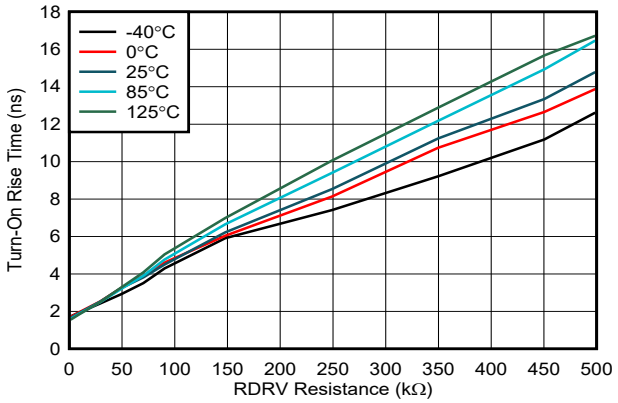

Figure 5-3. Turn-On Rise Time vs Drive-Strength Resistance

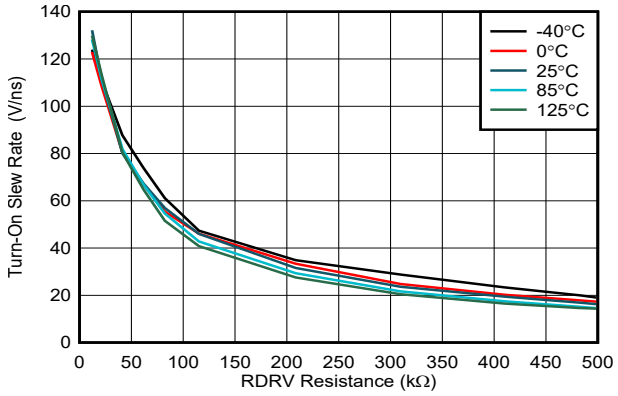

Figure 5-4. Turn-On Slew Rate vs Drive-Strength Resistance

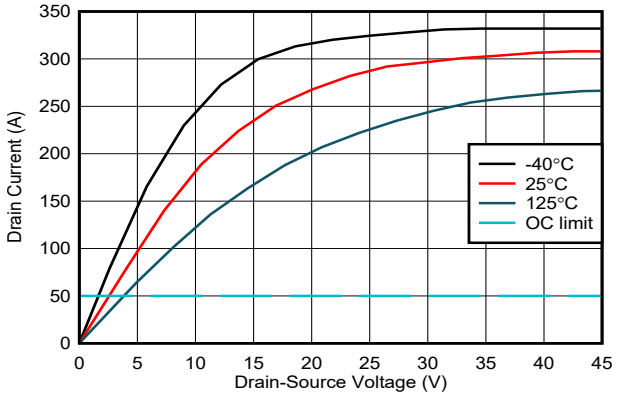

Figure 5-5. Drain Current vs Drain-Source Voltage

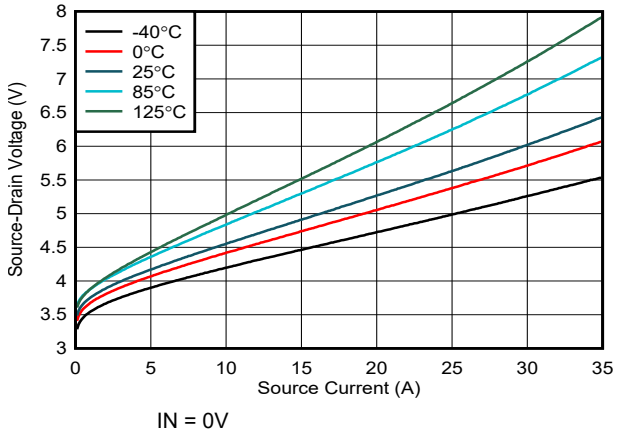

Figure 5-6. Off-State Source-Drain Voltage vs Source Current

5.7 Typical Characteristics (continued)

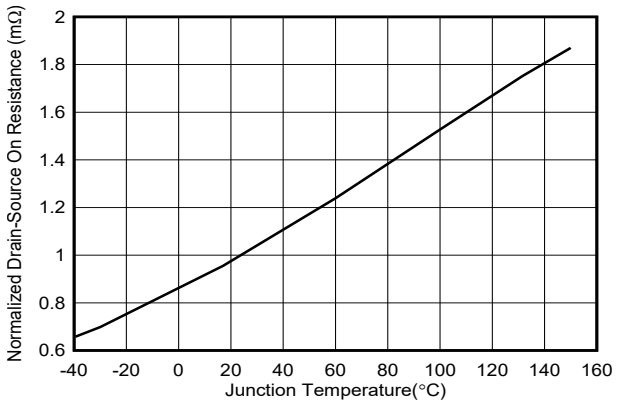

Figure 5-7. Normalized On-Resistance vs Junction Temperature

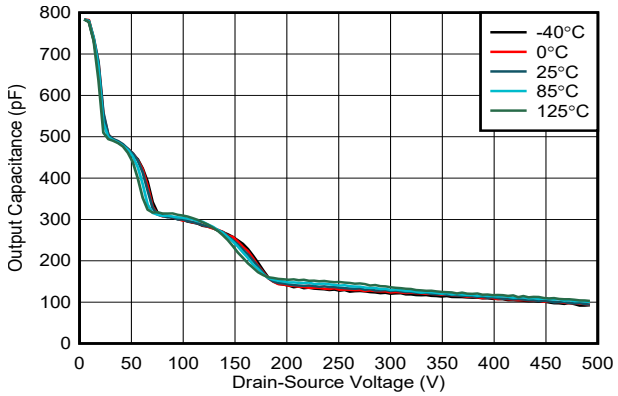

Figure 5-8. Output Capacitance vs Drain-Source Voltage

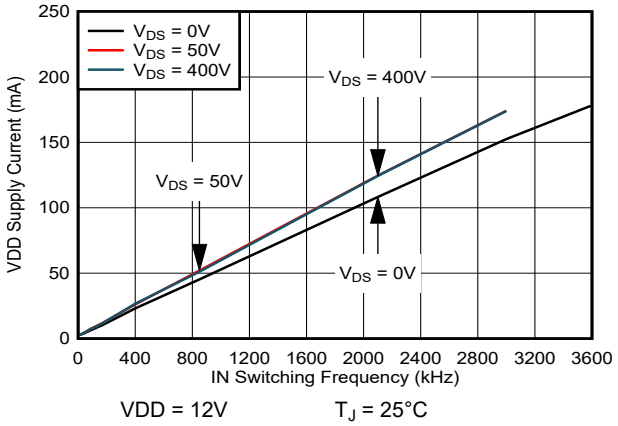

Figure 5-9. VDD Supply Current vs IN Switching Frequency

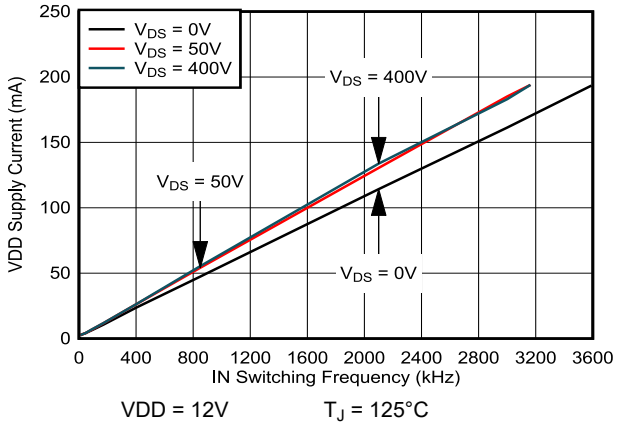

Figure 5-10. VDD Supply Current vs IN Switching Frequency

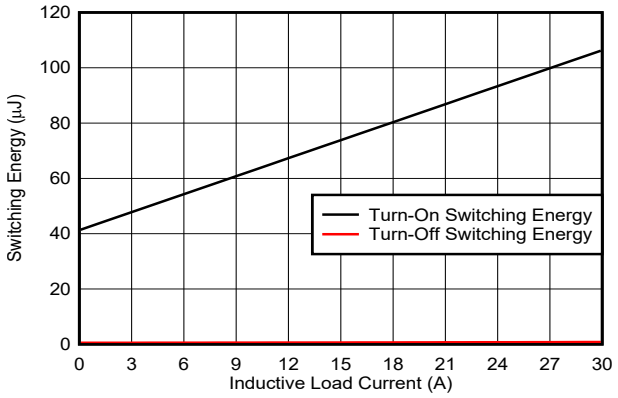

Figure 5-11. Half-Bridge Switching Energy vs Inductive Load Current

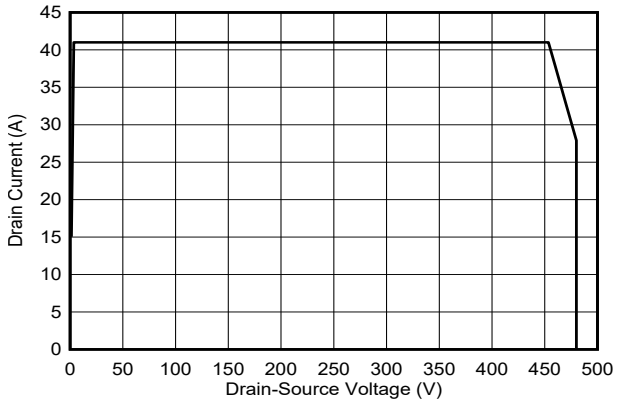

Figure 5-12. Repetitive Safe Operation Area

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6 Parameter Measurement Information

6.1 Switching Parameters

Figure 6-1 shows the circuit used to measure most switching parameters. The top device in this circuit is used to re-circulate the inductor current and functions in third-quadrant mode only. Only the LMG3422R050 must be used as the top device as it does not have the ideal-diode mode feature. Do not use the LMG3425R050 for the top device. If the top device has the ideal-diode mode feature, it will automatically turn on the GaN FET when the inductor current is re-circulating and cause a shoot-through current event when the bottom device turns on. The bottom device is the active device that turns on to increase the inductor current to the desired test current. The bottom device is then turned off and on to create switching waveforms at a specific inductor current. Both the drain current (at the source) and the drain-source voltage is measured. Figure 6-2 shows the specific timing measurement. TI recommends to use the half-bridge as a double pulse tester. Excessive third-quadrant operation can overheat the top device.

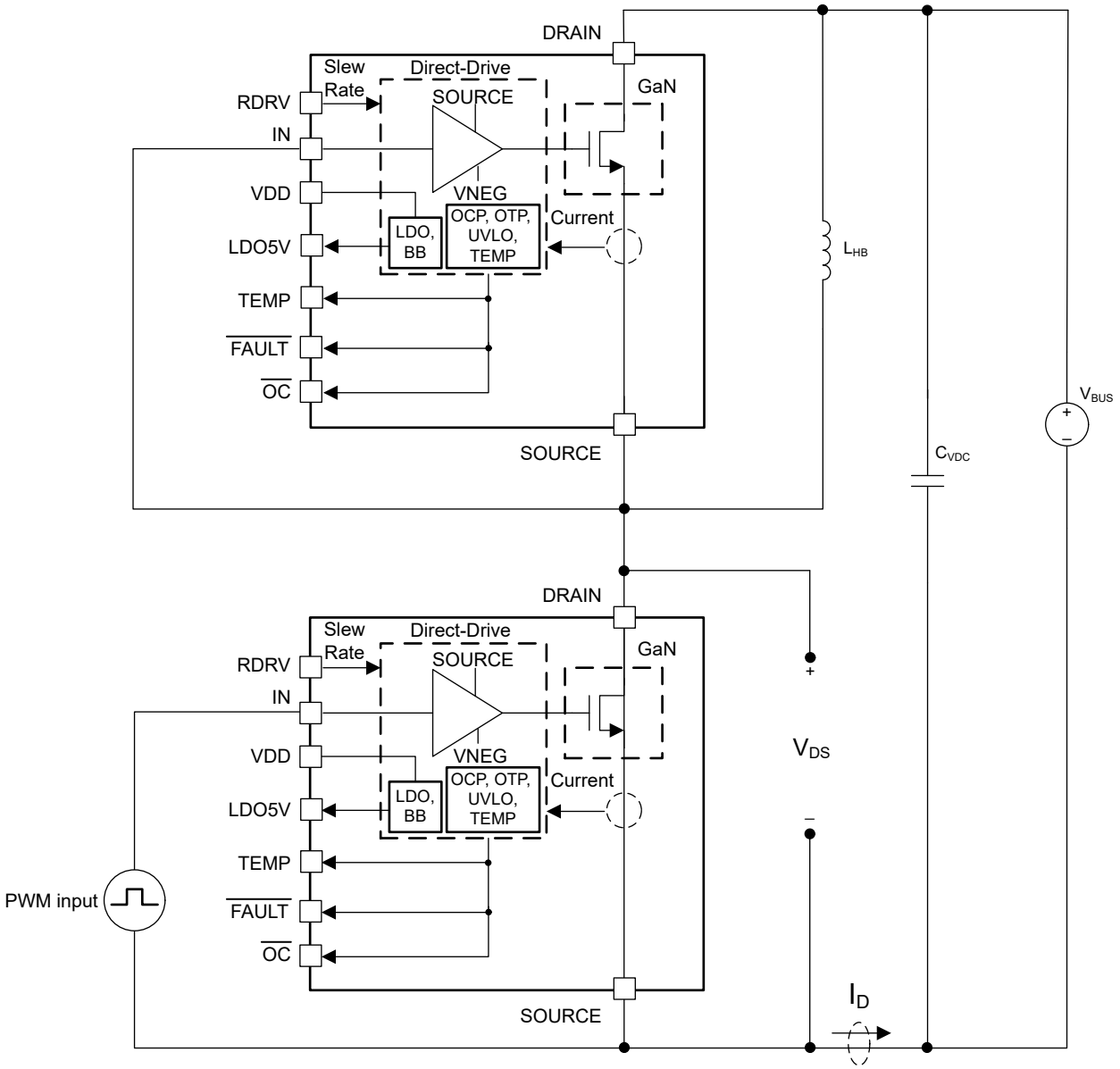

Figure 6-1. Circuit Used to Determine Switching Parameters

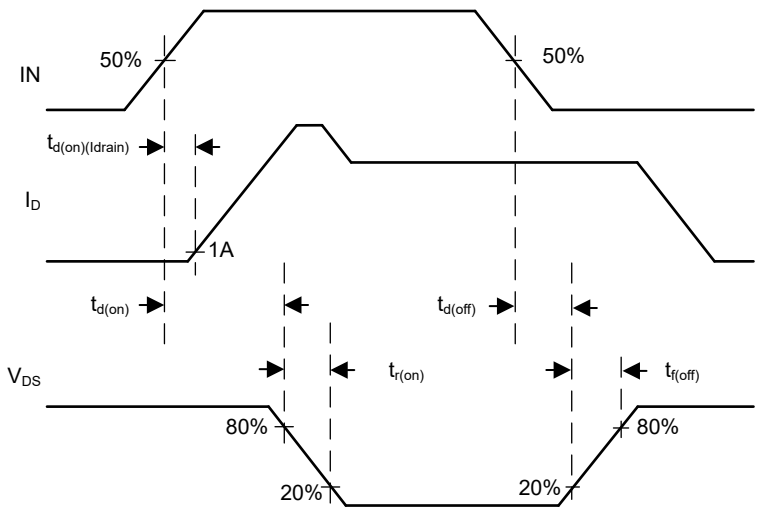

Figure 6-2. Measurement to Determine Propagation Delays and Slew Rates

6.1.1 Turn-On Times

The turn-on transition has three timing components: drain-current turn-on delay time, turn-on delay time, and turn-on rise time. The drain-current turn-on delay time is from when IN goes high to when the GaN FET drain-current reaches 1A. The turn-on delay time is from when IN goes high to when the drain-source voltage falls 20% below the bus voltage. Finally, the turn-on rise time is from when drain-source voltage falls 20% below the bus voltage to when the drain-source voltage falls 80% below the bus voltage. Note that the turn-on rise time is the same as the V_{DS} 80% to 20% fall time. All three turn-on timing components are a function of the RDRV pin setting.

6.1.2 Turn-Off Times

The turn-off transition has two timing components: turn-off delay time, and turn-off fall time. The turn-off delay time is from when IN goes low to when the drain-source voltage rises to 20% of the bus voltage. The turn-off fall time is from when the drain-source voltage rises to 20% of the bus voltage to when the drain-source voltage rises to 80% of the bus voltage. Note that the turn-off fall time is the same as the V_{DS} 20% to 80% rise time. The turn-off timing components are independent of the RDRV pin setting, but heavily dependent on the L_{HB} load current.

6.1.3 Drain-Source Turn-On Slew Rate

The drain-source turn-on slew rate, measured in volts per nanosecond, is the inverse of the turn-on rise time or equivalently the inverse of the V_{DS} 80% to 20% fall time. The RDRV pin is used to program the slew rate.

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6.1.4 Turn-On and Turn-Off Switching Energy

The turn-on and turn-off switching energy shown in Figure 5-11 represent the energy absorbed by the low-side device during the turn-on and turn-off transients of the circuit. As the circuit in Figure 6-1 represents a boost converter with input shorted to output, the switching energy is dissipated in the low-side device. The hard-switching turn-on loss composes of Coss loss of the half-bridge and the turn-on overlap loss while the turn-off loss is negligible as the inductor current is mainly charging the output capacitance of the device. The turn-on and turn-off losses have been calculated from experimental waveforms by integrating the product of the drain current with the drain-source voltage over the turn-on and turn-off times, respectively. The skew of probes for voltage and current are very important for accurate measurement of turn-on and turn-off energy.

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6.2 Safe Operation Area (SOA)

6.2.1 Repetitive SOA

The allowed repetitive SOA for the LMG3425R050 (Figure 5-12) is defined by the peak drain current (I_{DS}) and the drain to source voltage (V_{DS}) of the device during turn on. The peak drain current during switching is the sum of several currents going into drain terminal: the inductor current (I_{ind}); the current required to charge the C_{OSS} of the other GaN device in the totem pole; and the current required to charge the parasitic capacitance (C_{par}) on the switching node. 145pF is used as an average C_{OSS} of the device during switching. The parasitic capacitance on the switch node may be estimated by using the overlap capacitance of the PCB. A boost topology is used for the SOA testing. The circuit shown in Figure 6-3 is used to generate the SOA curve in Figure 5-12. For reliable operation, the junction temperature of the device must also be limited to 125°C. The I_{DS} of Figure 5-12 can be calculated by:

$$I_{DS} = I_{ind} + (145pF + C_{par}) * \text{Drain slew rate at peak current} \quad (1)$$

where drain slew rate at the peak current is estimated between 70% and 30% of the bus voltage, and C_{par} is the parasitic board capacitance at the switched node.

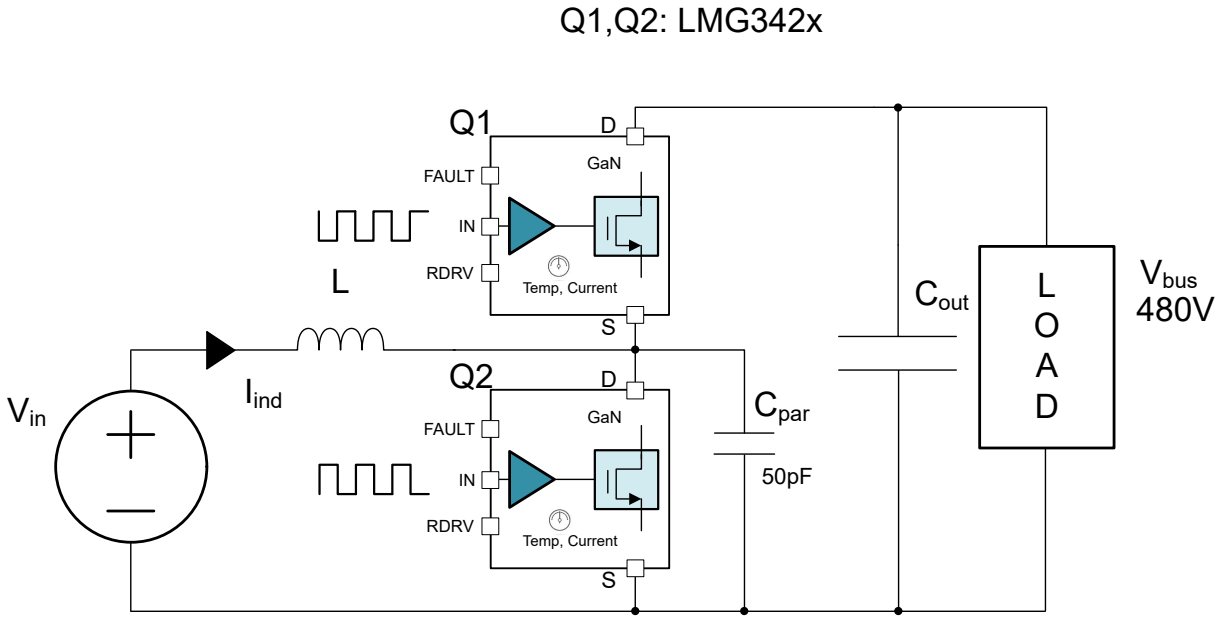

Figure 6-3. Circuit Used for SOA Curve

Refer to *Achieving GaN Products With Lifetime Reliability* for more details.

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7 Detailed Description

7.1 Overview

The LMG3425R050 is a high-performance power GaN device with integrated gate driver. The GaN device offers zero reverse recovery and ultra-low output capacitance, which enables high efficiency in bridge-based topologies. Direct-drive architecture is applied to control the GaN device directly by the integrated gate driver. This architecture provides superior switching performance compared to the traditional cascode approach and helps solve a number of challenges in GaN applications.

The integrated driver ensures the device stays off for high drain slew rates. The integrated driver protects the GaN device from overcurrent, short-circuit, overtemperature, VDD undervoltage, and a high-impedance RDRV pin. The integrated driver is also able to sense the die temperature and send out the temperature signal through a modulated PWM signal.

Unlike Si MOSFETs, GaN devices do not have a p-n junction from source to drain and thus have no reverse recovery charge. However, GaN devices still conduct from source to drain similar to a p-n junction body diode, but with higher voltage drop and higher conduction loss. Therefore, source-to-drain conduction time must be minimized while the LMG3425R050 GaN FET is turned off. The ideal-diode mode feature automatically minimizes the source-to-drain conduction loss that occur on the GaN FET soft-switched turn-on edge, similar to optimum dead-time control.

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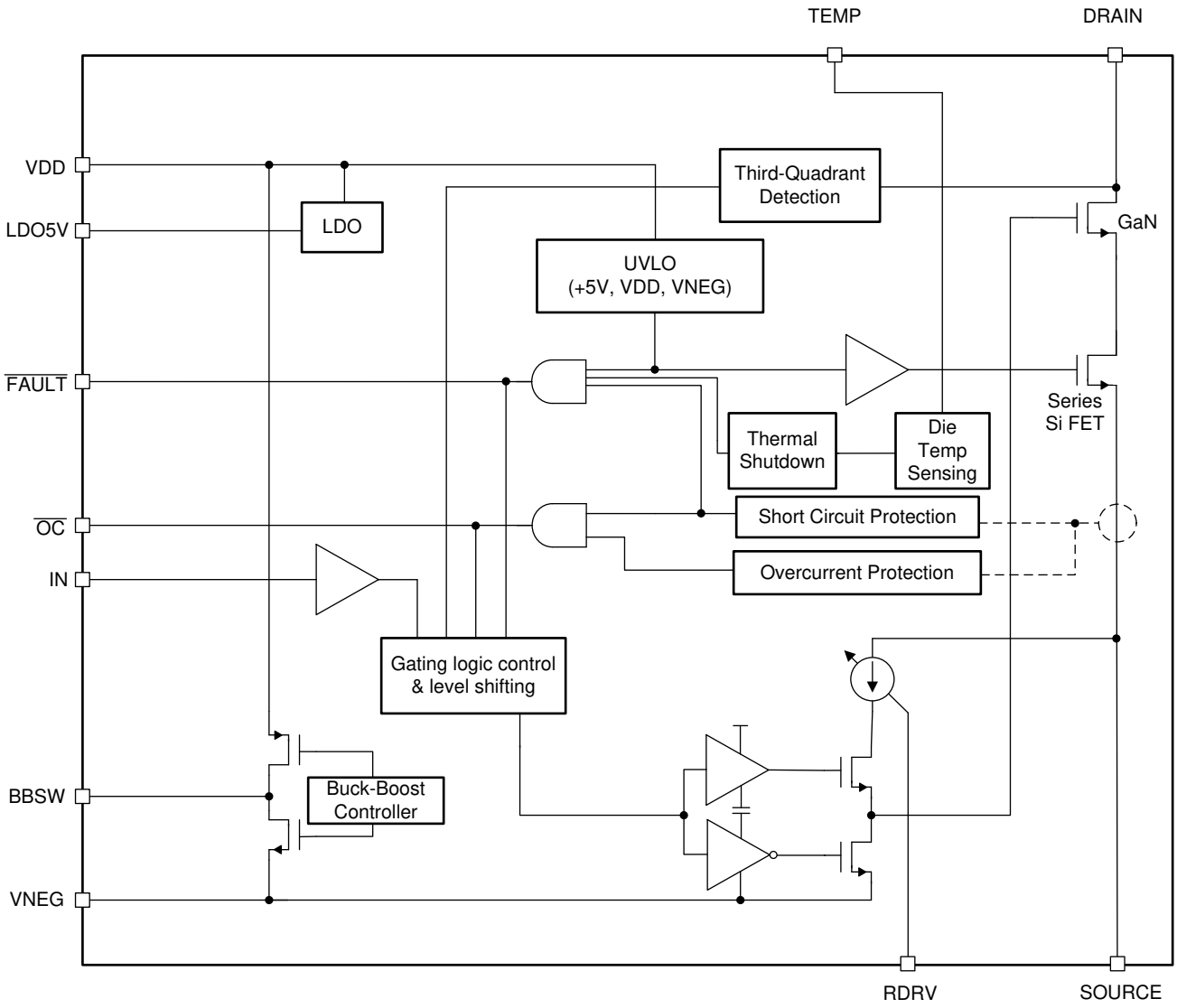
7.2 Functional Block Diagram



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7.3 Feature Description

The LMG3425R050 includes advanced features to provide superior switching performance and converter efficiency.

7.3.1 GaN FET Operation Definitions

For the purposes of this data sheet, the following terms are defined below. The SOURCE pin is assumed to be at 0 V for these definitions.

First-Quadrant Current = Positive current flowing internally from the DRAIN pin to the SOURCE pin.

Third-Quadrant Current = Positive current flowing internally from the SOURCE pin to the DRAIN pin.

First-Quadrant Voltage = Drain pin voltage – Source pin voltage = Drain pin voltage

Third-Quadrant Voltage = SOURCE pin voltage – DRAIN pin voltage = –DRAIN pin voltage

FET On-State = FET channel is at rated $R_{DS(on)}$. Both first-quadrant current and third-quadrant current can flow at rated $R_{DS(on)}$.

For LMG3425R050 in **On-State**, GaN FET internal gate voltage is held at the SOURCE pin voltage to achieve rated $R_{DS(on)}$. The GaN FET channel is at rated $R_{DS(on)}$ with V_{GS} = 0 V because the LMG3425R050 GaN FET is a depletion mode FET.

FET Off-State = FET channel is fully off for positive first-quadrant voltage. No first-quadrant current can flow. While first-quadrant current cannot flow in the FET Off-State, third-quadrant current still flows if the DRAIN voltage is taken sufficiently negative (positive third-quadrant voltage). For devices with an intrinsic p-n junction body diode, current flow begins when the DRAIN voltage drops enough to forward bias the p-n junction.

GaN FETS do not have an intrinsic p-n junction body diode. Instead, current flows because the GaN FET channel turns back on. In this case, the DRAIN pin becomes the electrical source and the SOURCE pin becomes the electrical drain. To enhance the channel in third-quadrant, the DRAIN (electrical source) voltage must be taken sufficiently low to establish a V_{GS} voltage greater than the GaN FET threshold voltage. The GaN FET channel is operating in saturation and only turns on enough to support the third-quadrant current as its saturated current.

For LMG3425R050 in **Off-State**, GaN FET internal gate voltage is held at the VNEG pin voltage to block all first-quadrant current. The VNEG voltage is lower than the GaN FET negative threshold voltage to cut off the channel.

To enhance the channel in off-state third quadrant, the LMG3425R050 DRAIN (electrical source) voltage must be taken sufficiently close to VNEG to establish a V_{GS} voltage greater than the GaN FET threshold voltage. Again, because the LMG3425R050 GaN FET is a depletion mode FET with a negative threshold voltage, this means the GaN FET turns on with DRAIN (electrical source) voltage between 0 V and VNEG. The typical off-state third-quadrant voltage is 5.3 V for third-quadrant current at 15 A. Thus, the off-state third-quadrant losses for the LMG3425R050 are significantly higher than a comparable power device with an intrinsic p-n junction body diode. The ideal-diode mode function described in *Ideal-Diode Mode Operation* can help mitigate these losses in specific situations.

7.3.2 Direct-Drive GaN Architecture

The LMG3425R050 uses a series Si FET to ensure the power IC stays off when VDD bias power is not applied. When the VDD bias power is off, the series Si FET is interconnected with the GaN device in a cascode mode, which is shown in the *Functional Block Diagram*. The gate of the GaN device is held within a volt of the series Si FET's source. When a high voltage is applied on the drain and the silicon FET blocks the drain voltage, the V_{GS} of the GaN device decreases until the GaN device passes the threshold voltage. Then, the GaN device is turned off and blocks the remaining major part of drain voltage. There is an internal clamp to make sure that the V_{DS} of the Si FET does not exceed its maximum rating. This feature avoids the avalanche of the series Si FET when there is no bias power.

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When LMG3425R050 is powered up with VDD bias power, the internal buck-boost converter generates a negative voltage (V_{VNEG}) that is sufficient to directly turn off the GaN device. In this case, the series Si FET is held on and the GaN device is gated directly with the negative voltage.

Comparing with traditional cascode drive GaN architecture, where the GaN gate is grounded and the Si MOSFET gate is being driven to control the GaN device, direct-drive configuration has multiple advantages. First, as the Si MOSFET does need to switch in every switching cycle, GaN gate-to-source charge (Q_{GS}) is lower and there's no Si MOSFET reverse-recovery related losses. Second, the voltage distribution between the GaN and Si MOSFET in off-mode in a cascode configuration can cause the MOSFET to avalanche due to high GaN drain-to-source capacitance (C_{DS}). Finally, the switching slew rate in direct-drive configuration can be controlled while cascode drive cannot. More information about the direct-drive GaN architecture can be found in *Direct-drive configuration for GaN devices*.

7.3.3 Drain-Source Voltage Capability

Due to the silicon FET's long reign as the dominant power-switch technology, many designers are unaware that the headline drain-source voltage cannot be used as an equivalent point to compare devices across technologies. The headline drain-source voltage of a silicon FET is set by the avalanche breakdown voltage. The headline drain-source voltage of a GaN FET is set by the long term reliability with respect to data sheet specifications.

Exceeding the headline drain-source voltage of a silicon FET can lead to immediate and permanent damage. Meanwhile, the breakdown voltage of a GaN FET is much higher than the headline drain-source voltage. For example, the breakdown voltage of the LMG3425R050 is more than 800V.

A silicon FET is usually the weakest link in a power application during an input voltage surge. Surge protection circuits must be carefully designed to ensure the silicon FET avalanche capability is not exceeded because it is not feasible to clamp the surge below the silicon FET breakdown voltage. Meanwhile, it is easy to clamp the surge voltage below a GaN FET breakdown voltage. In fact, a GaN FET can continue switching during the surge event which means output power is safe from interruption.

The LMG3425R050 drain-source capability is explained with the assistance of Figure 7-1. The figure shows the drain-source voltage versus time for a GaN FET for a single switch cycle in a switching application. No claim is made about the switching frequency or duty cycle. This device is not recommended for continuous voltage stress in non-switching applications.

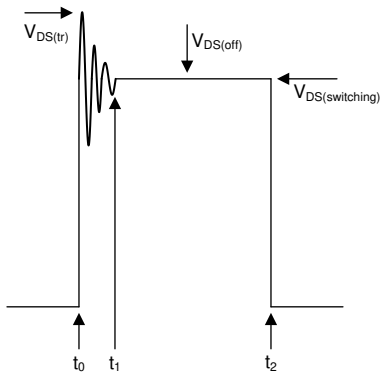

Figure 7-1. Drain-Source Voltage Switching Cycle

The waveform starts before t_0 with the FET in the on state. At t_0 the GaN FET turns off and parasitic elements cause the drain-source voltage to ring at a high frequency. The peak ring voltage is designated $V_{DS(tr)}$. The high frequency ringing has damped out by t_1. Between t_1 and t_2 the FET drain-source voltage is set by the characteristic response of the switching application. The characteristic is shown as a flat line, but other responses are possible. The voltage between t_1 and t_2 is designated $V_{DS(off)}$. At t_2 the GaN FET is turned on at a non-zero drain-source voltage. The drain-source voltage at t_2 is designated $V_{DS(switching)}$. Unique $V_{DS(tr)}$, $V_{DS(off)}$ and $V_{DS(switching)}$ parameters are shown because each can contribute to stress over the lifetime of the GaN FET.

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The LMG3425R050 drain-source surge voltage capability is seen with the absolute maximum ratings $V_{DS(tr)(surge)}$ and $V_{DS(surge)}$ in the *Specifications* where $V_{DS(tr)(surge)}$ maps to $V_{DS(tr)}$ in Figure 7-1 and $V_{DS(surge)}$ maps to both $V_{DS(off)}$ and $V_{DS(switching)}$ in Figure 7-1. More information about the surge capability of TI GaN FETs is found in *A New Approach to Validate GaN FET Reliability to Power-line Surges Under Use-conditions.*

7.3.4 Internal Buck-Boost DC-DC Converter

An internal inverting buck-boost converter generates a regulated negative rail for the turn-off supply of the GaN device. The buck-boost converter is controlled by a peak current mode, hysteretic controller. In normal operation, the converter remains in discontinuous-conduction mode, but can enter continuous-conduction mode during start-up. The converter is controlled internally and requires only a single surface-mount inductor and output bypass capacitor. Typically, the converter is designed to use a 4.7-µH inductor and a 2.2-µF output capacitor.

The buck-boost converter uses a peak current hysteretic control. As shown in Figure 7-2, the inductor current increases at the beginning of a switching cycle until the inductor reaches the peak current limit. Then the inductor current goes down to zero. The idle time between each current pulse is determined automatically by the buck-boost controller, and can be reduced to zero. Therefore, the maximum output current happens when the idle time is zero, and is decided by the peak current but to a first order is independent of the inductor value. However, the peak output current the buck-boost can deliver to the –14-V rail is proportional to the VDD input voltage. Therefore, the maximum switching frequency of the GaN that the buck-boost can support varies with VDD voltage and is only specified for operation up to 3.6 MHz for VDD voltages above 9 V.

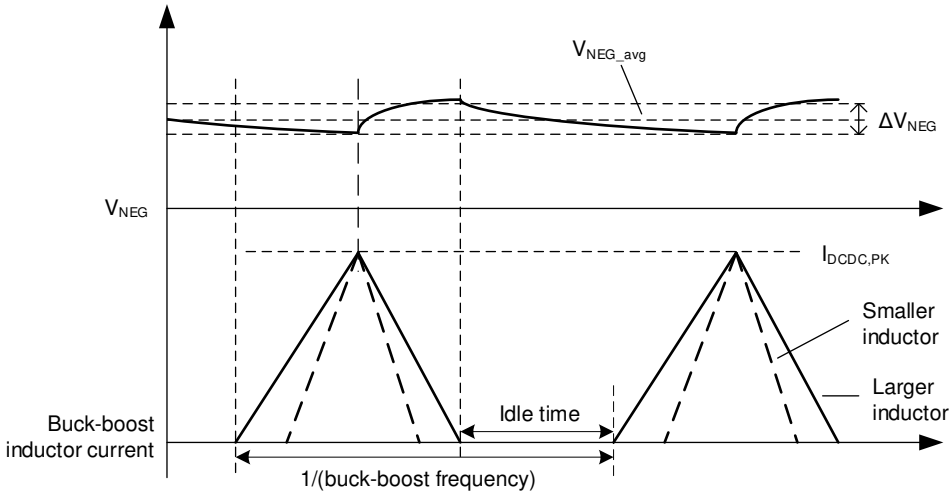

Figure 7-2. Buck-Boost Converter Inductor Current

The LMG3425R050 supports the GaN operation up to 3.6 MHz. As power consumption is very different in a wide switching frequency range enabled by the GaN device, two peak current limits are used to control the buck-boost converter. The two ranges are separated by IN positive-going threshold frequency. As shown in Figure 7-3, when switching frequency is in the lower range, the peak current is initially set to the lower value $I_{BBSW,M(low)}$ (typically 0.4A). When switching frequency is in the higher range, the peak current is raised to the higher value $I_{BBSW,M(high)}$ (typically 1 A) and requires a larger inductor. There is a filter on this frequency detection logic, therefore the LMG3425R050 requires five consecutive cycles at the higher frequency before it is set to the higher buck-boost peak current limit. The current limit does not go down again until power off after the higher limit is set. Even if the switching frequency returns to the lower range, the current limit does not decrease to the lower limit.

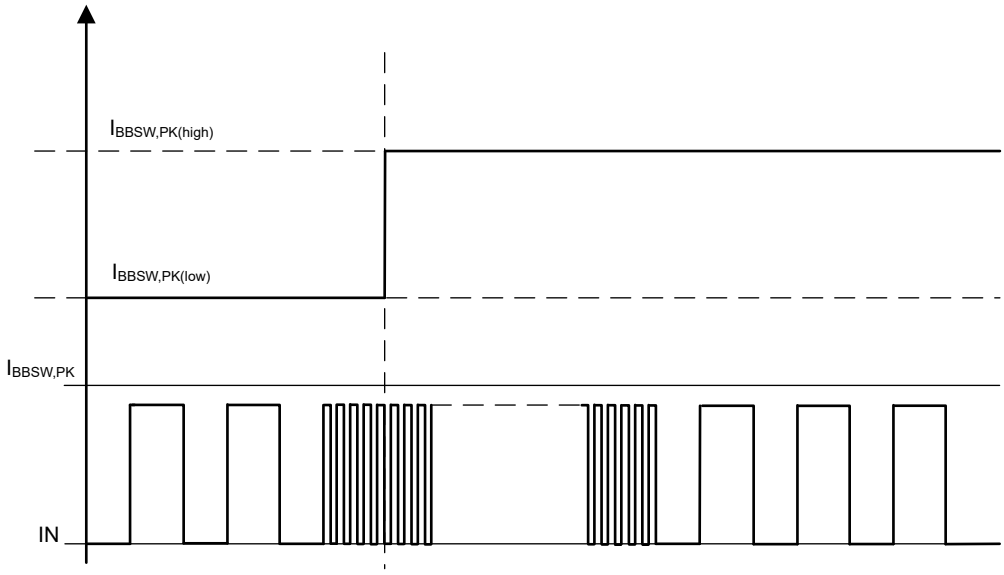

Figure 7-3. Buck-Boost Converter Peak Current

As the peak current of the buck-boost is subject to two different peak current limits which are 0.4A and 1A for low and high frequency operation (see *Internal Buck-Boost DC-DC Converter*), so the inductor must have a saturation current well above the rated peak current limit. After the higher limit is established by switching at a higher frequency, the current limit does not go back to the lower level even when GaN device is then switched at a lower frequency. Therefore, selecting an inductor according to the higher 1A limit is recommended.

7.3.5 VDD Bias Supply

Wide VDD voltage ranges from 7.5V to 18V are supported by internal regulators which supply the bias supplies needed for the internal circuits to function. If the VDD input voltage is less than 9V, then the maximum switching frequency is de-rated.

7.3.6 Auxiliary LDO

There is a 5V voltage regulator inside the part used to supply external loads, such as digital isolators for the high-side drive signal. The digital outputs of the part use this rail as their supply. No capacitor is required for stability, but transient response is poor if no external capacitor is provided. If the application uses this rail to supply external circuits, TI recommends to have a capacitor of at least 0.1µF for improved transient response. A larger capacitor can be used for further transient response improvement. The decoupling capacitor used here must be a low-ESR ceramic type. Capacitances above 0.47µF will slow down the start-up time of the LMG3425R050 due to the ramp-up time of the 5V rail.

7.3.7 Fault Protection

The GaN power IC integrates overcurrent protection (OCP), short-circuit protection (SCP), overtemperature protection (OTP), undervoltage lockout (UVLO) protection, and high-impedance RDRV pin protection.

7.3.7.1 Overcurrent Protection and Short-Circuit Protection

There are two types of current faults which can be detected by the driver: overcurrent fault and short-circuit fault.

The overcurrent protection (OCP) circuit monitors drain current and compares that current signal with an internally set limit $I_{T(OC)}$. Upon detection of the overcurrent, the LMG3425R050 conducts cycle-by-cycle overcurrent protection as shown in Figure 7-4. In this mode, the GaN device is shut off when the drain current crosses the $I_{T(OC)}$ plus a delay $t_{off(OC)}$, but the overcurrent signal clears after the IN pin signal goes low. In the next cycle, the GaN device can turn on as normal. The cycle-by-cycle function can be used in cases where steady-state operation current is below the OCP level but transient response can still reach current limit, while the circuit operation cannot be paused. The cycle-by-cycle function also prevents the GaN device from overheating by overcurrent induced conduction losses.

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The short-circuit protection (SCP) monitors the drain current and triggers if the *di/dt* of the current exceeds a threshold *di/dt* $_{T(SC)}$ as the current crosses between the OC and SC thresholds. It performs this *di/dt* detection by delaying the OC detection signal by an amount $t_{OC,window}$ and using a higher current SC detection threshold. If the delayed OC occurs before the non-delayed SC, the *di/dt* is below the threshold and an OC is triggered. If the SC is detected first, the *di/dt* is fast enough and the SC is detected as shown in Figure 7-5. This extremely high *di/dt* current would typically be caused by a short of the output of the half-bridge and can be damaging for the GaN to continue to operate in that condition. Therefore, if a short-circuit fault is detected, the GaN device is turned off with an intentionally slowed driver so that a lower overshoot voltage and ringing can be achieved during the turn-off event. This fast response circuit helps protect the GaN device even under a hard short-circuit condition. In this protection, the GaN device is shut off and held off until the fault is reset by either holding the IN pin low for a period of time defined in the *Specifications* or removing power from VDD.

During OCP or SCP in a half bridge, after the current reaches the upper limit and the device is turned off by protection, the PWM input of the device could still be high and the PWM input of the complementary device could still be low. In this case, the load current can flow through the third quadrant of the complementary device with no synchronous rectification. The high negative V_{DS} of the GaN device (–3 V to –5 V) from drain to source could lead to high third-quadrant loss, similar to dead-time loss but for a longer time.

For safety considerations, OCP allows cycle-by-cycle operation while SCP latches the device until reset. See the *Fault Reporting* section for information on how the OCP and SCP faults are reported.

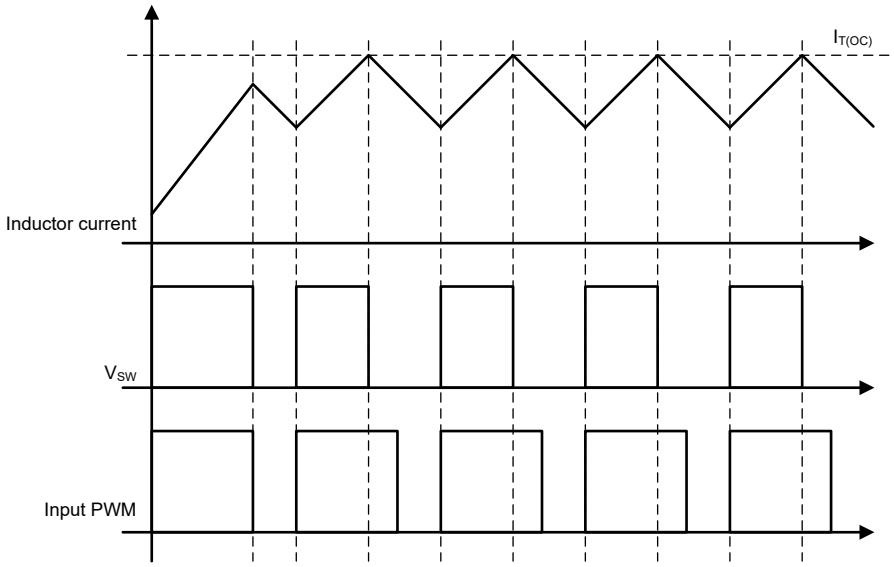

Figure 7-4. Cycle-by-Cycle OCP Operation

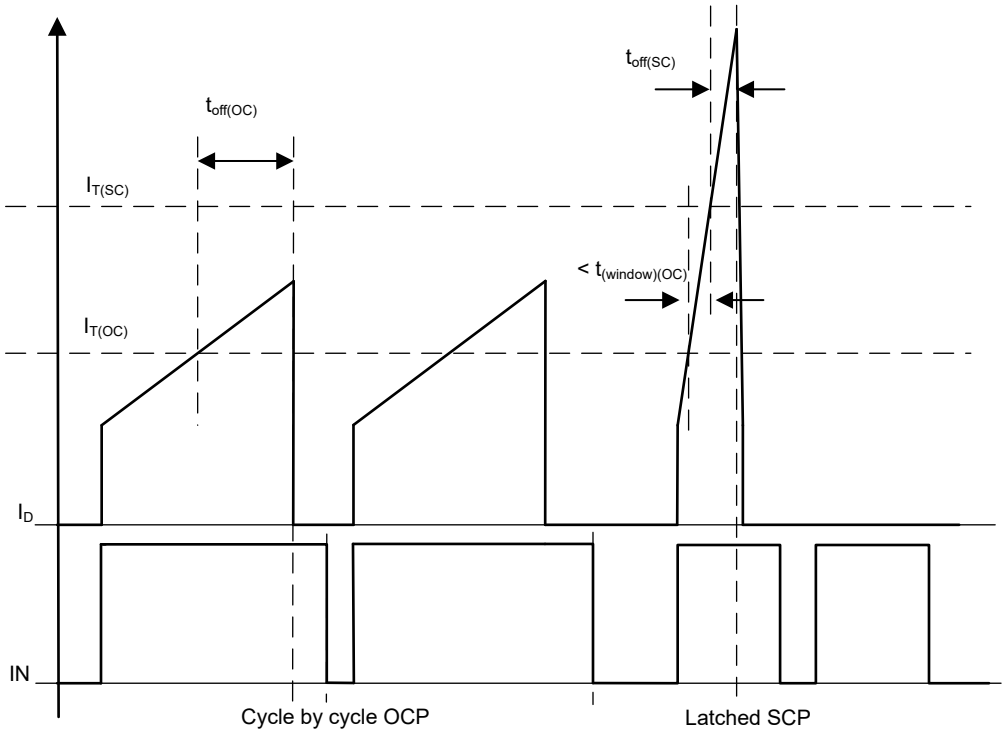

Figure 7-5. Overcurrent Detection vs Short-Circuit Detection

7.3.7.2 Overtemperature Shutdown Protection

The LMG3425R050 implements two overtemperature-shutdown (OTSD) protection functions, the GaN OTSD and the Driver OTSD. Two OTSD functions are needed to maximize device protection by sensing different locations in the device and protecting against different thermal-fault scenarios.

The GaN OTSD senses the GaN FET temperature. The GaN FET can overheat from both first-quadrant current and third-quadrant current. As explained in *GaN FET Operation Definitions*, a FET can prevent first-quadrant current by going into the off-state but is unable to prevent third-quadrant current. FET third-quadrant losses are a function of the FET technology, current magnitude, and if the FET is operating in the on-state or off-state. As explained in *GaN FET Operation Definitions*, the LMG3425R050 has much higher GaN FET third-quadrant losses in the off-state.

When the GaN FET is too hot, the best protection is to turn off the GaN FET when first-quadrant current tries to flow and turn on the GaN FET when third-quadrant current is flowing. This type of FET control is known as ideal-diode mode (IDM). When the GaN OTSD trip point is exceeded, the GaN OTSD puts the GaN FET into overtemperature-shutdown ideal-diode mode (OTSD-IDM) operation to achieve this optimum protection. OTSD-IDM is explained in *Ideal-Diode Mode Operation*.

The Driver OTSD senses the integrated driver temperature and trips at a higher temperature compared to the GaN OTSD. This second OTSD function exists to protect the LMG3425R050 from driver thermal-fault events while allowing sufficient temperature difference for OTSD-IDM to operate. These driver thermal events include shorts on the LDO5V, BBSW, and VNEG device pins. When the Driver OTSD trip point is exceeded, the Driver OTSD shuts off the LDO5V regulator, the VNEG buck-boost converter, and the GaN FET. Note that OTSD-IDM does not function in Driver OTSD. This is why the Driver OTSD must trip higher than the GaN OTSD function. Otherwise, GaN FET third-quadrant overheating cannot be addressed.

Besides the temperature difference in the GaN OTSD and Driver OTSD trip points, further temperature separation is obtained due to the thermal gradient difference between the GaN OTSD and Driver OTSD sense points. The GaN OTSD sensor is typically at least 20°C hotter than the driver OTSD sensor when the device is in GaN OTSD due to GaN FET power dissipation.

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The $\overline{\text{FAULT}}$ pin is asserted for either or both the GaN OTSD state and the Driver OTSD state. $\overline{\text{FAULT}}$ de-asserts and the device automatically returns to normal operation after both the GaN OTSD and Driver OTSD fall below their negative-going trip points. During cool down, when the device exits the Driver OTSD state but is still in the GaN OTSD state, the device automatically resumes OTSD-IDM operation.

7.3.7.3 UVLO Protection

The LMG3425R050 supports a wide range of VDD voltages. However, when the device is below UVLO threshold, the GaN device stops switching and is held off. The $\overline{\text{FAULT}}$ pin is pulled low as an indication of UVLO. The LDO and buck-boost are turned on by the rising-edge of the VIN UVLO and shuts off around 5V to 6V.

7.3.7.4 High-Impedance RDRV Pin Protection

For the cases where the RDRV pin is continuously monitored (see Drive-Strength Adjustment), the LMG3425R050 protects against dangerously slow turn-on times by continuously monitoring RDVR for a high impedance above the R_{RDRV} recommended operating condition range. The GaN FET is held off and The $\overline{\text{FAULT}}$ pin asserts when a high-impedance RDRV pin is detected. Normal operation resumes and the $\overline{\text{FAULT}}$ pin de-asserts when a high-impedance RDRV pin is no longer detected.

7.3.7.5 Fault Reporting

The LMG3422R050 can be configured to report faults either with both the $\overline{\text{FAULT}}$ and $\overline{\text{OC}}$ pins or just with the $\overline{\text{FAULT}}$ pin. Shorting the $\overline{\text{OC}}$ pin to ground during device VDD power up configures the LMG3422R050 to only report faults with the $\overline{\text{FAULT}}$ pin.

The LMG3426R050 does not have the $\overline{\text{OC}}$ pin and only reports faults with the $\overline{\text{FAULT}}$ pin.

The $\overline{\text{FAULT}}$ and $\overline{\text{OC}}$ pins are push-pull outputs. The high-level output voltage is pulled up to the LDO5V pin.

Table 7-1 shows the fault reporting truth table when both the $\overline{\text{FAULT}}$ pin and $\overline{\text{OC}}$ pins report faults.

Table 7-1. Fault Reporting Truth Table With Both the $\overline{\text{FAULT}}$ and $\overline{\text{OC}}$ Pins Reporting Faults

	No Fault	VDD UVLO	Overtemperature	High-Impedance RDRV Pin	Overcurrent	Short-Circuit
$\overline{\text{FAULT}}$	1	0	0	0	1	0
$\overline{\text{OC}}$	1	1	1	1	0	0

Table 7-2 shows the fault reporting truth table when only the $\overline{\text{FAULT}}$ pin reports faults.

Table 7-2. Fault Reporting Truth Table With Only the $\overline{\text{FAULT}}$ Pin Reporting Faults

	No Fault	VDD UVLO	Overtemperature	High-Impedance RDRV Pin	Overcurrent	Short-Circuit
$\overline{\text{FAULT}}$	1	0	0	0	0	0

7.3.8 Drive-Strength Adjustment

The LMG3425R050 allows users to adjust the drive strength of the device and obtain a desired slew rate, which provides flexibility when optimizing switching losses and noise coupling.

To adjust drive strength, a resistor can be placed between the RDRV pin and GND pin. The resistance determines the slew rate of the device, from 20 V/ns to 150V/ns, during turn-on. On the other hand, there are two dv/dt values that can be selected without the resistor: shorting the RDRV pin to ground sets the slew rate to 150V/ns, and shorting the RDRV pin to LDO5V sets the slew rate to 100V/ns. The device detects the short to LDO5V one time at power up. Once the short to LDO5V condition is detected, the device no longer monitors the RDRV pin. Otherwise, the RDRV pin is continuously monitored and the dv/dt setting can be changed by modulating the resistance during device operation. The modulation must be fairly slow since there is significant internal filtering to reject switching noise.

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Note

Parasitic power loop inductance can influence the voltage slew rate reading from the V_{DS} switching waveform. The inductance induces a drop on V_{DS} in the current rising phase before voltage falling phase, if this drop is more than 20% of the V_{DC}, the voltage slew rate reading can be influenced. Refer to Section 8.5.1.2 for the power loop design guideline and how to estimate the parasitic power loop inductance.

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7.3.9 Temperature-Sensing Output

The integrated driver senses the GaN die temperature and outputs the information through a modulated PWM signal on the TEMP pin. The typical PWM frequency is 9kHz with the same refresh rate. The minimum PWM pulse width is around 30ns, which can be observed at temperature below 25°C. The target temperature range is from 25°C to 150°C, and the corresponding PWM duty cycle is typically from 3% to 82%. Equation 2 can be used to calculate the typical junction temperature $T_{J,typ}$ in °C from the duty cycle D_{TEMP}:

$$T_{J,typ}\ (°C) = 162.3 * D_{TEMP} + 20.1 \quad (2)$$

The tolerances of typical measurement are listed in Table 7-3.

Table 7-3. Typical Junction Temperature Measurement Based on TEMP Signal and Tolerance

Typical T_J Measurement Based on TEMP Signal (°C)	25	85	125
Tolerance (°C)	±5	±6	±10

At temperatures above 150°C, the duty cycle continues to increase linearly until overtemperature fault happens. When overtemperature happens, the TEMP pin is pulled high to indicate this fault until the temperature is reduced to the normal range. There is a hysteresis to clear overtemperature fault.

7.3.10 Ideal-Diode Mode Operation

Off-state FETs act like diodes by blocking current in one direction (first quadrant) and allowing current in the other direction (third quadrant) with a corresponding *diode like* voltage drop. FETs, though, can also conduct third-quadrant current in the on-state at a significantly lower voltage drop. Ideal-diode mode (IDM) is when an FET is controlled to block first-quadrant current by going to the off-state and conduct third-quadrant current by going to the on-state, thus achieving an *ideal* lower voltage drop.

FET off-state third-quadrant current flow is commonly seen in power converters, both in normal and fault situations. As explained in *GaN FET Operation Definitions*, GaN FETs do not have an intrinsic p-n junction body diode to conduct off-state third-quadrant current. Instead, the off-state third-quadrant voltage drop for the LMG3425R050 is several times higher than a p-n junction voltage drop, which can impact efficiency in normal operation and device ruggedness in fault conditions.

To mitigate efficiency degradation, the LMG3425R050 implements an operational ideal-diode mode (OP-IDM) function. Meanwhile, to improve device ruggedness in a GaN FET overtemperature fault situation, all devices in the LMG3425R050 family implement a GaN FET overtemperature-shutdown ideal-diode mode (OTSD-IDM) function as referenced in *Overtemperature Shutdown Protection*. Both the OP-IDM and OTSD-IDM features are described in more detail in the following sections.

7.3.10.1 Operational Ideal-Diode Mode

Operational ideal-diode mode (OP-IDM) is implemented in the LMG3425R050 but not in the LMG3422R050. Understand that the OP-IDM function is not a general-purpose ideal-diode mode function which allows the LMG3425R050 to autonomously operate as a diode, including as an autonomous synchronous rectifier. Furthermore, the OP-IDM function is not intended to support an ideal-diode mode transition from the on-state to the off-state in a high-voltage, hard-switched application. Exposing the LMG3425R050 to this situation is akin to operating a half-bridge power stage with negative dead time with corresponding high shoot-through current.

Instead, as described below, the LMG3425R050 OP-IDM function is narrowly implemented to address a specific off-state third-quadrant current flow situation while minimizing situations where the ideal-diode mode can create a dangerous shoot-through current event.

OP-IDM is intended to minimize GaN FET off-state third-quadrant losses that occur in a zero-voltage switched (ZVS) event. ZVS events are seen in applications such as synchronous rectifiers and LLC converters. The ZVS event occurs at the FET off-state to on-state transition when an inductive element discharges the FET drain voltage before the FET is turned-on. The discharge ends with the inductive element pulling the FET drain-source voltage negative and the FET conducting off-state third-quadrant current.

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Power supply controllers use dead-time control to set the time for the ZVS event to complete before turning on the FET. Both the ZVS time and resulting FET off-state third-quadrant current are a function of the power converter operation. Long ZVS time and low third-quadrant current occur when the inductive element is slewing the FET with low current and short ZVS time and high third-quadrant current occur when the inductive element is slewing at the FET with high current. Sophisticated controllers optimally adjust the dead time to minimize third-quadrant losses. Simpler controllers use a fixed dead time to handle the longest possible ZVS time. Thus, in a fixed dead-time application, the highest possible off-state third-quadrant losses occur for the longest possible time.

OP-IDM mitigates the losses in a fixed dead-time application by automatically turning on the GaN FET as soon as third-quadrant current is detected. In this sense, OP-IDM can be described as providing a turn-on assist function with optimum dead-time control. Meanwhile, OP-IDM is not intended to be used to turn-off the GaN FET in normal operation. OP-IDM turnoff capability is only provided as a protection mechanism to guard against shoot-through current.

OP-IDM works within the confines of normal LMG3425R050 switching operation as controlled by the IN pin. The key consideration for the OP-IDM operation is to ensure the turn-on assist function is only activated on the ZVS edge. For example, third-quadrant current is seen in a LMG3425R050 used as a synchronous rectifier both before the IN pin goes high to turn on the GaN FET and after the IN pin goes low to turn off the GaN FET. OP-IDM turns on the GaN FET before the IN pin goes high when OP-IDM detects third-quadrant current. But it would be a mistake for OP-IDM to turn the GaN FET back on right after IN has turned it off because OP-IDM detects third-quadrant current. If OP-IDM were to turn on the GaN FET in this situation, it would create a shoot-through current event when the opposite-side power switch turns on. OP-IDM avoids this shoot-through current problem on the turn-off edge by requiring the drain voltage to first go positive before looking for the ZVS event.

The OP-IDM state machine is shown in Figure 7-6. Each state is assigned a state number in the upper right side of the state box.

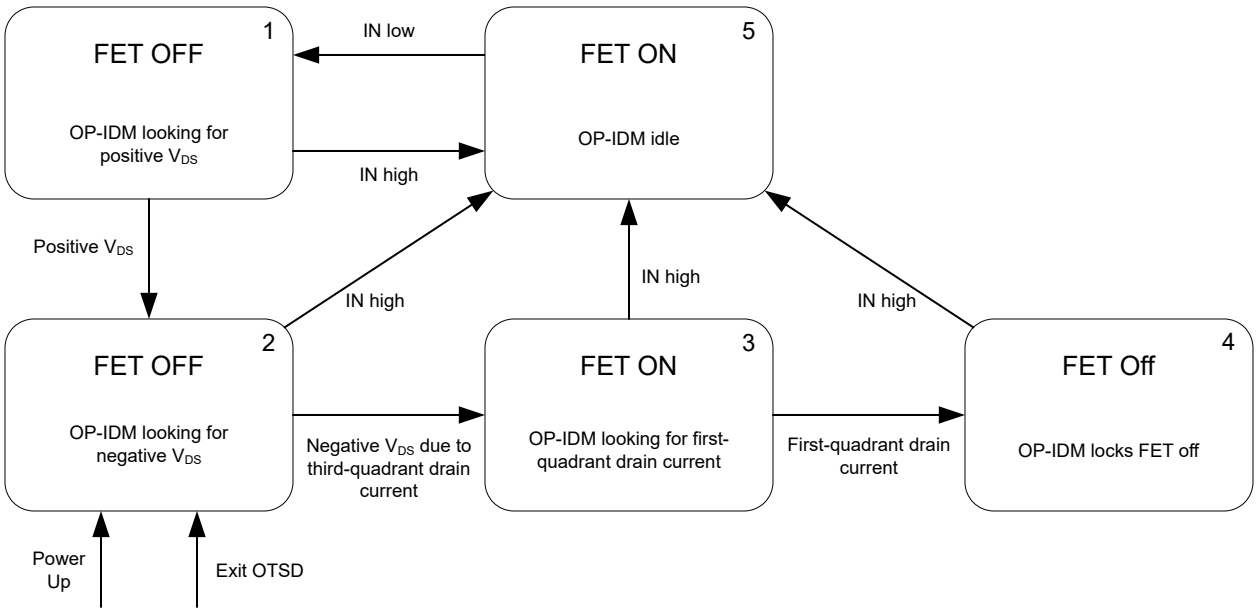

Figure 7-6. Operational Ideal-Diode Mode (OP-IDM) State Machine

1. A new OP-IDM cycle begins in OP-IDM state #1 after the IN pin goes low in OP-IDM state #5. OP-IDM turns off the GaN FET in OP-IDM state #1. OP-IDM monitors the GaN FET drain voltage, looking for a positive drain voltage to know it can now start looking for a ZVS event. After a positive GaN FET drain voltage is detected, the device moves to OP-IDM state #2.
2. OP-IDM keeps the GaN FET off in OP-IDM state #2. OP-IDM continues monitoring the GaN FET drain voltage. But this time it is looking for a negative drain voltage which means third-quadrant current is flowing

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after a ZVS event. This is also the starting state when the device powers up or exits OTSD. After a negative GaN FET drain voltage is detected, the device moves to OP-IDM state #3.

3. OP-IDM turns on the GaN FET in OP-IDM state #3. OP-IDM monitors the drain current in this state. Ideally, the device simply stays in this state until IN goes high. The drain current is monitored to protect against an unexpected shoot-through current event. If first-quadrant drain current is detected, the device moves to OP-IDM state #4.
4. OP-IDM locks the GaN FET off in OP-IDM state #4. The GaN FET only turns back on when the IN pin goes high.
5. The device moves to OP-IDM state #5 from any other state when the IN pin goes high. The GaN FET is commanded on in OP-IDM state #5. OP-IDM is idle in this state. A new OP-IDM switching cycle begins when IN goes low moving the device into OP-IDM state #1.

OP-IDM can only turn on the GaN FET once per IN cycle. If an unexpected shoot-through current is detected between OP-IDM turning on the GaN FET and the IN pin going high, OP-IDM locks the GaN FET off for the remainder of the IN cycle.

Understand that the OP-IDM function turns on the GaN FET, after IN goes low, if it sees a positive drain voltage followed by a negative drain voltage. A design using the LMG3425R030 must be analyzed for any situations where this sequence of events creates a shoot-through current event. The analysis must include all power system corner cases including start-up, shutdown, no load, overload, and fault events. Note that discontinuous mode conduction (DCM) operation can easily create an OP-IDM shoot-through current event when the ringing at the end of a DCM cycle triggers OP-IDM to turn on the GaN FET.

7.3.10.2 Overtemperature-Shutdown Ideal-Diode Mode

Overtemperature-shutdown ideal-diode mode (OTSD-IDM) is implemented in LMG3425R050. As explained in *Overtemperature Shutdown Protection*, ideal-diode mode provides the best GaN FET protection when the GaN FET is overheating.

OTSD-IDM accounts for all, some, or none of the power system operating when OTSD-IDM is protecting the GaN FET. The power system may not have the capability to shut itself down, in response to the LMG3425R050 asserting the $\overline{\text{FAULT}}$ pin in a GaN OTSD event, and just continue to try to operate. Parts of the power system can stop operating due to any reason such as a controller software bug or a solder joint breaking or a device shutting off to protect itself. At the moment of power system shutdown, the power system stops providing gate drive signals but the inductive elements continue to force current flow while they discharge.

The OTSD-IDM state machine is shown in Figure 7-7. Each state is assigned a state number in the upper right side of the state box. The OTSD-IDM state machine has a similar structure to the OP-IDM state machine. Similar states use the same state number.

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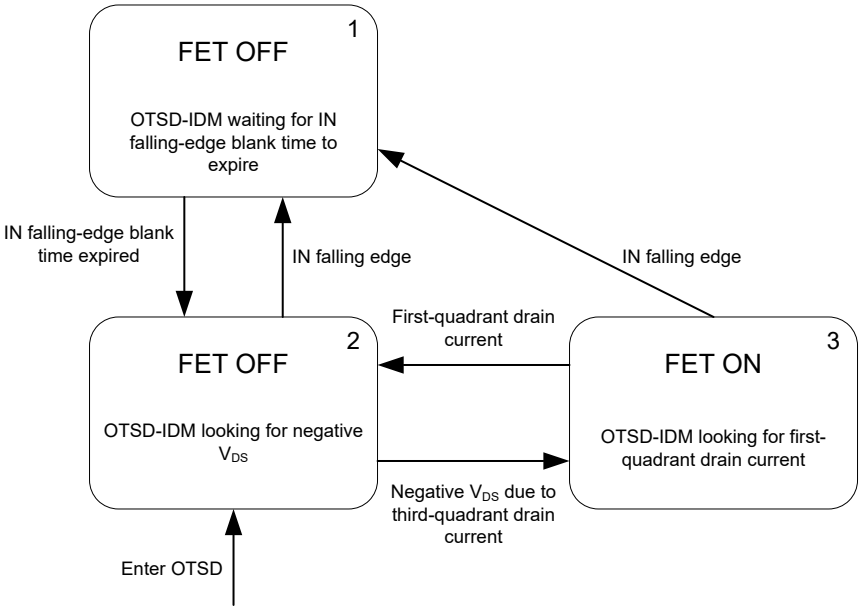

Figure 7-7. Overtemperature-Shutdown Ideal-Diode Mode (OTSD-IDM) State Machine

1. The LMG3425R050 GaN FET always goes to state #1 if a falling edge is detected on the IN pin. OTSD-IDM turns off the GaN FET in OTSD-IDM state #1. OTSD-IDM is waiting for the IN falling edge blank time to expire. This time gives the opposite-side FET time to switch to create a positive drain voltage. After the blank time expires, the device moves to OTSD-IDM state #2.
2. For OTSD-IDM state #2, OTSD-IDM keeps the GaN FET off if it is coming from OTSD-IDM state #1 and turns the GaN FET off if it is coming from OTSD-IDM state #3. OTSD-IDM is monitoring the GaN FET drain voltage in OP-IDM state #2. It is looking for a negative drain voltage which means third-quadrant current is flowing. This is also the starting state when the device enters OTSD. After a negative GaN FET drain voltage is detected, the device moves to OTSD-IDM state #3
3. OTSD-IDM turns on the GaN FET in OTSD-IDM state #3. OTSD-IDM monitors the drain current in this state. If first-quadrant drain current is detected, the device moves to OTSD-IDM state #2.

State #1 is used to protect against shoot-through current in a similar manner to OP-IDM state #1. The difference is that state #1 in the OTSD-IDM state machine waits for a fixed time period before proceeding to state #2. The fixed time period is to give the opposite-side switch time to switch and create a positive drain voltage. A fixed time is used to avoid a stuck condition for cases where a positive drain voltage is not created.

State #1 will help protect against shoot-through currents if the converter continues switching when the LMG3425R050 enters OTSD. Meanwhile, if the converter initiates switching with the LMG3425R050 already in OTSD, shoot-through current protection can be obtained by switching the OTSD device first to force it to progress though state #1. For example, the synchronous rectifier in a boost PFC can go into OTSD during initial input power application as the inrush current charges the PFC output cap. A shoot-through current event can be avoided if converter switching begins by switching the synchronous rectifier FET before switching the boost PFC FET.

If there is no IN signal, the state machine only moves between states #2 and #3 as a classic ideal-diode mode state machine. This allows all the inductive elements to discharge, when the power system shuts off, with minimum discharge stress created in the GaN FET.

Note that the OTSD-IDM state machine has no protection against repetitive shoot-through current events. There are degenerate cases, such as the LMG3425R050 losing its IN signal during converter operation, which can expose the OTSD-IDM to repetitive shoot-through current events. There is no good solution in this scenario. If OTSD-IDM did not allow repeated shoot-thru current events, the GaN FET would instead be exposed to excessive off-state third-quadrant losses.

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7.4 Start-Up Sequence

Figure 7-8 shows the start up sequence of LMG3425R050.

Time interval A: V_{DD} starts to build up. $\overline{FAULT}$ signal is initially pulled low.

Time interval B: After V_{DD} passes the UVLO threshold $V_{VDD,T+(UVLO)}$, both LDO5V and V_{NEG} start to built up. In a typical case where C_{LDO5V} = 100nF and C_{VNEG} = 2.2µF, LDO5V reaches its UVLO threshold earlier than V_{NEG}. The start-up time may vary if different capacitors are utilized. If V_{DD} has some glitches and falls below UVLO threshold $V_{VDD,T-(UVLO)}$ in this time interval, LDO5V and V_{NEG} will stop building up and only resume when V_{DD} goes above $V_{VDD,T+(UVLO)}$ again. A longer start-up time is expected in this case.

Time interval C: After LDO5V and V_{NEG} both reach their thresholds, the $\overline{FAULT}$ signal is cleared (pulled high) and the device is able to switch following the IN pin signal.

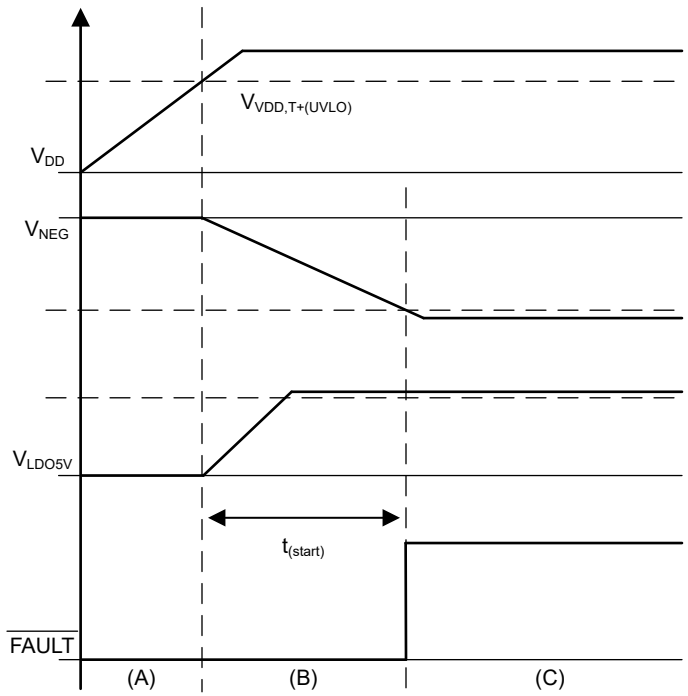

Figure 7-8. Start-Up Timing Diagram

7.5 Device Functional Modes

The device has one mode of operation that applies when operated within the Recommended Operating Conditions.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LMG3425R050 is a power IC targeting hard-switching and soft-switching applications operating up to 480V bus voltages. GaN devices offer zero reverse-recovery charge enabling high-frequency, hard-switching in applications like the totem-pole PFC. Low Q_{oss} of GaN devices also benefits soft-switching converters, such as the LLC and phase-shifted full-bridge configurations. As half-bridge configurations are the foundation of the two mentioned applications and many others, this section describes how to use the LMG3425R050 in a half-bridge configuration.

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8.2 Typical Application

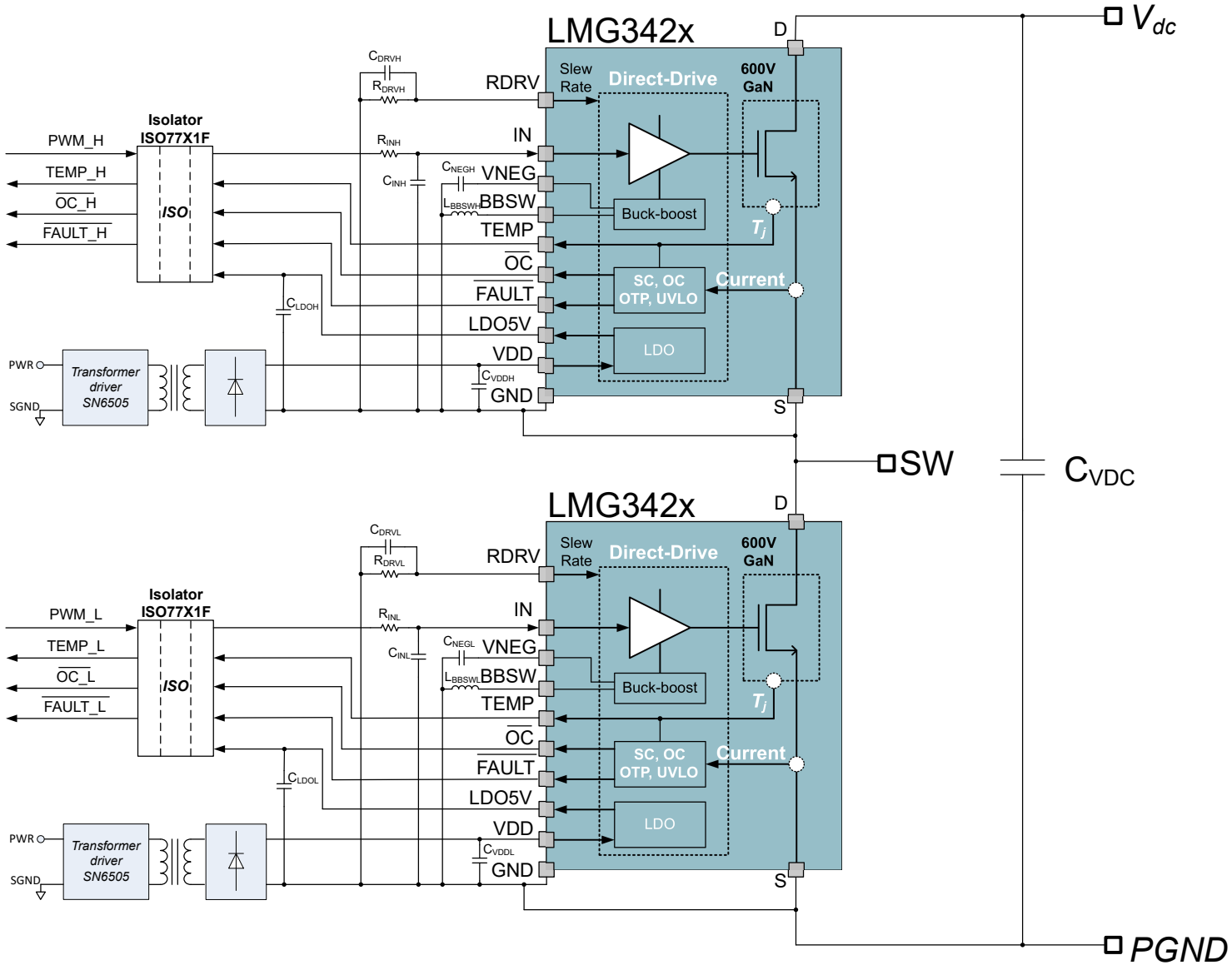

Figure 8-1. Typical Half-Bridge Application With Isolated Power Supply

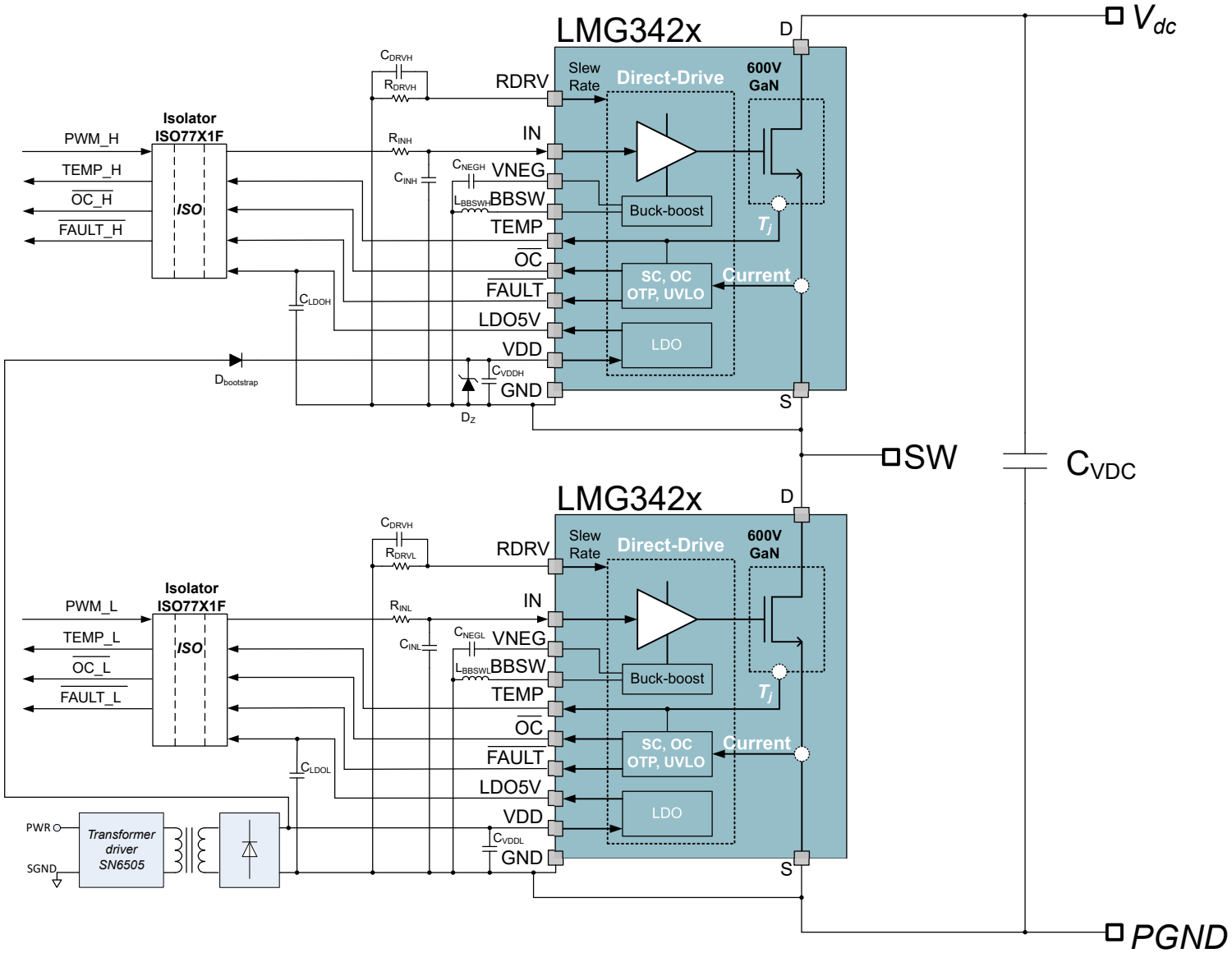

Figure 8-2. Typical Half-Bridge Application With Bootstrap

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8.2.1 Design Requirements

This design example is for a hard-switched boost converter which is representative of PFC applications. Table 8-1 shows the system parameters for this design.

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	200VDC
Output voltage	400VDC
Input (inductor) current	20A
Switching frequency	100kHz

8.2.2 Detailed Design Procedure

In high-voltage power converters, circuit design and PCB layout are essential for high-performance power converters. As designing a power converter is out of the scope of this document, this data sheet describes how to build well-behaved half-bridge configurations with the LMG3425R050.

8.2.2.1 Slew Rate Selection

The slew rate of LMG3425R050 can be adjusted between approximately 20 V/ns and 150V/ns by connecting a resistor, R_{RDRV}, from the RDRV pin to GND. The RDRV pin is a high-impedance node if a large R_{RDRV} resistor is used. Therefore it can be susceptible to coupling from the drain or other fast-slewing high-voltage nodes if it is not well-shielded. This will manifest itself as an unstable switching *dv/dt* and in extreme cases transient faults due to the RDRV being detected as open. Shielding the pin in the layout should be a priority, however if this coupling is still a problem, a cap of up to 1nF from RDRV to GND can be added to stabilize the pin voltage.

The slew rate affects GaN device performance in terms of:

- Switching loss
- Voltage overshoot
- Noise coupling
- EMI emission

Generally, high slew rates provide low switching loss, but high slew rates can also create higher voltage overshoot, noise coupling, and EMI emissions. Following the design recommendations in this data sheet helps mitigate the challenges caused by a high slew rate. The LMG3425R050 offers circuit designers the flexibility to select the proper slew rate for the best performance of their applications.

8.2.2.2 Signal Level-Shifting

In half-bridges, high-voltage level shifters or digital isolators must be used to provide isolation for signal paths between the high-side device and control circuit. Using an isolator is optional for the low-side device. However, using and isolator equalizes the propagation delays between the high-side and low-side signal paths, and provides the ability to use different grounds for the GaN device and the controller. If an isolator is not used on the low-side device, the control ground and the power ground must be connected at the device and nowhere else on the board. For more information, see *Layout Guidelines*. With fast-switching devices, common ground inductance can easily cause noise issues without the use of an isolator.

Choosing a digital isolator for level-shifting is important for improvement of noise immunity. As GaN device can easily create high dv/dt, > 50V/ns, in hard-switching applications, TI highly recommends to use isolators with high common-mode transient immunity (CMTI) and low barrier capacitance. Isolators with low CMTI can easily generate false signals, which could cause shoot-through. The barrier capacitance is part of the isolation capacitance between the signal ground and power ground, which is in direct proportion to the common mode current and EMI emission generated during the switching. Additionally, TI strongly encourages to select isolators which are not edge-triggered. In an edge-triggered isolator, a high dv/dt event can cause the isolator to flip states and cause circuit malfunction.

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Generally, ON/OFF keyed isolators with default output low are preferred, such as the TI ISO77xxF or ISO67xxF series. Default low state ensures the system will not shoot-through when starting up or recovering from fault events. As a high CMTI event would only cause a very short (a few nanoseconds) false pulse, TI recommends a low pass filter, like 300Ω and 22pF R-C filter, to be placed at the driver input to filter out these false pulses.

8.2.2.3 Buck-Boost Converter Design

Figure 8-3 and Figure 8-4 show the buck-boost converter efficiency versus load current with different inductors and peak current modes. A minimum inductance value of 3µH is preferred for the buck-boost converter so that the di/dt across the inductor is not too high. This leaves enough margin for the control loop to respond. As a result, the maximum di/dt of the inductor is limited to 6A/µs. On the other hand, large inductance also limits the transient response for stable output voltage, and it is preferred to have inductors less than 10µH.

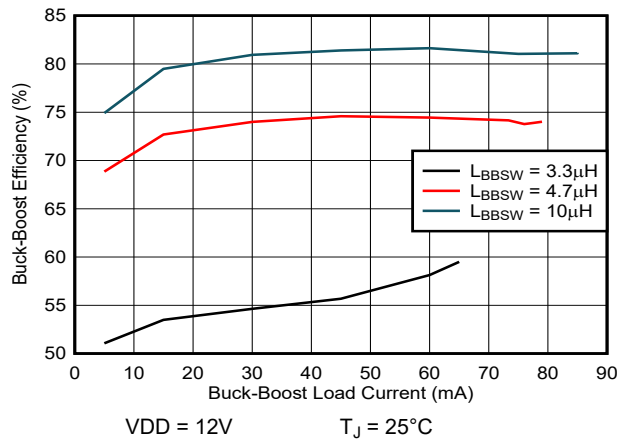

Figure 8-3. Buck-Boost Efficiency vs Load When $I_{BBSW,PK} = I_{BBSW,PK(low)}$

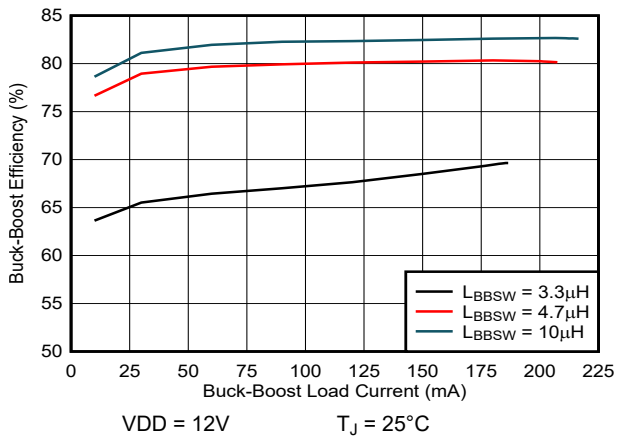

Figure 8-4. Buck-Boost Efficiency vs Load When $I_{BBSW,PK} = I_{BBSW,PK(high)}$

8.2.3 Application Curves

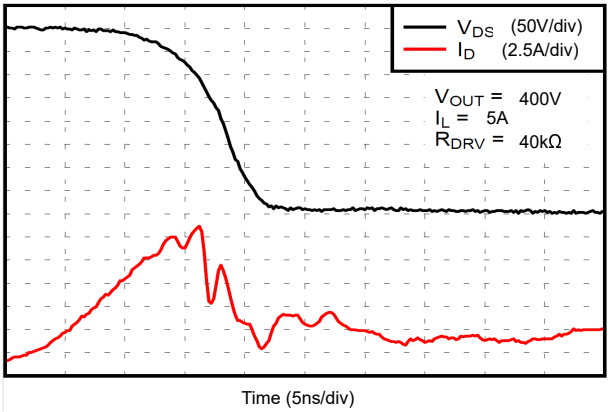

Figure 8-5. Turn-On Waveform in Application Example

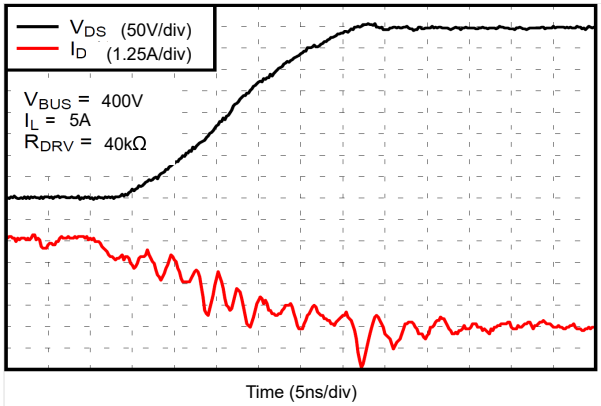

Figure 8-6. Turn-Off Waveform in Application Example

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8.3 Do's and Don'ts

The successful use of GaN devices in general, and LMG3425R050 in particular, depends on proper use of the device. When using the LMG3425R050, *DO*:

- Read and fully understand the data sheet, including the application notes and layout recommendations.
- Use a four-layer board and place the return power path on an inner layer to minimize power-loop inductance.
- Use small, surface-mount bypass and bus capacitors to minimize parasitic inductance.
- Use the proper size decoupling capacitors and locate them close to the IC as described in *Layout Guidelines*.
- Use a signal isolator to supply the input signal for the low-side device. If not, ensure the signal source is connected to the signal GND plane which is tied to the power source *only* at the LMG3425R050 IC.
- Use the $\overline{\text{FAULT}}$ pin to determine power-up state and to detect overcurrent and overtemperature events and safely shut off the converter.

To avoid issues in your system when using the LMG3425R050, *DON'T*:

- Use a single-layer or two-layer PCB for the LMG3425R050 as the power-loop and bypass capacitor inductances is excessive and prevent proper operation of the IC.
- Reduce the bypass capacitor values below the recommended values.
- Allow the device to experience drain transients above 600V as they can damage the device.
- Allow significant third-quadrant conduction when the device is OFF or unpowered, which can cause overheating. Self-protection features cannot protect the device in this mode of operation.
- Ignore the $\overline{\text{FAULT}}$ pin output.

8.4 Power Supply Recommendations

The LMG3425R050 only requires an unregulated VDD power supply from 7.5V to 18V. The low-side supply can be obtained from the local controller supply. The supply of the high-side device must come from an isolated supply or a bootstrap supply.

8.4.1 Using an Isolated Power Supply

Using an isolated power supply to power the high-side device has the advantage that it works regardless of continued power-stage switching or duty cycle. Using an isolated power supply can also power the high-side device before power-stage switching begins for a smooth start-up.

The isolated supply can be obtained with a push-pull converter, a flyback converter, a FlyBuck™ converter, or an isolated power module. When using an unregulated supply, the input of LMG3425R050 must not exceed the maximum supply voltage. A 16V TVS diode can be used to clamp the VDD voltage of LMG3425R050 for additional protection. Minimizing the inter-winding capacitance of the isolated power supply or transformer is necessary to reduce switching loss in hard-switched applications. Furthermore, capacitance across the isolated bias supply inject high currents into the signal-ground of the LMG3425R050 and can cause problematic ground-bounce transients. A common-mode choke can alleviate most of these issues.

8.4.2 Using a Bootstrap Diode

In half-bridge configuration, a floating supply is necessary for the high-side device. To obtain the best performance of LMG3425R050, TI highly recommends *Using an Isolated Power Supply*. A bootstrap supply can be used with the recommendations of this section.

8.4.2.1 Diode Selection

The LMG3425R050 offers no reverse-recovery charge and very limited output charge. Hard-switching circuits using the LMG3425R050 also exhibit high voltage slew rates. A compatible bootstrap diode must not introduce high output charge and reverse-recovery charge.

A silicon carbide diode, like the GB01SLT06-214, can be used to avoid reverse-recovery effects. The SiC diode has an output charge of 3nC. Althought there is additional loss from its output charge, it does not dominate the losses of the switching stage.

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8.4.2.2 Managing the Bootstrap Voltage

In a synchronous buck or other converter where the low-side switch occasionally operates in third-quadrant, the bootstrap supply charges through a path that includes the third-quadrant voltage drop of the low-side LMG3425R050 during the dead time as shown in Figure 8-7. This third-quadrant drop can be large, which can over-charge the bootstrap supply in certain conditions. The V_{DD} supply of LMG3425R050 must be kept below 18V.

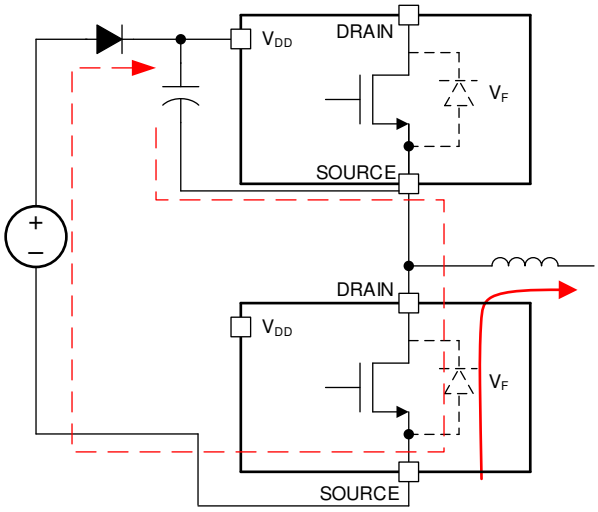

Figure 8-7. Charging Path for Bootstrap Diode

As shown in Figure 8-8, the recommended bootstrap supply includes a bootstrap diode, a series resistor, and a 16V TVS or zener diode in parallel with the V_{DD} bypass capacitor to prevent damaging the high-side LMG3425R050. The series resistor limits the charging current at start-up and when the low-side device is operating in third-quadrant mode. This resistor must be selected to allow sufficient current to power the LMG3425R050 at the desired operating frequency. At 100kHz operation, TI recommends a value of approximately 2Ω. At higher frequencies, this resistor value must be reduced or the resistor omitted entirely to ensure sufficient supply current.

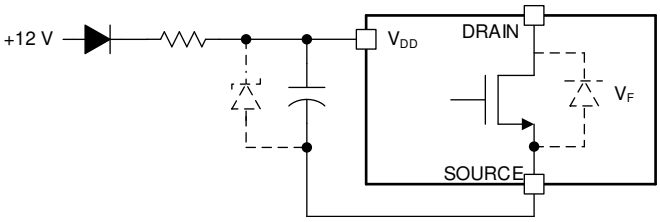

Figure 8-8. Suggested Bootstrap Regulation Circuit

8.5 Layout

8.5.1 Layout Guidelines

The layout of the LMG3425R050 is critical to its performance and functionality. Because the half-bridge configuration is typically used with these GaN devices, layout recommendations are considered with this configuration. A four-layer or higher layer count board is required to reduce the parasitic inductances of the layout to achieve suitable performance. Figure 8-9 summarizes the critical layout guidelines, and more details are further elaborated in the following sections.

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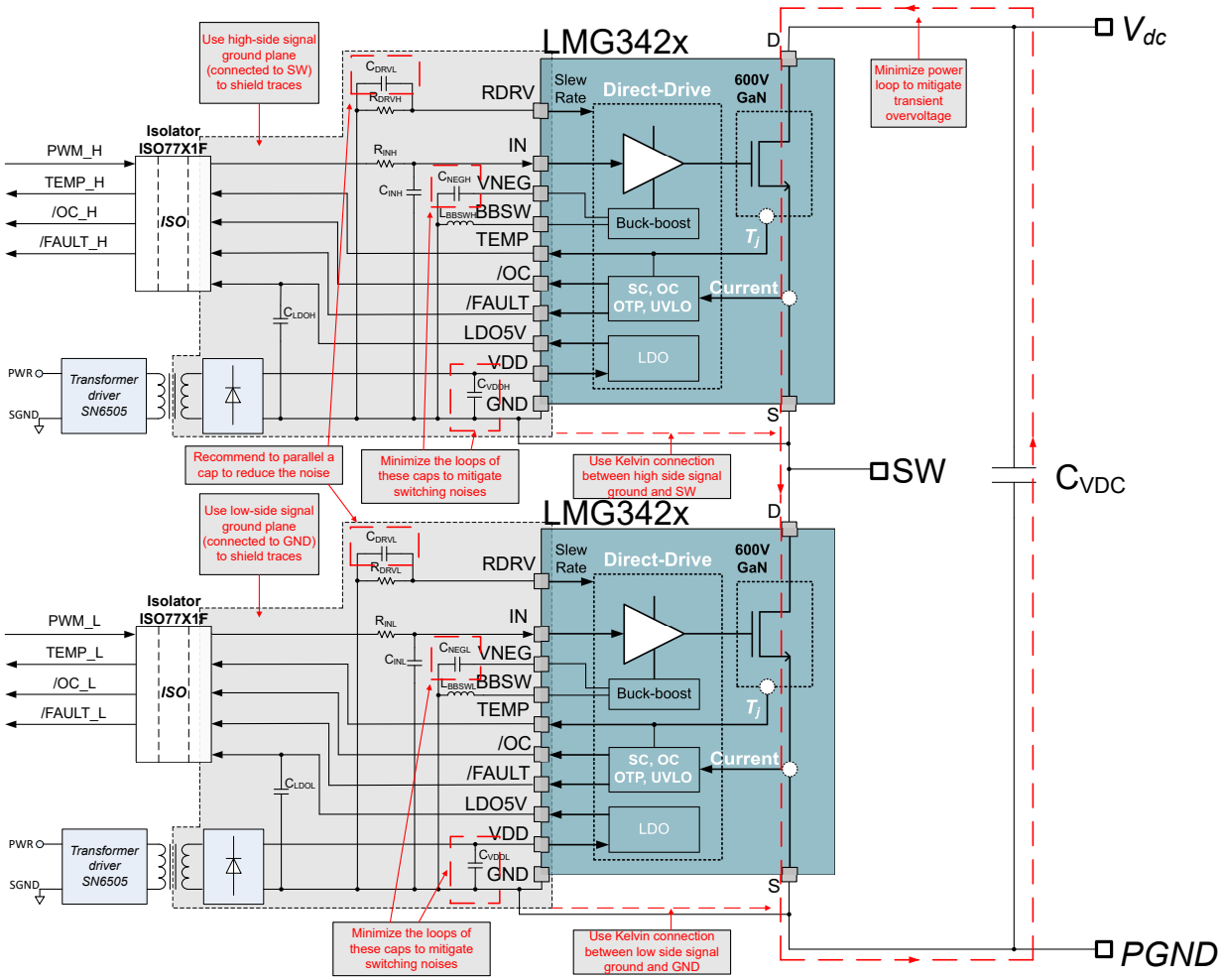

Figure 8-9. Typical Schematic With Layout Considerations

8.5.1.1 Solder-Joint Reliability

Large QFN packages can experience high solder-joint stress. TI recommends several best practices to ensure solder-joint reliability. First, the instructions for the NC1 and NC2 anchor pins found in Table 4-1 must be followed. Second, all the LMG3425R050 board solder pads must be non-solder-mask defined (NSMD) as shown in the land pattern example in *Mechanical, Packaging, and Orderable Information*. Finally, any board trace connected to an NSMD pad must be less than 2/3 the width of the pad on the pad side where it is connected. The trace must maintain this 2/3 width limit for as long as it is not covered by solder mask. After the trace is under solder mask, there are no limits on the trace dimensions. All these recommendations are followed in the *Layout Example*.

8.5.1.2 Power-Loop Inductance

The power loop, comprising of the two devices in the half bridge and the high-voltage bus capacitance, undergoes high *di/dt* during switching events. By minimizing the inductance of this loop, ringing and electromagnetic interference (EMI) can be reduced, as well as reducing voltage stress on the devices.

Place the power devices as close as possible to minimize the power-loop inductance. The decoupling capacitors are positioned in line with the two devices. They can be placed close to either device. In *Layout Examples*, the decoupling capacitors are placed on the same layer as the devices. The return path (PGND in this case) is located on second layer in close proximity to the top layer. By using inner layer and not bottom layer, the vertical dimension of the loop is reduced, thus minimizing inductance. A large number of vias near both the

device terminal and bus capacitance carries the high-frequency switching current to inner layer while minimizing impedance.

The power loop inductance can be estimated based on the ringing frequency f_{ring} of the drain-source voltage switching waveform based on the following equation:

$$L_{pl} = \frac{1}{4\pi^2 f_{ring}^2 C_{ring}} \tag{3}$$

where C_{ring} is equal to C_{OSS} at the bus voltage (refer to Figure 5-8 for the typical value) plus the drain-source parasitic capacitance from the board and load inductor or transformer.

As the parasitic capacitance of load components is hard to characterize, it is recommended to capture the V_{DS} switching waveform without load components to estimate the power loop inductance. Typically, the power loop inductance of the *Layout Example* is around 2.5nH.

8.5.1.3 Signal-Ground Connection

The LMG3425R050's SOURCE pin is internally connected to GND pins of the power IC, the signal-ground reference. Local signal-ground planes must be connected to GND pins with low impedance star connection. In addition, the return path for the passives associated to the driver (for example, bypass capacitance) must be connected to the GND pins. In *Layout Example*, local signal-ground planes are located on second layer to act as the return path for the local circuitry. The local signal-ground planes are not connected to the high-current SOURCE pins except the star connection at GND pins.

8.5.1.4 Bypass Capacitors

The gate drive loop impedance must be minimized to obtain good performance. Although the gate driver is integrated on package, the bypass capacitance for the driver is placed externally. As the GaN device is turned off to a negative voltage, the impedance of the path to the external VNEG capacitor is included in the gate drive loop. The VNEG capacitor must be placed close to VNEG and GND pins.

The VDD pin bypass capacitors, C1 and C11, must also be placed close to the VDD pin with low impedance connections.

8.5.1.5 Switch-Node Capacitance

GaN devices have very low output capacitance and switch quickly with a high *dv/dt*, yielding very low switching losses. To preserve this low switching losses, additional capacitance added to the output node must be minimized. The PCB capacitance at the switch node can be minimized by following these guidelines:

- Minimize overlap between the switch-node plane and other power and ground planes.
- Make the GND return path under the high-side device thinner while still maintaining a low-inductance path.
- Choose high-side isolator ICs and bootstrap diodes with low capacitance.
- Place the power inductor as close to the GaN device as possible.
- Power inductors must be constructed with a single-layer winding to minimize intra-winding capacitance.
- If a single-layer inductor is not possible, consider placing a small inductor between the primary inductor and the GaN device to effectively shield the GaN device from the additional capacitance.
- If a back-side heat-sink is used, use the least amount of area of the switch-node copper coverage on the bottom copper layer to improve the thermal dissipation.

8.5.1.6 Signal Integrity

The control signals to the LMG3425R050 must be protected from the high *dv/dt* caused by fast switching. Coupling between the control signals and the drain can cause circuit instability and potential destruction. Route the control signals (IN, $\overline{FAULT}$ and $\overline{OC}$) over a ground plane placed on an adjacent layer. In *Layout Example*, for example, all the signals are routed on layers close to the local signal ground plane.

Capacitive coupling between the traces for the high-side device and the static planes, such as PGND and HVBUS, could cause common mode current and ground bounce. The coupling can be mitigated by reducing

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overlap between the high-side traces and the static planes. For the high-side level shifter, ensure no copper from either the input or output side extends beneath the isolator or the CMTI of the device can be compromised.

8.5.1.7 High-Voltage Spacing

Circuits using the LMG3425R050 involve high voltage, potentially up to 600V. When laying out circuits using the LMG3425R050, understand the creepage and clearance requirements for the application and how they apply to the GaN device. Functional (or working) isolation is required between the source and drain of each transistor, and between the high-voltage power supply and ground. Functional isolation or perhaps stronger isolation (such as reinforced isolation) can be required between the input circuitry to the LMG3425R050 and the power controller. Choose signal isolators and PCB spacing (creepage and clearance) distances which meet your isolation requirements.

If a heat sink is used to manage thermal dissipation of the LMG3425R050, ensure necessary electrical isolation and mechanical spacing is maintained between the heat sink and the PCB.

8.5.1.8 Thermal Recommendations

The LMG3425R050 is a lateral device grown on a Si substrate. The thermal pad is connected to the source of device. The LMG3425R050 can be used in applications with significant power dissipation, for example, hard-switched power converters. In these converters, cooling using just the PCB can not be sufficient to keep the part at a reasonable temperature. To improve the thermal dissipation of the part, TI recommends a heat sink is connected to the back of the PCB to extract additional heat. Using power planes and numerous thermal vias, the heat dissipated in the LMG3425R050 can be spread out in the PCB and effectively passed to the other side of the PCB. A heat sink can be applied to bare areas on the back of the PCB using an thermal interface material (TIM). The solder mask from the back of the board underneath the heat sink can be removed for more effective heat removal.

Refer to the *High Voltage Half Bridge Design Guide for LMG3410 Smart GaN FET* application note for more recommendations and performance data on thermal layouts.

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8.5.2 Layout Examples

Correct layout of the LMG3425R050 and its surrounding components is essential for correct operation. The layouts shown here reflect the GaN device schematic in Figure 8-1. These layouts are shown to produce good results and is intended as a guideline. However, it can be possible to obtain acceptable performance with alternate layout schemes. Additionally, please refer to the land pattern example in *Mechanical, Packaging, and Orderable Information* for the latest recommended PCB footprint of the device.

The the top-layer layout and mid-layer layout are shown. The layouts are zoomed in to the LMG3425R050 U1 and U2 component placements. The mid-layer layout includes the outlines of the top level components to assist the reader in lining up the top-layer and mid-layer layouts.

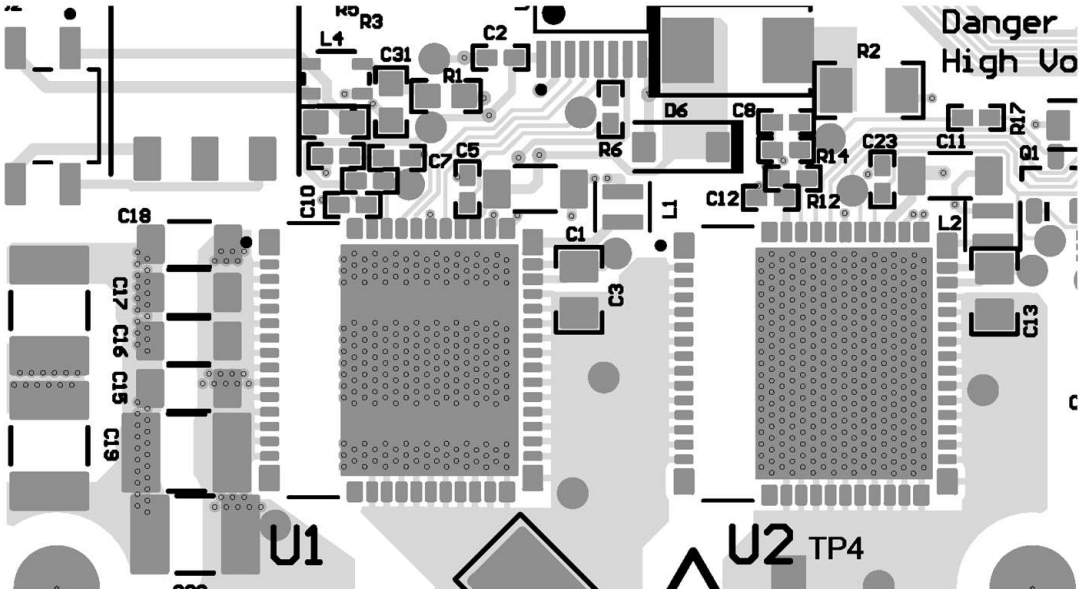

Figure 8-10. Half-Bridge Top-Layer Layout

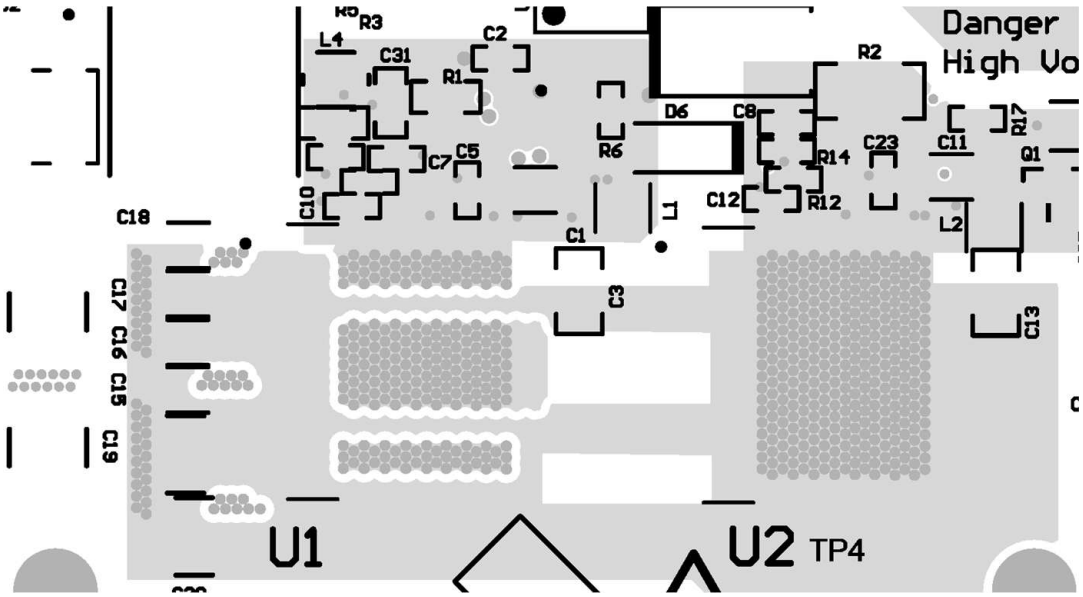

Figure 8-11. Half-Bridge Mid-Layer Layout

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9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

- Texas Instruments, *High Voltage Half Bridge Design Guide for LMG3410 Smart GaN FET* application note
- Texas Instruments, *A New Approach to Validate GaN FET Reliability to Power-line Surges Under Use-conditions*
- Texas Instruments, *Achieving GaN Products With Lifetime Reliability*
- Texas Instruments, *Direct-drive configuration for GaN devices*

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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9.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2024	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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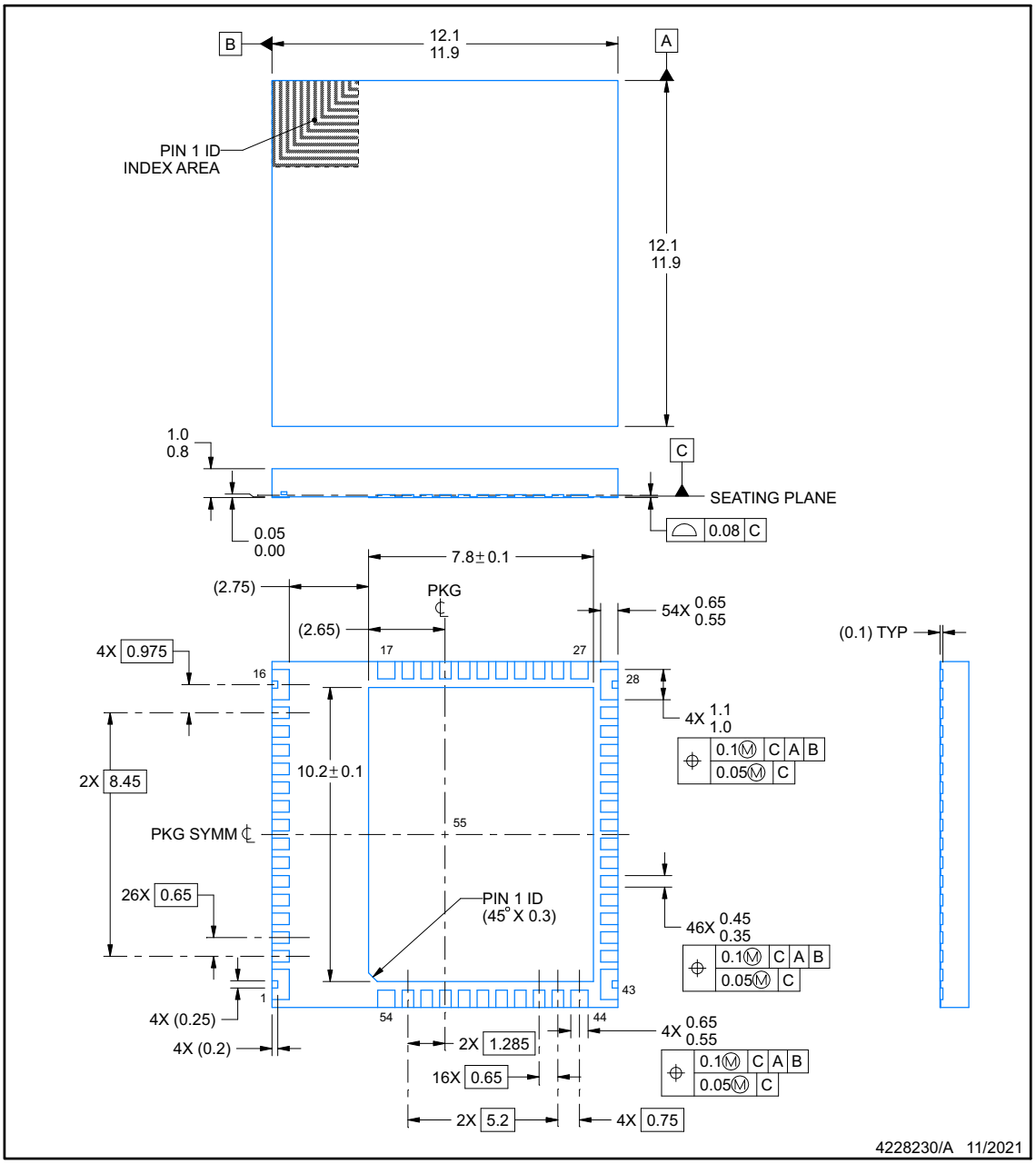
PACKAGE OUTLINE

RQZ0054A-C01

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

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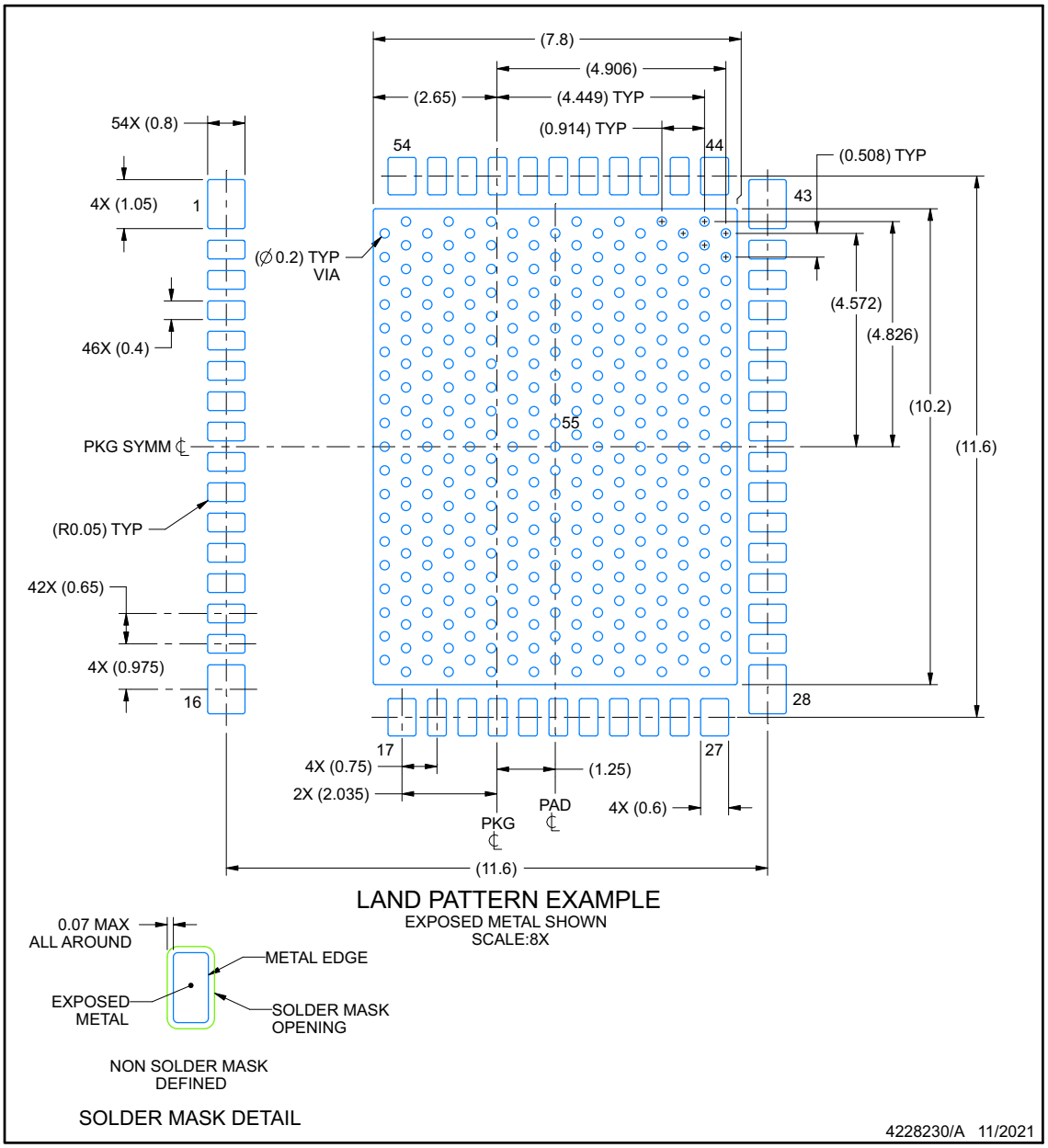
EXAMPLE BOARD LAYOUT

RQZ0054A-C01

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. All pads must be NSMD for mechanical performance, refer to the device datasheet for trace connection recommendations to the pads.
6. Filling the thermal pad with thermal vias is recommended for thermal performance, refer to the device datasheet. Vias must be filled and planarized.

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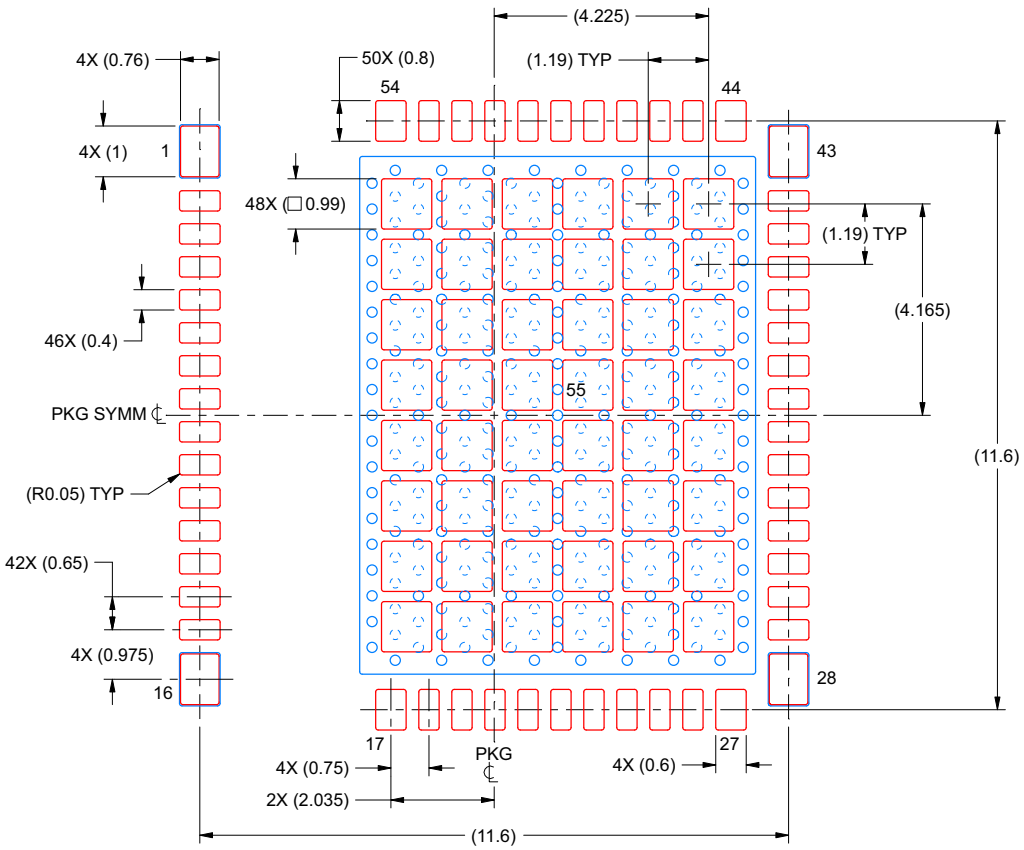
EXAMPLE STENCIL DESIGN

RQZ0054A-C01

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 1, 16, 28 & 43: 90%
PAD 55: 60%
SCALE:8X

4228230/A 11/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMG3425R050RQZR	Active	Production	VQFN (RQZ) | 54	2000 | LARGE T&R	ROHS Exempt	NIPDAU	Level-3-260C-168 HR	-40 to 150	LMG3425 R050
LMG3425R050RQZR.A	Active	Production	VQFN (RQZ) | 54	2000 | LARGE T&R	ROHS Exempt	NIPDAU	Level-3-260C-168 HR	-40 to 150	LMG3425 R050
LMG3425R050RQZR.B	Active	Production	VQFN (RQZ) | 54	2000 | LARGE T&R	ROHS Exempt	NIPDAU	Level-3-260C-168 HR	-40 to 150	LMG3425 R050
LMG3425R050RQZT	Active	Production	VQFN (RQZ) | 54	250 | SMALL T&R	ROHS Exempt	NIPDAU	Level-3-260C-168 HR	-40 to 150	LMG3425 R050
LMG3425R050RQZT.A	Active	Production	VQFN (RQZ) | 54	250 | SMALL T&R	ROHS Exempt	NIPDAU	Level-3-260C-168 HR	-40 to 150	LMG3425 R050
LMG3425R050RQZT.B	Active	Production	VQFN (RQZ) | 54	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 150	LMG3425 R050

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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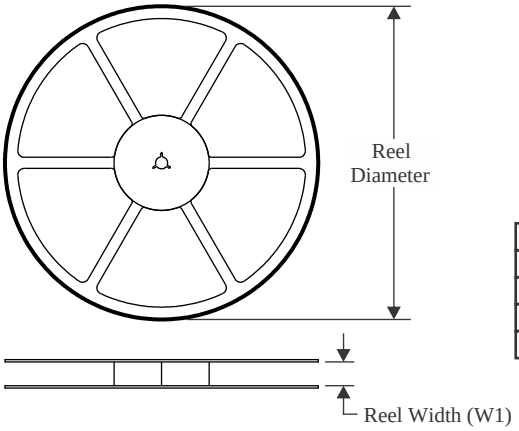
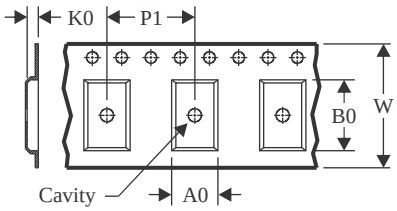
TAPE AND REEL INFORMATION

REEL DIMENSIONS

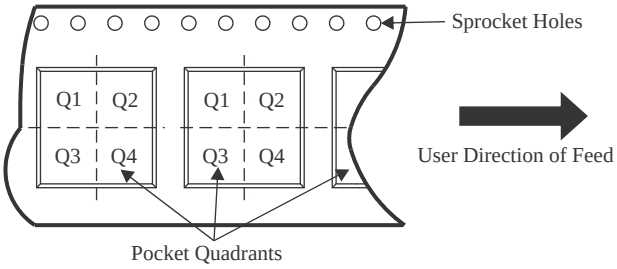


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

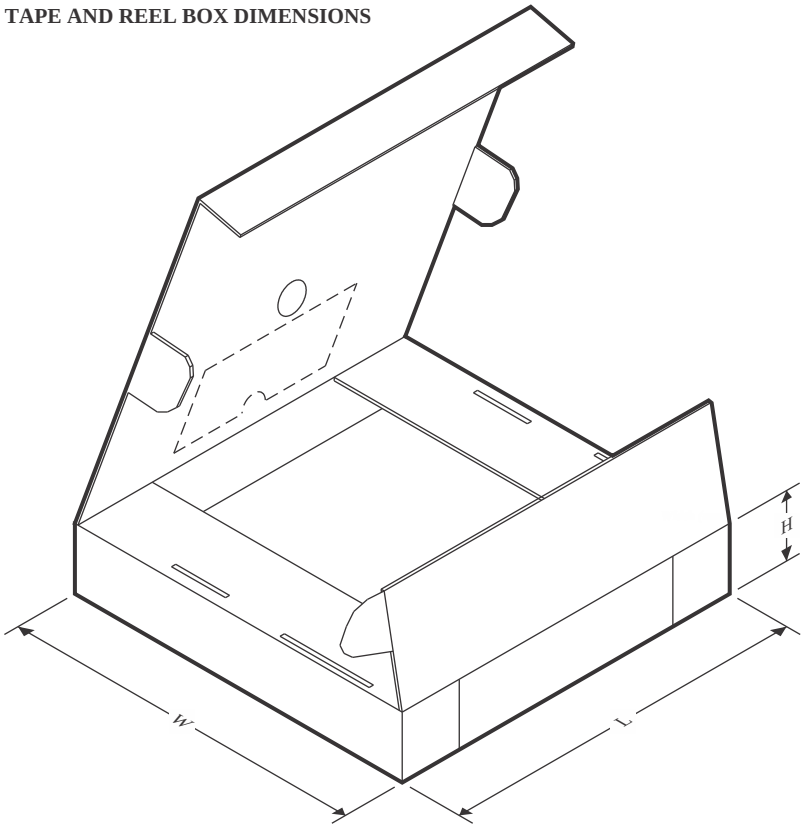
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMG3425R050RQZR	VQFN	RQZ	54	2000	330.0	24.4	12.35	12.35	1.5	16.0	24.0	Q2
LMG3425R050RQZT	VQFN	RQZ	54	250	180.0	24.4	12.35	12.35	1.5	16.0	24.0	Q2

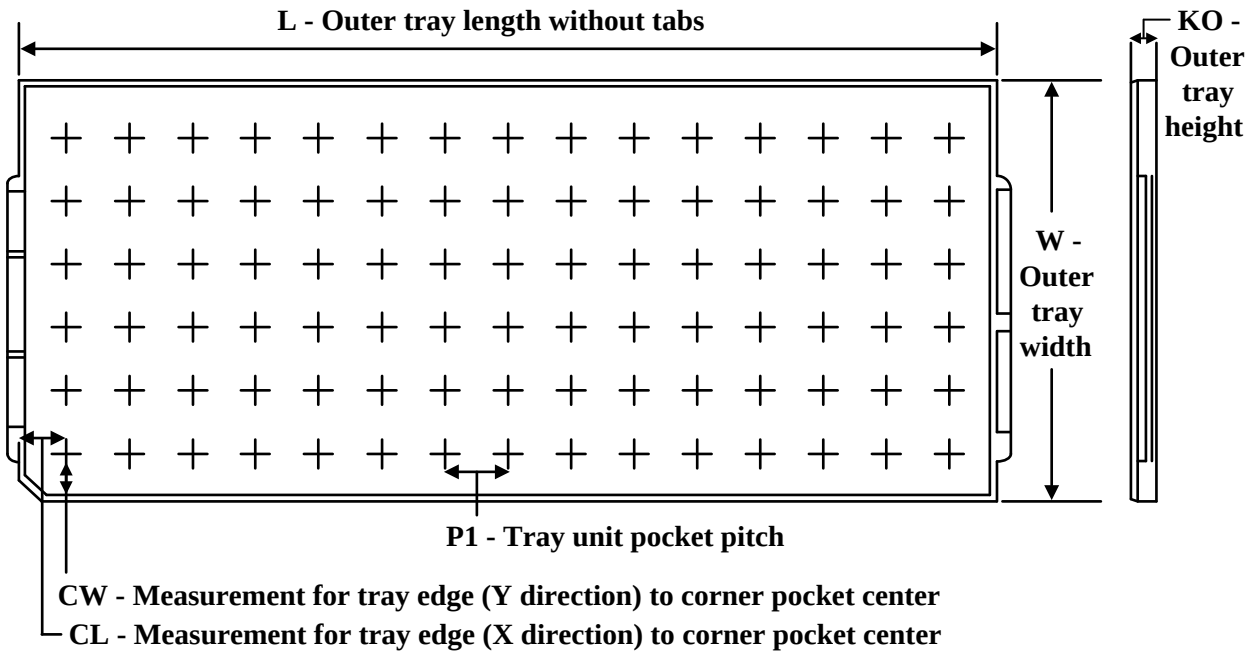
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMG3425R050RQZR	VQFN	RQZ	54	2000	350.0	350.0	43.0
LMG3425R050RQZT	VQFN	RQZ	54	250	213.0	191.0	55.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
LMG3425R050RQZR	RQZ	VQFN	54	2000	8 x 21	180	322.6	135.9	7620	14.65	11	11.95
LMG3425R050RQZR.A	RQZ	VQFN	54	2000	8 x 21	180	322.6	135.9	7620	14.65	11	11.95
LMG3425R050RQZR.B	RQZ	VQFN	54	2000	8 x 21	180	322.6	135.9	7620	14.65	11	11.95
LMG3425R050RQZT	RQZ	VQFN	54	250	8 x 21	180	322.6	135.9	7620	14.65	11	11.95
LMG3425R050RQZT.A	RQZ	VQFN	54	250	8 x 21	180	322.6	135.9	7620	14.65	11	11.95
LMG3425R050RQZT.B	RQZ	VQFN	54	250	8 x 21	180	322.6	135.9	7620	14.65	11	11.95

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