LM3243 High-Current Step-Down Converter for 2G, 3G, and 4G RF Power Amplifiers

1 Features

- Input Voltage Range: 2.7 V to 5.5 V
- High-Efficiency PFM and PWM Modes With Internal Synchronous Rectification
- Analog Bypass Function with Low Dropout Resistance (45 mΩ Typical)
- Dynamically Adjustable Output Voltage: 0.4 V to 3.6 V (Typical) in PFM and PWM Modes
- Maximum Load Current: 2.5 A in PWM Mode
- PWM Switching Frequency: 2.7 MHz (Average)
- Modulated Switching Frequency to Aid Rx Band Compliance
- Operates From a Single Li-ion Cell (2.7 V to 5.5 V)
- Current and Thermal Overload Protection
- ACB Reduces Inductor Requirements and Size
- Minimum Total Solution Size by Using Small Footprint and Case Size Inductor and Capacitors

2 Applications

- Cellular Phones
- Hand-Held Radios
- RF PC Cards
- Battery-Powered RF Devices

3 Description

The LM3243 is a DC-DC converter optimized for powering multi-mode 2G, 3G, and 4G RF power amplifiers (PAs) from a single Lithium-Ion cell. The LM3243 steps down an input voltage from 2.7 V to 5.5 V to a dynamically adjustable output voltage of 0.4 V to 3.6 V. The output voltage is set through a VCON analog input that adjusts the output voltage to ensure efficient operation at all power levels of the RF PA.

The LM3243 operates in constant frequency PWM mode producing a small and predictable amount of output voltage ripple. This enables best ECTEL power requirements in GMSK and EDGE spectral compliance, with the minimal amount of filtering and excess headroom. When operating in PFM mode, the LM3243 enables the lowest DG09 current consumption and therefore maximizes system efficiency.

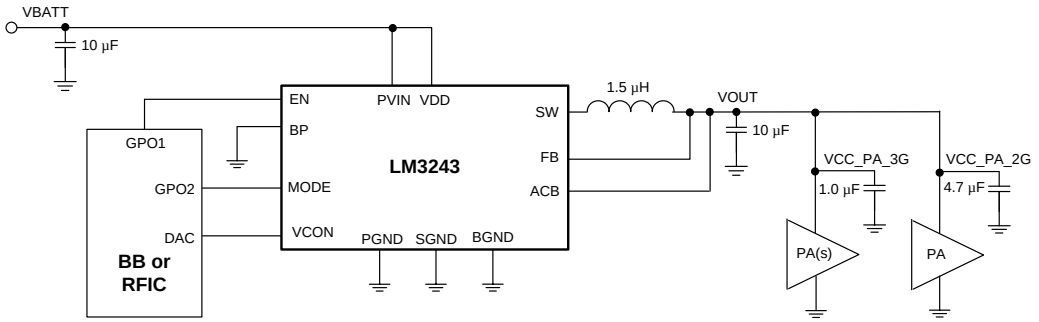
The LM3243 has a unique *A*ctive *C*urrent assist and analog *B*ypass (ACB) feature to minimize inductor size without any loss of output regulation for the entire battery voltage and RF output power range, until dropout. ACB provides a parallel current path, when needed, to limit the maximum inductor current to 1.4 A (typical) while still driving a 2.5-A load. The ACB also enables operation with minimal dropout voltage. When considering using the LM3243 in a system design, see the *Layout* section of this data sheet.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (MAX)
LM3243	DSBGA (16)	2.049 mm × 2.049 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical System Application Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (February 2013) to Revision C	Page
• Added *Device Information* and *Pin Configuration and Functions* sections, ESD Rating table, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections	1

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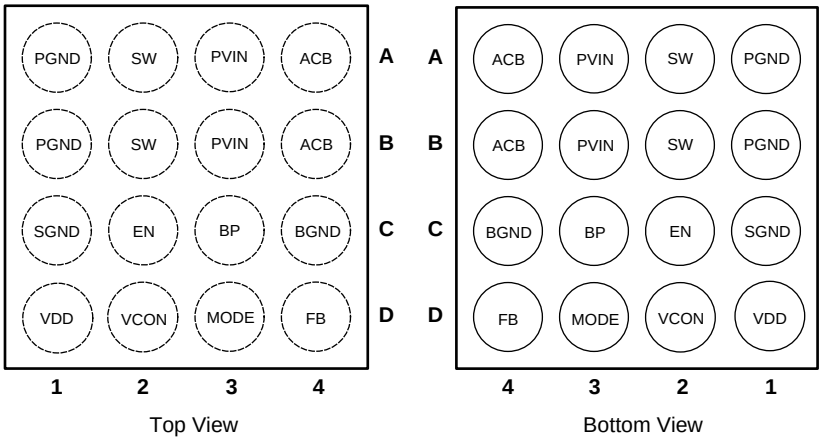
5 Pin Configuration and Functions

TMD Package
16-Pin DSBGA



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
A1	PGND	Ground	Power ground to the internal NFET switch.
B1			
C1	SGND	Ground	Signal analog and control ground (low current).
D1	VDD	Power	Analog supply input.
A2	SW	Analog	Switching node connection to the internal PFET switch and NFET synchronous rectifier. Connect to an inductor with a saturation current rating that exceeds the $I_{LIM,PFET,Steady\ State}$ current limit specification of the LM3243.
B2			
C2	EN	Digital/Input	Enable input. Set this digital input HIGH for normal operation. For shutdown, set low. Pin has an 800-kΩ internal pulldown resistor.
D2	VCON	Analog	Voltage control analog input. V_{OUT} = 2.5 × VCON.
A3	PVIN	Power	Power supply voltage input to the internal PFET switch and ACB.
B3			
C3	BP	Digital	Bypass mode input. Set the pin HIGH for forced Bypass mode operation. Set the pin LOW for automatic analog bypass mode (recommended).
D3	MODE	Digital/Input	PWM/PFM mode selection input. Setting the pin HIGH allows for PFM or PWM, depending on the load current. Setting the pin LOW forces the part to be in PWM only.
A4	ACB	Output	Analog Current Bypass (ACB). Connect to the output at the output filter capacitor.
B4			
C4	BGND	Ground	ACB ground (high current).
D4	FB	Analog	Feedback analog input. Connect to the output at the output filter capacitor.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1][2][3]

	MIN	MAX	UNIT
VDD, PVIN to SGND	−0.2	6	V
PGND to SGND	−0.2	0.2	V
EN, FB, VCON, BP, MODE	(SGND − 0.2)	(VDD + 0.2)	V
SW, ACB	(PGND − 0.2)	(PVIN + 0.2)	V
PVIN to VDD	−0.2	0.2	V
Continuous power dissipation[4]	Internally limited		
Junction temperature, T_{J-MAX}		150	°C
Maximum lead temperature (soldering, 10 sec)		150	°C
Storage temperature, T_{stg}	−65°	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) *Absolute Maximum Ratings* indicate limits beyond which damage to the component may occur. *Recommended Operating Conditions* are conditions under which operation of the device is specified. Operating Ratings do not imply verified performance limits. For performance limits and associated test conditions, see *Electrical Characteristics* .
(3) All voltages are with respect to the potential at the GND pins. The LM3243 is designed for mobile phone applications where turnon after power-up is controlled by the system controller and where requirements for a small package size overrule increased die size for internal undervoltage lock-out (UVLO) circuitry. Thus, it should be kept in shutdown by holding the EN pin LOW until the input voltage exceeds 2.7 V.
(4) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typical) and disengages at T_J = 130°C (typical).

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1][2]

	MIN	NOM	MAX	UNIT
Input voltage	2.7		5.5	V
Recommended load current			2.5	A
Junction temperature, T_J	−30		125	°C
Ambient temperature, T_A[3]	−30		90	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pins. The LM3243 is designed for mobile phone applications where turnon after power up is controlled by the system controller and where requirements for a small package size overrule increased die size for internal undervoltage lock-out (UVLO) circuitry. Thus, it should be kept in shutdown by holding the EN pin LOW until the input voltage exceeds 2.7 V.
(3) In applications where high-power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be de-rated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (R_{\theta JA} \times P_{D-MAX})$. At higher power levels duty cycle usage is assumed to drop (that is, max power 12.5% usage is assumed) for 2G mode.

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6.4 Thermal Information

THERMAL METRIC[1]		LM3243 TMD (DSBGA) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	50	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Unless otherwise noted, all specifications apply to Typical System Application Diagram with: PVIN = VDD = EN = 3.8 V, BP = 0 V. All typical (TYP) limits apply for $T_A = T_J = 25°C$, and all minimum (MIN) and maximum (MAX) apply over the full operating ambient temperature range (−30°C ≤ $T_A = T_J$ ≤ +90°C), unless otherwise specified.[1][2][3]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{FB,\ LOW}$	Feedback voltage at low setting	VCON = 0.16 V, MODE = LOW[3]	0.35	0.40	0.45	V
$V_{FB,\ HIGH}$	Feedback voltage at high setting	VCON = 1.44 V, V_{IN} = 3.9 V, MODE = LOW[3]	3.492	3.6	3.708	V
I_{SHDN}	Shutdown supply current	EN = SW = VCON = 0 V[4]		0.02	4	µA
I_{q_PFM}	DC bias current into VDD	No switching[5] MODE = HIGH		260	310	µA
I_{q_PWM}	DC bias current into VDD	No switching[5] MODE = LOW		975	1100	µA
$I_{LIM,PFET,Transient}$	Positive transient peak current limit	VCON = 0.6 V[6]		1.9	2.1	A
$I_{LIM,PFET,Steady\ State}$	Positive steady-state peak current limit	VACB = 3.05 V VCON = 0.6 V[6]	1.34	1.45	1.65	A
$I_{LIM,\ P_ACB}$	Positive active current assist peak current limit	VCON = 0.6 V, VACB = 2.8 V[6]	1.4	1.7	2	A
$I_{LIM,\ NFET}$	NFET switch negative peak current limit	VCON = 1 V[6]	−1.69	−1.50	−1.31	A
F_{OSC}	Average Internal oscillator frequency	VCON = 1 V	2.43	2.7	2.97	MHz
V_{IH}	Logic HIGH input threshold	BP, EN, MODE	1.2			V
V_{IL}	Logic LOW input threshold	BP, EN, MODE			0.5	V
I_{EN}	EN pin pulldown current	EN = 3.6 V	0	5	10	µA
I_{IN}	Pin input current	BP, MODE	–1		1	µA
I_{VCON}	VCON pin leakage current	VCON = 1 V	–1		1	µA
Gain	VCON to V_{OUT} Gain	0.16 V ≤ VCON ≤ 1.44 V[7]		2.5		V/V

(1) All voltages are with respect to the potential at the GND pins. The LM3243 is designed for mobile phone applications where turnon after power up is controlled by the system controller and where requirements for a small package size overrule increased die size for internal undervoltage lock-out (UVLO) circuitry. Thus, it should be kept in shutdown by holding the EN pin LOW until the input voltage exceeds 2.7 V.
(2) Minimum and Maximum limits are specified by design, test, or statistical analysis.
(3) The parameters in the electrical characteristics table are tested under open loop conditions at PVIN = VDD = 3.8 V. For performance over the input voltage range and closed-loop results, refer to the datasheet curves.
(4) Shutdown current includes leakage current of PFET.
(5) I_q specified here is when the part is not switching. For operating input current at no load, refer to datasheet curves.
(6) Current limit is built-in, fixed, and not adjustable.
(7) Linearity limits are ±3% or ±50 mV, whichever is larger.

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6.6 System Characteristics

The following spec table entries are specified by design and verifications providing the component values in the Typical System Application Diagram are used (L = 1.5 µH, DCR = 120 mΩ, TOKO DFE201610C-1R5N, C_{IN} = 10 µF, 6.3 V, 0402, Samsung CL05A106MQ5NUN, C_{OUT} = 10 µF + 4.7 µF + 3 × 1 µF + 3300 pF: 6.3 V, 0402, Samsung CL05A106MQ5NUN, CL05A475MQNRN; 6.3 V, 0201 Samsung CL03A105MQ3CSN; 6.3 V, 01005 Murata GRM022R60J332K). *These parameters are not verified by production testing.* Minimum (MIN) and maximum (MAX) values are specified over the ambient temperature range T_A = −30°C to 90°C. Typical (TYP) values are specified at PVIN = VDD = EN = 3.8 V, BP = 0 V and T_A = 25°C unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{tot_drop}	Total dropout resistance in bypass mode	VCON = 1.5 V Max value at V_{IN} = 3.1 V Inductor ESR ≤ 151 mΩ		45	55	mΩ
C_{IN}	Pin input capacitance for BP, EN, MODE	Test frequency = 100 KHz		5		pF
I_{OUT}	Maximum load current in PWM mode	Switcher + ACB	2.5			A
$I_{OUT,\ PU}$	Maximum output transient pullup current limit	Switcher + ACB(1)	3			A
$I_{OUT,\ PD,\ PWM}$	PWM maximum output transient pulldown current limit	Switcher + ACB(1)			−3	A
$I_{OUT,\ MAX\text{-}PFM}$	Maximum output load current in PFM mode	V_{IN} = 3.8 V, VCON < 1 MODE = HIGH(1)	85			mA
Linearity	Linearity in control range of VCON = 0.16 V to 1.44 V	V_{IN} = 4.2 V(2) Monotonic in nature	−3%		3%	
Linearity	Linearity in control range of VCON = 0.16 V to 1.44 V	V_{IN} = 4.2 V(2) Monotonic in nature	−50		50	mV
η	Efficiency	V_{IN} = 3.8 V, V_{OUT} = 1.8 V I_{OUT} = 10 mA MODE = HIGH (PFM)	79%	82%		
η	Efficiency	V_{IN} = 3.8 V, V_{OUT} = 0.5 V I_{OUT} = 5 mA MODE = HIGH (PFM)	58%	60%		
η	Efficiency	V_{IN} = 3.8 V, V_{OUT} = 3.5 V I_{OUT} = 1900 mA MODE = LOW (PWM)	89%	92%		
η	Efficiency	V_{IN} = 3.8 V, V_{OUT} = 2.5 V I_{OUT} = 250 mA MODE = LOW (PWM)	90%	93%		
η	Efficiency	V_{IN} = 3.8 V, V_{OUT} = 1.6 V I_{OUT} = 130 mA MODE = LOW (PWM)	83%	86%		
η	Efficiency	V_{IN} = 3.8 V, V_{OUT} = 1 V I_{OUT} = 400 mA MODE = LOW (PWM)	81%	84%		
V_{RIPPLE}	Ripple voltage at no pulse skipping condition	V_{IN} = 0.4 V to 3.6 V V_{OUT} = 0.4 V to 3.6 V, R_{OUT} = 1.9 Ω(3) MODE = LOW		1	3	mVpp
V_{RIPPLE}	Ripple voltage at pulse skipping condition	V_{IN} = 5.5 V to dropout, V_{OUT} = 3.6 V, R_{OUT} = 1.9 Ω(3)			8	mVpp
V_{RIPPLE}	PFM ripple voltage	V_{IN} = 3.2 V, V_{OUT} < 1.125 V I_{OUT} =10 mA, MODE = HIGH			50	mVpp
V_{RIPPLE}	PFM ripple voltage	V_{IN} = 3.2 V, V_{OUT} ≤ 0.5 V, I_{OUT} = 5 mA MODE = HIGH			50	mVpp
Line_tr	Line transient response	V_{IN} = 3.6 V to 4.2 V, T_R = T_F = 10 µs, V_{OUT} = 1 V I_{OUT} = 600 mA, MODE = LOW		50		mVpk

(1) Current limit is built-in, fixed, and not adjustable.
(2) Linearity limits are ±3% or ±50 mV, whichever is larger.
(3) Ripple voltage should be measured at C_{OUT} electrode on a well-designed PC board and using the suggested inductor and capacitors.

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System Characteristics (continued)

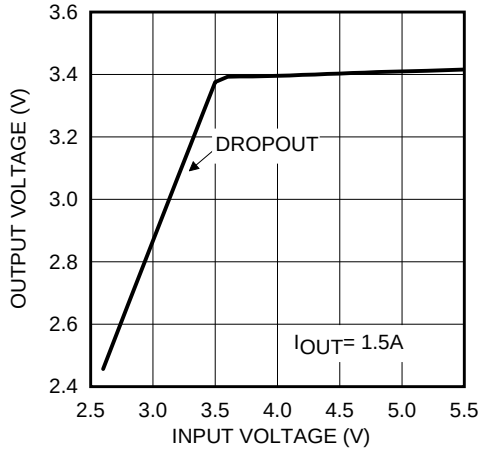
The following spec table entries are specified by design and verifications providing the component values in the Typical System Application Diagram are used (L = 1.5 µH, DCR = 120 mΩ, TOKO DFE201610C-1R5N, C_{IN} = 10 µF, 6.3 V, 0402, Samsung CL05A106MQ5NUN, C_{OUT} = 10 µF + 4.7 µF + 3 × 1 µF + 3300 pF: 6.3 V, 0402, Samsung CL05A106MQ5NUN, CL05A475MQNRN; 6.3 V, 0201 Samsung CL03A105MQ3CSN; 6.3 V, 01005 Murata GRM022R60J332K). *These parameters are not verified by production testing.* Minimum (MIN) and maximum (MAX) values are specified over the ambient temperature range T_A = −30°C to 90°C. Typical (TYP) values are specified at PVIN = VDD = EN = 3.8 V, BP = 0 V and T_A = 25°C unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Load_tr	Load transient response	V_{OUT} = 3 V, T_R = T_F = 10 µs I_{OUT} = 0 A to 1.2 A MODE = LOW		40		mVpk
Maximum Duty Cycle	Maximum duty cycle	MODE = LOW	100%			
PFM_Freq	Minimum PFM frequency	V_{IN} = 3.2 V, V_{OUT} = 1 V I_{OUT} = 10 mA, MODE = HIGH	100	160		kHz
		V_{IN} = 3.2 V, V_{OUT} = 0.5 V I_{OUT} = 5 mA, MODE = HIGH	34	55		

6.7 Timing Requirements

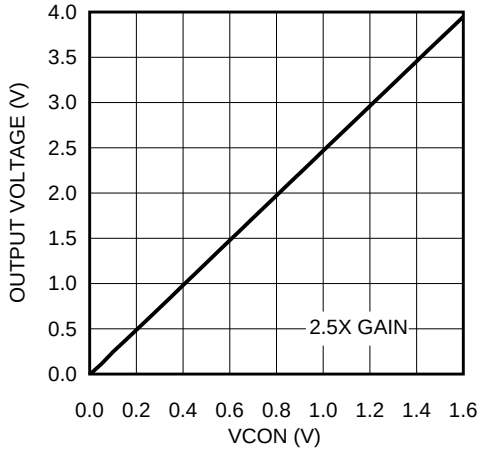
		MIN	MAX	UNIT
t_{SETUP}	Time for SW pin to become active upon power up; EN = LOW-to-HIGH	30		µs
t_{ON}	Turnon time (time for output to reach 90% of final value after EN LOW-to-HIGH transition) EN = LOW-to-HIGH, V_{IN} = 4.2 V, VCON = 1.36 V, V_{OUT} = 3.4 V, I_{OUT} ≤ 1 mA		50	µs
$t_{RESPONSE}$	Time for V_{OUT} to rise from 0 V to 3 V (90% or 2.7 V); V_{IN} = 4.2 V, R_{LOAD} = 6.8 Ω, VCON = 0 V to 1.2 V		20	µs
	Time for V_{OUT} to fall from 3.6 V to 2.6 V (10% or 2.7 V) V_{IN} = 4.2 V, R_{LOAD} = 6.8 Ω, VCON = 1.44 V to 1.04 V		20	
	Time for V_{OUT} to rise from 1.8 V to 2.8 V (90% or 2.7 V) V_{IN} = 4.2 V, R_{LOAD} = 1.9 Ω, VCON = 0.72 V to 1.12 V		15	
	Time for V_{OUT} to fall from 2.8 V to 1.8 V (10% or 1.9 V) V_{IN} = 4.2 V, R_{LOAD} = 1.9 Ω, VCON = 1.12 V to 0.72 V		15	
	Time for V_{OUT} to rise from 0 V to 3.4 V (90% or 3.1 V) V_{IN} = 4.2 V, R_{LOAD} = 1.9 Ω, VCON = 0 V to 1.36 V		20	
	Time for V_{OUT} to fall from 3.4 V to 0.4 V (10% or 0.7 V) V_{IN} = 4.2 V, R_{LOAD} = 1.9 Ω, VCON = 1.36 V to 0.16 V		20	
t_{Bypass}	Time for V_{OUT} to rise from 0 V to PVIN after BP LOW-to-HIGH transition (90%) VCON = 0 V, I_{OUT} ≤ 1 mA		20	µs
$t_{Bypass, ON}$	Bypass turnon time. Time for V_{OUT} to rise from 0 V to PVIN after EN LOW-to-HIGH transition (90% or 3.24) EN = V_{IN}= 3.8 V, I_{OUT} ≤ 1 mA		50	µs

6.8 Typical Characteristics



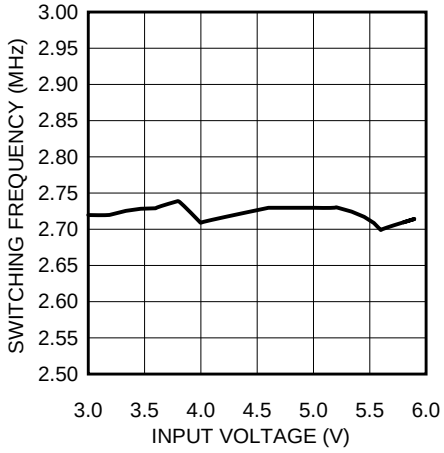
V_{OUT} = 3.4 V V_{IN} = 4.3 V down to Dropout

Figure 1. Output Voltage vs. Supply Voltage



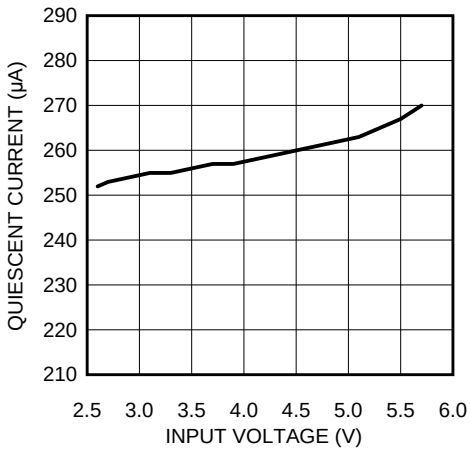
V_{IN} = 4.2 V R_{LOAD} = 6.8 Ω 0.16 V < VCON < 1.4 V

Figure 2. Output Voltage vs. VCON Voltage



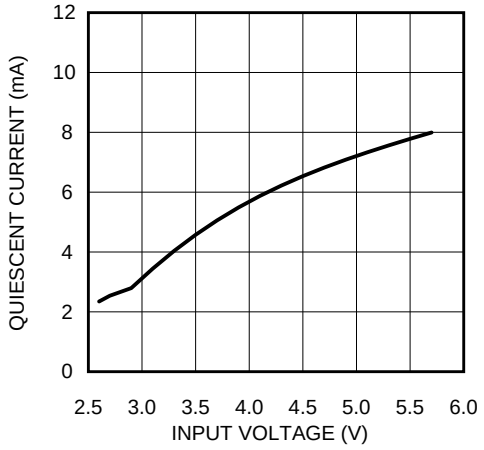
V_{IN} = 3.8 V V_{OUT} = 2.5 V I_{OUT} = 700 mA

Figure 3. Center-Switching Frequency vs. Supply Voltage



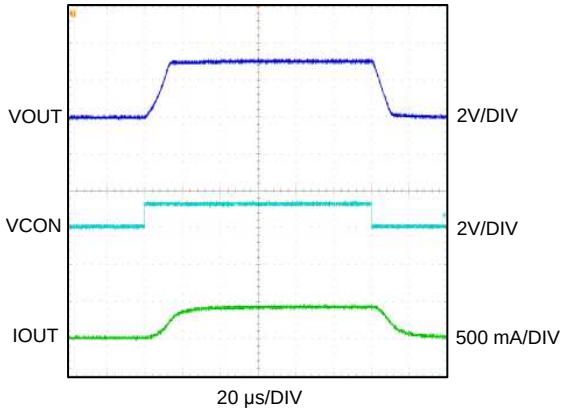
2.7 V < V_{IN}< 5.5 V (No Load) V_{OUT} = 1 V

Figure 4. Quiescent Current (PFM) vs. Supply Voltage



2.7 V < V_{IN}< 5.5 V (No Load) V_{OUT} = 2.5 V

Figure 5. Quiescent Current (PWM) vs. Supply Voltage



V_{IN} = 3.8 V R_{LOAD} = 6.8 Ω V_{OUT} = 0 V to 3 V

Figure 6. VCON Transient (3G/4G)

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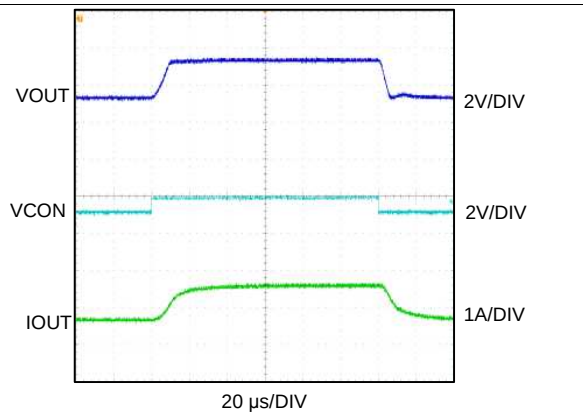
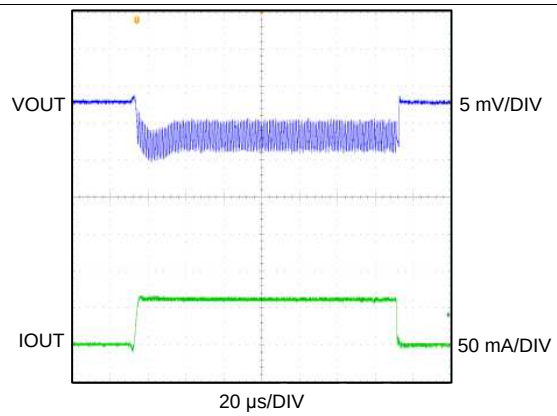
Typical Characteristics (continued)



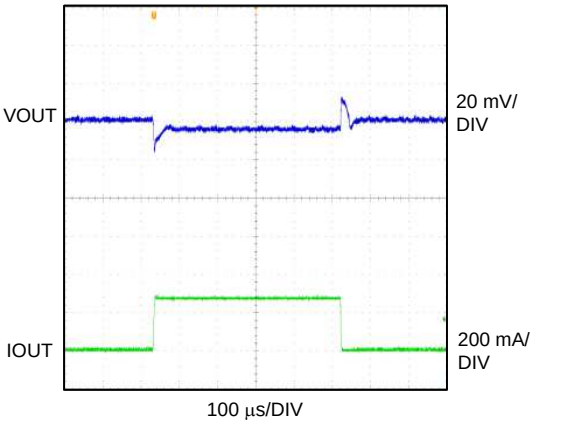
V_{IN} = 4.2 V R_{LOAD} = 1.9 Ω V_{OUT} = 1.4 V to 3.4 V

Figure 7. VCON Transient (PWM)



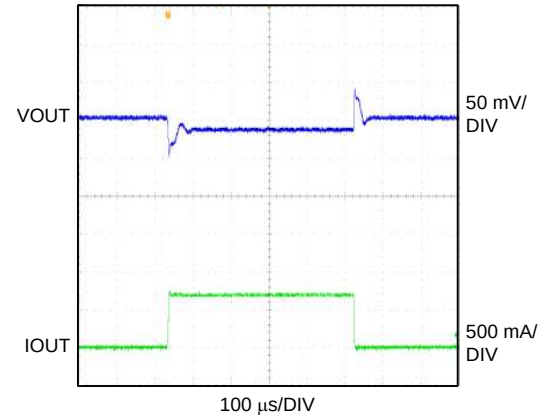
V_{IN} = 3.6 V V_{OUT} = 1 V I_{OUT} = 0 mA to 60 mA

Figure 8. Load Transient In PFM Mode



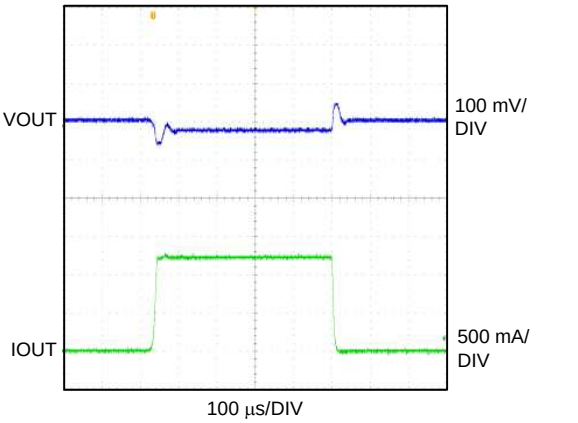
V_{IN} = 3.8 V V_{OUT} = 2.5 V I_{OUT} = 0 mA to 300 mA

Figure 9. Load Transient In PWM Mode



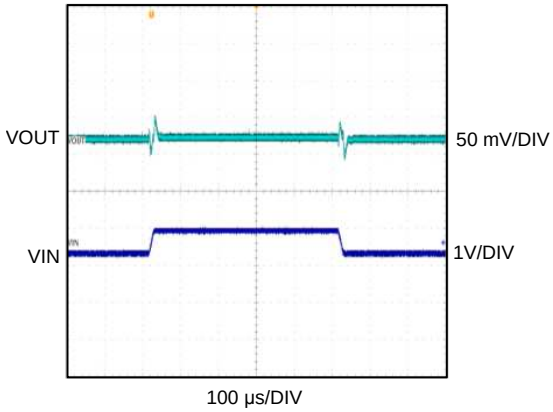
V_{IN} = 3.8 V V_{OUT} = 3 V I_{OUT} = 0 mA to 700 mA

Figure 10. Load Transient In PWM Mode



V_{IN} = 4.2 V V_{OUT} = 3 V I_{OUT} = 0 mA to 1.2 A

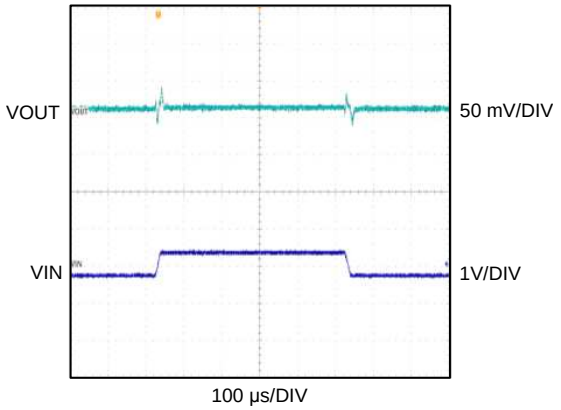
Figure 11. Load Transient In PWM Mode



V_{IN} = 3.6 V to 4.2 V R_{LOAD} = 6.8 Ω V_{OUT} = 2.5 V

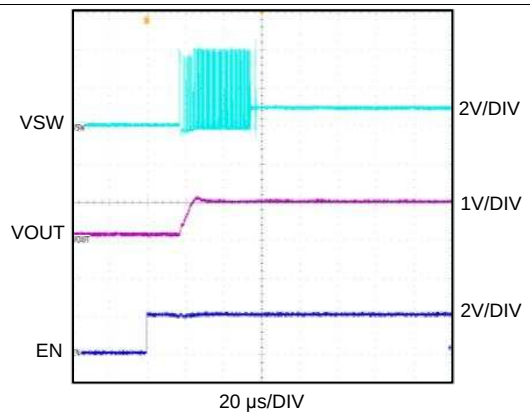
Figure 12. Line Transient

Typical Characteristics (continued)



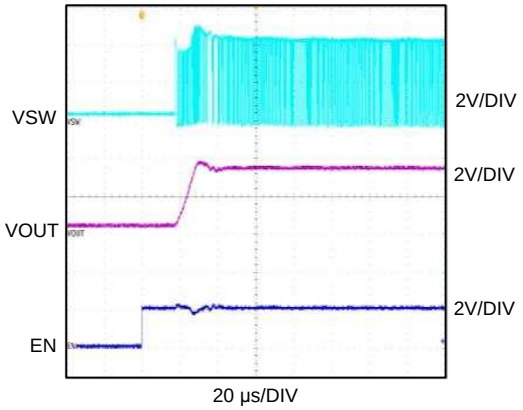
V_{IN} = 3.6 V to 4.2 V R_{LOAD} = 6.8 Ω V_{OUT} = 1 V

Figure 13. Line Transient



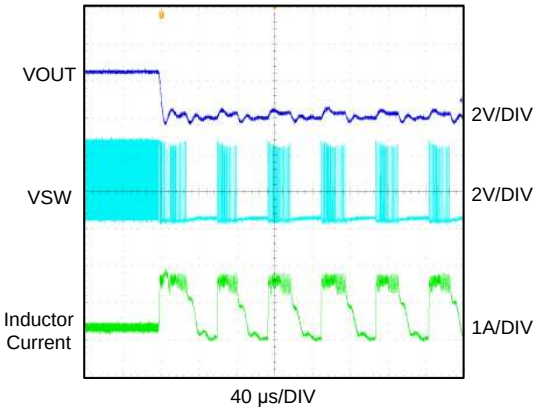
V_{IN} = 3.8 V V_{OUT} = 1 V No load, EN = Low-to-High

Figure 14. Start-up in PFM Mode



V_{IN} = 4.2 V V_{OUT} = 3.4 V No load, EN = Low-to-High

Figure 15. Start-up In PWM Mode



V_{IN} = 4.2 V R_{LOAD} = 6.8 Ω to V_{OUT} Shorted V_{OUT} = 2.5 V

Figure 16. Timed-Current Limit

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7 Detailed Description

7.1 Overview

The LM3243 is a high-efficiency step-down DC-DC converter optimized to power the RF power amplifier (PA) in cell phones, portable communication devices, or battery-powered RF devices with a single Li-Ion battery. It operates in fixed-frequency pulse width modulation (PWM) mode for 2G transmissions (with MODE = LOW), automatic mode transition between PFM and PWM mode for 3G/4G RF PA operation (with MODE = HIGH), forced bypass mode (with BP = HIGH), or in shutdown mode (with EN = LOW).

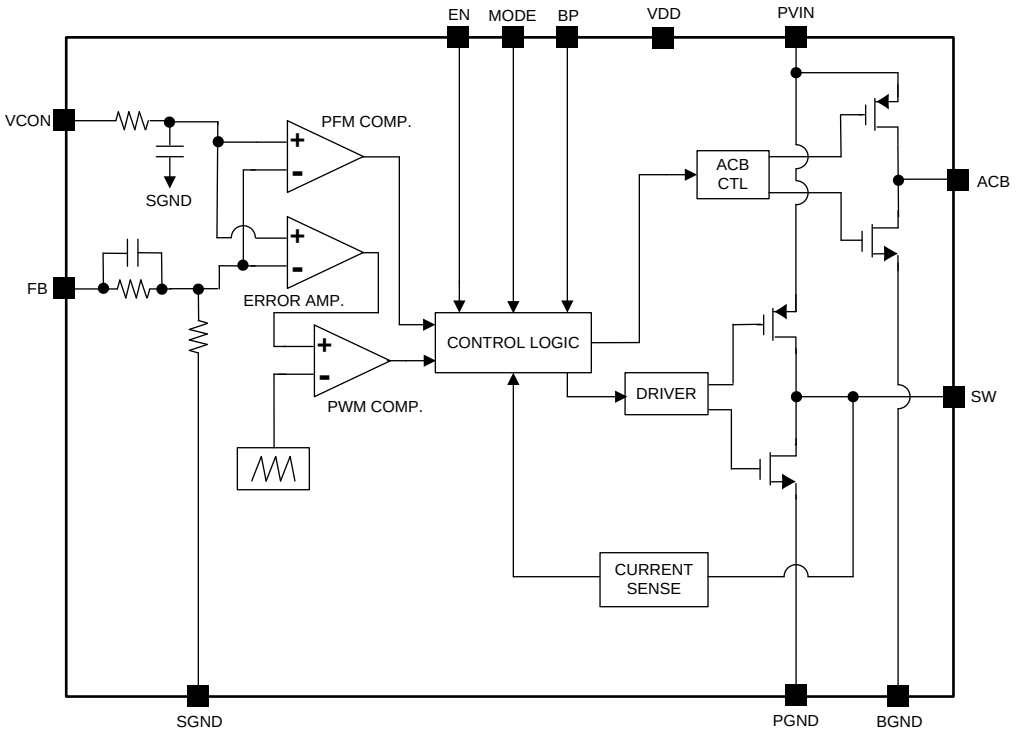
The fixed-frequency PWM mode provides high efficiency and very low output voltage ripple. In PFM mode, the converter operates with reduced switching frequencies and lower supply current to maintain high efficiencies. The forced bypass mode allows the user to drive the output directly from the input supply through a bypass FET. The shutdown mode turns the LM3243 off and reduces current consumption to 0.02 µA (typical).

In PWM and PFM modes of operation, the output voltage of the LM3243 can be dynamically programmed from 0.4 V to 3.6 V (typical) by adjusting the voltage on VCON. Current overload protection and thermal overload protection are also provided.

The LM3243 was engineered with *A*ctive *C*urrent assist and analog *B*ypass (ACB). This unique feature allows the converter to support maximum load currents of 2.5 A (minimum) while keeping a small footprint inductor and meeting all of the transient behaviors required for operation of a multi-mode RF Power Amplifier. The ACB circuit provides an additional current path when the load current exceeds 1.4 A (typical) or as the switcher approaches dropout. Similarly, the ACB circuit allows the converter to respond with faster VCON output voltage transition times by providing extra output current on rising and falling output edges. The ACB circuit also performs the function of analog bypass. Depending upon the input voltage, output voltage and load current, the ACB circuit automatically and seamlessly transitions the converter into analog bypass while maintaining output voltage regulation and low output voltage ripple. Full bypass (100% duty cycle operation) will occur if the total dropout resistance in bypass mode (R_{tot_drop} = 45 mΩ) is insufficient to regulate the output voltage.

The LM3243 device's 16-pin DSBGA package is the best solution for space-constrained applications such as cell phones and other hand-held devices. The high switching frequency, 2.7 MHz (typical) in PWM mode, reduces the size of input capacitors, output capacitors and of the inductor. Use of a DSBGA package is best suited for opaque case applications and requires special design considerations for implementation. (Refer to *DSBGA Package Assembly and Use*.) Because the LM3243 does not implement UVLO, the system controller should set EN = LOW during power-up and UVLO conditions. (Refer to *Shutdown Mode*).

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 ACB

The 3GPP time mask requirement for 2G requires high current to be sourced by the LM3243. These high currents are required for a small time during transients or under a heavy load. Over-rating the switching inductor for these higher currents would increase the solution size and will not be an optimum solution. Thus, to allow an optimal inductor size for such a load, an alternate current path is provided from the input supply through the ACB pin. Once the switcher current limit $I_{LIM,PFET,SteadyState}$ is reached, the ACB circuit starts providing the additional current required to support the load. The ACB circuit also minimizes the dropout voltage by having the analog bypass FET in parallel with V_{OUT}. The LM3243 can provide up to 2.5 A (minimum) of current in bypass mode with a 4-A (maximum) peak current limit.

7.3.2 Bypass Operation

The Bypass circuit provides an analog bypass function with very low dropout resistance (R_{tot_drop} = 45 mΩ typical). When BP = LOW the part will be in automatic bypass mode which will automatically determine the amount of bypass needed to maintain voltage regulation. When the input supply voltage to the LM3243 is lowered to a level where the commanded duty cycle is higher than what the converter is capable of providing, the part will go into pulse-skipping mode. The switching frequency will be reduced to maintain a low and well-behaved output voltage ripple. The analog bypass circuit will allow the converter to stay in regulation until full bypass is reached (100% duty cycle operation). The converter comes out of full bypass and back into analog bypass regulation mode with a similar reverse process.

To override the automatic bypass mode, either set VCON > (V_{IN})/(2.5) (but less than V_{IN}) or set BP = HIGH for forced bypass function. Forced bypass function is valid for 2.7 V < V_{IN} < 5.5 V.

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Feature Description (continued)

7.3.3 Mode Pin

The MODE pin changes the state of the converter to one of the two allowed modes of operation. Setting the MODE pin HIGH (> 1.2 V) sets the device for automatic transition between pulse frequency modulation (PFM) and PWM mode operation. In this mode, the converter operates in PFM mode to maintain the output voltage regulation at very light loads and transitions into PWM mode at loads exceeding 95 mA (typical). The PWM switching frequency is 2.7 MHz (typical). Setting the MODE pin LOW (< 0.5 V) sets the device for PWM mode operation. The switching operation is in PWM mode only, and the switching frequency is also 2.7 MHz (typical).

7.3.4 Dynamic Adjustment Of Output Voltage

The output voltage of the LM3243 can be dynamically adjusted by changing the voltage on the VCON pin. In RF PA applications, peak power is required when the handset is far away from the base station. To maximize the power savings, the LM3243 output should be set just high enough to achieve the desired PA linearity. Hence, during low-power requirements, reduction of supply voltage to the PA can reduce power consumption from the PA, making the operation more efficient and promote longer battery life. Please refer to *Setting The Output Voltage* for further details.

7.3.5 Internal Synchronous Rectification

The LM3243 uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop, thus increasing efficiency. The reduced forward voltage drop in the internal NFET synchronous rectifier significantly improves efficiency for low output voltage operation. The NFET is designed to conduct through its intrinsic body diode during the transient intervals, eliminating the need of an external diode.

7.3.6 Current Limit

The LM3243 current limit feature protects the converter during current overload conditions. Both SW and ACB pins have positive and negative current limits. The positive and negative current limits bound the SW and ACB currents in both directions. The SW pin has two positive current limits. The $I_{LIM,PFET,SteadyState}$ current limit triggers the ACB circuit. Once the peak inductor current exceeds $I_{LIM,PFET,SteadyState}$, the ACB circuit starts assisting the switcher and provides just enough current to keep the inductor current from exceeding $I_{LIM,PFET,SteadyState}$ allowing the switcher to operate at maximum efficiency. Transiently a second current limit $I_{LIM,PFET,Transient}$ of 1.9 A (typical) or 2.1 A (maximum) limits the maximum peak inductor current possible. The output voltage will fall out of regulation only after both SW and ACB output pin currents reach their respective current limits of $I_{LIM,PFET,Transient}$ and $I_{LIM,P-ACB}$.

7.3.7 Timed Current Limit

If the load or output short circuit pulls the output voltage to 0.3 V or lower and the peak inductor current sustains $I_{LIM,\ PFET}$ Transient more than 10 µs, the LM3243 switches to a timed current limit mode. In this mode, the internal PFET switch is turned off. After approximately 30 µs, the device will return to the normal operation.

7.3.8 Thermal Overload Protection

The LM3243 device has a thermal overload protection that protects itself from short-term misuse and overload conditions. If the junction temperature exceeds 150°C, the LM3243 shuts down. Normal operation resumes after the temperature drops below 130°C. Prolonged operation in thermal overload condition may damage the device and is therefore not recommended.

7.4 Device Functional Modes

7.4.1 PWM Operation

When the LM3243 operates in PWM mode, the switching frequency is constant, and the switcher regulates the output voltage by changing the energy-per-cycle to support the load required. During the first portion of each switching cycle, the control block in the LM3243 turns on the internal PFET switch. This allows current to flow from the input through the inductor and to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of $(V_{IN} – V_{OUT})/L$, by storing energy in its magnetic field.

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Device Functional Modes (continued)

During the second portion of each cycle, the control block turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. The inductor draws current from ground through the NFET and to the output filter capacitor and load, which ramps the inductor current down with a slope of $-V_{OUT}/L$. The output filter capacitor stores charge when the inductor current is greater than the load current and releases it when the inductor current is less than the load current, smoothing the voltage across the load.

At the next rising edge of the clock, the cycle repeats. An increase of load pulls the output voltage down, increasing the error signal. As the error signal increases, the peak inductor current becomes higher, thus increasing the average inductor current. The output voltage is therefore regulated by modulating the PFET switch on-time to control the average current sent to the load. The circuit generates a duty-cycle modulated rectangular signal that is averaged using a low pass filter formed by the inductor and output capacitor. The output voltage is equal to the average of the duty-cycle modulated rectangular signal.

7.4.2 PFM Mode

With MODE = HIGH, the LM3243 automatically transitions to from PWM into PFM operation if the average inductor current is less than 75 mA (typical) and $V_{IN} - V_{OUT} > 0.6$ V. The switcher regulates the fixed output voltage by transferring a fixed amount of energy during each cycle and modulating the frequency to control the total power delivered to the output. The converter switches only as needed to support the demand of the load current, therefore maximizing efficiency. If the load current should increase during PFM mode to more than 95 mA (typical), the part will automatically transition into constant frequency PWM mode. A 20 mA (typical) hysteresis window exists between PFM and PWM transitions.

After a transient event, the part temporarily operates in 2.7 MHz (typical) fixed-frequency PWM mode to quickly charge or discharge the output. This is true for start-up conditions or if MODE pin is toggled LOW-to-HIGH. Once the output reaches its target output voltage, and the load is less than 75 mA (typical), then the part will seamlessly transition into PFM mode (assuming it is not in forced bypass or auto bypass condition).

7.4.3 Mode Selection

Table 1 shows the LM3243 parameters for the given modes (PWM or PFM/PWM).

Table 1. Parameters Under Different Modes

PARAMETER/MODE	PWM	PFM/PWM
MODE pin	LOW	HIGH
BP pin	LOW	LOW
Frequency at loads = 75 mA (typical)	2.7 MHz (typical)	Variable
Frequency at loads = 95 mA (typical)	2.7 MHz (typical)	2.7 MHz (typical)
V_{OUT}	2.5 × VCON	2.5 × VCON
Maximum load steady state	2.5 A (min.)	75 mA (minimum in PFM) or 2.5 A (minimum in PWM)

7.4.4 Shutdown Mode

To shut down the LM3243 pull the EN pin LOW (< 0.5 V). In shutdown mode, the current consumption is 0.02 µA (typical) and the PFET switch, NFET synchronous rectifier, reference voltage source, control and bias circuit are turned OFF. To enable LM3243 pull EN HIGH (> 1.2V), and the mode of operation will be dependent on the voltage applied to the MODE pin.

Since the LM3243 does not feature a undervoltage lock-out (UVLO) circuit, the EN pin should be set LOW to turn off the LM3243 during power up and during UVLO conditions. For cell-phone applications, the system controller determines the power supply sequence; thus, it is up to the system controller to ensure proper sequencing by using all of the available pins and functions properly.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM3243 DC-DC converter steps down an input voltage from 2.7 V to 5.5 V to a dynamically adjustable output voltage of 0.4 V to 3.6 V.

8.2 Typical Application

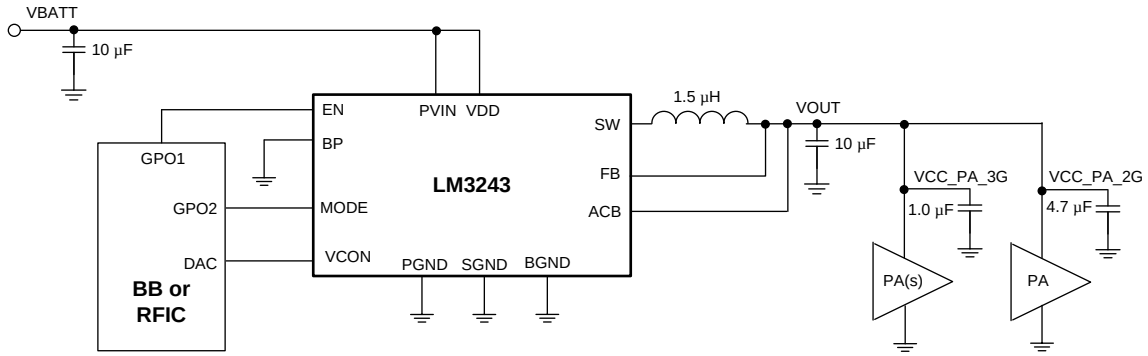

Figure 17. LM3243 Typical Application

8.2.1 Design Requirements

For typical step-down converter applications, use the parameters listed in Table 2.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	2.7 V to 5.5 V
Minimum output voltage	0.4 V to 3.6 V
Output current range	0 to 2.5 A

8.2.2 Detailed Design Procedure

8.2.2.1 Inductor Selection

A 1.5 µH inductor is needed for optimum performance and functionality of the LM3243. In the case of 2G transmission current bursts, the effective overall RMS current requirements are reduced. Therefore, please consult with the inductor manufacturers to determine if some of their smaller components will meet your application needs even though the classical inductor specification does not appear to meet the LM3243 RMS current specifications.

LM3243 automatically manages the inductor peak and RMS (or steady current peak) current through the SW pin. The SW pin has two positive current limits. The first is the 1.45 A typical (or 1.65 A maximum.) over-limit current protection. It sets the upper steady-state inductor peak current (as detailed in the Electrical Characteristics Table - $I_{LIM,PFET,SteadyState}$). It is the dominant factor limiting the inductor's I_{SAT} requirement. The second is a over-limit current protection. It limits the maximum peak inductor current during large signal transients (that is, < 20 µs) to 1.9 A typical (or 2.1 A maximum). A minimum inductance of 0.3 µH should be maintained at the second current limit.

The ACB circuit automatically adjusts its output current to keep the steady-state inductor current below the steady-state peak current limit. Thus, the inductor RMS current will effectively always be less than the $I_{LIM,PFET,SteadyState}$ during the transmit burst. In addition, as in the case with 2G where the output current comes in bursts, the effective overall RMS current would be much lower.

For good efficiency, the inductor's resistance should be less than 0.2 Ω; low DCR inductors (< 0.2 Ω) are recommended. Table 3 suggests some inductors and suppliers.

Table 3. Suggested Inductors and Their Suppliers

MODEL	VENDOR	SIZE (mm)	I_{SAT} −30%	DCR
DFE201610C-1R5M (1285AS-H-1R5M)	TOKO	2 × 1.6 × 1	2.2 A	120 mΩ
PSD20161T-1R5MS	CYNTEC	2 × 1.6 × 1	1.6 A	143 mΩ
TFM201610-1R5M	TDK	2 × 1.6 mm × 1	2.2 A	140 mΩ

8.2.2.2 Capacitor Selection

The LM3243 is designed to use ceramic capacitors for its input and output filters. Use a 10-µF capacitor for the input and approximately 10-µF total output capacitance. Capacitor types such as X5R, X7R are recommended for both filters. These provide an optimal balance between small size, cost, reliability and performance for cell phones and similar applications. Table 4 lists suggested part numbers and suppliers. DC bias characteristics of the capacitors must be considered while selecting the voltage rating and case size of the capacitor. Smaller case sizes for the output capacitor mitigate piezo-electric vibrations of the capacitor when the output voltage is stepped up and down at fast rates. However, they have a bigger percentage drop in value with DC bias. For even smaller total solution size, 0402 case size capacitors are recommended for filtering. Use of multiple 2.2-µF or 1-µF capacitors can also be considered. For RF Power Amplifier applications, split the output capacitor between DC-DC converter and RF Power Amplifiers: 10 µF (C_{OUT1}) + 4.7 µF (C_{OUT2}) + 3 × 1 µF (C_{OUT3}) is recommended. The optimum capacitance split is application dependent, and for stability the actual total capacitance (taking into account effects of capacitor DC bias, temperature de-rating, aging and other capacitor tolerances) should target 10 µF with 2.5-V DC bias (measured at 0.5 V_{RMS}). Place all the output capacitors very close to the respective device. A high-frequency capacitor (3300 pF) is highly recommended to be placed next to C_{OUT1}.

Table 4. Suggested Capacitors And Their Suppliers

CAPACITANCE	MODEL	SIZE (W × L) (mm)	VENDOR
10 µF	GRM185R60J106M	1.6 × 0.8	Murata
10 µF	CL05A106MQ5NUN	1 × 0.5	Samsung
4.7 µF	CL05A475MQ5NRN	1 × 0.5	Samsung
1.0 µF	CL03A105MQ3CSN	0.6 × 0.3	Samsung
3300 pF	GRM022R60J332K	0.4 × 0.2	Murata

8.2.2.3 Setting The Output Voltage

8.2.2.3.1 DAC Control

An analog voltage to the VCON pin can dynamically program the output voltage from 0.4 V (typical) to 3.6 V (typical) in both PFM and PWM modes of operation, without the need for external resistors. The output voltage is governed by Table 5.

Table 5. Output Voltage Selection

VCON (V)	V_{OUT} (V)
VCON = 0.16V to 1.44V	2.5 × VCON

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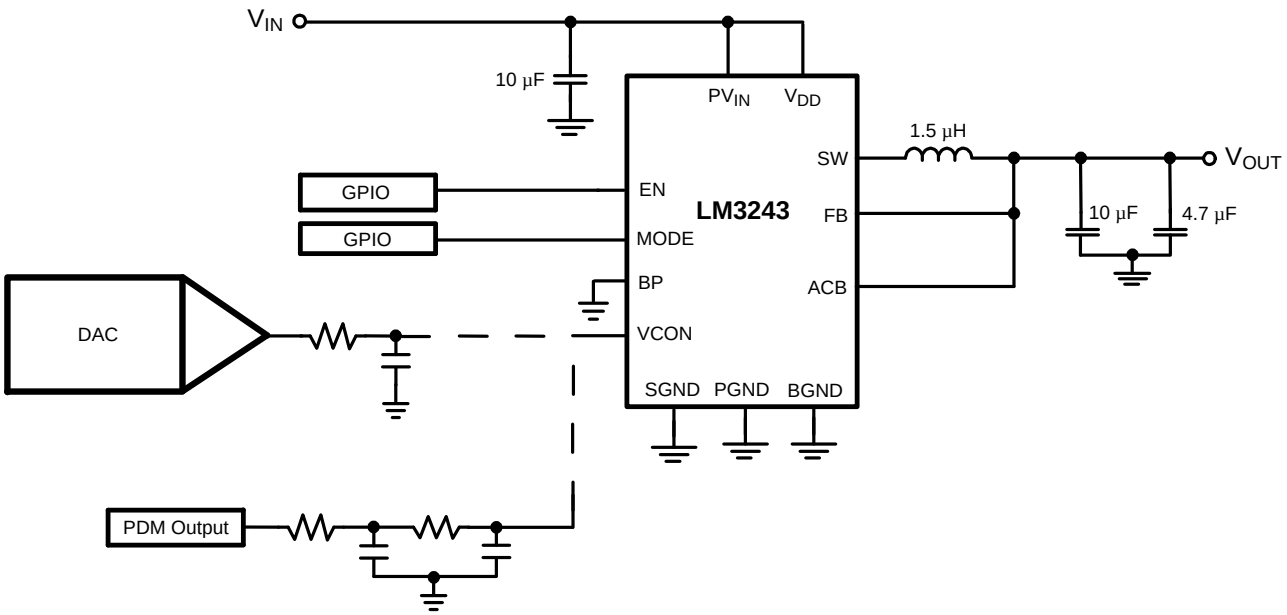

Figure 18. Dynamic Adjustment of Output Voltage With DAC or PDM

8.2.2.3.2 PDM-Based VCON Signal

Figure 18 shows the application circuit that enables the LM3243 to dynamically adjust the output voltage using a GPIO pin from the system controller. Figure 19 shows the waveforms when adjusted dynamically. The PDM signal of the GPIO is filtered using a low-pass filter and fed to the VCON pin. As the bitstream of the PDM signal changes, the voltage on the VCON pin changes. Thus, the GPIO pin can be used to dynamically adjust the output voltage. The double low-pass filter reduces the ripple at VCON to avoid any excessive VCON-induced ripple at the output voltage.

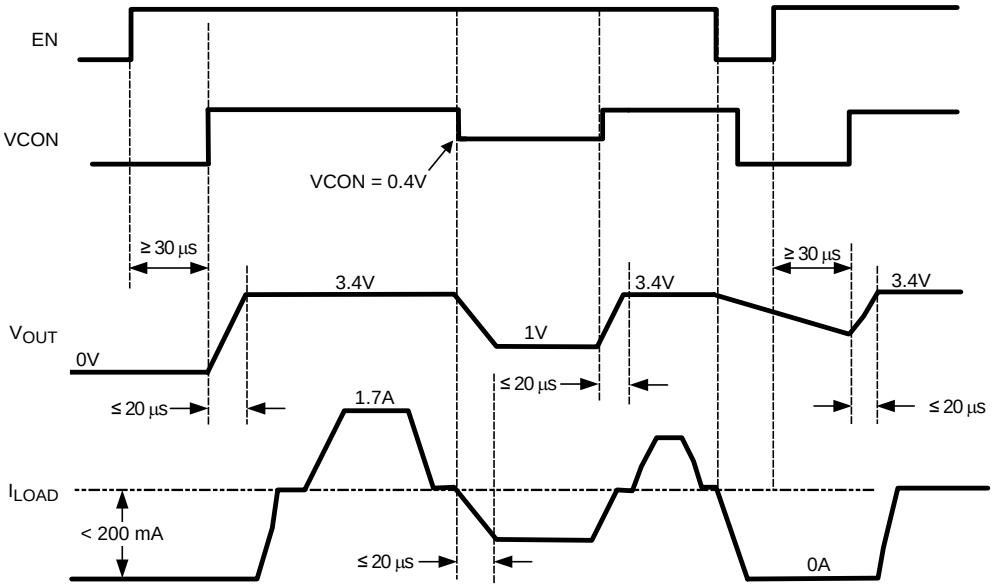

Figure 19. Dynamic Adjustment of Output Voltage With GPIO

8.2.2.3.3 VCON Pin

Figure 20 shows the equivalent CRC circuit for the VCON pin. This circuit is internal to the part and should be taken into consideration when driving this pin.

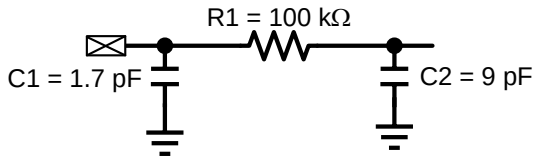

Figure 20. VCON Pin Equivalent CRC Circuit

8.2.2.4 EN Input Control

Use the system controller to drive the EN HIGH or LOW with a comparator, Schmitt trigger or logic gate. Set EN = HIGH (> 1.2 V) for normal operation and LOW (< 0.5 V) for shutdown mode to reduce current consumption to 0.02-µA (typical) current.

8.2.2.5 Start-Up

The waveform Figure 21 in shows the start-up condition. First, V_{IN} should take on a value between 2.7 V and 5.5 V. Next, EN should go HIGH (> 1.2 V). Finally, VCON should be set to a value that corresponds to the required output voltage (V_{OUT} = VCON × 2.5). V_{OUT} will reach its steady-state value in less than 50 µs. To optimize the start-up time and behavior of the output voltage, the LM3243 will always start up in PWM mode (even when MODE = HIGH and output load current ≤ 75 mA), then seamlessly transition into PFM mode.

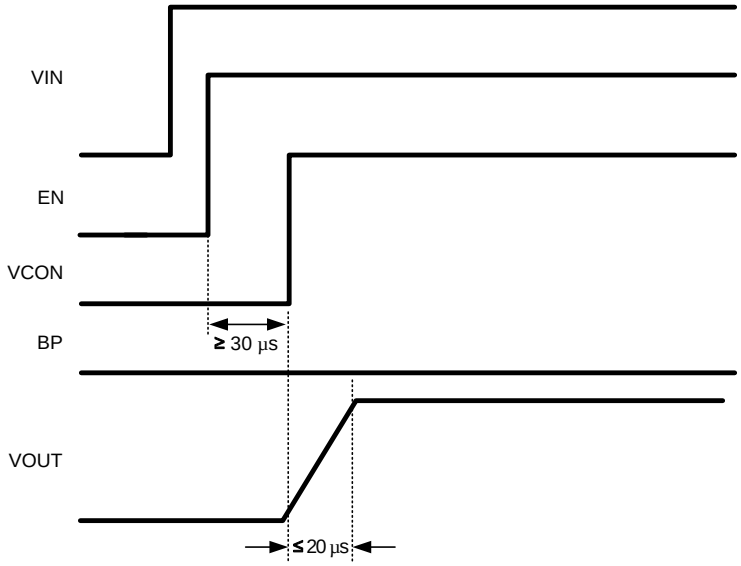

Figure 21. Start-Up Sequence and Conditions

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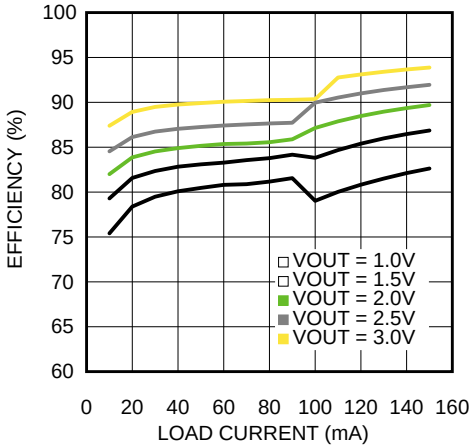
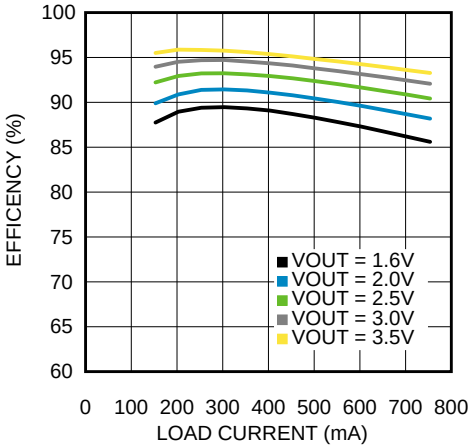
8.2.3 Application Curves



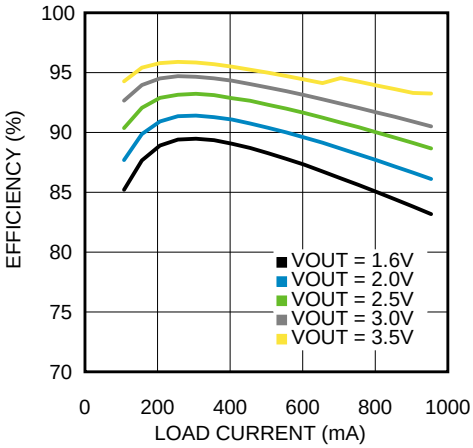
V_{IN} = 3.8 V

Figure 22. Efficiency vs. Load Current



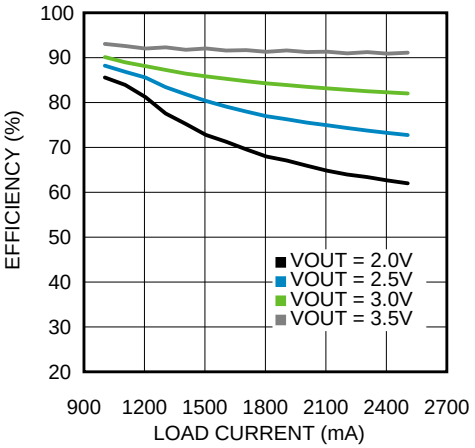
V_{IN} = 3.8 V I_{OUT} = 150 mA To 750 mA

Figure 23. Efficiency vs. Load Current



V_{IN} = 3.8 V I_{OUT} = 100 mA To 1 A

Figure 24. Efficiency vs. Load Current



V_{IN} = 3.8 V I_{OUT} = 1 A To 2.5 A

Figure 25. Efficiency vs. Load Current

9 Power Supply Recommendations

The LM3243 device is designed to operate from an input voltage supply range between 2.7 V and 5.5 V. This input supply should be well-regulated and able to withstand maximum input current and maintain stable voltage without voltage drop even at load transition condition.

10 Layout

10.1 Layout Guidelines

PC board layout is critical to successfully designing a DC-DC converter into a product. A properly planned board layout optimizes the performance of a DC-DC converter and minimizes effects on surrounding circuitry while also addressing manufacturing issues that can have adverse impacts on board quality and final product yield.

10.1.1 PCB Considerations

Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. Erroneous signals could be sent to the DC-DC converter device, resulting in poor regulation or instability. Poor layout can also result in re-flow problems leading to poor solder joints between the DSBGA package and board pads. Poor solder joints can result in erratic or degraded performance of the converter.

10.1.1.1 Energy Efficiency

Minimize resistive losses by using wide traces between the power components and doubling up traces on multiple layers when possible

10.1.1.2 EMI

By its very nature, any switching converter generates electrical noise. The circuit board designer's challenge is to minimize, contain, or attenuate such switcher-generated noise. A high-frequency switching converter, such as the LM3243, switches Ampere level currents within nanoseconds, and the traces interconnecting the associated components can act as radiating antennas. The following guidelines are offered to help to ensure that EMI is maintained within tolerable levels.

To help minimize radiated noise:

- Place the LM3243 switcher, its input capacitor, and output filter inductor and capacitor close together, and make the interconnecting traces as short as possible.
- Arrange the components so that the switching current loops curl in the same direction. During the first half of each cycle, current flows from the input filter capacitor, through the internal PFET of the LM3243 and the inductor, to the output filter capacitor, then back through ground, forming a current loop. In the second half of each cycle, current is pulled up from ground, through the internal synchronous NFET of the LM3243 by the inductor, to the output filter capacitor and then back through ground, forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
- Make the current loop area(s) as small as possible. Interleave doubled traces with ground planes or return paths, where possible, to further minimize trace inductances.

To help minimize conducted noise in the ground-plane:

- Reduce the amount of switching current that circulates through the ground plane: Connect the ground bumps of the LM3243 and its input filter capacitor together using generous component-side copper fill as a pseudo-ground plane. Then connect this copper fill to the system ground-plane (if one is used) by multiple vias located at the input filter capacitor ground terminal. The multiple vias help to minimize ground bounce at the LM3243 by giving it a low-impedance ground connection.

To help minimize coupling to the DC-DC converter voltage feedback trace:

- Route noise sensitive traces, such as the voltage feedback path (FB), as directly as possible from the switcher FB pad to the VOUT pad of the output capacitor, but keep it away from noisy traces between the power components.

To help minimize noise coupled back into power supplies:

- **Use a star connection to route from the VBATT power input to Switcher PVIN and to VBATT_PA.**
- Route traces for minimum inductance between supply pins and bypass capacitor(s).
- Route traces to minimize inductance between bypass capacitors and the ground plane.
- Maximize power supply trace inductance(s) to reduce coupling among function blocks.
- Inserting a ferrite bead in-line with power supply traces can offer a favorable tradeoff in terms of board area, by attenuating noise that might otherwise propagate through the supply connections, allowing the use of

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Layout Guidelines (continued)

fewer bypass capacitors.

VBATT Star Connection: It is critically important to use a 'Star' connection from VBATT supply to LM3243 PVIN and from VBATT to PA modules as implementing a 'daisy chain' supply connection may add noise to the PA output.

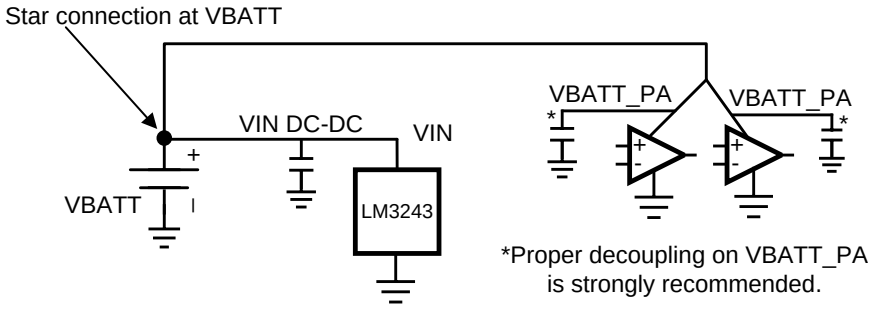

Figure 26. VBATT Star Connection on VIN And VBATT_PA

10.1.2 Manufacturing Considerations

The LM3243 package employs a 16-pin (4 × 4) array of 0.24-mm solder balls, with a 0.4-mm pad pitch. A few simple design rules will go a long way to ensuring a good layout.

- Pad size should be 0.225 ± 0.02 mm. Solder mask opening should be 0.325 ± 0.02 mm.
- As a thermal relief, connect to each pad with 9 mil wide, 6 mil long traces and incrementally increase each trace to its optimal width. Symmetry is important to ensure the solder bumps re-flow evenly. Refer to TI Application Note AN-1112 *DSBGA Wafer Level Chip Scale Package* (SNVA009).

10.2 Layout Example

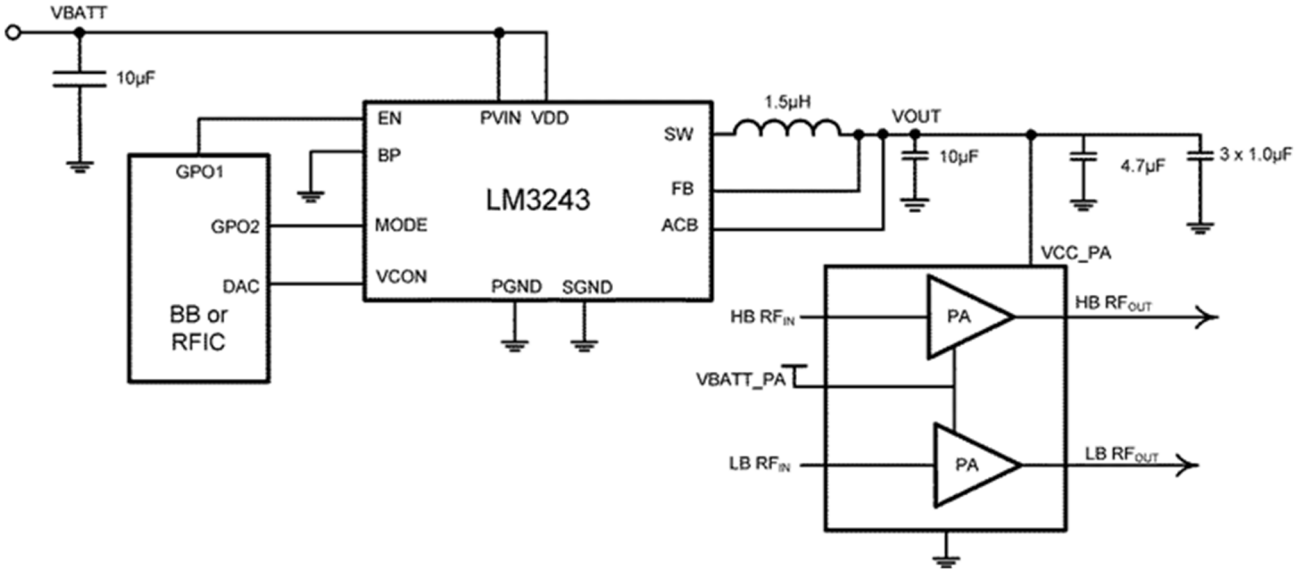

Figure 27. Simplified LM3243 RF Evaluation Board Schematic

Layout Example (continued)

10.2.1 LM3243 RF Evaluation Board

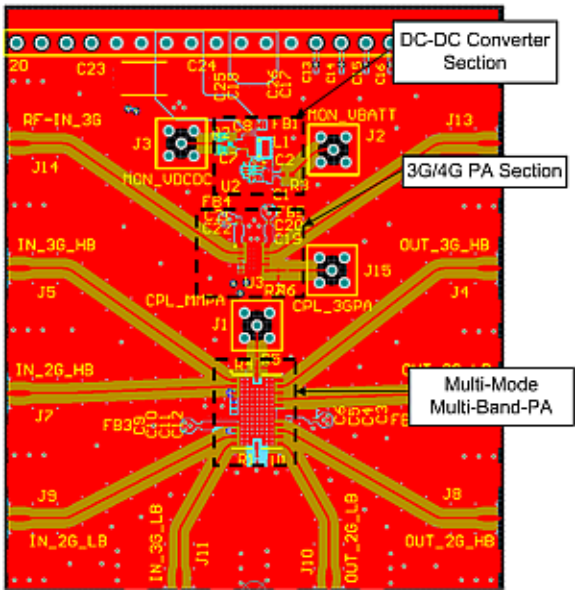

Figure 28. Top View of RF Evaluation Board With PAs

10.2.2 DC-DC Converter Section

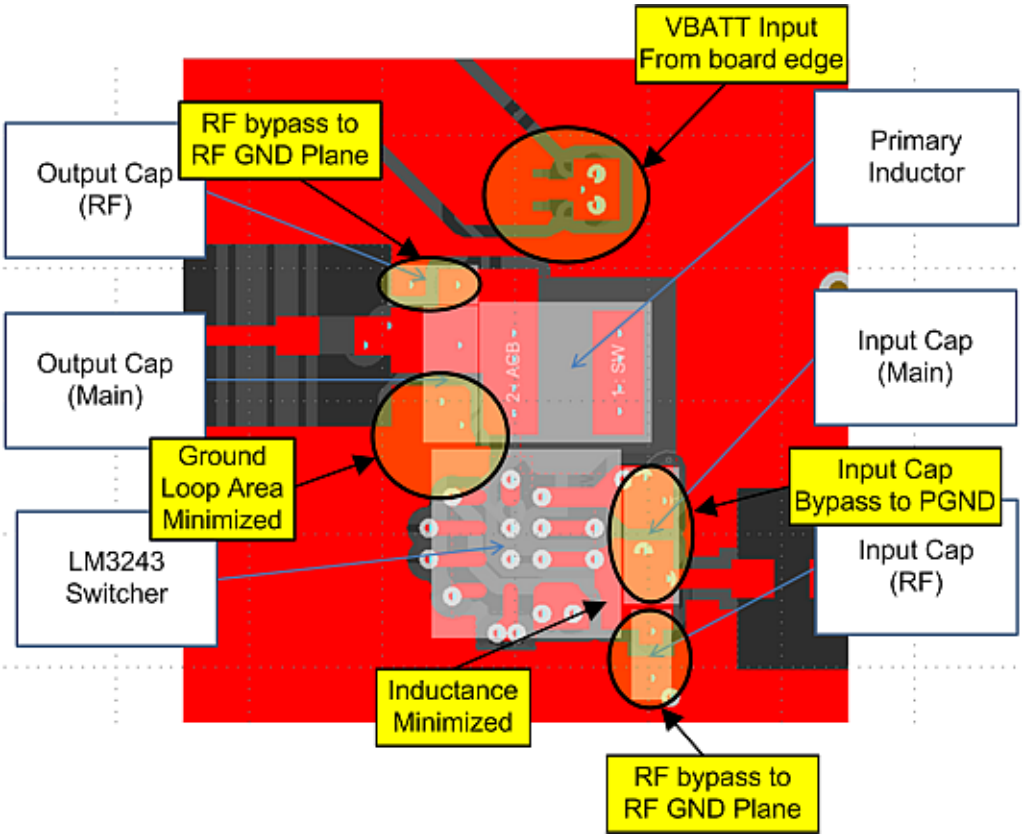

Figure 29. Top Layer

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Layout Example (continued)

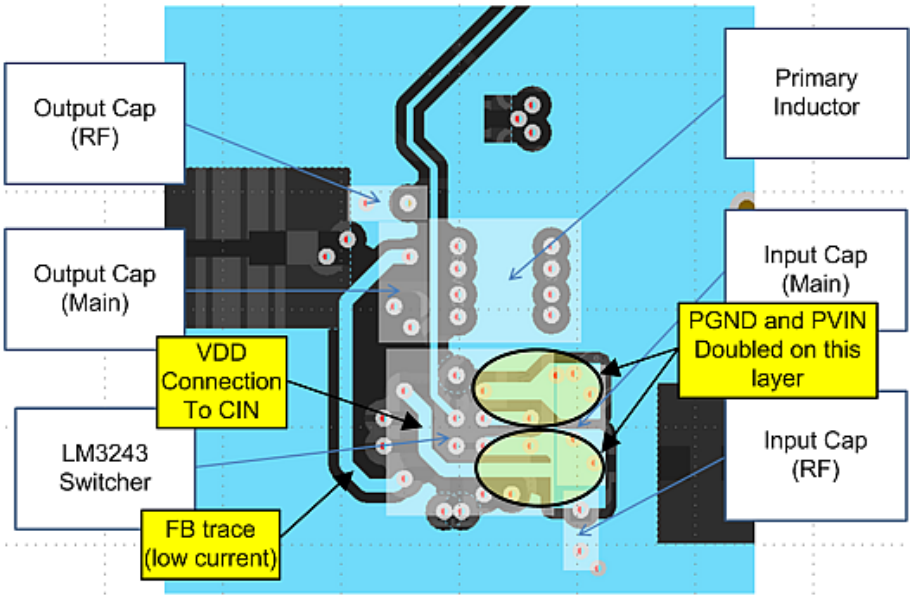

Figure 30. Board Layer 2 - FB, VDD, Additional Routing For PGND, PVIN

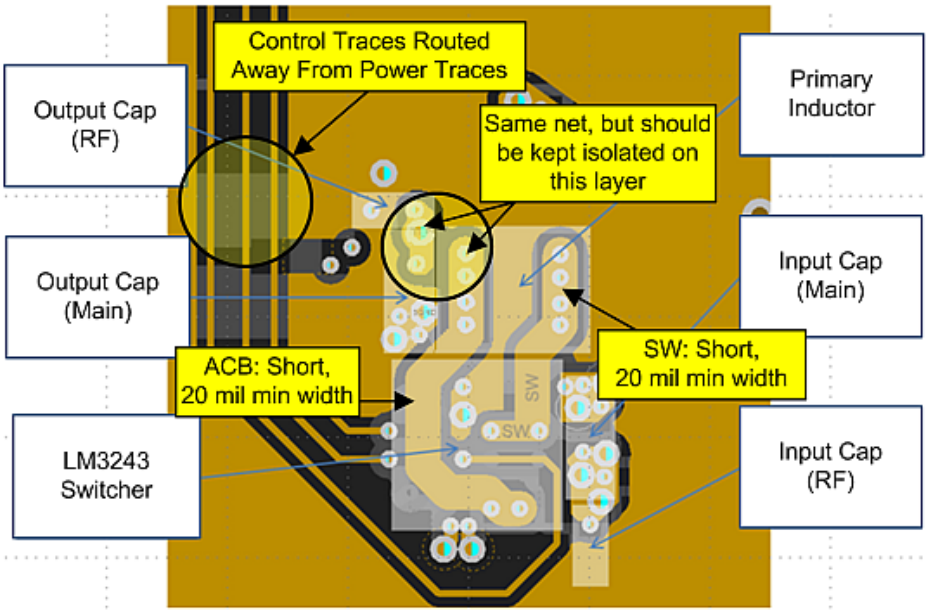

Figure 31. Board Layer 2 - Switcher Detail

Layout Example (continued)

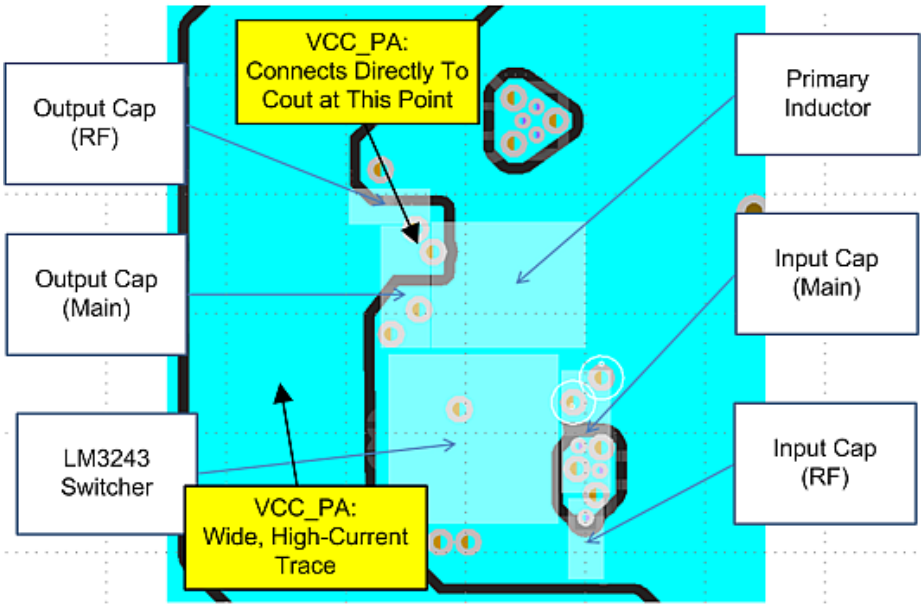

Figure 32. Board Layer 4 - GND Plane VCC_PA

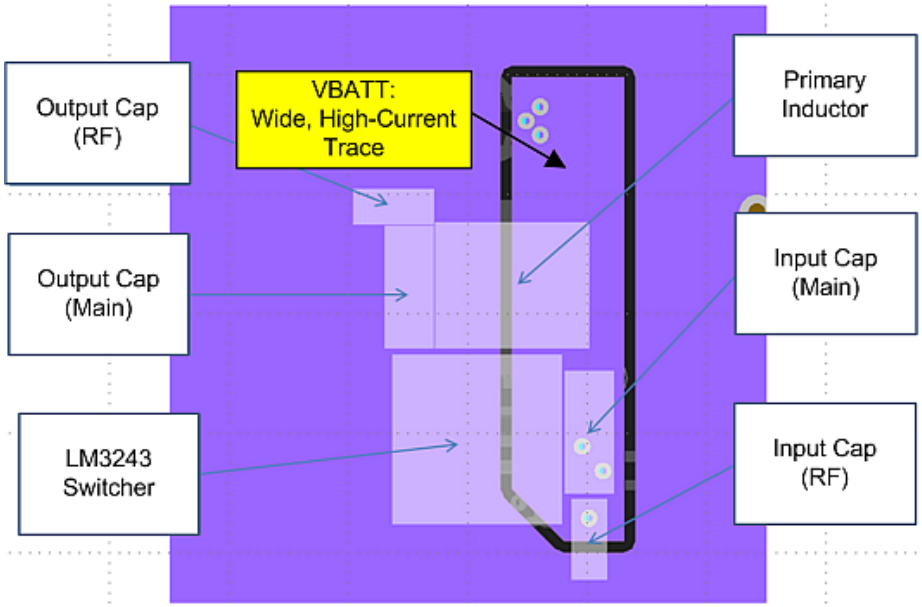

Figure 33. Board Layer 5 - VBATT_SW Connection

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Layout Example (continued)

10.2.3 VBATT Star Supply Connection

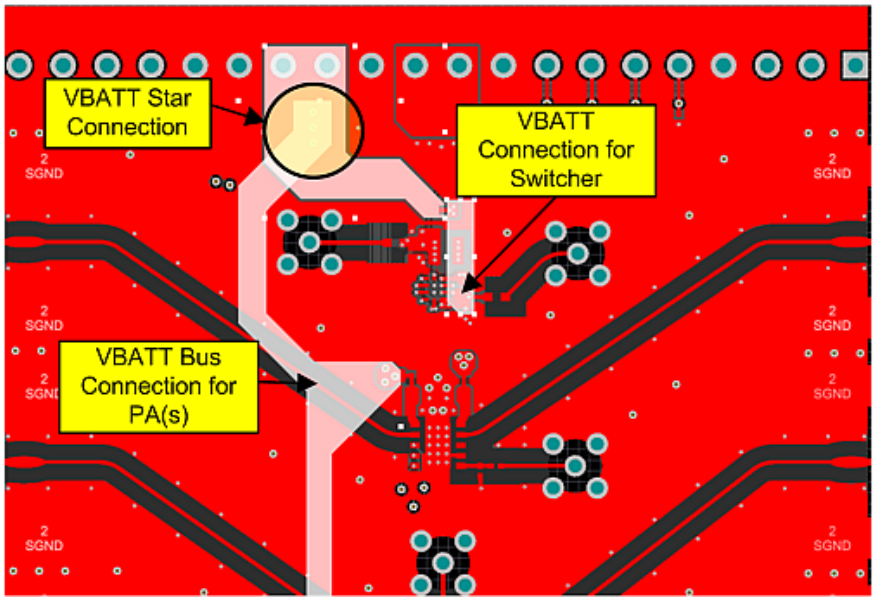

Figure 34. Multiple Board Layers - VBATT Supply Star Connection

10.3 DSBGA Package Assembly and Use

Use of the DSBGA package requires specialized board layout, precision mounting and careful re-flow techniques, as detailed in TI Application Note AN-1112 *DSBGA Wafer Level Chip Scale Package* (SNVA009). Please refer to the section *Surface Mount Assembly Considerations.* For best results in assembly, local alignment fiducials on the PC board should be used to facilitate placement of the device.

The pad style used with DSBGA package must be the NSMD (non-solder mask defined) type. This means that the solder-mask opening is larger than the pad size. This prevents a lip that would otherwise form if the solder-mask and pad overlap, which would hold the device off the surface of the board and interfere with mounting. See SNVA009 for specific instructions how to do this.

The 16-pin package used for LM3243 has 265 micron solder balls and requires 0.225-mm pads for mounting the circuit board. The trace to each pad should enter the pad with a 90°entry angle to prevent debris from being caught in deep corners. Initially, the trace to each pad should be 5.6 mil wide, for a section approximately 5 mil long, as a thermal relief. Then each trace should neck up or down to its optimal width. An important criterion is symmetry to insure the solder bumps on the LM3243 re-flow evenly and that the device solders level to the board. In particular, special attention must be paid to the pads for bumps A1, A3, B1, and B3 since PGND and PVIN are typically connected to large copper planes, inadequate thermal reliefs can result in inadequate re-flow of these bumps.

The DSBGA package is optimized for the smallest possible size in applications with red-opaque or infrared-opaque cases. Because the DSBGA package lacks the plastic encapsulation characteristic of larger devices, it is vulnerable to light. Backside metallization and/or epoxy coating, along with front-side shading by the printed circuit board, reduce this sensitivity. However, the package has exposed die edges that are sensitive to light in the read and infrared range shining on the package's exposed die edges.

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11 Device and Documentation Support

11.1 Device Support

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11.2 Documentation Support

11.2.1 Related Documentation

For additional information, see the following:

TI Application Note AN-1112 *DSBGA Wafer Level Chip Scale Package* (SNVA009).

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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11.4 Trademarks

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11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM3243TME/NOPB	Active	Production	DSBGA (YFQ) | 16	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-30 to 90	S57
LM3243TME/NOPB.A	Active	Production	DSBGA (YFQ) | 16	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-30 to 90	S57
LM3243TME/NOPB.B	Active	Production	DSBGA (YFQ) | 16	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-30 to 90	S57
LM3243TMX/NOPB	Active	Production	DSBGA (YFQ) | 16	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-30 to 90	S57
LM3243TMX/NOPB.A	Active	Production	DSBGA (YFQ) | 16	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-30 to 90	S57
LM3243TMX/NOPB.B	Active	Production	DSBGA (YFQ) | 16	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-30 to 90	S57

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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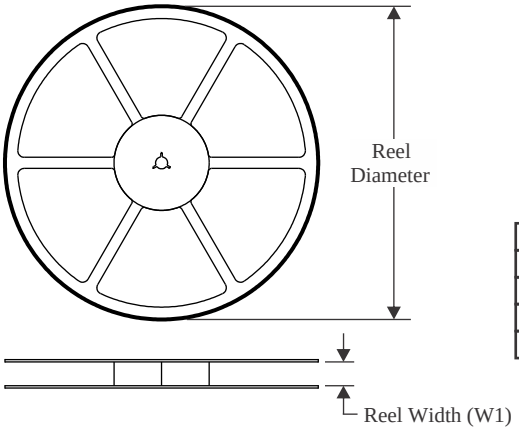
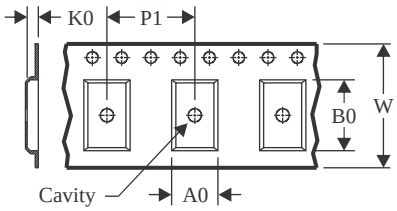
TAPE AND REEL INFORMATION

REEL DIMENSIONS

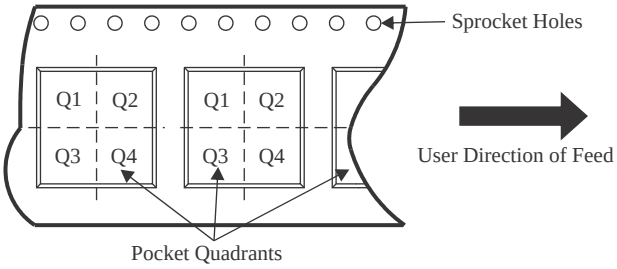


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

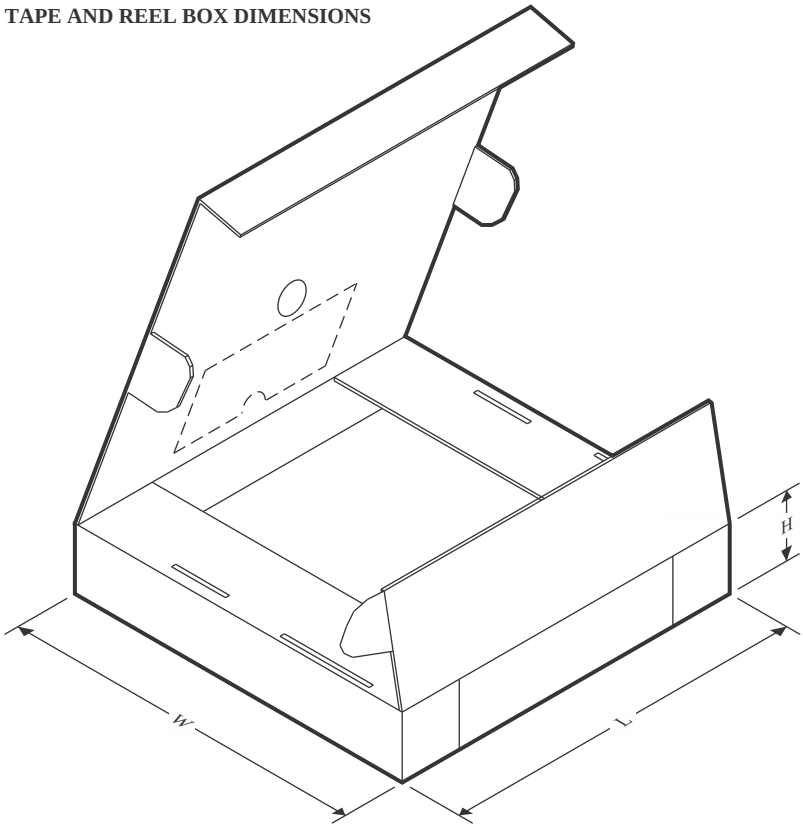
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3243TME/NOPB	DSBGA	YFQ	16	250	178.0	8.4	2.08	2.08	0.76	4.0	8.0	Q1
LM3243TMX/NOPB	DSBGA	YFQ	16	3000	178.0	8.4	2.08	2.08	0.76	4.0	8.0	Q1

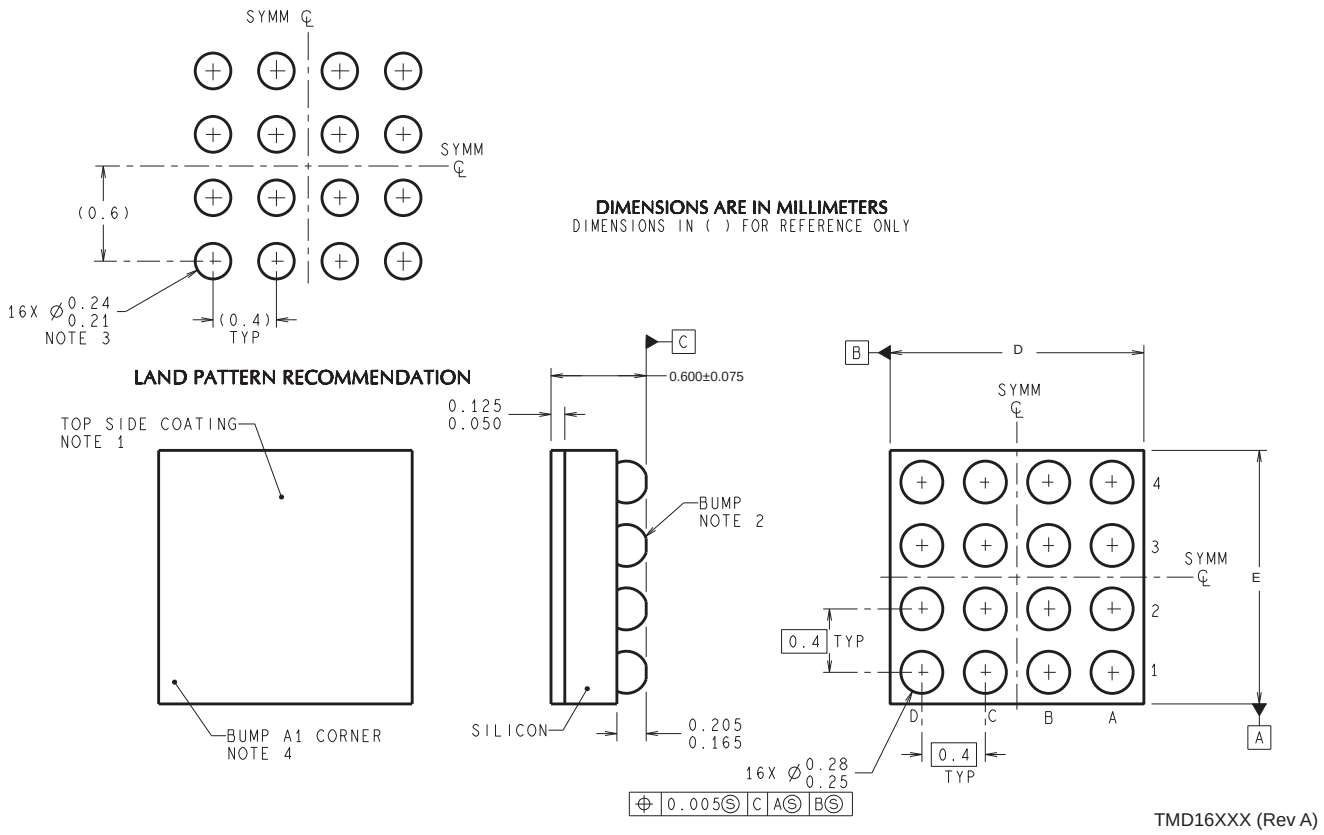
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3243TME/NOPB	DSBGA	YFQ	16	250	208.0	191.0	35.0
LM3243TMX/NOPB	DSBGA	YFQ	16	3000	208.0	191.0	35.0

YFQ0016



D: Max = 2.049 mm, Min =1.989 mm

E: Max = 2.049 mm, Min =1.989 mm

4215081/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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