Dual, 12-Bit, 65MSPS, +3.3V Analog-to-Digital Converter

FEATURES

- **Single +3.3V Supply**
- **High SNR: 70.7dBFS at f_{IN} = 5MHz**
- **Total Power Dissipation:**
  Internal Reference: 371mW
  External Reference: 335mW
- **Internal or External Reference**
- **Low DNL: ±0.3LSB**
- **Flexible Input Range: 1.5V_{PP} to 2V_{PP}**
- **TQFP-64 Package**

APPLICATIONS

- **Communications IF Processing**
- **Communications Base Stations**
- **Test Equipment**
- **Medical Imaging**
- **Video Digitizing**
- **CCD Digitizing**

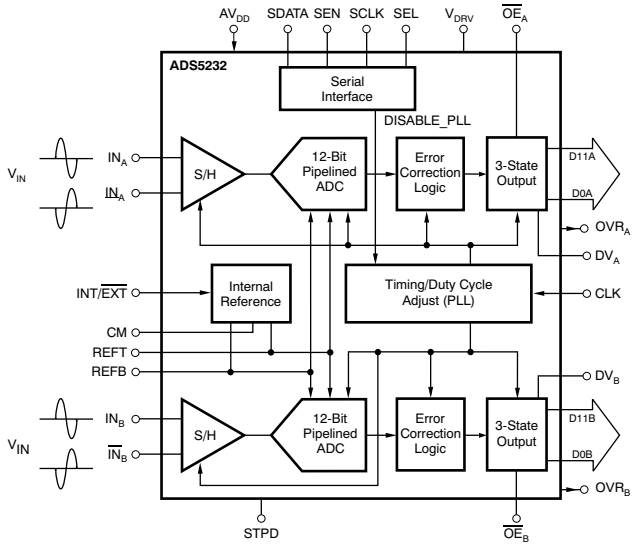
DESCRIPTION

The ADS5232 is a dual, high-speed, high dynamic range, 12-bit pipelined analog-to-digital converter (ADC). This converter includes a high-bandwidth sample-and-hold amplifier that gives excellent spurious performance up to and beyond the Nyquist rate. The differential nature of the sample-and-hold amplifier and ADC circuitry minimizes even-order harmonics and gives excellent common-mode noise immunity.

The ADS5232 provides for setting the full-scale range of the converter without any external reference circuitry. The internal reference can be disabled, allowing low-drive, external references to be used for improved tracking in multichannel systems.

The ADS5232 provides an over-range indicator flag to indicate an input signal that exceeds the full-scale input range of the converter. This flag can be used to reduce the gain of front-end gain control circuitry. There is also an output enable pin to allow for multiplexing and testing on a PC board.

The ADS5232 employs digital error correction techniques to provide excellent differential linearity for demanding imaging applications. The ADS5232 is available in a TQFP-64 package.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS5232	TQFP-64	PAG	–40°C to +85°C	ADS5232IPAG	ADS5232IPAG	Tray, 160
					ADS5232IPAGT	Tape and Reel, 250

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

Supply Voltage Range, AVDD	–0.3V to +3.8V
Supply Voltage Range, VDRV	–0.3V to +3.8V
Voltage Between AVDD and VDRV	–0.3V to +0.3V
Voltage Applied to External REF Pins	–0.3V to +2.4V
Analog Input Pins(2)	–0.3V to min [3.3V, (AVDD + 0.3V)]
Case Temperature	+100°C
Operating Free-Air Temperature Range, T_A	–40°C to +85°C
Lead Temperature	+260°C
Junction Temperature	+105°C
Storage Temperature	–65°C +150°C

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

(2) The DC voltage applied on the input pins should not go below –0.3V. Also, the DC voltage should be limited to the lower of either 3.3V or (AVDD + 0.3V). If the input can go higher than +3.3V, then a resistor greater than or equal to 25Ω should be added in series with each of the input pins. Also, the duty cycle of the overshoot beyond +3.3V should be limited. The overshoot duty cycle can be defined either as a percentage of the time of overshoot over a clock period, or over the entire device lifetime. For a peak voltage between +3.3V and +3.5V, a duty cycle up to 10% is acceptable. For a peak voltage between +3.5V and +3.7V, the overshoot duty cycle should not exceed 1%. Any overshoot beyond +3.7V should be restricted to less than 0.1% duty cycle, and never exceed +3.9V.

RECOMMENDED OPERATING CONDITIONS

	ADS5232			
	MIN	TYP	MAX	UNITS
SUPPLIES AND REFERENCES				
Analog Supply Voltage, AVDD	3.0	3.3	3.6	V
Output Driver Supply Voltage, VDRV	3.0	3.3	3.6	V
REF_T — External Reference Mode	1.875	2.0	2.05	V
REF_B — External Reference Mode	0.95	1.0	1.125	V
REFCM = (REF_T + REF_B)/2 – External Reference Mode(1)		V_{CM} ± 50mV		V
Reference = (REF_T – REF_B) – External Reference Mode	0.75	1.0	1.1	V
Analog Input Common-Mode Range(1)		V_{CM} ± 50mV		V
CLOCK INPUT AND OUTPUTS				
ADCLK Input Sample Rate				
PLL Enabled (default)	20		65	MSPS
PLL Disabled	2		30(2)	MSPS
ADCLK Duty Cycle				
PLL Enabled (default)	45		55	MSPS
Low-Level Voltage Clock Input			0.6	V
High-Level Voltage Clock Input	2.2			V
Operating Free-Air Temperature, T_A	–40		+85	°C
Thermal Characteristics:				
θ_{JA}		42.8		°C/W
θ_{JC}		18.7		°C/W

(1) These voltages need to be set to 1.5V ± 50mV if they are derived independent of V_{CM}.
(2) When the PLL is disabled, the clock duty cycle needs to be controlled well, especially at higher speeds. A 45%–55% duty cycle variation is acceptable up to a frequency of 30MSPS. If the device needs to be operated in the PLL disabled mode beyond 30MSPS, then the duty cycle needs to be maintained within 48%–52% duty cycle.

ELECTRICAL CHARACTERISTICS

T_{MIN} = –40°C and T_{MAX} = +85°C. Typical values are at T_A = +25°C, clock frequency = 65MSPS, 50% clock duty cycle, AVDD = 3.3V, VDRV = 3.3V, transformer-coupled inputs, –1dBFS, I_{SET} = 56.2kΩ, and internal voltage reference, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS5232 MIN	ADS5232 TYP	ADS5232 MAX	UNITS
DC ACCURACY						
	No Missing Codes			Tested		
DNL	Differential Nonlinearity	f_{IN} = 5MHz	–0.9	±0.3	+0.9	LSB
INL	Integral Nonlinearity	f_{IN} = 5MHz	–2.5	±0.4	+2.5	LSB
	Offset Error(1)		–0.75	±0.2	+0.75	%FS
	Offset Temperature Coefficient(2)			±6		ppm/°C
	Fixed Attenuation in Channel(3)			1		%FS
	Fixed Attenuation Matching Across Channels			0.01	0.2	dB
	Gain Error/Reference Error(4)		–3.5	±1.0	+3.5	% FS
	Gain Error Temperature Coefficient			±40		ppm/°C
POWER REQUIREMENTS(5)						
Internal Reference						
	Power Dissipation(5)	Analog Only (AVDD)		260	297	mW
		Output Driver (VDRV)		111	142	mW
	Total Power Dissipation			371	439	mW
External Reference						
	Power Dissipation	Analog Only (AVDD)		224		mW
		Output Driver (VDRV)		111		mW
	Total Power Dissipation			335		mW
	$VREF_T$		1.875	2	2.05	mW
	$VREF_B$		0.95	1	1.125	mW
Total Power-Down			88			mW
REFERENCE VOLTAGES						
$VREF_T$	Reference Top (internal)		1.9	2.0	2.1	V
$VREF_B$	Reference Bottom (internal)		0.9	1.0	1.1	V
V_{CM}	Common-Mode Voltage		1.4	1.5	1.6	V
	V_{CM} Output Current(6)	±50mV Change in Voltage		±2		mA
$VREF_T$	Reference Top (external)		1.875			V
$VREF_B$	Reference Bottom (external)				1.125	V
	External Reference Common-Mode			V_{CM} ± 50mV		V
	External Reference Input Current(7)			1.0		mA

(1) Offset error is the deviation of the average code from mid-code with –1dBFS sinusoid from ideal mid-code (2048). Offset error is expressed in terms of % of full-scale.
(2) If the offset at temperatures T_1 and T_2 are O_1 and O_2, respectively (where O_1 and O_2 are measured in LSBs), the offset temperature coefficient in ppm/°C is calculated as $(O_1 – O_2)/(T_1 – T_2) \times 1E6/4096$.
(3) Fixed attenuation in the channel arises because of a fixed attenuation in the sample-and-hold amplifier. When the differential voltage at the analog input pins is changed from $–V_{REF}$ to $+V_{REF}$, the swing of the output code is expected to deviate from the full-scale code (4096LSB) by the extent of this fixed attenuation. NOTE: V_{REF} is defined as $(REF_T – REF_B)$.
(4) The reference voltages are trimmed at production so that $(VREF_T – VREF_B)$ is within ± 35mV of the ideal value of 1V. This specification does not include fixed attenuation.
(5) Supply current can be calculated from dividing the power dissipation by the supply voltage of 3.3V.
(6) The V_{CM} output current specified is the drive of the V_{CM} buffer if loaded externally.
(7) Average current drawn from the reference pins in the external reference mode.

ELECTRICAL CHARACTERISTICS (continued)

T_{MIN} = –40°C and T_{MAX} = +85°C. Typical values are at T_A = +25°C, clock frequency = 65MSPS, 50% clock duty cycle, AVDD = 3.3V, VDRV = 3.3V, transformer-coupled inputs, –1dBFS, I_{SET} = 56.2kΩ, and internal voltage reference, unless otherwise noted.

PARAMETER	TEST CONDITIONS	ADS5232 MIN	ADS5232 TYP	ADS5232 MAX	UNITS
ANALOG INPUT					
Differential Input Capacitance			3		pF
Analog Input Common-Mode Range			V_{CM} ± 0.05		V
Differential Input Voltage Range	Internal Reference		2.02		V_{PP}
	External Reference		2.02 × ($VREF_T$ – $VREF_B$)		V_{PP}
Voltage Overload Recovery Time(8)			3		CLK Cycles
Input Bandwidth	–3dBFS Input, 25Ω Series Resistance		300		MHz
DIGITAL DATA INPUTS					
Logic Family			+3V CMOS Compatible		
V_{IH} High-Level Input Voltage	V_{IN} = 3.3V	2.2			V
V_{IL} Low-Level Input Voltage	V_{IN} = 3.3V			0.6	V
C_{IN} Input Capacitance			3		pF
DIGITAL OUTPUTS					
Data Format			Straight Offset Binary(9)		
Logic Family			CMOS		
Logic Coding			Straight Offset Binary or BTC		
Low Output Voltage (I_{OL} = 50µA)				+0.4	V
High Output Voltage (I_{OH} = 50µA)		+2.4			V
3-State Enable Time			2		Clocks
3-State Disable Time			2		Clocks
Output Capacitance			3		pF
SERIAL INTERFACE					
SCLK Serial Clock Input Frequency				20	MHz
CONVERSION CHARACTERISTICS					
Sample Rate		20		65	MSPS
Data Latency			6		CLK Cycles

(8) A differential ON/OFF pulse is applied to the ADC input. The differential amplitude of the pulse in its ON (high) state is twice the full-scale range of the ADC, while the differential amplitude of the pulse in its OFF (low) state is zero. The overload recovery time of the ADC is measured as the time required by the ADC output code to settle within 1% of full-scale, as measured from its mid-code value when the pulse is switched from ON (high) to OFF (low).

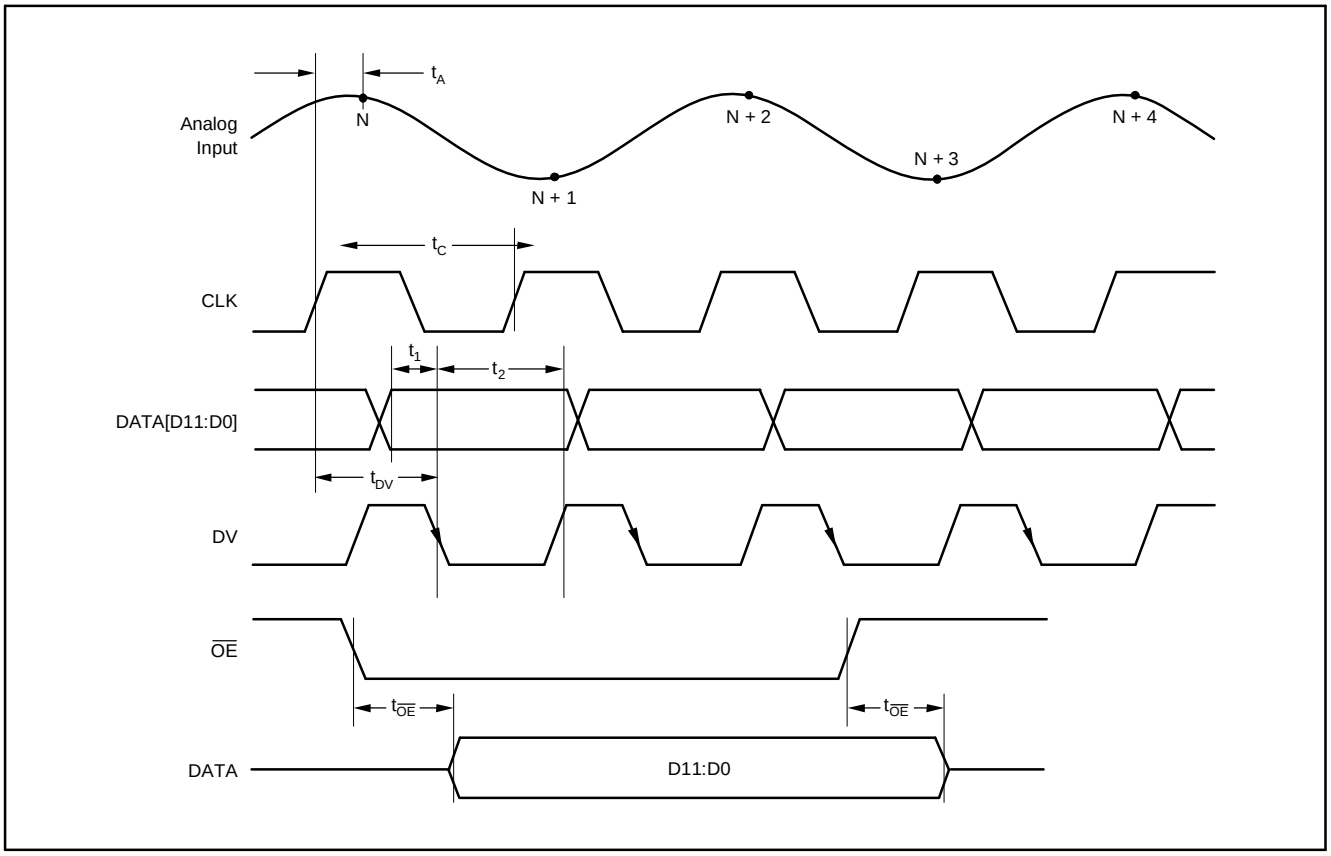
(9) Option for Binary Two's Complement Output.

AC CHARACTERISTICS

T_{MIN} = –40°C and T_{MAX} = +85°C. Typical values are at T_A = +25°C, clock frequency = maximum specified, 50% clock duty cycle, AVDD = 3.3V, VDRV = 3.3V, –1dBFS, I_{SET} = 56.2kΩ, and internal voltage reference, unless otherwise noted.

PARAMETER		CONDITIONS	ADS5242			UNITS
			MIN	TYP	MAX	
DYNAMIC CHARACTERISTICS						
SFDR	Spurious-Free Dynamic Range	f_{IN} = 5MHz	75	86		dBc
		f_{IN} = 32.5MHz		85		dBc
		f_{IN} = 70MHz		83		dBc
HD_2	2nd-Order Harmonic Distortion	f_{IN} = 5MHz	82	92		dBc
		f_{IN} = 32.5MHz		87		dBc
		f_{IN} = 70MHz		85		dBc
HD_3	3rd-Order Harmonic Distortion	f_{IN} = 5MHz	75	86		dBc
		f_{IN} = 32.5MHz		85		dBc
		f_{IN} = 70MHz		83		dBc
SNR	Signal-to-Noise Ratio	f_{IN} = 5MHz	68	70.7		dBFS
		f_{IN} = 32.5MHz		69.5		dBFS
		f_{IN} = 70MHz		67.5		dBFS
SINAD	Signal-to-Noise and Distortion	f_{IN} = 5MHz	67.5	70.3		dBFS
		f_{IN} = 32.5MHz		69		dBFS
		f_{IN} = 70MHz		67		dBFS
	Crosstalk	5MHz Full-Scale Signal Applied to 1 Channel; Measurement Taken on the Channel with No Input Signal		–85		dBc
IMD3	Two-Tone, Third-Order Intermodulation Distortion	f_1 = 4MHz at –7dBFS f_2 = 5MHz at –7dBFS		90.9		dBFS

TIMING DIAGRAM



TIMING CHARACTERISTICS(1)

Typical values at T_A = +25°C, AVDD = VDRV = 3.3V, sampling rate and PLL state are as indicated, input clock at 50% duty cycle, and total capacitive loading = 10pF, unless otherwise noted.

PARAMETER		MIN	TYP	MAX	UNITS
65MSPS With PLL ON					
t_A	Aperture Delay		2.1		ns
	Aperture Jitter		1.0		ps
t_1	Data Setup Time(2)	2	3.2		ns
t_2	Data Hold Time(3)	6.3	8.5		ns
t_D	Data Latency		6		Clocks
t_{DR}, t_{DF}	Data Rise/Fall Time(4)	0.5	2	3	ns
	Data Valid (DV) Duty Cycle	30	40	55	%
t_{DV}	Input Clock Rising to DV Fall Edge	10	11.5	14	ns

(1) Specifications assured by design and characterization; not production tested.
(2) Measured from data becoming valid (at a high level = 2.0V and a low level = 0.8V) to the 50% point of the falling edge of DV.
(3) Measured from the 50% point of the falling edge of DV to the data becoming invalid.
(4) Measured between 20% to 80% of logic levels.

TIMING CHARACTERISTICS (continued)

Typical values at T_A = +25°C, AVDD = VDRV = 3.3V, sampling rate and PLL state are as indicated, input clock at 50% duty cycle, and total capacitive loading = 10pF, unless otherwise noted.

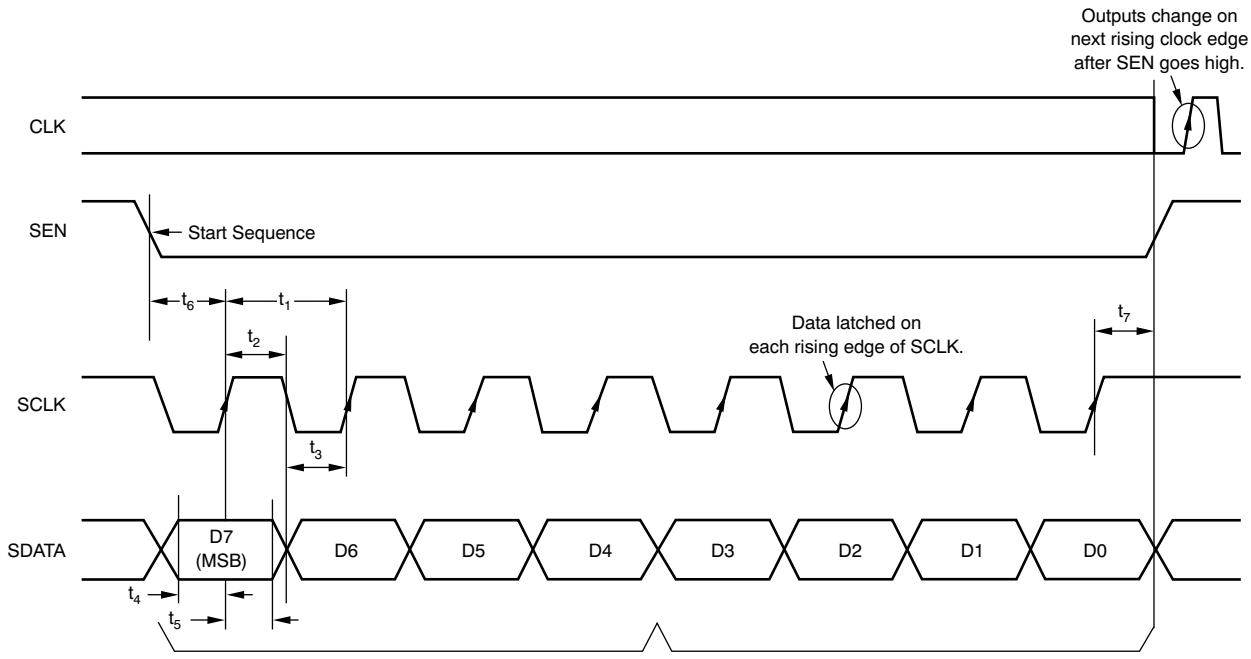
PARAMETER		MIN	TYP	MAX	UNITS
50MSPS With PLL ON					
t_A	Aperture Delay		2.1		ns
	Aperture Jitter		1.0		ps
t_1	Data Setup Time	3.2	4.5		ns
t_2	Data Hold Time	10	11		ns
t_D	Data Latency		6		Clocks
t_{DR}, t_{DF}	Data Rise/Fall Time	0.5	2	3	ns
	Data Valid (DV) Duty Cycle	30	40	55	%
t_{DV}	Input Clock Rising to DV Fall Edge	11.5	13.5	15.5	ns
40MSPS With PLL ON					
t_A	Aperture Delay		2.1		ns
	Aperture Jitter		1.0		ps
t_1	Data Setup Time	3.7	5.5		ns
t_2	Data Hold Time	11.5	13.5		ns
t_D	Data Latency		6		Clocks
t_{DR}, t_{DF}	Data Rise/Fall Time	0.5	2	3	ns
	Data Valid (DV) Duty Cycle	30	40	55	%
t_{DV}	Input Clock Rising to DV Fall Edge	13.5	16	18.5	ns
30MSPS With PLL OFF					
t_A	Aperture Delay		2.1		ns
	Aperture Jitter		1.0		ps
t_1	Data Setup Time	8	10		ns
t_2	Data Hold Time	14	19		ns
t_D	Data Latency		6		Clocks
t_{DR}, t_{DF}	Data Rise/Fall Time	0.5	2	3.5	ns
	Data Valid (DV) Duty Cycle	30	45	55	%
t_{DV}	Input Clock Rising to DV Fall Edge	16	19	21	ns
20MSPS With PLL ON					
t_A	Aperture Delay		2.1		ns
	Aperture Jitter		1.0		ps
t_1	Data Setup Time	10	12		ns
t_2	Data Hold Time	20	25		ns
t_D	Data Latency		6		Clocks
t_{DR}, t_{DF}	Data Rise/Fall Time	0.5	2	3.5	ns
	Data Valid (DV) Duty Cycle	30	45	55	%
t_{DV}	Input Clock Rising to DV Fall Edge	20	25	30	ns
20MSPS With PLL OFF					
t_A	Aperture Delay		2.1		ns
	Aperture Jitter		1.0		ps
t_1	Data Setup Time	10	12		ns
t_2	Data Hold Time	20	25		ns
t_D	Data Latency		6		Clocks
t_{DR}, t_{DF}	Data Rise/Fall Time	0.5	2	3.5	ns
	Data Valid (DV) Duty Cycle	30	45	55	%
t_{DV}	Input Clock Rising to DV Fall Edge	20	25	30	ns
2MSPS With PLL OFF					
t_A	Aperture Delay		2.1		ns
	Aperture Jitter		1.0		ps
t_1	Data Setup Time	150	200		ns

TIMING CHARACTERISTICS (continued)

Typical values at T_A = +25°C, AVDD = VDRV = 3.3V, sampling rate and PLL state are as indicated, input clock at 50% duty cycle, and total capacitive loading = 10pF, unless otherwise noted.

PARAMETER		MIN	TYP	MAX	UNITS
t_2	Data Hold Time	200	250		ns
t_D	Data Latency		6		Clocks
t_{DR}, t_{DF}	Data Rise/Fall Time	0.5	2	3.5	ns
	Data Valid (DV) Duty Cycle	30	45	55	%
t_{DV}	Input Clock Rising to DV Fall Edge	200	225	250	ns

SERIAL INTERFACE TIMING



NOTE: Data is shifted in MSB first.

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_1	Serial CLK Period	50			ns
t_2	Serial CLK High Time	20			ns
t_3	Serial CLK Low Time	20			ns
t_4	Data Setup Time	5			ns
t_5	Data Hold Time	5			ns
t_6	SEN Fall to SCLK Rise	8			ns
t_7	SCLK Rise to SEN Rise	8			ns

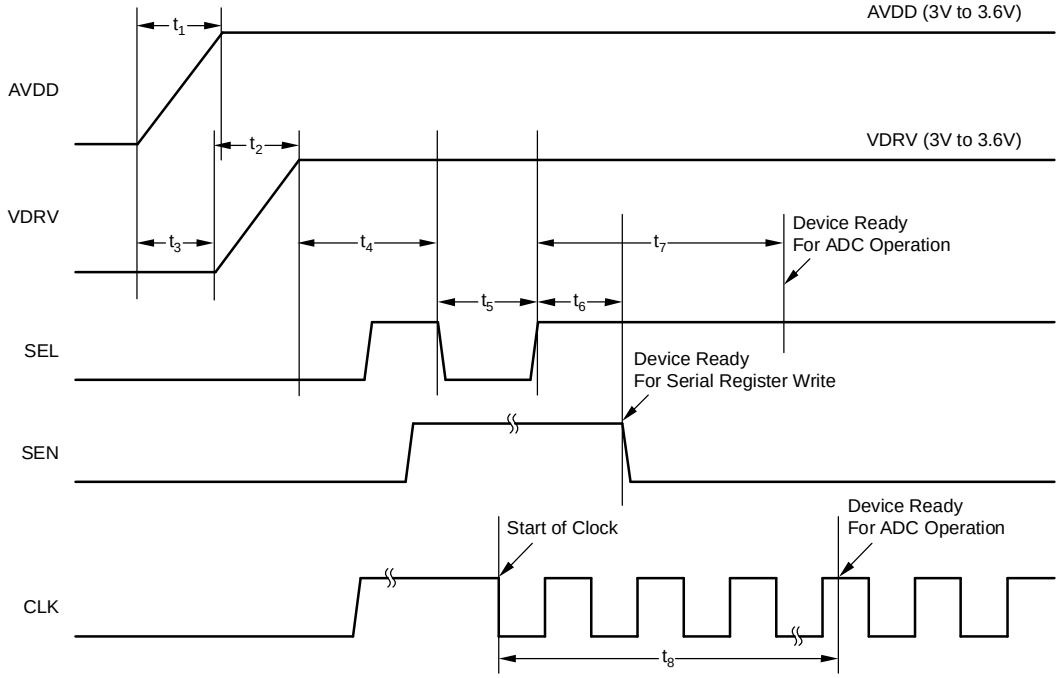
SERIAL REGISTER MAP: Shown for the Case Where Serial Interface is Used[1]

ADDRESS				DATA				DESCRIPTION
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	X	X	X	**0**	Normal Mode
0	0	0	0	X	X	X	**1**	Power-Down Both Channels
0	0	0	0	X	X	**0**	X	Straight Offset Binary Output
0	0	0	0	X	X	**1**	X	Binary Two's Complement Output
0	0	0	0	X	**0**	X	X	Channel B Digital Outputs Enabled
0	0	0	0	X	**1**	X	X	Channel B Digital Outputs Tri-Stated
0	0	0	0	**0**	X	X	X	Channel A Digital Outputs Enabled
0	0	0	0	**1**	X	X	X	Channel A Digital Outputs Tri-Stated
0	0	1	0	**0**	**0**	0	0	Normal Mode
0	0	1	0	**0**	**1**	0	0	All Digital Outputs Set to '1'
0	0	1	0	**1**	**0**	0	0	All Digital Outputs Set to '0'
0	0	1	1	**0**	**0**	X	0	Normal Mode
0	0	1	1	**1**	**X**	X	0	Channel A Powered Down
0	0	1	1	**X**	**1**	X	0	Channel B Powered Down
0	0	1	1	X	X	**0**	0	PLL Enabled (default)
0	0	1	1	X	X	**1**	0	PLL Disabled

(1) X = don't care.

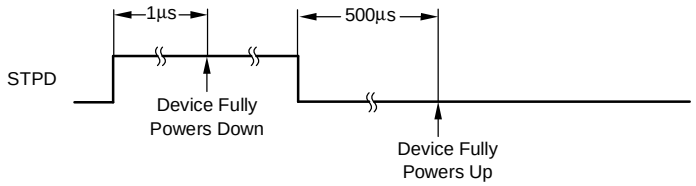
RECOMMENDED POWER-UP SEQUENCING

Shown for the case where the serial interface is used.



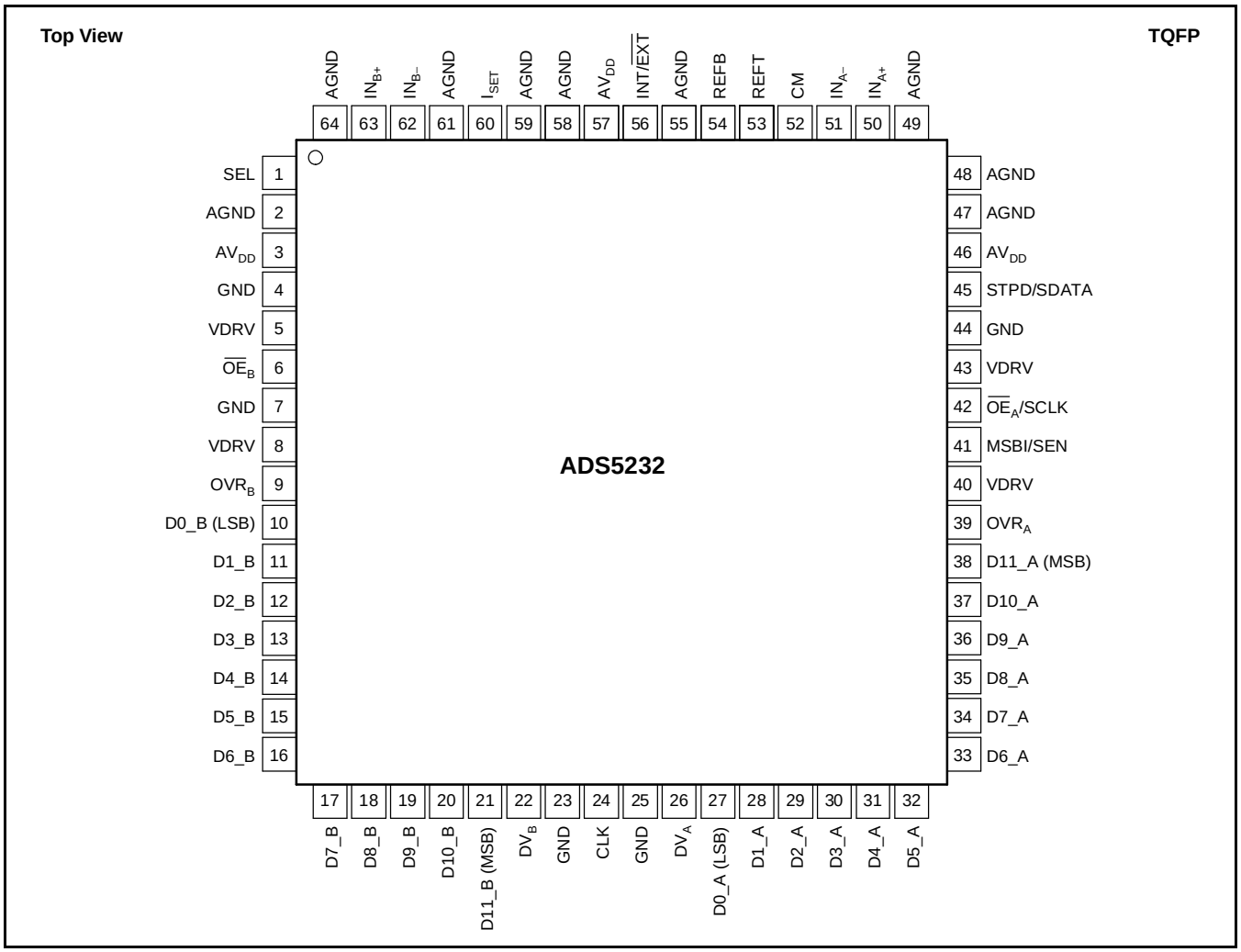
NOTE: 10µs < t_1 < 50ms; 10µs < t_2 < 50ms; −10ms < t_3 < 10ms; t_4 > 10ms; t_5 > 100ns; t_6 > 100ns; t_7 > 10ms; and t_8 > 100µs.

POWER-DOWN TIMING



NOTE: The shown power−up time is based on 1µF bypass capacitors on the reference pins.
See the *Theory of Operation* section for details.

PIN CONFIGURATION



PIN DESCRIPTIONS

NAME	PIN #	I/O	DESCRIPTION
AGND	2, 47–49, 55, 58, 59, 61, 64		Analog Ground
AVDD	3, 46, 57		Analog Supply
CLK	24	I	Clock Input
CM	52	O	Common-Mode Voltage Output
D0_A (LSB)	27	O	Data Bit 12 (D0), Channel A
D1_A	28	O	Data Bit 11 (D1), Channel A
D2_A	29	O	Data Bit 10 (D2), Channel A
D3_A	30	O	Data Bit 9 (D3), Channel A
D4_A	31	O	Data Bit 8 (D4), Channel A
D5_A	32	O	Data Bit 7 (D5), Channel A
D6_A	33	O	Data Bit 6 (D6), Channel A
D7_A	34	O	Data Bit 5 (D7), Channel A
D8_A	35	O	Data Bit 4 (D8), Channel A
D9_A	36	O	Data Bit 3 (D9), Channel A
D10_A	37	O	Data Bit 2 (D10), Channel A
D11_A (MSB)	38	O	Data Bit 1 (D11), Channel A
D0_B (LSB)	10	O	Data Bit 12 (D0), Channel B

PIN DESCRIPTIONS (continued)

NAME	PIN #	I/O	DESCRIPTION
D1_B	11	O	Data Bit 11 (D1), Channel B
D2_B	12	O	Data Bit 10 (D2), Channel B
D3_B	13	O	Data Bit 9 (D3), Channel B
D4_B	14	O	Data Bit 8 (D4), Channel B
D5_B	15	O	Data Bit 7 (D5), Channel B
D6_B	16	O	Data Bit 6 (D6), Channel B
D7_B	17	O	Data Bit 5 (D7), Channel B
D8_B	18	O	Data Bit 4 (D8), Channel B
D9_B	19	O	Data Bit 3 (D9), Channel B
D10_B	20	O	Data Bit 2 (D10), Channel B
D11_B (MSB)	21	O	Data Bit 1 (D11), Channel B
DV_A	26	O	Data Valid, Channel A
DV_B	22	O	Data Valid, Channel B
GND	4, 7, 23, 25, 44		Output Buffer Ground
IN_A	50	I	Analog Input, Channel A
$\overline{IN}_A$	51	I	Complementary Analog Input, Channel A
IN_B	63	I	Analog Input, Channel B
$\overline{IN}_B$	62	I	Complementary Analog Input, Channel B
INT/$\overline{EXT}$	56	I	Reference Select; 0 = External (Default), 1 = Internal; Force high to set for internal reference operation.
I_{SET}	60	O	Bias Current Setting Resistor of 56.2kΩ to Ground
MSBI/SEN	41	I	When SEL = 0, MSBI (Most Significant Bit Invert) 1 = Binary Two's Complement, 0 = Straight Offset Binary (Default) When SEL = 1, SEN (Serial Write Enable)
$\overline{OE}_A$/SCLK	42	I	When SEL = 0, $\overline{OE}_A$ (Output Enable Channel A) 0 = Enabled (Default), 1 = Tri-State When SEL = 1, SCLK (Serial Write Clock)
$\overline{OE}_B$	6	I	Output Enable, Channel B (0 = Enabled [Default], 1 = Tri-State)
OVR_A	39	O	Over-Range Indicator, Channel A
OVR_B	9	O	Over-Range Indicator, Channel B
REF_B	54	I/O	Bottom Reference/Bypass (2Ω resistor in series with a 0.1μF capacitor to ground)
REF_T	53	I/O	Top Reference/Bypass (2Ω resistor in series with a 0.1μF capacitor to ground)
SEL	1	I	Serial interface select signal. Setting SEL = 0 configures pins 41, 42, and 45 as MSBI, $\overline{OE}_A$, and STPD, respectively. With SEL = 0, the serial interface is disabled. Setting SEL = 1 enables the serial interface and configures pins 41, 42, and 45 as SEN, SCLK, and SDATA, respectively. Serial registers can be programmed using these three signals. When used in this mode of operation, it is essential to provide a low-going pulse on SEL in order to reset the serial interface registers as soon as the device is powered up. SEL therefore also has the functionality of a $\overline{RESET}$ signal.
STPD/SDATA	45	I	When SEL = 0, STPD (Power Down) 0 = Normal Operation (Default), 1 = Enabled When SEL = 1, SDATA (Serial Write Data)
VDRV	5, 8, 40, 43		Output Buffer Supply

DEFINITION OF SPECIFICATIONS

Analog Bandwidth

The analog input frequency at which the spectral power of the fundamental frequency (as determined by FFT analysis) is reduced by 3dB.

Aperture Delay

The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs.

Aperture Uncertainty (Jitter)

The sample-to-sample variation in aperture delay.

Clock Duty Cycle

Pulse width high is the minimum amount of time that the ADCLK pulse should be left in logic '1' state to achieve rated performance. Pulse width low is the minimum time that the ADCLK pulse should be left in a low state (logic '0'). At a given clock rate, these specifications define an acceptable clock duty cycle.

Differential Nonlinearity (DNL)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation of any single LSB transition at the digital output from an ideal 1 LSB step at the analog input. If a device claims to have no missing codes, it means that all possible codes (for a 12-bit converter, 4096 codes) are present over the full operating range.

Effective Number of Bits (ENOB)

The ENOB is a measure of converter performance as compared to the theoretical limit based on quantization noise.

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02}$$

Integral Nonlinearity (INL)

INL is the deviation of the transfer function from a reference line measured in fractions of 1 LSB using a *best straight line* or *best fit* determined by a least square curve fit. INL is independent from effects of offset, gain or quantization errors.

Maximum Conversion Rate

The encode rate at which parametric testing is performed. This is the maximum sampling rate where certified operation is given.

Minimum Conversion Rate

This is the minimum sampling rate where the ADC still works.

Signal-to-Noise and Distortion (SINAD)

SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but not including DC.

$$\text{SINAD} = 10\text{Log}_{10}\frac{P_S}{P_N + P_D}$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the full-scale range of the converter.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at DC and the first eight harmonics.

$$\text{SNR} = 10\text{Log}_{10}\frac{P_S}{P_N}$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the full-scale range of the converter.

Spurious-Free Dynamic Range

The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

Two-Tone, Third-Order Intermodulation Distortion

Two-tone IMD3 is the ratio of power of the fundamental (at frequencies f_1 and f_2) to the power of the worst spectral component of third-order intermodulation distortion at either frequency $2f_1 - f_2$ or $2f_2 - f_1$. IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the full-scale range of the converter.

TYPICAL CHARACTERISTICS

T_{MIN} = –40°C and T_{MAX} = +85°C. Typical values are at T_A = +25°C, clock frequency = 65MSPS, 50% clock duty cycle, AVDD = 3.3V, VDRV = 3.3V, transformer-coupled inputs, –1dBFS, I_{SET} = 56.2kΩ, and internal voltage reference, unless otherwise noted.

SPECTRAL PERFORMANCE

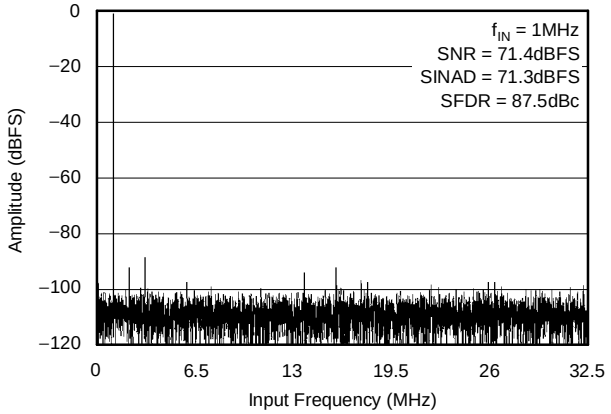


Figure 1.

SPECTRAL PERFORMANCE

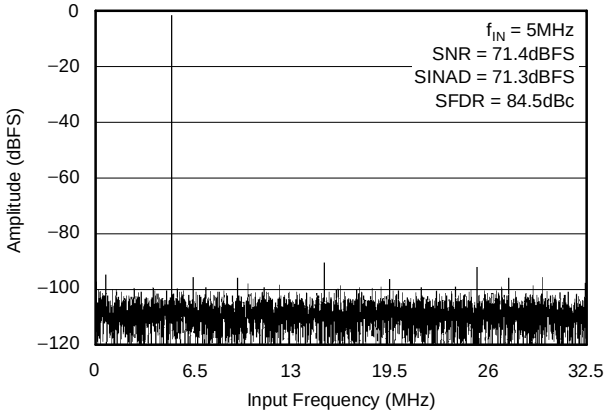


Figure 2.

SPECTRAL PERFORMANCE

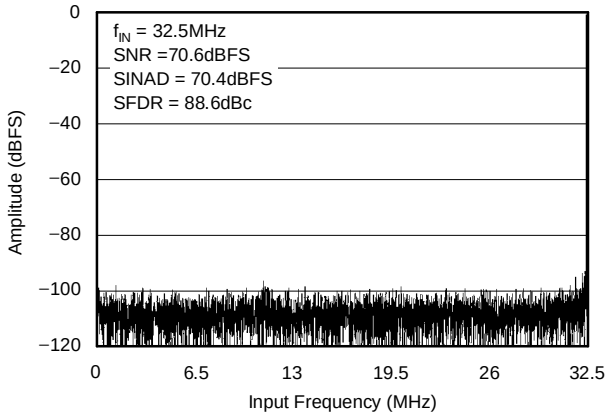


Figure 3.

SPECTRAL PERFORMANCE

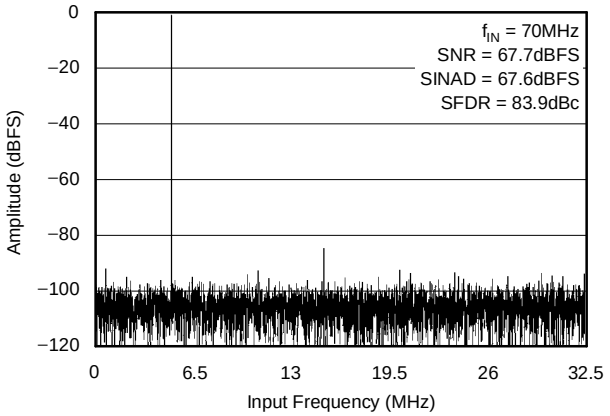


Figure 4.

INTERMODULATION DISTORTION

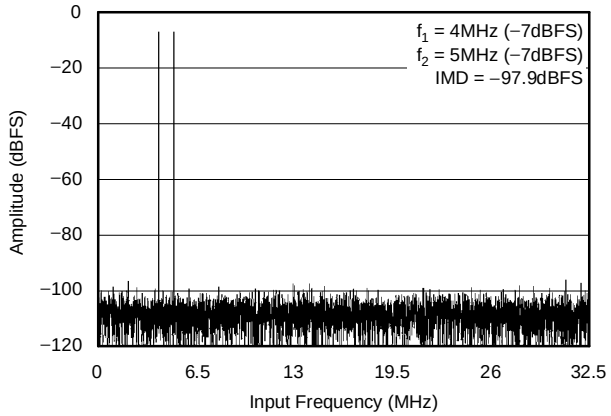


Figure 5.

DIFFERENTIAL NONLINEARITY

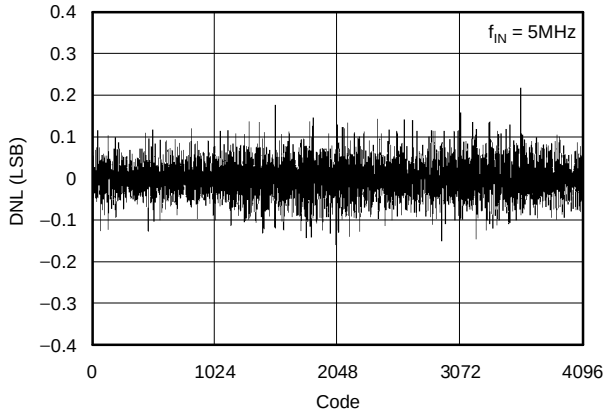


Figure 6.

TYPICAL CHARACTERISTICS (continued)

T_{MIN} = –40°C and T_{MAX} = +85°C. Typical values are at T_A = +25°C, clock frequency = 65MSPS, 50% clock duty cycle, AVDD = 3.3V, VDRV = 3.3V, transformer-coupled inputs, –1dBFS, I_{SET} = 56.2kΩ, and internal voltage reference, unless otherwise noted.

INTEGRAL NONLINEARITY

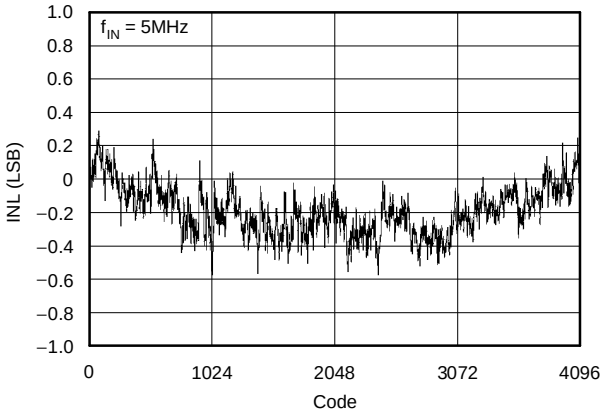


Figure 7.

IAVDD, IVDRV vs CLOCK FREQUENCY

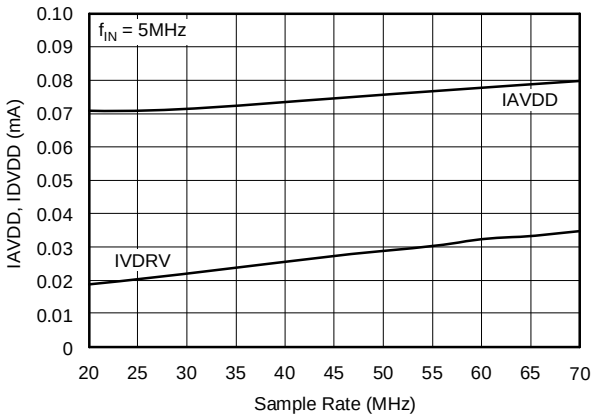


Figure 8.

DYNAMIC PERFORMANCE vs CLOCK FREQUENCY

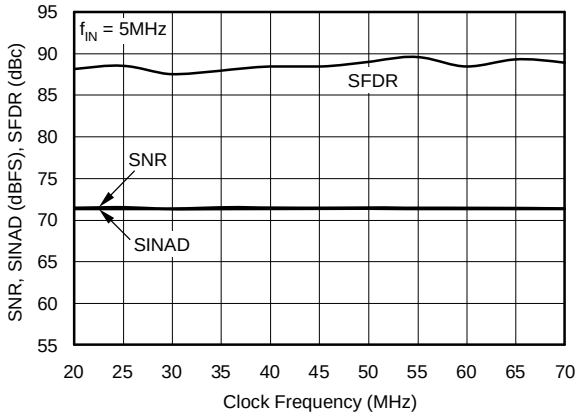


Figure 9.

DYNAMIC PERFORMANCE vs INPUT FREQUENCY

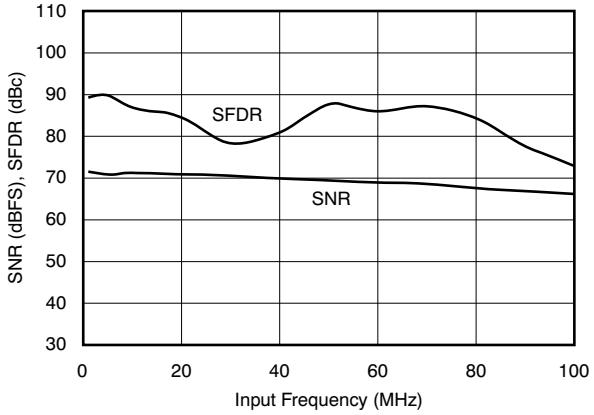


Figure 10.

DYNAMIC PERFORMANCE vs INPUT FREQUENCY

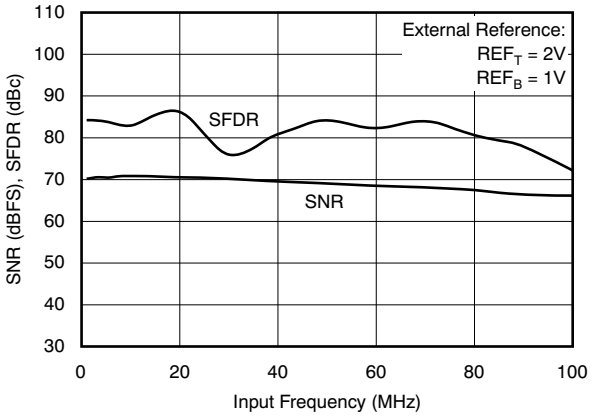


Figure 11.

DYNAMIC PERFORMANCE vs CLOCK DUTY CYCLE WITH PLL ENABLED (default)

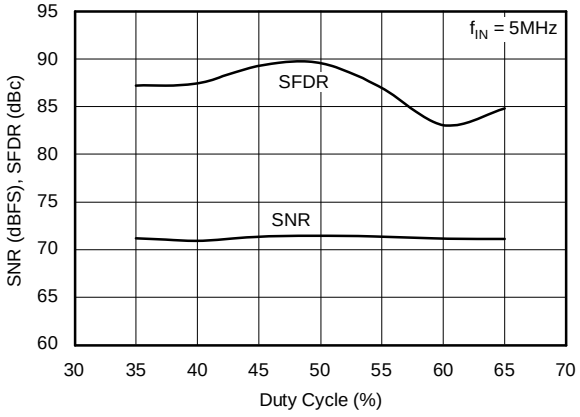


Figure 12.

TYPICAL CHARACTERISTICS (continued)

T_{MIN} = –40°C and T_{MAX} = +85°C. Typical values are at T_A = +25°C, clock frequency = 65MSPS, 50% clock duty cycle, AVDD = 3.3V, VDRV = 3.3V, transformer-coupled inputs, –1dBFS, I_{SET} = 56.2kΩ, and internal voltage reference, unless otherwise noted.

DYNAMIC PERFORMANCE vs TEMPERATURE

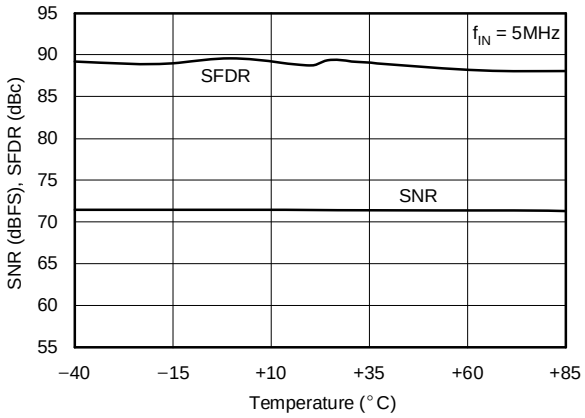


Figure 13.

POWER DISSIPATION vs TEMPERATURE

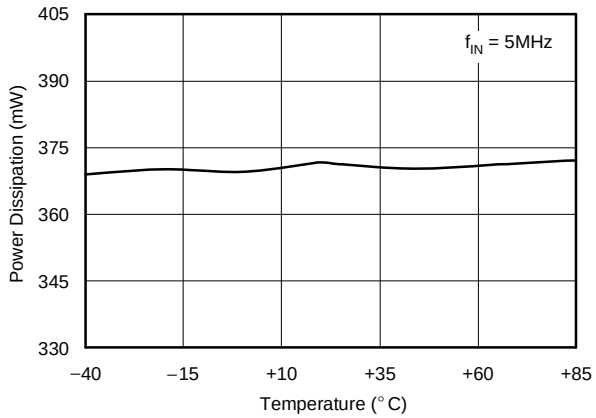


Figure 14.

OUTPUT NOISE

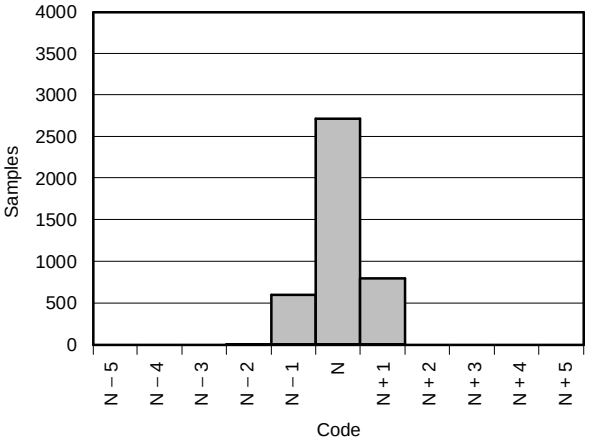


Figure 15.

SWEPT INPUT POWER

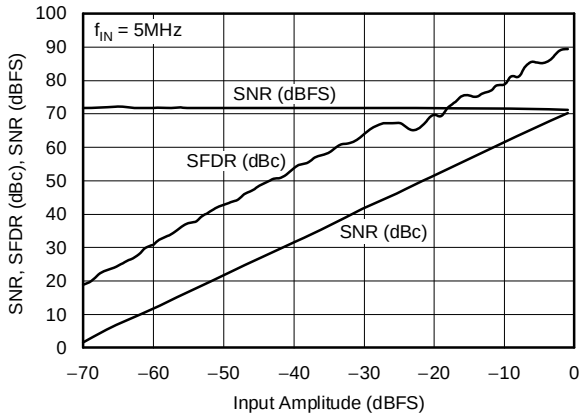


Figure 16.

SWEPT INPUT POWER

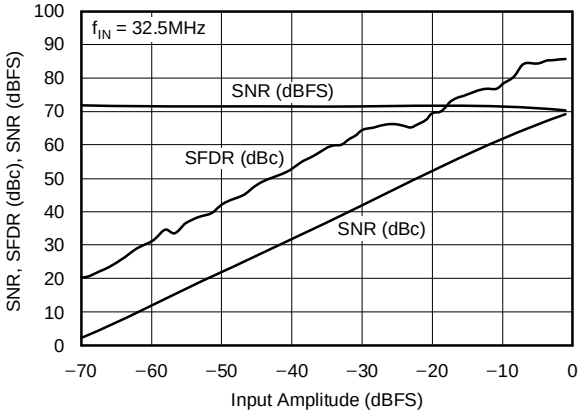


Figure 17.

APPLICATION INFORMATION

THEORY OF OPERATION

The ADS5232 is a dual-channel, simultaneous sampling analog-to-digital converter (ADC). Its low power and high sampling rate of 65MSPS is achieved using a state-of-the-art switched capacitor pipeline architecture built on an advanced low-voltage CMOS process. The ADS5232 operates from a +3.3V supply voltage for both its analog and digital supply connections. The ADC core of each channel consists of a combination of multi-bit and single-bit internal pipeline stages. Each stage feeds its data into the digital error correction logic, ensuring excellent differential linearity and no missing codes at the 12-bit level. The conversion process is initiated by the rising edge of the external clock. Once the signal is captured by the input sample-and-hold amplifier, the input sample is sequentially converted within the pipeline stages. This process results in a data latency of six clock cycles, after which the output data is available as a 12-bit parallel word, coded in either straight offset binary (SOB) or binary two's complement (BTC) format. Since a common clock controls the timing of both channels, the analog signal is sampled simultaneously. The data on the parallel ports is updated simultaneously as well. Further processing can be timed using the individual data valid output signal of each channel. The ADS5232 features internal references that are trimmed to ensure a high level of accuracy and matching. The internal references can be disabled to allow for external reference operation.

INPUT CONFIGURATION

The analog input for the ADS5232 consists of a differential sample-and-hold architecture implemented using a switched capacitor technique; see Figure 18. The sampling circuit consists of a low-pass RC filter at the input to filter out noise components that potentially could be differentially coupled on the input pins. The inputs are sampled on two 4pF capacitors. The RLC model is illustrated in Figure 18.

INPUT DRIVER CONFIGURATIONS

Transformer-Coupled Interface

If the application requires a signal conversion from a single-ended source to drive the ADS5232 differentially, an RF transformer could be a good solution. The selected transformer must have a center tap in order to apply the common-mode DC voltage (V_{CM}) necessary to bias the converter inputs. AC grounding the center tap will generate the differential signal swing across the secondary winding. Consider a step-up transformer to take advantage of signal amplification without the introduction of another noise source. Furthermore, the reduced signal swing from the source may lead to improved distortion performance. The differential input configuration may provide a noticeable advantage for achieving good SFDR performance over a wide range of input frequencies. In this mode, both inputs (IN and $\overline{\text{IN}}$) of the ADS5232 see matched impedances.

Figure 19 illustrates the schematic for the suggested transformer-coupled interface circuit. The component values of the RC low-pass filter may be optimized depending on the desired roll-off frequency.

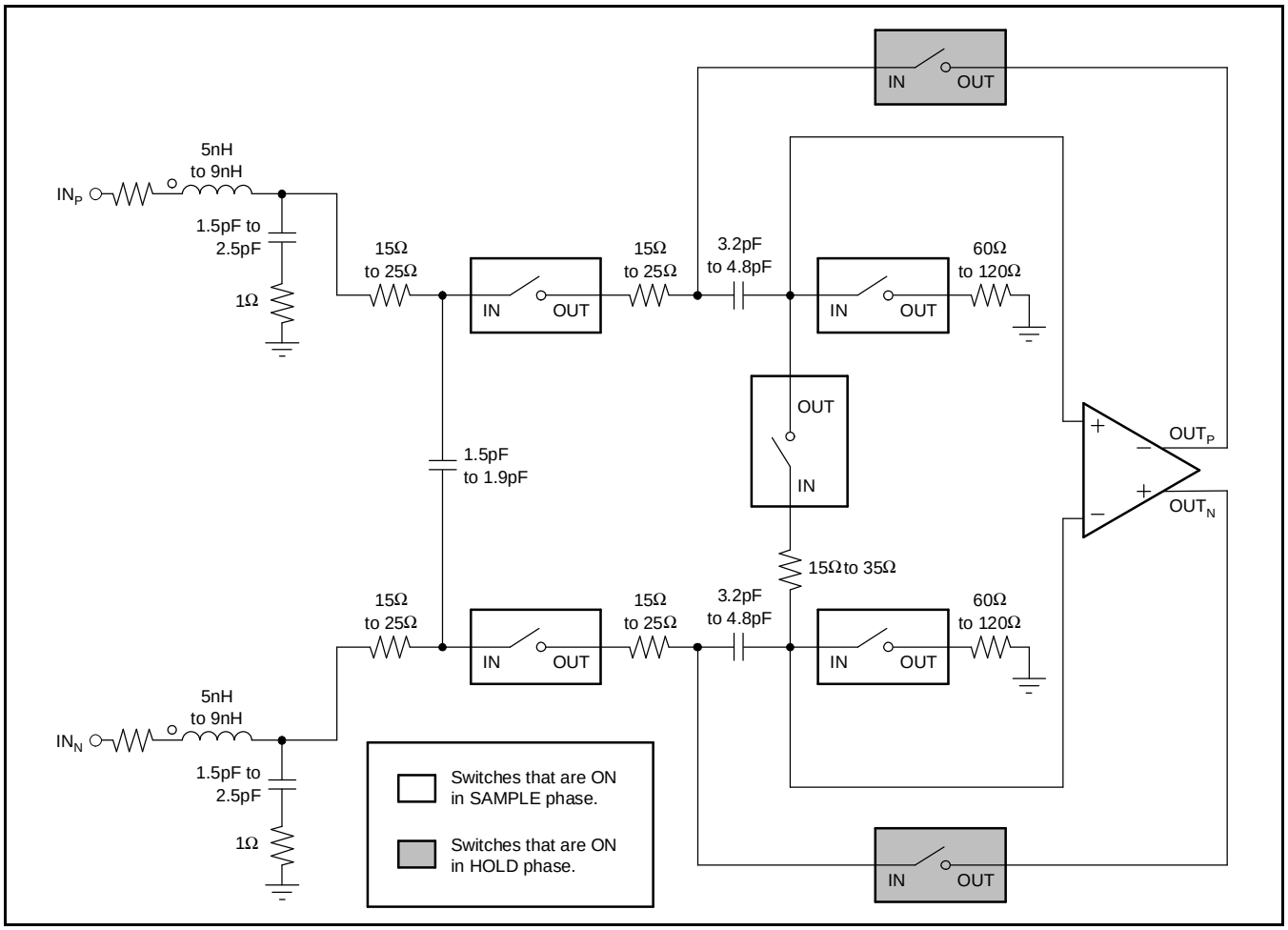


Figure 18. Input Circuitry

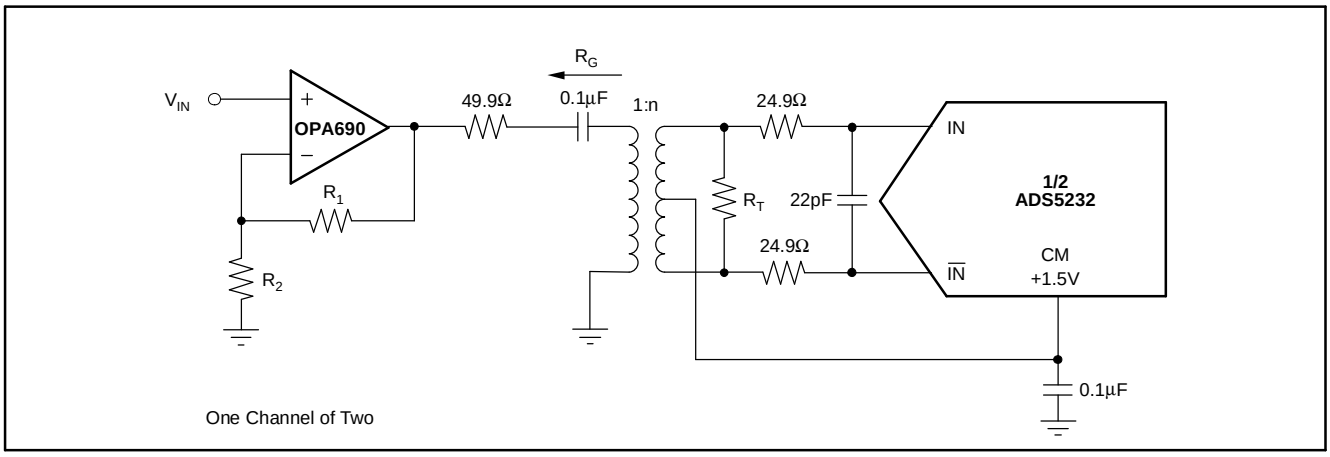


Figure 19. Converting a Single-Ended Input Signal into a Differential Signal Using an RF-Transformer

DC-Coupled Input with Differential Amplifier

Applications that have a requirement for DC-coupling a differential amplifier, such as the THS4503, can be used to drive the ADS5232; this design is shown in Figure 20. The THS4503 amplifier easily allows a single-ended to differential conversion, which reduces component cost.

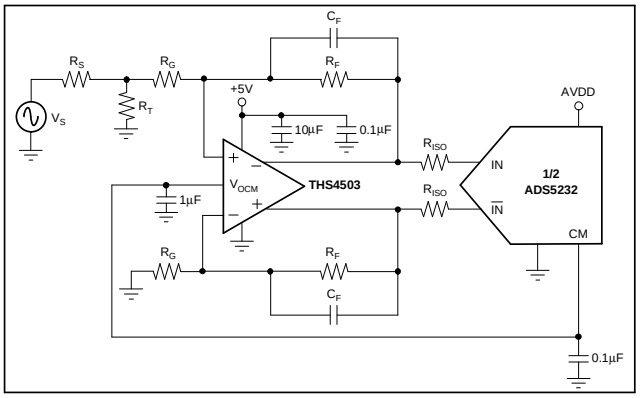


Figure 20. Using the THS4503 with the ADS5232

In addition, the V_{OCM} pin on the THS4503 can be directly tied to the common-mode pin (CM) of the ADS5232 to set up the necessary bias voltage for the converter inputs. In the circuit example shown in Figure 20, the THS4503 is configured for unity gain. If required, a higher gain can easily be achieved as well by adding small capacitors (such as 10pF) in parallel with the feedback resistors to create a low-pass filter. Since the THS4503 is driving a capacitive load, small series resistors in the output ensure stable operation. Further details of this and the overall operation of the THS4503 may be found in its product data sheet (available for download at www.ti.com). In general, differential amplifiers provide a high-performance driver solution for baseband applications, and other differential amplifier models may be selected depending on the system requirements.

Input Over-Voltage Recovery

The differential full-scale input range supported by the ADS5232 is $2V_{PP}$. For a nominal value of V_{CM} (+1.5V), IN and $\overline{IN}$ can swing from 1V to 2V. The ADS5232 is especially designed to handle an over-voltage differential peak-to-peak voltage of 4V (2.5V and 0.5V swings on IN and $\overline{IN}$). If the input common-mode voltage is not considerably different from V_{CM} during overload (less than 300mV), recovery from an over-voltage input condition is expected to be within three clock cycles. All of the amplifiers in the sample-and-hold stage and the ADC core are especially designed for excellent recovery from an overload signal.

REFERENCE CIRCUIT

Internal Reference

All bias currents required for the proper operation of the ADS5232 are set using an external resistor at I_{SET} (pin 60), as shown in Figure 21. Using a 56.2kΩ resistor on I_{SET} generates an internal reference current of about 20µA. This current is mirrored internally to generate the bias current for the internal blocks. While a 5% resistor tolerance is adequate, deviating from this resistor value alters and degrades device performance. For example, using a larger external resistor at I_{SET} reduces the reference bias current and thereby scales down the device operating power.

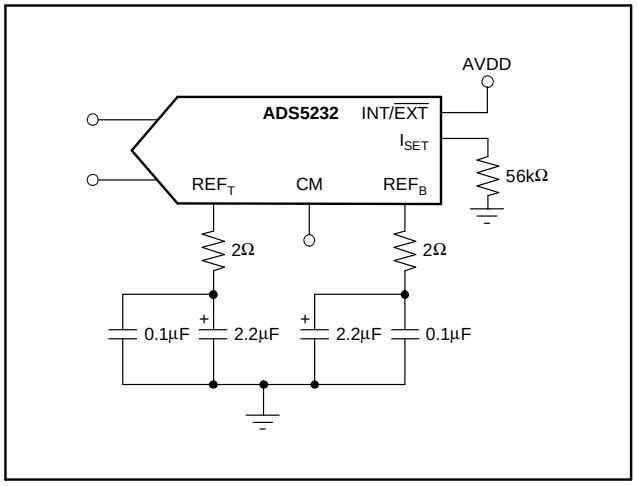


Figure 21. Internal Reference Circuit

As part of the internal reference circuit, the ADS5232 provides a common-mode voltage output at pin 52, CM. This common-mode voltage is typically +1.5V. While this is similar to the common-mode voltage used internally within the ADC pipeline core, the CM-pin has an independent buffer amplifier, which can deliver up to ±2mA of current to an external circuit for proper input signal level shifting and biasing. In order to obtain optimum dynamic performance, the analog inputs should be biased to the recommended common-mode voltage (1.5V). While good performance can be maintained over a certain CM-range, larger deviations may compromise device performance and could also negatively affect the overload recovery behavior. Using the internal reference mode requires the INT/$\overline{EXT}$ pin to be forced high, as shown in Figure 21.

The ADS5232 requires solid high-frequency bypassing on both reference pins, REF_T and REF_B; see Figure 21. Use ceramic 0.1µF capacitors (size 0603, or smaller), located as close as possible to the pins.

External Reference

The ADS5232 also supports the use of external reference voltages. External reference voltage mode involves applying an external top reference at REF_T (pin 53) and a bottom reference at REF_B (pin 54). Setting the ADS5232 for external reference mode also requires taking the INT/$\overline{EXT}$ pin low. In this mode, the internal reference buffer is tri-stated. Since the switching current for the two ADC channels comes from the externally-forced references, it is possible for the device performance to be slightly lower than when the internal references are used. It should be noted that in external reference mode, V_{CM} and I_{SET} continue to be generated from the internal bandgap voltage, as they are in the internal reference mode. Therefore, it is important to ensure that the common-mode voltage of the externally-forced reference voltages matches to within 50mV of V_{CM} ($+1.5V_{DC}$).

The external reference circuit must be designed to drive the internal reference impedance seen between the REF_T and REF_B pins. To establish the drive requirements, consider that the external reference circuit needs to supply an average switching current of at least 1mA. This dynamic switching current depends on the actual device sampling rate and the signal level. The external reference voltages can vary as long as the value of the external top reference stays within the range of +1.875V to +2.0V, and the external bottom reference stays within +1.0V to +1.125V. Consequently, the full-scale input range can be set between $1.5V_{PP}$ and $2V_{PP}$ (FSR = 2x [REF_T – REF_B]).

CLOCK INPUT

The ADS5232 requires a single-ended clock source. The clock input, CLK, represents a CMOS-compatible logic input with an input impedance of about 5pF. For high input frequency sampling, it is recommended to use a clock source with very low jitter. A low-jitter clock is essential in order to preserve the excellent ac performance of the ADS5232. The converter itself is specified for a low 1.0ps (rms) jitter. Generally, as the input frequency increases, clock jitter becomes more dominant in maintaining a good signal-to-noise ratio (SNR). This condition is particularly critical in IF-sampling applications; for example, where the sampling frequency is lower than the input frequency (under-sampling). The following equation can be used to calculate the achievable SNR for a given input frequency and clock jitter (t_{JA} in ps_{RMS}):

$$SNR = 20LOG_{10}\frac{1}{(2\pi f_{IN} t_{JA})} \quad (1)$$

The ADS5232 will enter into a power-down mode if the sampling clock rate drops below a limit of approximately 2MSPS. If the sampling rate is increased above this threshold, the ADS5232 will automatically resume normal operation.

PLL CONTROL

The ADS5232 has an internal PLL that is enabled by default. The PLL enables a wide range of clock duty cycles. Good performance is obtained for duty cycles up to 40%–60%, though the ensured electrical specifications presume that the duty cycle is between 45%–55%. The PLL automatically limits the minimum frequency of operation to 20MSPS. For operation below 20MSPS, the PLL can be disabled by programming the internal registers through the serial interface. With the PLL disabled, the clock speed can go down to 2MSPS. With the PLL disabled, the clock duty cycle needs to be constrained closer to 50%.

OUTPUT INFORMATION

The ADS5232 provides two channels with 12 data outputs (D11 to D0, with D11 being the MSB and D0 the LSB), data-valid outputs (DV_A, DV_B, pin 26 and pin 22, respectively), and individual out-of-range indicator output pins (OVR_A/OVR_B, pin 39 and pin 9, respectively).

The output circuitry of the ADS5232 has been designed to minimize the noise produced by transients of the data switching, and in particular its coupling to the ADC analog circuitry.

DATA OUTPUT FORMAT (MSBI)

The ADS5232 makes two data output formats available: the *Straight Offset Binary* code (SOB) or the *Binary Two's Complement* code (BTC). The selection of the output coding is controlled by the MSBI (pin 41). Because the MSBI pin has an internal pull-down, the ADS5232 will operate with the SOB code as its default setting. Forcing the MSBI pin high will enable BTC coding. The two code structures are identical, with the exception that the MSB is inverted for BTC format; as shown in Table 1.

OUTPUT ENABLE ($\overline{OE}$)

Digital outputs of the ADS5232 can be set to high-impedance (tri-state), exercising the output enable pins, $\overline{OE}_A$ (pin 42), and $\overline{OE}_B$ (pin 6). Internal pull-downs configure the output in enable mode for normal operation. Applying a logic high voltage will disable the outputs. Note that the $\overline{OE}$-function is not designed to be operated dynamically (that is, as a fast multiplexer) because it may lead to corrupt conversion results. Refer to the Electrical Characteristics table to observe the specified tri-state enable and disable times.

OVER-RANGE INDICATOR (OVR)

If the analog input voltage exceeds the full-scale range set by the reference voltages, an over-range condition exists. The ADS5232 incorporates a function that monitors the input voltage and detects any such out-of-range condition. This operation functions for each of the two channels independently. The current state can be read at the over-range indicator pins (pins 9 and 39). This output is low when the input voltage is within the defined input range. It will change to high if the applied signal exceeds the full-scale range. It should be noted that each of the OVR outputs is updated along with the data output corresponding to the particular sampled analog input voltage. Therefore, the OVR state is subject to the same pipeline delay as the digital data (six clock cycles).

OUTPUT LOADING

It is recommended that the capacitive loading on the data output lines be kept as low as possible, preferably below 15pF. Higher capacitive loading will cause larger dynamic currents as the digital outputs are changing. Such high current surges can feed back to the analog portion of the ADS5232 and adversely affect device performance. If necessary, external buffers or latches close to the converter output pins may be used to minimize the capacitive loading.

SERIAL INTERFACE

The ADS5232 has a serial interface that can be used to program internal registers. The serial interface is disabled if SEL is connected to 0.

When the serial interface is to be enabled, SEL serves the function of a $\overline{RESET}$ signal. After the supplies have stabilized, it is necessary to give the device a low-going pulse on SEL. This results in all internal registers resetting to their default value of 0 (inactive). Without a reset, it is possible that registers may be in their non-default state on power-up. This condition may cause the device to malfunction.

Table 1. Coding Table for Differential Input Configuration and $2V_{PP}$ Full-Scale Input Range

DIFFERENTIAL INPUT	STRAIGHT OFFSET BINARY (SOB; MSBI = 0) D11.....D0	BINARY TWO'S COMPLEMENT (BTC; MSBI = 1) D11.....D0
+FS (IN = +2V, $\overline{IN}$ = +1V)	1111 1111 1111	0111 1111 1111
+1/2 FS	1100 0000 0000	0100 0000 0000
Bipolar Zero (IN = $\overline{IN}$ = CMV)	1000 0000 0000	0000 0000 0000
–1/2 FS	0100 0000 0000	1100 0000 0000
–FS (IN = +1V, $\overline{IN}$ = +2V)	0000 0000 0000	1000 0000 0000

POWER-DOWN MODE

The ADS5232 has a power-down pin, STPD (pin 45). The internal pull-down is in default mode for the device during normal operation. Forcing the STPD pin high causes the device to enter into power-down mode. In power-down mode, the reference and clock circuitry as well as all the channels are powered down. Device power consumption drops to less than 90mW. As previously mentioned, the ADS5232 also enters into a power-down mode if the clock speed drops below 2MSPS (see the *Clock Input* section).

When STPD is pulled high, the internal buffers driving REF_T and REF_B are tri-stated and the outputs are forced to a voltage roughly equal to half of the voltage on AV_{DD}. Speed of recovery from the power-down mode depends on the value of the external capacitance on the REF_T and REF_B pins. For capacitances on REF_T and REF_B less than 1µF, the reference voltages settle to within 1% of their steady-state values in less than 500µs. Either of the two channels can also be selectively powered-down through the serial interface when it is enabled.

The ADS5232 also has an internal circuit that monitors the state of stopped clocks. If ADCLK is stopped for longer than 250ns, or if it runs at a speed less than 2MHz, this monitoring circuit generates a logic signal that puts the device in a partial power-down state. As a result, the power consumption of the device is reduced when CLK is stopped. The recovery from such a partial power-down takes approximately 100µs. This constraint is described in Table 2.

Table 2. Time Constraints Associated with Device Recovery from Power-Down and Clock Stoppage

DESCRIPTION	TYP	REMARKS
Recovery from power-down mode (STPD = 1 to STPD = 0).	500µs	Capacitors on REF_T and REF_B less than 1µF.
Recovery from momentary clock stoppage (< 250ns).	10µs	
Recovery from extended clock stoppage (> 250ns).	100µs	

LAYOUT AND DECOUPLING CONSIDERATIONS

Proper grounding and bypassing, short lead length, and the use of ground planes are particularly important for high frequency designs. Achieving optimum performance with a fast sampling converter such as the ADS5232 requires careful attention to the printed circuit board (PCB) layout to minimize the effects of board parasitics and to optimize component placement. A multilayer board usually ensures best results and allows convenient component placement.

The ADS5232 should be treated as an analog component and the supply pins connected to clean analog supplies. This layout ensures the most consistent performance results, since digital supplies often carry a high level of switching noise, which could couple into the converter and degrade device performance. As mentioned previously, the output buffer supply pins (VDRV) should also be connected to a low-noise supply. Supplies of adjacent digital circuits may carry substantial current transients. The supply voltage should be filtered before connecting to the VDRV pin of the converter. All ground pins should directly connect to an analog ground.

Because of its high sampling frequency, the ADS5232 generates high frequency current transients and noise (clock feed-through) that are fed back into the supply and reference lines. If not sufficiently bypassed, this feed-through adds noise to the conversion process. All AV_{DD} pins may be bypassed with 0.1µF ceramic chip capacitors (size 0603, or smaller). A similar approach may be used on the output buffer supply pins, VDRV. In order to minimize the lead and trace inductance, the capacitors should be located as close to the supply pins as possible. Where double-sided component mounting is allowed, they are best placed directly under the package. In addition, larger bipolar decoupling capacitors (2.2µF to 10µF), effective at lower frequencies, may also be used on the main supply pins. They can be placed on the PCB in proximity (< 0.5") to the ADC.

If the analog inputs to the ADS5232 are driven differentially, it is especially important to optimize towards a highly symmetrical layout. Small trace length differences may create phase shifts, compromising a good distortion performance. For this reason, the use of two single op amps rather than one dual amplifier enables a more symmetrical layout and a better match of parasitic capacitances. The pin orientation of the ADS5232 quad-flat package follows a *flow-through* design, with the analog inputs located on one side of the package while the digital outputs are located on the opposite side. This design provides a good physical isolation between the analog and digital connections. While designing the layout, it is important to keep the analog signal traces separated from any digital lines to prevent noise coupling onto the analog portion.

Single-ended clock lines must be short and should not cross any other signal traces.

Short circuit traces on the digital outputs will minimize capacitive loading. Trace length should be kept short to the receiving gate (< 2") with only one CMOS gate connected to one digital output.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS5232IPAG	Active	Production	TQFP (PAG) | 64	160 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-4-260C-72 HR	-40 to 85	ADS5232IPAG
ADS5232IPAG.A	Active	Production	TQFP (PAG) | 64	160 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-4-260C-72 HR	-40 to 85	ADS5232IPAG
ADS5232IPAGG4.A	Active	Production	TQFP (PAG) | 64	160 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-4-260C-72 HR	-40 to 85	ADS5232IPAG

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

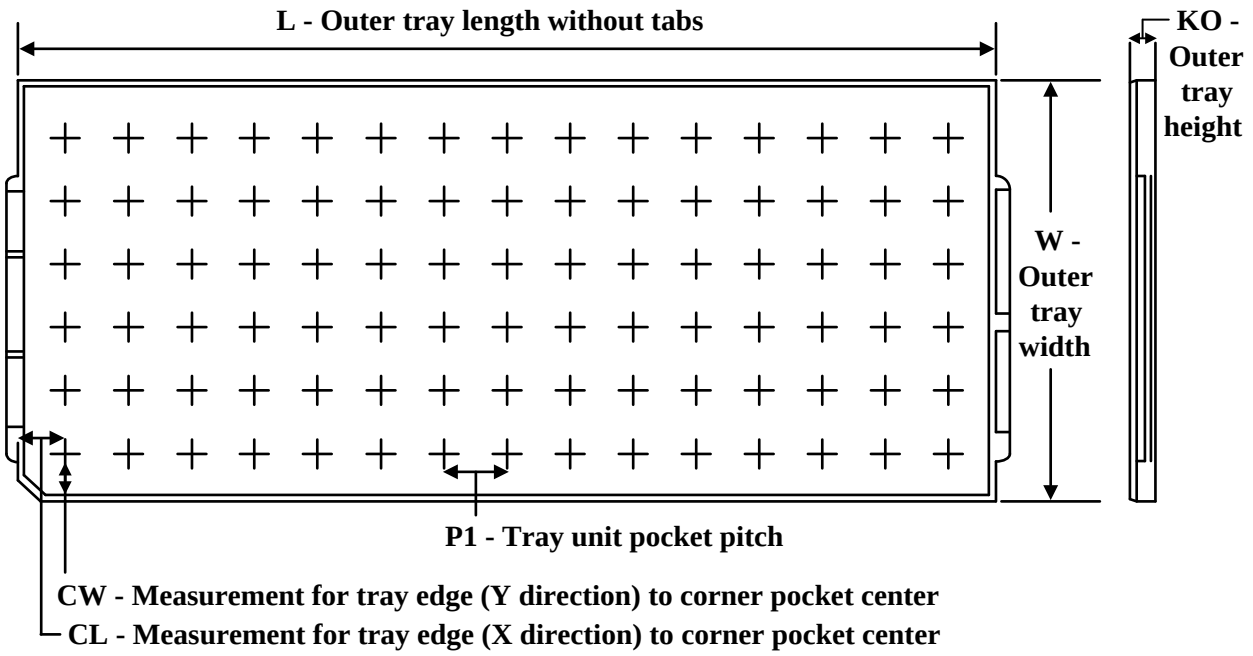
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TRAY

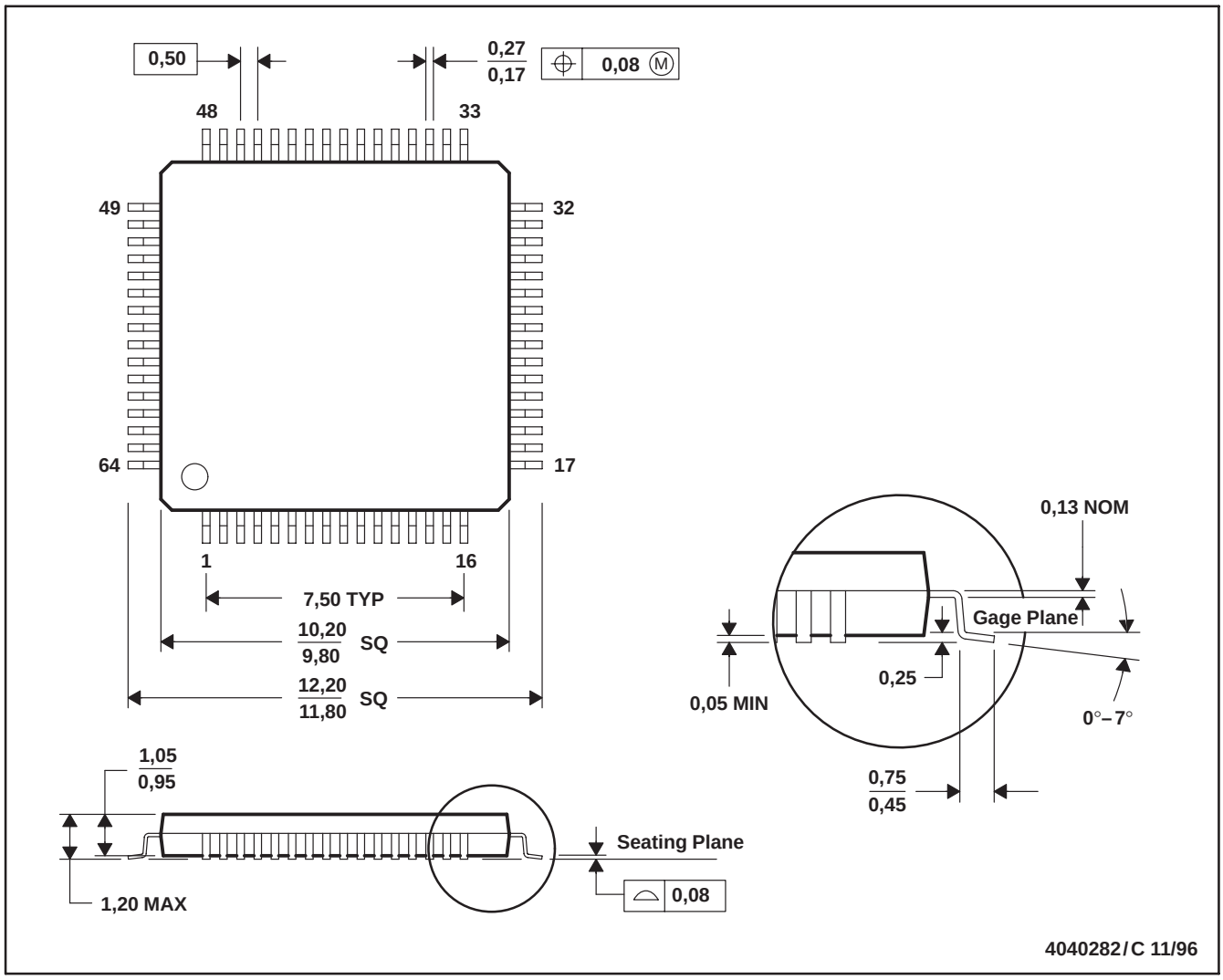


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

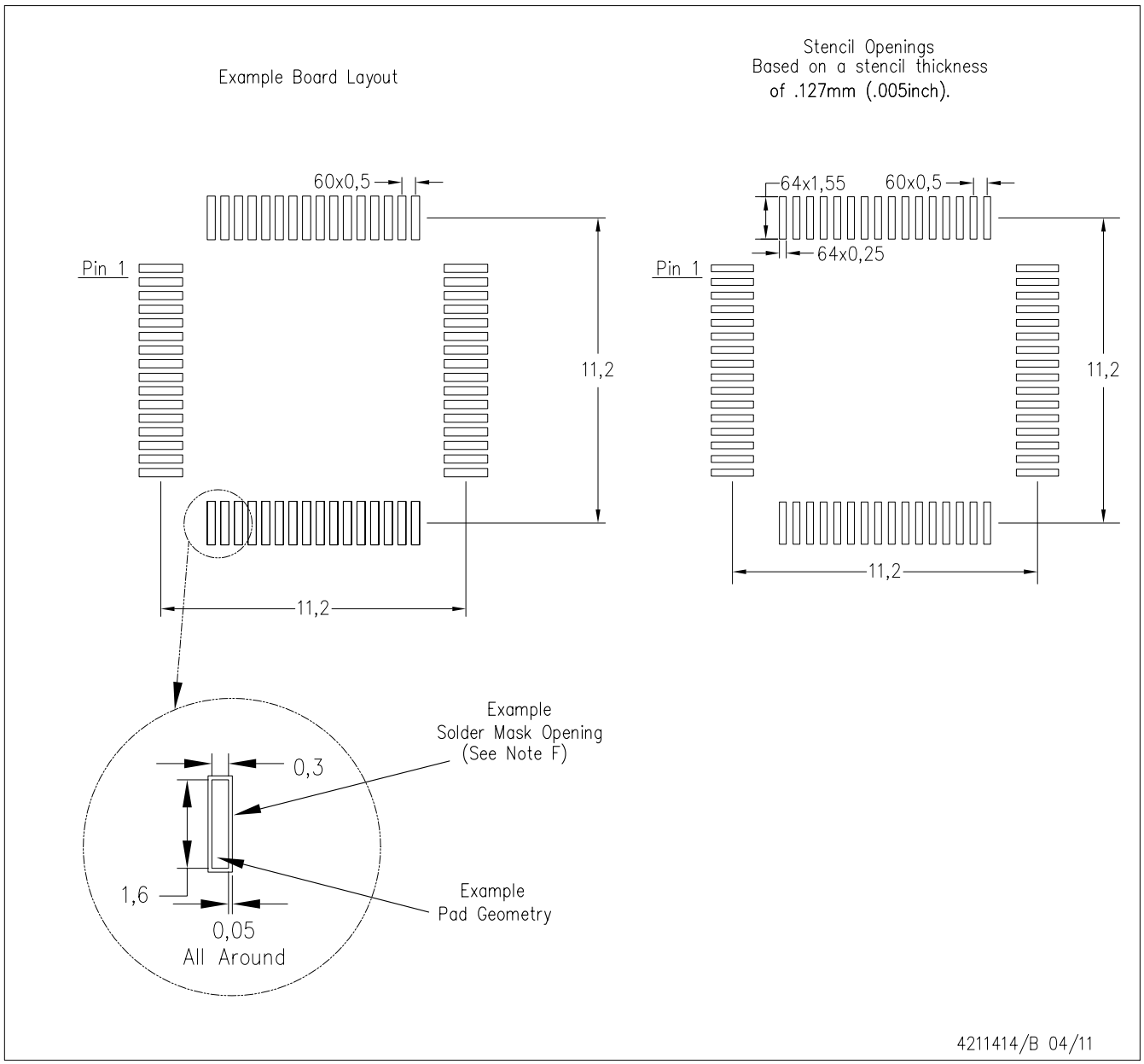
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
ADS5232IPAG	PAG	TQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
ADS5232IPAG.A	PAG	TQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
ADS5232IPAGG4.A	PAG	TQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13

PAG (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



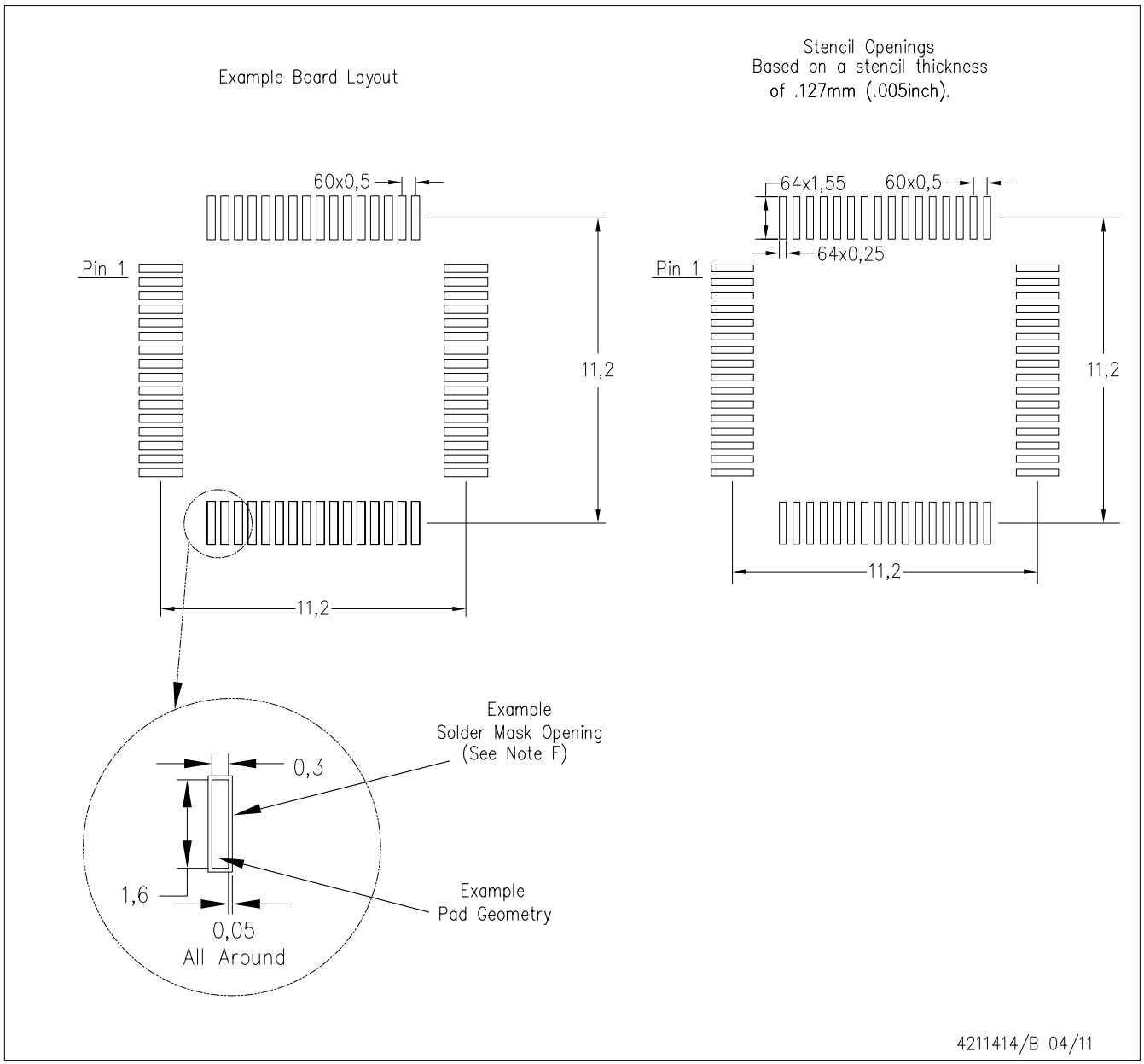
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PAG (S–PQFP–G64) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PAG (S–PQFP–G64) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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