ADS131M04-Q1 Automotive, 4-Channel, 64-kSPS, Simultaneous-Sampling, 24-Bit, Delta-Sigma ADC

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- 4 simultaneously sampling differential inputs
- Programmable data rate up to 64 kSPS
- Programmable gain up to 128
- Noise performance:
  - 102-dB dynamic range at gain = 1, 4 kSPS
  - 80-dB dynamic range at gain = 64, 4 kSPS
- Total harmonic distortion: –100 dB
- High-impedance inputs for direct sensor connection:
  - 330-kΩ input impedance for gains of 1, 2, and 4
  - ≥1-MΩ input impedance for gains of 8, 16, 32, 64, and 128
- Programmable channel-to-channel phase delay calibration:
  - Resolution = 244 ns, f_{CLKIN} = 8.192 MHz
- Fast start-up:
  - First data within 0.5 ms of supply ramp
- Integrated negative charge pump allows input signals below ground
- Crosstalk between channels: –120 dB
- Low-drift internal voltage reference
- CRC on communications and register map
- Analog and digital supplies: 2.7 V to 3.6 V
- Low-power consumption: 3.3 mW at 3-V AVDD and DVDD
- Package: 20-pin TSSOP

2 Applications

- Automotive battery management systems (BMS):
  - Current-shunt measurements
  - Voltage measurements using external resistor dividers
  - Temperature measurements using thermistors or analog output temperature sensors
- EV charging stations:
  - DC e-metering
  - AC e-metering
- Energy storage systems (ESS)

3 Description

The ADS131M04-Q1 is a four-channel, simultaneously sampling, 24-bit, delta-sigma (ΔΣ), analog-to-digital converter (ADC) that offers wide dynamic range and low power, making the device designed for automotive battery management systems (BMS). The ADC inputs can be directly interfaced to shunt resistors for bidirectional battery-current measurements, to resistor-divider networks for high-voltage measurements, or to temperature sensors (such as thermistors or analog output temperature sensors).

The individual ADC channels can be independently configured depending on the sensor input. A low-noise, programmable gain amplifier (PGA) provides gains ranging from 1 to 128 to amplify low-level signals. Additionally, this device integrates channel-to-channel phase calibration and offset and gain calibration registers to help remove signal-chain errors.

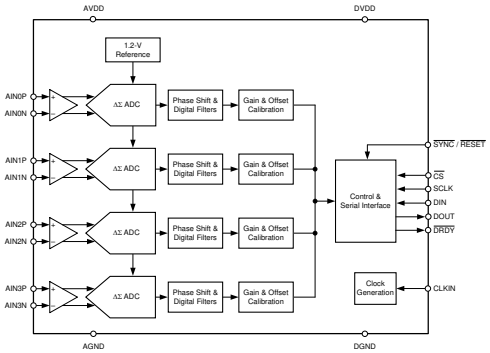
A low-drift, 1.2-V reference is integrated into the device, reducing printed circuit board (PCB) area. Optional cyclic redundancy checks (CRCs) on the data input, data output, and register map maintain communication integrity.

The complete analog front-end (AFE) is offered in a 20-pin TSSOP package and is specified over the automotive temperature range of –40°C to +125°C.

Package Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS131M04-Q1	TSSOP (20)	6.50 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Block Diagram

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2022) to Revision A (August 2022)	Page
• Changed document status from *advance information* to *production data*	1

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5 Pin Configuration and Functions

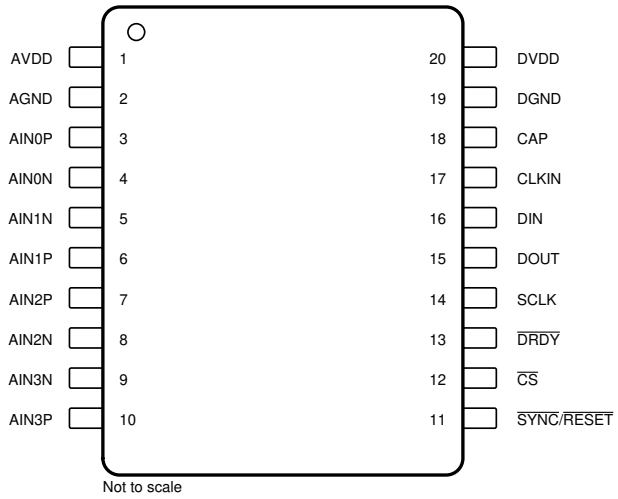

Figure 5-1. PW Package, 20-Pin TSSOP (Top View)

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION[(1)]
NAME	NO.		
AGND	2	Supply	Analog ground
AIN0N	4	Analog input	Negative analog input 0
AIN0P	3	Analog input	Positive analog input 0
AIN1N	5	Analog input	Negative analog input 1
AIN1P	6	Analog input	Positive analog input 1
AIN2N	8	Analog input	Negative analog input 2
AIN2P	7	Analog input	Positive analog input 2
AIN3N	9	Analog input	Negative analog input 3
AIN3P	10	Analog input	Positive analog input 3
AVDD	1	Supply	Analog supply. Connect a 1-µF capacitor to AGND.
CAP	18	Analog output	Digital low-dropout (LDO) regulator output. Connect a 220-nF capacitor to DGND.
CLKIN	17	Digital input	Main clock input
$\overline{CS}$	12	Digital input	Chip select; active low
DGND	19	Supply	Digital ground
DIN	16	Digital input	Serial data input
DOUT	15	Digital output	Serial data output
$\overline{DRDY}$	13	Digital output	Data ready; active low
DVDD	20	Supply	Digital I/O supply. Connect a 1-µF capacitor to DGND.
SCLK	14	Digital input	Serial data clock
$\overline{SYNC}$/$\overline{RESET}$	11	Digital input	Conversion synchronization or system reset; active low

(1) See the *Unused Inputs and Outputs* section for details on how to connect unused pins.

6 Specifications

6.1 Absolute Maximum Ratings

see [(1)]

		MIN	MAX	UNIT
Power-supply voltage	AVDD to AGND	–0.3	3.9	V
	AGND to DGND	–0.3	0.3	
	DVDD to DGND	–0.3	3.9	
	DVDD to DGND, CAP tied to DVDD	–0.3	2.2	
	CAP to DGND	–0.3	2.2	
Analog input voltage	AINxP, AINxN	AGND – 1.6	AVDD + 0.3	
Digital input voltage	$\overline{CS}$, CLKIN, DIN, SCLK, $\overline{SYNC}$/$\overline{RESET}$	DGND – 0.3	DVDD + 0.3	
Input current	Continuous, all pins except power-supply pins	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–60	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[(1)] HBM ESD classification level 2		±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD classification level C4B	Corner pins	±750	
			All other non-corner pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

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6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	Analog power supply	AVDD to AGND, normal operating modes	2.7	3.0	3.6	V
		AVDD to AGND, standby and current-detect modes	2.4	3.0	3.6	
		AGND to DGND	–0.3	0	0.3	
	Digital power supply	DVDD to DGND	2.7	3.0	3.6	V
		DVDD to DGND, DVDD shorted to CAP (digital LDO bypassed)	1.65	1.8	2	
ANALOG INPUTS(1)						
V_{AINxP}, V_{AINxN}	Absolute input voltage	Gain = 1, 2, or 4	AGND – 1.3		AVDD	V
		Gain = 8, 16, 32, 64 or 128	AGND – 1.3		AVDD – 1.8	
V_{IN}	Differential input voltage	$V_{IN} = V_{AINxP} - V_{AINxN}$	$–V_{REF}$ / Gain		V_{REF} / Gain	V
EXTERNAL CLOCK SOURCE						
f_{CLKIN}	External clock frequency	High-resolution mode	0.3	8.192	8.4	MHz
		Low-power mode	0.3	4.096	4.15	
		Very-low-power mode	0.3	2.048	2.08	
	Duty cycle		40%	50%	60%	
DIGITAL INPUTS						
	Input voltage		DGND		DVDD	V
TEMPERATURE RANGE						
T_A	Operating ambient temperature		–40		125	°C

(1) The subscript "x" signifies the channel. For example, the positive analog input to channel 0 is named AIN0P. See the *Pin Configuration and Functions* section for the pin names.

6.4 Thermal Information

THERMAL METRIC(1)		ADS131M04-Q1 PW (TSSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	94.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	34.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	46.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at AVDD = 3 V, DVDD = 3 V, f_{CLKIN} = 8.192 MHz, data rate = 4 kSPS, all channels enabled, global-chop mode disabled and gain = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
I_B	Input bias current	Gain = 1, 2, or 4, V_{INP} = V_{INN} = 0 V, I_B = (I_{BP} + I_{BN}) / 2		0.6		µA
	Input bias current	Gain = 8, 16, 32, 64 or 128, V_{INP} = V_{INN} = 0 V, I_B = (I_{BP} + I_{BN}) / 2		0.2		
Z_{in}	Differential input impedance	Gain = 1, 2, or 4		300		kΩ
		Gain = 8, 16, 32, 64, or 128		±1 (1)		µA/V
ADC CHARACTERISTICS						
	Resolution		24			Bits
	Gain settings			1, 2, 4, 8, 16, 32, 64, 128		
f_{DATA}	Data rate	High-resolution mode, f_{CLKIN} = 8.192 MHz	250		64k	SPS
		Low-power mode, f_{CLKIN} = 4.096 MHz	125		32k	
		Very-low-power mode, f_{CLKIN} = 2.048 MHz	62.5		16k	
	Startup time	Measured from supplies at 90% to first $\overline{DRDY}$ falling edge		0.5		ms
ADC PERFORMANCE						
INL	Integral nonlinearity (best fit)			6		ppm of FSR
	Offset error (input referred)			±175		µV
		Global-chop mode, channel 0		±35		
		Global-chop mode, channels 1-3		±15		
	Offset drift			300		nV/°C
		Global-chop mode		200		
	Offset error time drift	1000 hours at 85°C		4		µV
	Gain error			±0.1%		
	Gain drift			1		ppm/°C
		Including internal reference		8.5		
	Gain error time drift	1000 hours at 85°C		400		ppm
CMRR	Common-mode rejection ratio	At dc		100		dB
		f_{CM} = 50 Hz or 60 Hz		94		
PSRR	Power-supply rejection ratio	AVDD at dc		75		dB
		DVDD at dc		88		
		AVDD supply, f_{PS} = 50 Hz or 60 Hz		78		
		DVDD supply, f_{PS} = 50 Hz or 60 Hz		85		
	Input-referred noise			5.35		$µV_{RMS}$
		During fast-startup		1.5		mV_{RMS}
	Dynamic range	Gain = 1	99	102		dB
		Gain = 64		80		
		All other gain settings		See Table 7-1		
	Crosstalk	f_{IN} = 50 Hz or 60 Hz		–120		dB
SNR	Signal-to-noise ratio	f_{IN} = 50 Hz or 60 Hz, gain = 1, V_{IN} = –0.5 dBFS, normalized		100		dB
		f_{IN} = 50 Hz or 60 Hz, gain = 64, V_{IN} = –0.5 dBFS, normalized		79		

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6.5 Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at AVDD = 3 V, DVDD = 3 V, f_{CLKIN} = 8.192 MHz, data rate = 4 kSPS, all channels enabled, global-chop mode disabled and gain = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THD	Total harmonic distortion	f_{IN} = 50 Hz or 60 Hz (up to 50 harmonics), V_{IN} = –0.5 dBFS		–100		dB
SFDR	Spurious-free dynamic range	f_{IN} = 50 Hz or 60 Hz (up to 50 harmonics), V_{IN} = –0.5 dBFS		105		dB
INTERNAL VOLTAGE REFERENCE						
V_{REF}	Internal reference voltage			1.2		V
	Accuracy	T_A = 25°C		±0.1%		
	Temperature drift			7.5	20	ppm/°C
DIGITAL INPUTS/OUTPUTS						
V_{IL}	Logic input level, low		DGND		0.2 DVDD	V
V_{IH}	Logic input level, high		0.8 DVDD		DVDD	V
V_{OL}	Logic output level, low	I_{OL} = –1 mA			0.2 DVDD	V
V_{OH}	Logic output level, high	I_{OH} = 1 mA	0.8 DVDD			V
I_{IN}	Input current	DGND < $V_{Digital\ Input}$ < DVDD	–1		1	µA
POWER SUPPLY						
I_{AVDD}	Analog supply current	High-resolution mode		3.5	4.0	mA
		Low-power mode		2.0	2.2	
		Very-low-power mode		1.0	1.2	
		Current-detect mode		0.9		mA
		Standby mode		0.3		µA
I_{DVDD}	Digital supply current(2)	High-resolution mode		0.4	0.5	mA
		Low-power mode		0.2	0.3	
		Very-low-power mode		0.1	0.2	
		Current-detect mode		0.065		mA
		Standby mode		1		µA
P_D	Power dissipation	High-resolution mode		12		mW
		Low-power mode		6.6		
		Very-low-power mode		3.3		
		Current-detect mode		2.9		
		Standby mode		3.9		µW

(1) Specified in µA/V because current can flow either into or out of the input pin.
(2) Currents measured with SPI idle.

6.6 Timing Requirements

over operating ambient temperature range, DOUT load: 20 pF || 100 kΩ (unless otherwise noted)

		MIN	MAX	UNIT
1.65 V ≤ DVDD ≤ 2.0 V				
$t_{w(CLH)}$	Pulse duration, CLKIN high	49		ns
$t_{w(CLL)}$	Pulse duration, CLKIN low	49		ns
$t_{c(SC)}$	SCLK period	64		ns
$t_{w(SCL)}$	Pulse duration, SCLK low	32		ns
$t_{w(SCH)}$	Pulse duration, SCLK high	32		ns
$t_{d(CSSC)}$	Delay time, first SCLK rising edge after $\overline{CS}$ falling edge	16		ns
$t_{d(SCCS)}$	Delay time, $\overline{CS}$ rising edge after final SCLK falling edge	10		ns
$t_{w(CSH)}$	Pulse duration, $\overline{CS}$ high	20		ns
$t_{su(DI)}$	Setup time, DIN valid before SCLK falling egde	5		ns
$t_{h(DI)}$	Hold time, DIN valid after SCLK falling edge	8		ns
$t_{w(RSL)}$	Pulse duration, $\overline{SYNC}/\overline{RESET}$ low to generate device reset	2048		t_{CLKIN}
$t_{w(SYL)}$	Pulse duration, $\overline{SYNC}/\overline{RESET}$ low for synchronization	1	2047	t_{CLKIN}
$t_{su(SY)}$	Setup time, $\overline{SYNC}/\overline{RESET}$ valid before CLKIN rising edge	10		ns
2.7 V ≤ DVDD ≤ 3.6 V				
$t_{w(CLL)}$	Pulse duration, CLKIN low	49		ns
$t_{w(CLH)}$	Pulse duration, CLKIN high	49		ns
$t_{c(SC)}$	SCLK period	40		ns
$t_{w(SCL)}$	Pulse duration, SCLK low	20		ns
$t_{w(SCH)}$	Pulse duration, SCLK high	20		ns
$t_{d(CSSC)}$	Delay time, first SCLK rising edge after $\overline{CS}$ falling edge	16		ns
$t_{d(SCCS)}$	Delay time, $\overline{CS}$ rising edge after final SCLK falling edge	10		ns
$t_{w(CSH)}$	Pulse duration, $\overline{CS}$ high	15		ns
$t_{su(DI)}$	Setup time, DIN valid before SCLK falling egde	5		ns
$t_{h(DI)}$	Hold time, DIN valid after SCLK falling edge	8		ns
$t_{w(RSL)}$	Pulse duration, $\overline{SYNC}/\overline{RESET}$ low to generate device reset	2048		t_{CLKIN}
$t_{w(SYL)}$	Pulse duration, $\overline{SYNC}/\overline{RESET}$ low for synchronization	1	2047	t_{CLKIN}
$t_{su(SY)}$	Setup time, $\overline{SYNC}/\overline{RESET}$ valid before CLKIN rising edge	10		ns

6.7 Switching Characteristics

over operating ambient temperature range, DOUT load: 20 pF || 100 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
1.65 V ≤ DVDD ≤ 2.0 V						
$t_{p(CSDO)}$	Propagation delay time, $\overline{CS}$ falling edge to DOUT driven				50	ns
$t_{p(SCDO)}$	Progapation delay time, SCLK rising edge to valid new DOUT				32	ns
$t_{p(CSDOZ)}$	Propagation delay time, $\overline{CS}$ rising edge to DOUT high impedance				75	ns
$t_{w(DRH)}$	Pulse duration, $\overline{DRDY}$ high			4		t_{CLKIN}
$t_{w(DRL)}$	Pulse duration, $\overline{DRDY}$ low			4		t_{CLKIN}
	SPI timeout		32768			t_{CLKIN}
t_{POR}	Power-on-reset time	Measured from supplies at 90% to first $\overline{DRDY}$ rising edge		250		µs
t_{REGACQ}	Register default acquisition time			5		µs

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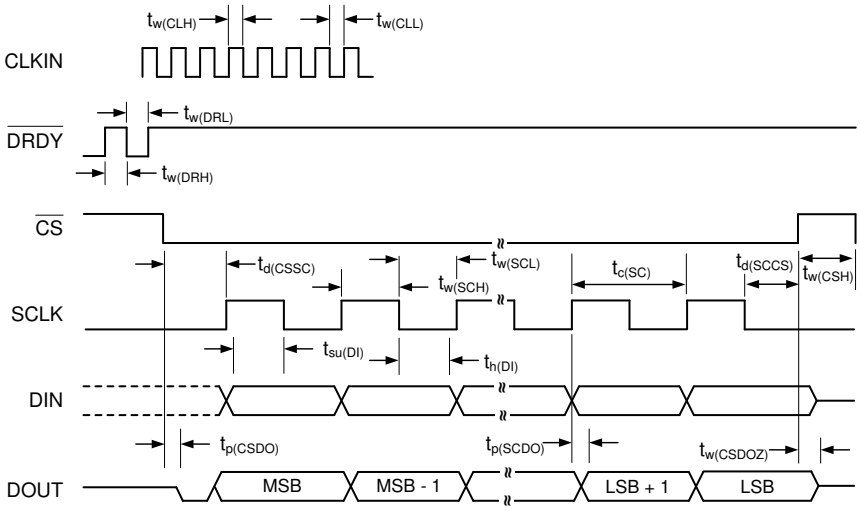
6.7 Switching Characteristics (continued)

over operating ambient temperature range, DOUT load: 20 pF || 100 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
2.7 V ≤ DVDD ≤ 3.6 V						
$t_{p(CSDO)}$	Propagation delay time, $\overline{CS}$ falling edge to DOUT driven				50	ns
$t_{p(SCDO)}$	Progapation delay time, SCLK rising edge to valid new DOUT				20	ns
$t_{p(CSDOZ)}$	Propagation delay time, $\overline{CS}$ rising edge to DOUT high impedance				75	ns
$t_{w(DRH)}$	Pulse duration, $\overline{DRDY}$ high			4		t_{CLKIN}
$t_{w(DRL)}$	Pulse duration, $\overline{DRDY}$ low			4		t_{CLKIN}
	SPI timeout		32768			t_{CLKIN}
t_{POR}	Power-on-reset time	Measured from supplies at 90% to first $\overline{DRDY}$ rising edge		250		µs
t_{REGACQ}	Register default acquisition time			5		µs

6.8 Timing Diagrams



NOTE: SPI settings are CPOL = 0 and CPHA = 1. $\overline{CS}$ transitions must take place when SCLK is low.

Figure 6-1. SPI Timing Diagram

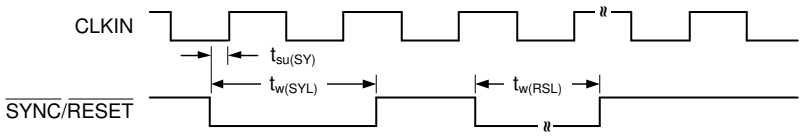


Figure 6-2. $\overline{SYNC}$/$\overline{RESET}$ Timing Requirements

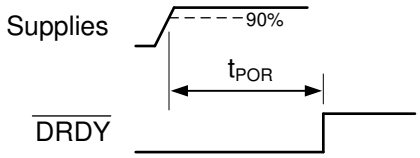


Figure 6-3. Power-On-Reset Timing

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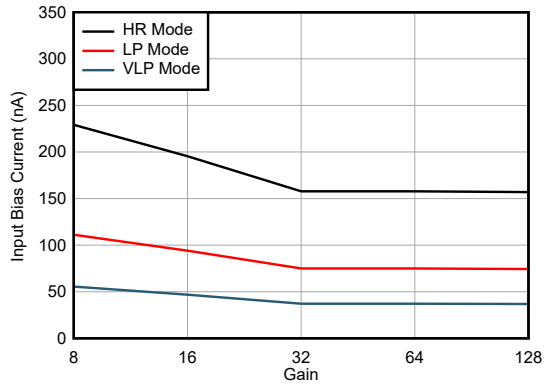
6.9 Typical Characteristics

at T_A = 25°C, AVDD = 3 V, DVDD = 3 V, f_{CLKIN} = 8.192 MHz, data rate = 4 kSPS, and gain = 1 with global-chop mode disabled (unless otherwise noted)



Gains of 8, 16, 32, 64, and 128 only

Figure 6-4. Input Bias Current vs Gain

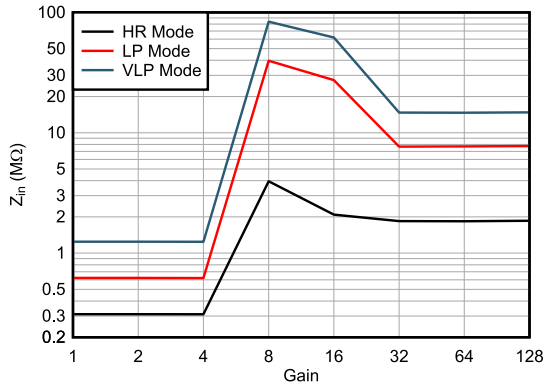


Figure 6-5. Input Impedance vs Gain

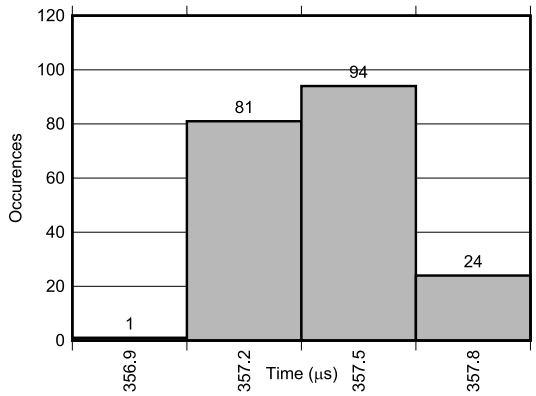
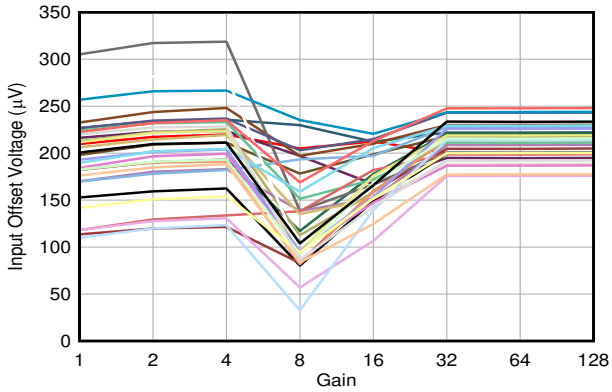


Figure 6-6. Start-Up Time Histogram



30 units, channel 1

Figure 6-7. Input Offset Voltage vs Gain

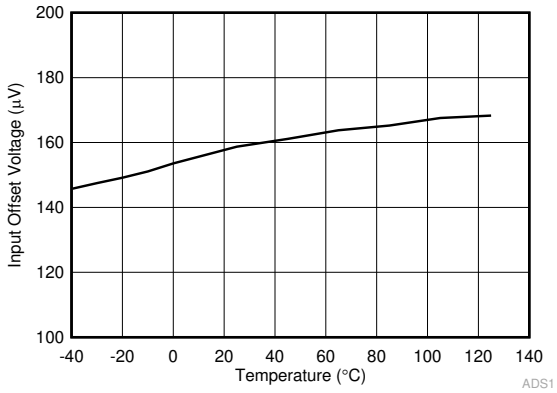
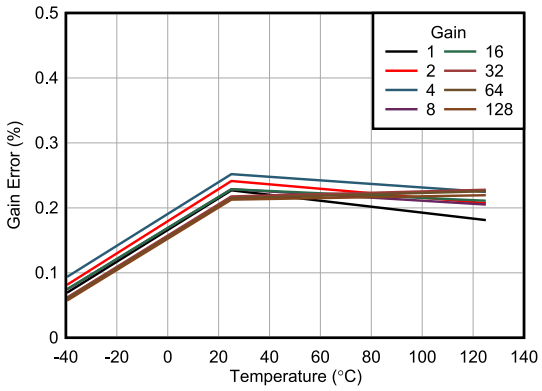


Figure 6-8. Input Offset Voltage vs Temperature

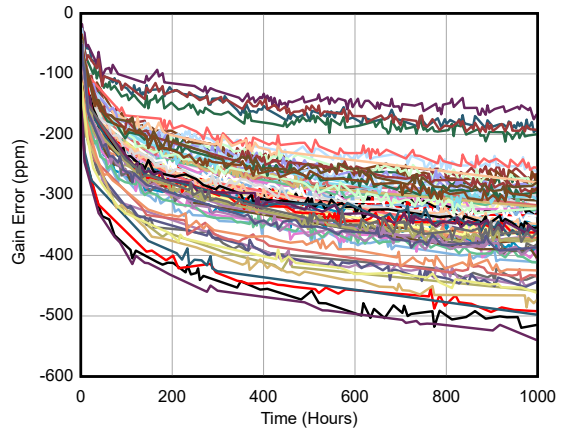


Includes internal reference error

Figure 6-9. Gain Error vs Temperature

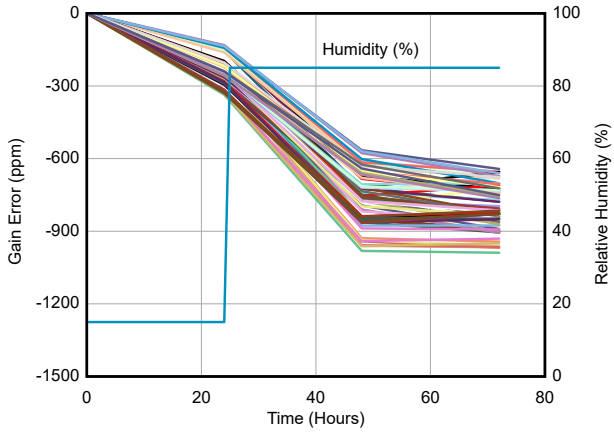
6.9 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3 V, DVDD = 3 V, f_{CLKIN} = 8.192 MHz, data rate = 4 kSPS, and gain = 1 with global-chop mode disabled (unless otherwise noted)



18 units, all channels

Figure 6-10. Gain Error vs Time



18 units, all channels

Figure 6-11. Gain Error vs Time Across Humidity

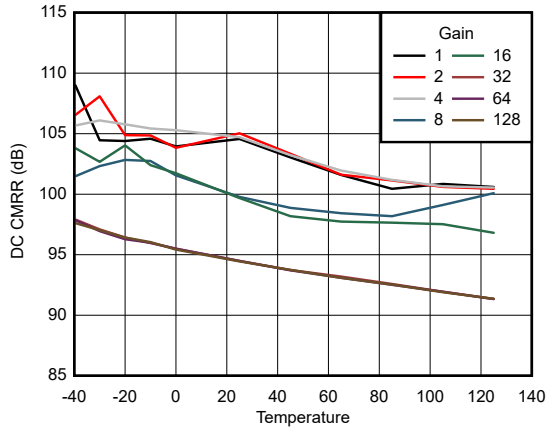


Figure 6-12. DC CMRR vs Temperature

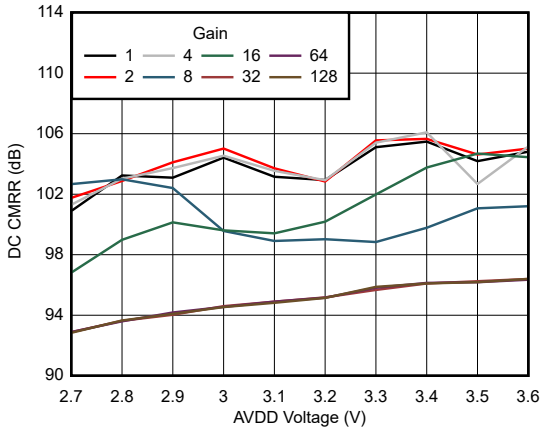


Figure 6-13. DC CMRR vs AVDD Voltage

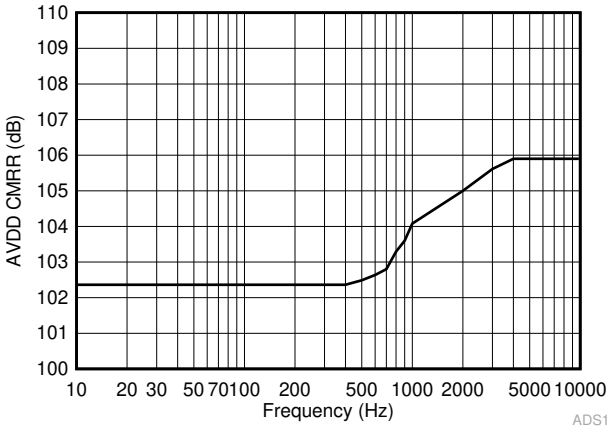


Figure 6-14. AVDD CMRR vs Frequency

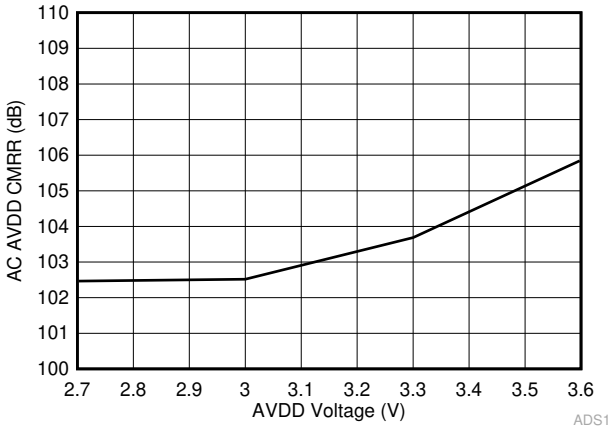


Figure 6-15. AC CMRR vs AVDD Voltage

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6.9 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3 V, DVDD = 3 V, f_{CLKIN} = 8.192 MHz, data rate = 4 kSPS, and gain = 1 with global-chop mode disabled (unless otherwise noted)

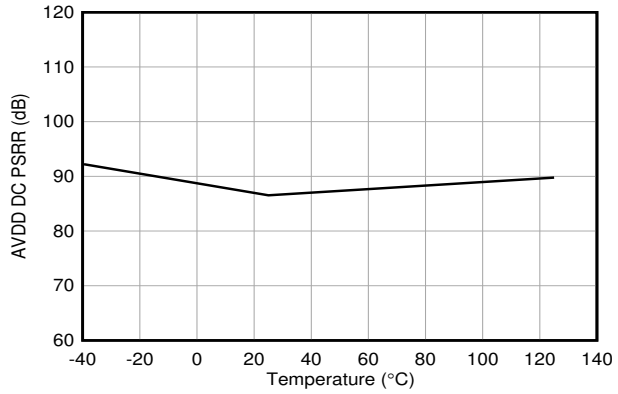

Figure 6-16. DC AVDD PSRR vs Temperature

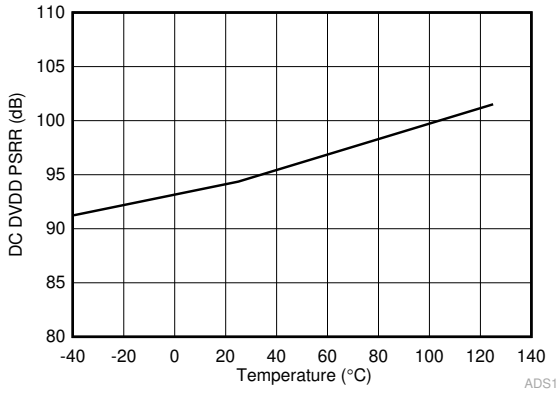

Figure 6-17. DC DVDD PSRR vs Temperature

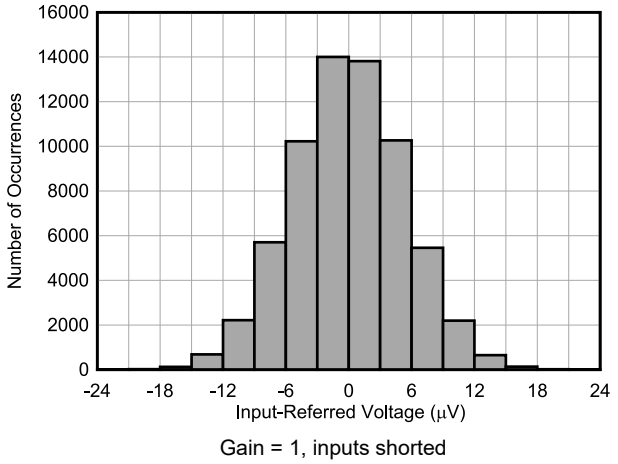

Figure 6-18. Single Device Noise Histogram at 4 kSPS

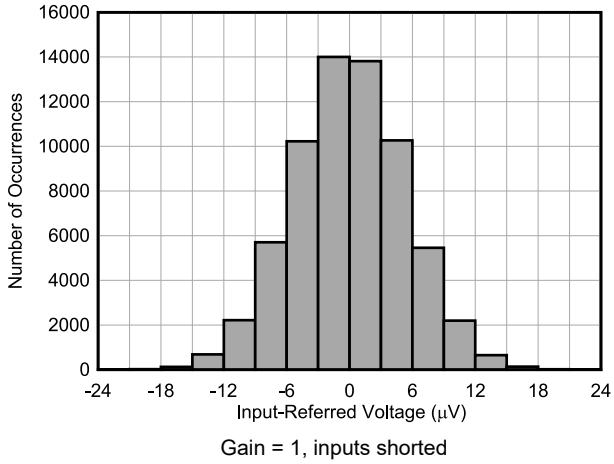

Figure 6-19. Single Device Noise Histogram at 32 kSPS

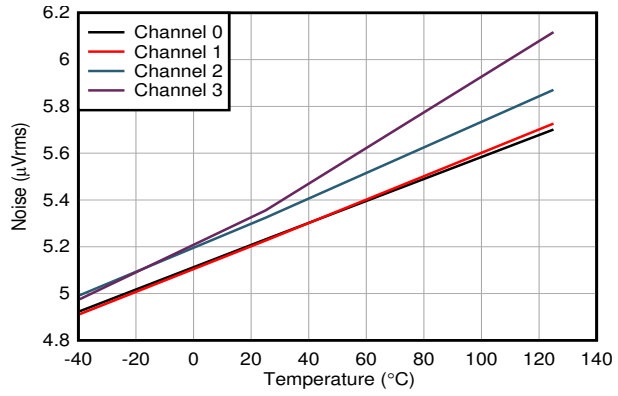

Figure 6-20. Noise vs Temperature

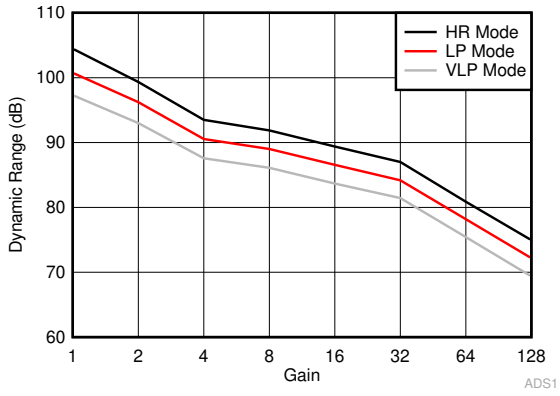

Figure 6-21. Dynamic Range at 4 kSPS vs Gain

6.9 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3 V, DVDD = 3 V, f_{CLKIN} = 8.192 MHz, data rate = 4 kSPS, and gain = 1 with global-chop mode disabled (unless otherwise noted)

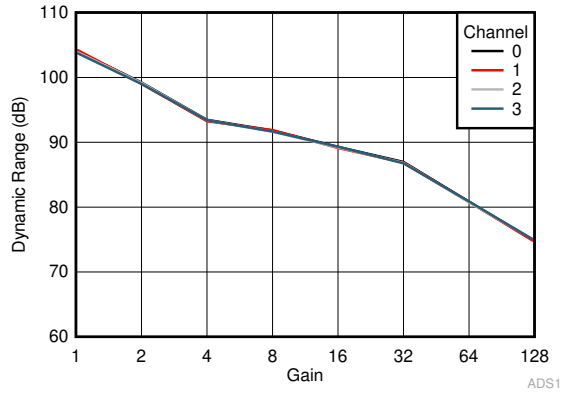

Figure 6-22. Dynamic Range vs Gain

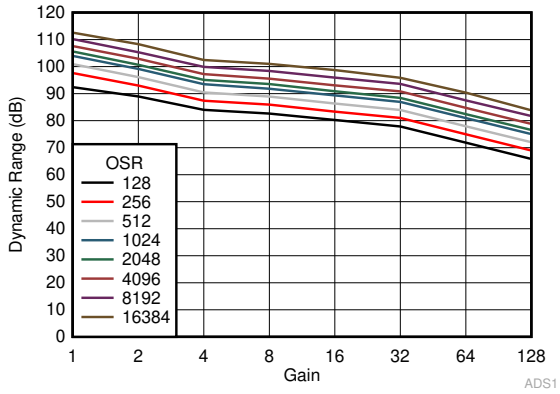

Figure 6-23. Dynamic Range vs Gain

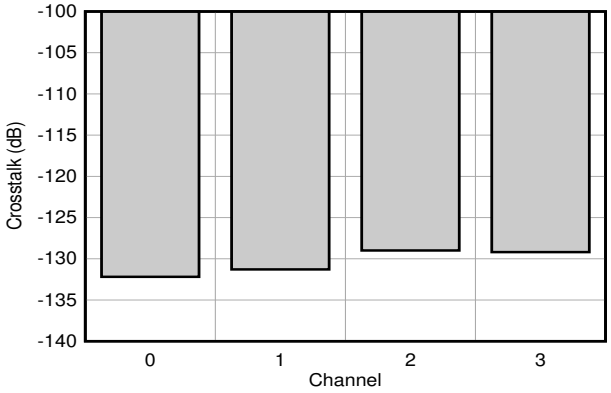

Figure 6-24. Crosstalk vs Channel

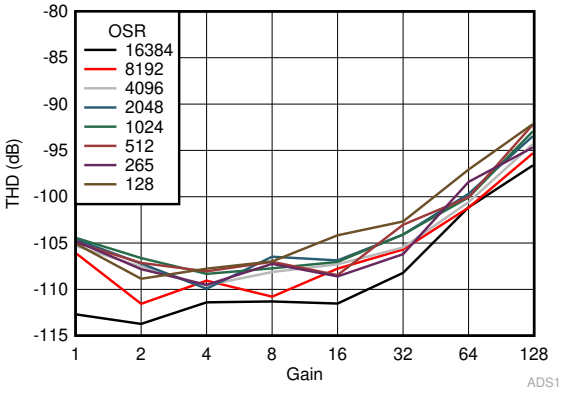

Figure 6-25. THD vs Gain

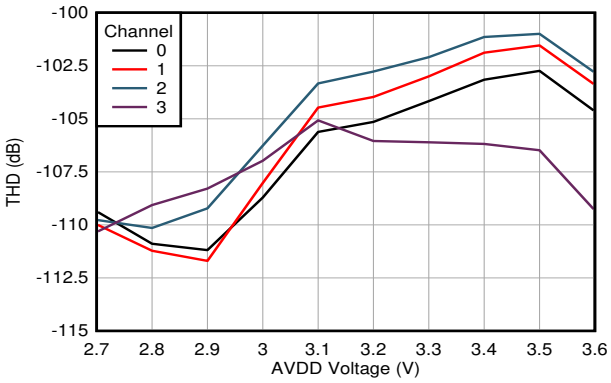

Figure 6-26. THD vs AVDD Voltage

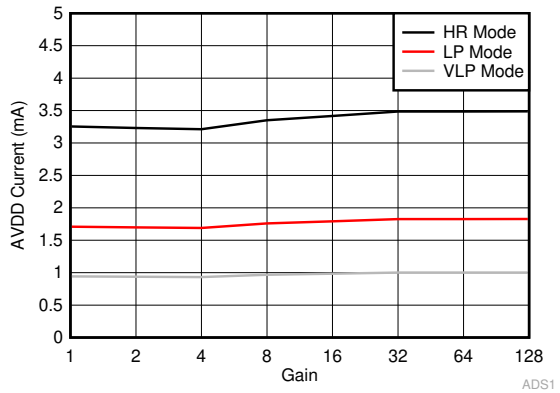

Figure 6-27. AVDD Current vs Gain

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6.9 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3 V, DVDD = 3 V, f_{CLKIN} = 8.192 MHz, data rate = 4 kSPS, and gain = 1 with global-chop mode disabled (unless otherwise noted)

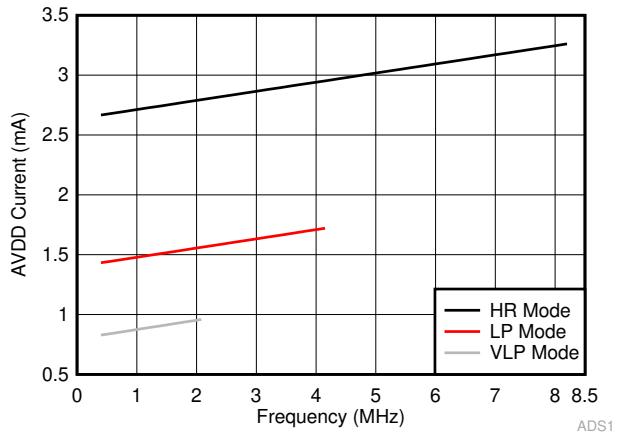

Figure 6-28. AVDD Current vs CLKIN Frequency

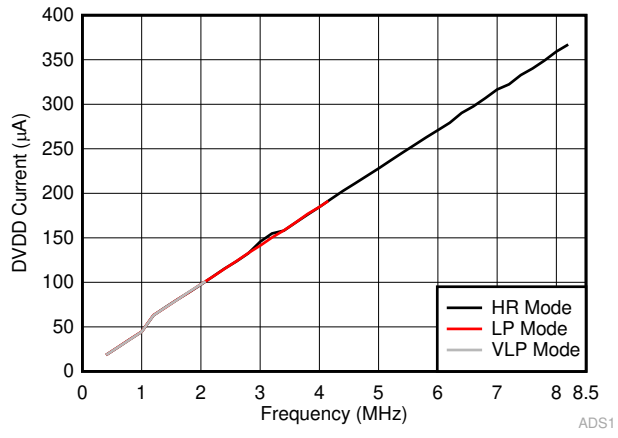

Figure 6-29. DVDD Current vs CLKIN Frequency

7 Parameter Measurement Information

7.1 Noise Measurements

Adjust the data rate and gain to optimize the ADS131M04-Q1 noise performance. When averaging is increased by reducing the data rate, noise drops correspondingly. Table 7-1 summarizes the ADS131M04-Q1 noise performance using the 1.2-V internal reference and a 3.0-V analog power supply. The data are representative of typical noise performance at T_A = 25°C when f_{CLKIN} = 8.192 MHz. The modulator clock frequency f_{MOD} is equal to f_{CLKIN} / 2. The data shown are typical input-referred noise results with the analog inputs shorted together and taking an average of multiple readings across all channels. A minimum 1 second of consecutive readings are used to calculate the RMS. Table 7-2 shows the dynamic range and effective resolution calculated from the noise data. Equation 1 calculates dynamic range. Equation 2 calculates effective resolution. In each case, V_{REF} corresponds to the internal 1.2-V reference. In global-chop mode, noise is improved by a factor of $\sqrt{2}$.

The noise performance scales with the OSR and gain settings, but is independent from the configured power mode. Thus, the device exhibits the same noise performance in different power modes when selecting the same OSR and gain settings. However, the data rate at the OSR settings scales based on the applied clock frequency for the different power modes.

$$\text{Dynamic Range} = 20 \times \log\left(\frac{V_{REF}}{\sqrt{2} \times \text{Gain} \times V_{RMS}}\right) \tag{1}$$

$$\text{Effective Resolution} = \log_2\left(\frac{2 \times V_{REF}}{\text{Gain} \times V_{RMS}}\right) \tag{2}$$

Table 7-1. Noise (μV_{RMS}) at T_A = 25°C

OSR	DATA RATE (kSPS), f_{CLKIN} = 8.192 MHz	GAIN							
		1	2	4	8	16	32	64	128
16384	0.25	1.90	1.69	1.56	0.95	0.64	0.42	0.42	0.42
8192	0.5	2.39	2.13	2.13	1.29	0.86	0.57	0.57	0.57
4096	1	3.38	2.99	2.88	1.74	1.17	0.77	0.77	0.77
2048	2	4.25	3.91	3.79	2.27	1.52	1.00	1.00	1.00
1024	4	5.35	4.68	4.52	2.70	1.82	1.20	1.20	1.20
512	8	7.56	6.62	6.37	3.82	2.55	1.69	1.69	1.69
256	16	10.68	9.56	9.09	5.42	3.63	2.39	2.39	2.40
128	32	21.31	15.26	13.52	7.89	5.21	3.41	3.42	3.42
64	64	75.34	41.63	26.84	14.59	8.9	5.57	5.58	5.58

Table 7-2. Dynamic Range (Effective Resolution) at T_A = 25°C

OSR	DATA RATE (kSPS), f_{CLKIN} = 8.192 MHz	GAIN							
		1	2	4	8	16	32	64	128
16384	0.25	113 (20.3)	108 (19.4)	103 (18.6)	101 (18.3)	98 (17.8)	96 (17.5)	90 (16.5)	84 (15.4)
8192	0.5	111 (19.9)	106 (19.1)	100 (18.1)	98 (17.8)	96 (17.4)	93 (17.0)	87 (16.0)	81 (15.0)
4096	1	108 (19.4)	103 (18.6)	97 (17.7)	96 (17.4)	93 (17.0)	91 (16.6)	85 (15.6)	79 (14.6)
2048	2	106 (19.1)	101 (18.2)	95 (17.3)	93 (17.0)	91 (16.6)	88 (16.2)	82 (15.2)	76 (14.2)
1024	4	104 (18.8)	99 (18.0)	93 (17.0)	92 (16.8)	89 (16.3)	87 (15.9)	81 (14.9)	75 (13.9)
512	8	101 (18.3)	96 (17.5)	90 (16.5)	89 (16.3)	86 (15.8)	84 (15.4)	78 (14.4)	72 (13.4)
256	16	98 (17.8)	93 (16.9)	87 (16.0)	86 (15.8)	83 (15.3)	81 (14.9)	75 (13.9)	69 (12.9)
128	32	92 (16.8)	89 (16.3)	84 (15.4)	83 (15.2)	80 (14.8)	78 (14.4)	72 (13.4)	65 (12.4)
64	64	81 (15.0)	80 (14.8)	78 (14.4)	77 (14.3)	75 (14.0)	74 (13.7)	68 (12.7)	62 (11.7)

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8 Detailed Description

8.1 Overview

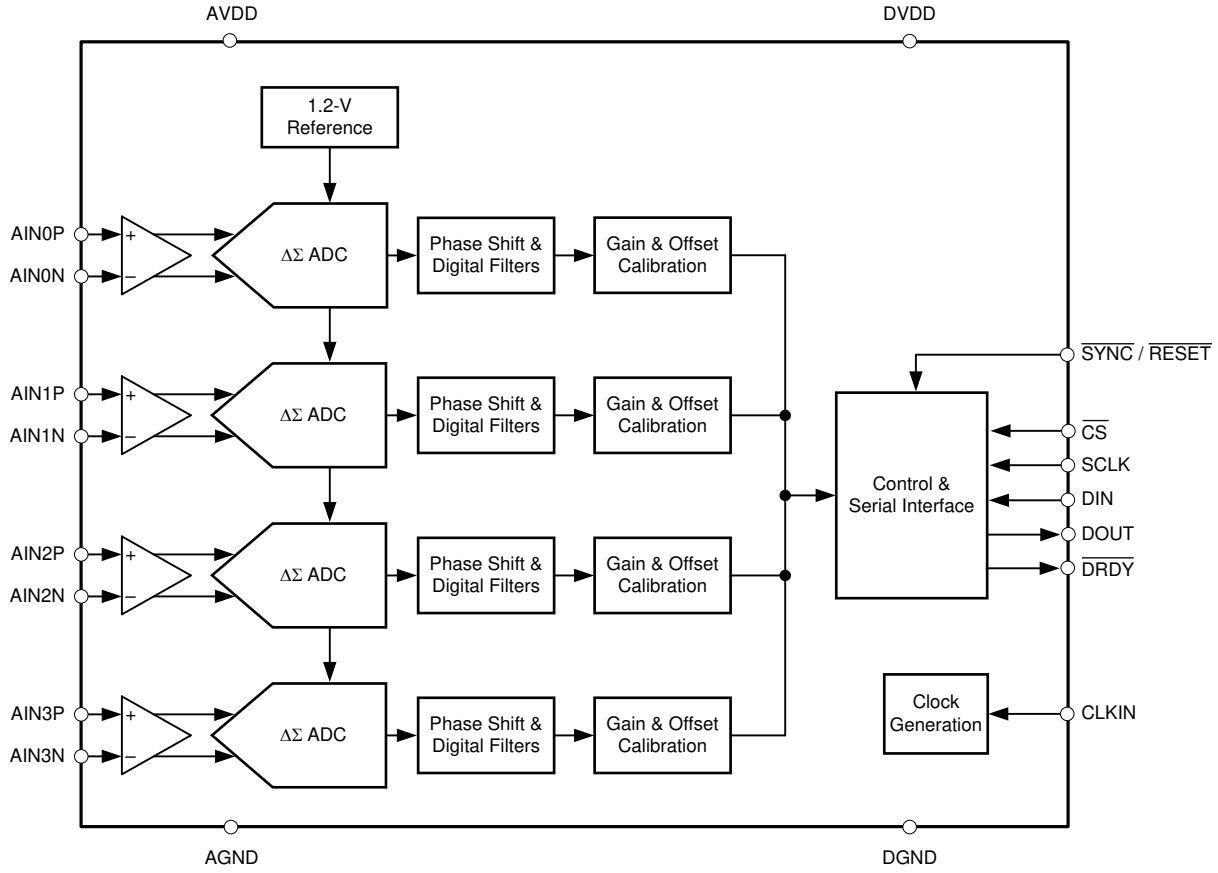
The ADS131M04-Q1 is a low-power, four-channel, simultaneous-sampling, 24-bit, delta-sigma (ΔΣ) analog-to-digital converter (ADC) with a low-drift internal reference voltage. The dynamic range, size, feature set, and power consumption are optimized for cost-sensitive applications requiring simultaneous-sampling.

The ADS131M04-Q1 requires both analog and digital supplies. The analog power supply (AVDD – AGND) can operate between 2.7 V and 3.6 V. An integrated negative charge pump allows absolute input voltages as low as 1.3 V below AGND, which enables measurements of input signals varying around ground with a single-ended power supply. The digital power supply (DVDD – DGND) accepts both 1.8-V and 3.3-V supplies. The device features a programmable gain amplifier (PGA) with gains up to 128. An integrated input precharge buffer enabled at gains greater than 4 ensures high input impedance at high PGA gain settings. The ADC receives the reference voltage from an integrated 1.2-V reference. The device allows differential input voltages as large as the reference. Three power-scaling modes allow designers to trade power consumption for ADC dynamic range.

Each channel on the ADS131M04-Q1 contains a digital decimation filter that demodulates the output of the ΔΣ modulators. The filter enables data rates as high as 32 kSPS per channel in high-resolution mode. The relative phase of the samples can be configured between channels, thus enabling an accurate compensation for the sensor phase response. Offset and gain calibration registers can be programmed to automatically adjust output samples for measured offset and gain errors. The *Functional Block Diagram* provides a detailed diagram of the ADS131M04-Q1.

The device communicates via a serial programming interface (SPI)-compatible interface. Several SPI commands and internal registers control the operation of the ADS131M04-Q1. Other devices can be added to the same SPI bus by adding discrete $\overline{CS}$ control lines. The $\overline{SYNC}$/$\overline{RESET}$ pin can be used to synchronize conversions between multiple ADS131M04-Q1 devices as well as to maintain synchronization with external events.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input ESD Protection Circuitry

Basic electrostatic discharge (ESD) circuitry protects the ADS131M04-Q1 inputs from ESD and overvoltage events in conjunction with external circuits and assemblies. Figure 8-1 depicts a simplified representation of the ESD circuit. The protection for input voltages exceeding AVDD can be modeled as a simple diode.

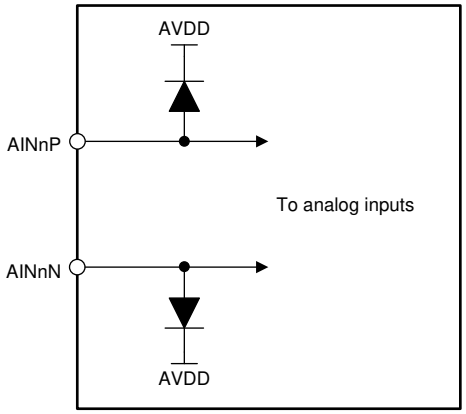


Figure 8-1. Input ESD Protection Circuitry

The ADS131M04-Q1 has an integrated negative charge pump that allows for input voltages below AGND with a unipolar supply. Consequently, shunt diodes between the inputs and AGND cannot be used to clamp excessive negative input voltages. Instead, the same diode that clamps overvoltage is used to clamp undervoltage at the reverse breakdown voltage. Take care to prevent input voltages or currents from exceeding the limits provided in the *Absolute Maximum Ratings* table.

8.3.2 Input Multiplexer

Each channel of the ADS131M04-Q1 has a dedicated input multiplexer. The multiplexer controls which signals are routed to the ADC channels. Configure the input multiplexer using the MUXn[1:0] bits in the CHn_CFG register. The input multiplexer allows the following inputs to be connected to the ADC channel:

- The analog input pins corresponding to the given channel
- AGND, which is helpful for offset calibration
- Positive DC test signal
- Negative DC test signal

See the *Internal Test Signals* section for more information about the test signals. Figure 8-2 shows a diagram of the input multiplexer on the ADS131M04-Q1.

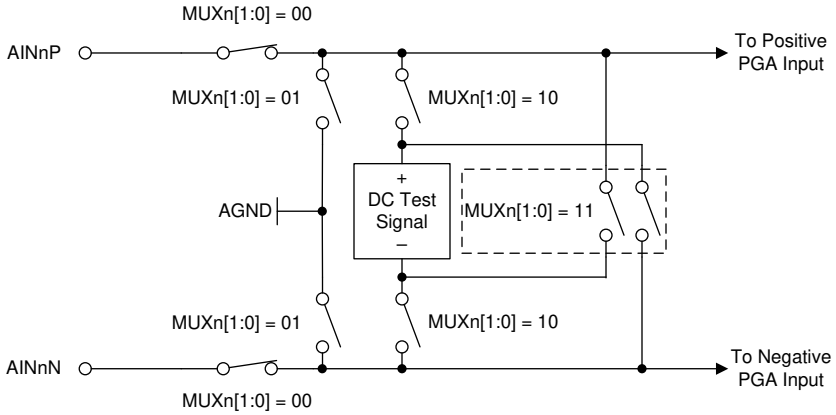


Figure 8-2. Input Multiplexer

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8.3.3 Programmable Gain Amplifier (PGA)

Each channel of the ADS131M04-Q1 features an integrated programmable gain amplifier (PGA) that provides gains of 1, 2, 4, 8, 16, 32, 64, and 128. The gains for all channels are individually controlled by the PGAGAINn bits for each channel in the GAIN1 register.

Varying the PGA gain scales the differential full-scale input voltage range (FSR) of the ADC. Equation 3 describes the relationship between FSR and gain. Equation 3 uses the internal reference voltage, 1.2 V, as the scaling factor without accounting for gain error caused by tolerance in the reference voltage.

$$FSR = \pm 1.2\ V / Gain \quad (3)$$

Table 8-1 shows the corresponding full-scale ranges for each gain setting.

Table 8-1. Full-Scale Range

GAIN SETTING	FSR
1	±1.2 V
2	±600 mV
4	±300 mV
8	±150 mV
16	±75 mV
32	±37.5 mV
64	±18.75 mV
128	±9.375 mV

The input impedance of the PGA dominates the input impedance characteristics of the ADS131M04-Q1. The PGA input impedance for gain settings up to 4 behaves according to Equation 4 without accounting for device tolerance and change over temperature. Minimize the output impedance of the circuit that drives the ADS131M04-Q1 inputs to obtain the best possible gain error, INL, and distortion performance.

$$330\ k\Omega \times 4.096\ MHz / f_{MOD} \quad (4)$$

where:

- f_{MOD} is the ΔΣ modulator frequency, f_{CLKIN} / 2

The device uses an input precharge buffer for PGA gain settings of 8 and higher. The input impedance at these gain settings is very high. Specifying the input bias current for these gain settings is therefore more useful. A plot of input bias current for the high gain settings is provided in Figure 6-5.

8.3.4 Voltage Reference

The ADS131M04-Q1 uses an internally generated, low-drift, band-gap voltage to supply the reference for the ADC. The reference has a nominal voltage of 1.2 V, allowing the differential input voltage to swing from –1.2 V to 1.2 V. The reference circuitry starts up very quickly to accommodate the fast start-up feature of this device. The device waits until after the reference circuitry is fully settled before generating conversion data.

8.3.5 Clocking and Power Modes

An LVCMOS clock must be provided at the CLKIN pin continuously when the ADS131M04-Q1 is running in normal operation. The frequency of the clock can be scaled in conjunction with the power mode to provide a tradeoff between power consumption and dynamic range.

The PWR[1:0] bits in the CLOCK register allow the device to be configured in one of three power modes: high-resolution (HR) mode, low-power (LP) mode, and very low-power (VLP) mode. Changing the PWR[1:0] bits scales the internal bias currents to achieve the expected power levels. The external clock frequency must follow the guidance provided in the *Recommended Operating Conditions* table corresponding to the intended power mode in order for the device to perform according to the specification.

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8.3.6 ΔΣ Modulator

The ADS131M04-Q1 uses a delta-sigma (ΔΣ) modulator to convert the analog input voltage to a one's density modulated digital bit-stream. The ΔΣ modulator oversamples the input voltage at a frequency many times greater than the output data rate. The modulator frequency, f_{MOD}, of the ADS131M04-Q1 is equal to half the controller clock frequency, that is, $f_{MOD} = f_{CLKIN} / 2$.

The output of the modulator is fed back to the modulator input through a digital-to-analog converter (DAC) as a means of error correction. This feedback mechanism shapes the modulator quantization noise in the frequency domain to make the noise more dense at higher frequencies and less dense in the band of interest. The digital decimation filter following the ΔΣ modulator significantly attenuates the out-of-band modulator quantization noise, allowing the device to provide excellent dynamic range.

8.3.7 Digital Filter

The ΔΣ modulator bitstream feeds into a digital filter. The digital filter is a linear phase, finite impulse response (FIR), low-pass sinc-type filter that attenuates the out-of-band quantization noise of the ΔΣ modulator. The digital filter demodulates the output of the ΔΣ modulator by averaging. The data passing through the filter is decimated and downsampled, to reduce the rate at which data come out of the modulator (f_{MOD}) to the output data rate (f_{DATA}). The decimation factor is defined as per Equation 5 and is called the *oversampling ratio (OSR)*.

$$OSR = f_{MOD} / f_{DATA} \tag{5}$$

The OSR is configurable and set by the OSR[2:0] bits in the CLOCK register. There are eight OSR settings in the ADS131M04-Q1, allowing eight different data rate settings for any given controller clock frequency. Table 8-2 lists the OSR settings and their corresponding output data rates for the nominal CLKIN frequencies mentioned.

The OSR determines the amount of averaging of the modulator output in the digital filter and therefore also the filter bandwidth. The filter bandwidth directly affects the noise performance of the ADC because lower bandwidth results in lower noise whereas higher bandwidth results in higher noise. See Table 7-1 for the noise specifications for various OSR settings.

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Table 8-2. OSR Settings and Data Rates for Nominal Controller Clock Frequencies

POWER MODE	NOMINAL CONTROLLER CLOCK FREQUENCY	f_{MOD}	OSR	OUTPUT DATA RATE
HR	8.192 MHz	4.096 MHz	64	64 kSPS
			128	32 kSPS
			256	16 kSPS
			512	8 kSPS
			1024	4 kSPS
			2048	2 kSPS
			4096	1 kSPS
			8192	500 SPS
			16384	250 SPS
LP	4.096 MHz	2.048 MHz	64	32 kSPS
			128	16 kSPS
			256	8 kSPS
			512	4 kSPS
			1024	2 kSPS
			2048	1 kSPS
			4096	500 SPS
			8192	250 SPS
			16384	125 SPS
VLP	2.048 MHz	1.024 MHz	64	16 kSPS
			128	8 kSPS
			256	4 kSPS
			512	2 kSPS
			1024	1 kSPS
			2048	500 SPS
			4096	250 SPS
			8192	125 SPS
			16384	62.5 SPS

8.3.7.1 Digital Filter Implementation

Figure 8-3 shows the digital filter implementation of the ADS131M04-Q1. The modulator bit-stream feeds two parallel filter paths, a sinc^3 filter, and a fast-settling filter path.

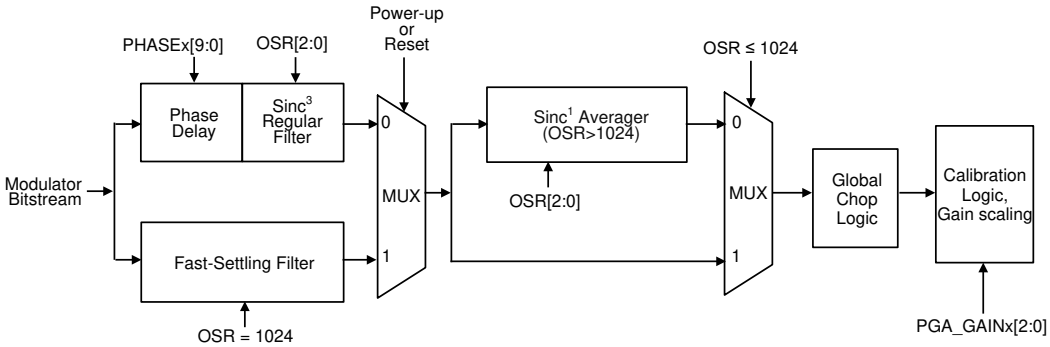

Figure 8-3. Digital Filter Implementation

8.3.7.1.1 Fast-Settling Filter

At power-up or after a device reset, the ADS131M04-Q1 selects the fast-settling filter to allow for settled output data generation with minimal latency. The fast-settling filter has the characteristic of a first-order sinc filter ($sinc^1$). After two conversions, the device switches to and remains in the $sinc^3$ filter path until the next time the device is reset or powered cycled.

The fast-settling filter exhibits wider bandwidth and less stop-band attenuation than the $sinc^3$ filter. Consequently, the noise performance when using the fast-settling filter is not as high as with the $sinc^3$ filter. The first two samples available from the ADS131M04-Q1 after a supply ramp or reset have the noise performance and frequency response corresponding to the fast-settling filter as specified in the *Electrical Characteristics* table in the *Specifications* section, whereas subsequent samples have the noise performance and frequency response consistent with the $sinc^3$ filter. See the *Fast Start-Up Behavior* section for more details regarding the fast start-up capabilities of the ADS131M04-Q1.

8.3.7.1.2 SINC^3 and SINC^3 + SINC^1 Filter

The ADS131M04-Q1 selects the $sinc^3$ filter path two conversion after power-up or device reset. For OSR settings of 64 to 1024 the $sinc^3$ filter output directly feeds into the global-chop and calibration logic. For OSR settings of 2048 and higher the $sinc^3$ filter is followed by a $sinc^1$ filter. As shown in Table 8-3, the $sinc^3$ filter operates at a fixed OSR of 1024 in this case while the $sinc^1$ filter implements the additional OSRs of 2 to 16. That means when an OSR of 4096 (for example) is selected, the $sinc^3$ filter operates at an OSR of 1024 and the $sinc^1$ filter at an OSR of 4.

The filter has infinite attenuation at integer multiples of the data rate except for integer multiples of f_{MOD}. Like all digital filters, the digital filter response of the ADS131M04-Q1 repeats at integer multiples of the modulator frequency, f_{MOD}. The data rate and filter notch frequencies scale with f_{MOD}.

When possible, plan frequencies for unrelated periodic processes in the application for integer multiples of the data rate such that any parasitic effect they have on data acquisition is effectively canceled by the notches of the digital filter. Avoid frequencies near integer multiples of f_{MOD} whenever possible because tones in these bands can alias to the band of interest.

The $sinc^3$ and $sinc^3$ + $sinc^1$ filters for a given channel require time to settle after a channel is enabled, the channel multiplexer or gain setting is changed, or a resynchronization event occurs. See the *Synchronization* section for more details on resynchronization. Table 8-3 lists the settling times of the $sinc^3$ and $sinc^3$ + $sinc^1$ filters for each OSR setting. The ADS131M04-Q1 does not gate unsettled data. Therefore, the host must account for the filter settling time and disregard unsettled data if any are read. The data at the next $\overline{DRDY}$ falling edge after the filter settling time listed in Table 8-3 has expired can be considered fully settled.

Table 8-3. Digital Filter Start-Up Times After Power-Up or Resynchronization

OSR (OVERALL)	OSR (SINC^3)	OSR (SINC^1)	SETTLING TIME (t_{CLKIN})
64	64	N/A	728
128	128	N/A	856
256	256	N/A	1112
512	512	N/A	1624
1024	1024	N/A	2648
2048	1024	2	4696
4096	1024	4	8792
8192	1024	8	16984
16384	1024	16	33368

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8.3.7.2 Digital Filter Characteristic

Equation 6 calculates the z-domain transfer function of a sinc^3 filter that is used for OSRs of 1024 and lower.

$$\left|H(z)\right| = \left|\frac{1 - Z^{-N}}{N\left(1 - Z^{-1}\right)}\right|^3 \tag{6}$$

where N is the OSR.

Equation 7 calculates the transfer function of a sinc^3 filter in terms of the continuous-time frequency parameter *f*.

$$H(f)\,\Big| = \left|\frac{\sin\left(\frac{N\pi f}{f_{MOD}}\right)}{N \times \sin\left(\frac{\pi f}{f_{MOD}}\right)}\right|^3 \tag{7}$$

where N is the OSR.

Figure 8-4 and Figure 8-5 show the digital filter response of the fast-settling filter and the sinc^3 filter for OSRs of 1024 and lower. Figure 8-6 and Figure 8-7 show the digital filter response of the sinc^3 + sinc^1 filter for an OSR of 4096.

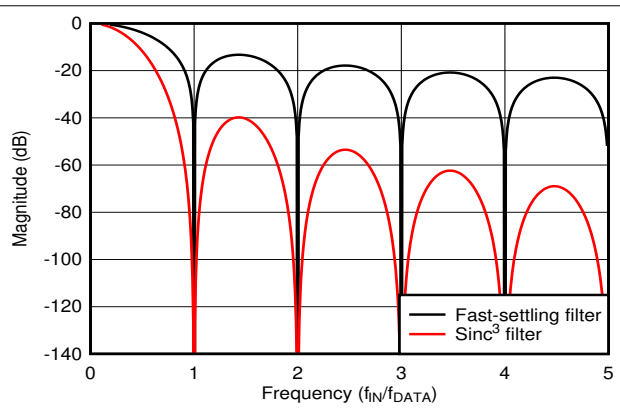

Figure 8-4. Fast-Settling and Sinc^3 Digital Filter Response

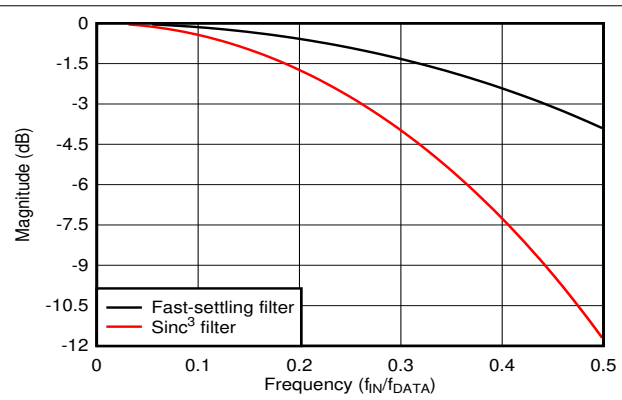

Figure 8-5. Fast-Settling and Sinc^3 Digital Filter Response, Pass-Band Detail

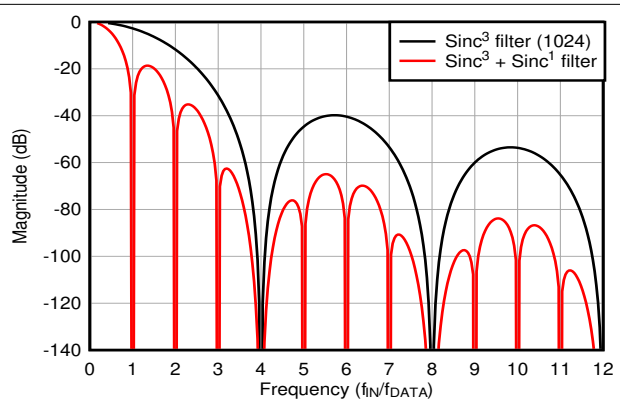

Figure 8-6. Digital Filter Response for OSR = 1024 and OSR = 4096

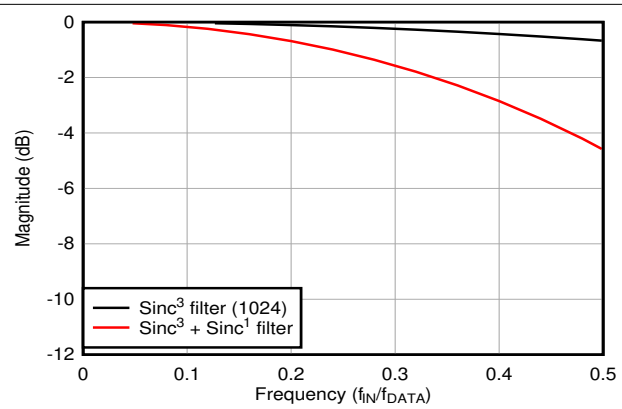

Figure 8-7. Digital Filter Response for OSR = 1024 and OSR = 4096, Pass-Band Detail

8.3.8 DC Block Filter

The ADS131M04-Q1 includes an optional high-pass filter to eliminate any systematic offset or low-frequency noise. The filter is enabled by writing any value in the DCBLOCK[3:0] bits in the CD_TH_LSB register besides 0h. The DC block filter can be enabled and disabled on a channel-by-channel basis by the DCBLKn_DIS bit in the CHn_CFG register for each respective channel.

Figure 8-8 shows the topology of the DC block filter. Coefficient *a* represents a register configurable value that configures the cutoff frequency of the filter. The cutoff frequency is configured using the DCBLOCK[3:0] bits in the CD_TH_LSB register. Table 8-4 describes the characteristics of the filter for various DCBLOCK[3:0] settings. The data provided in Table 8-4 is provided for an 8.192-MHz CLKIN frequency and a 4-kSPS data rate. The frequency response of the filter response scales directly with the frequency of CLKIN and the data rate.

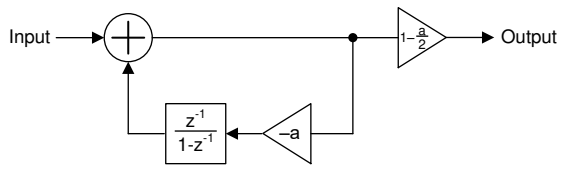

Figure 8-8. DC Block Filter Topology

Table 8-4. DC Block Filter Characteristics

DCBLOCK[3:0]	*a* COEFFICIENT	–3-dB CORNER(1)	PASS-BAND ATTENUATION(1)		SETTLING TIME (Samples)	
			50 Hz	60 Hz	SETTLED >99%	FULLY SETTLED
0h	DC block filter disabled					
1h	1/4	181 Hz	11.5 dB	10.1 dB	17	88
2h	1/8	84.8 Hz	5.89 dB	4.77 dB	36	187
3h	1/16	41.1 Hz	2.24 dB	1.67 dB	72	387
4h	1/32	20.2 Hz	657 mdB	466 mdB	146	786
5h	1/64	10.0 Hz	171 mdB	119 mdB	293	1585
6h	1/128	4.99 Hz	43.1 mdB	29.9 mdB	588	3182
7h	1/256	2.49 Hz	10.8 mdB	7.47 mdB	1178	6376
8h	1/512	1.24 Hz	2.69 mdB	1.87 mdB	2357	12764
9h	1/1024	622 mHz	671 µdB	466 µdB	4714	25540
Ah	1/2048	311 mHz	168 µdB	116 µdB	9430	51093
Bh	1/4096	155 mHz	41.9 µdB	29.1 µdB	18861	102202
Ch	1/8192	77.7 mHz	10.5 µdB	7.27 µdB	37724	204447
Dh	1/16384	38.9 mHz	2.63 µdB	1.82 µdB	75450	409156
Eh	1/32768	19.4 mHz	655 ndB	455 ndB	150901	820188
Fh	1/65536	9.70 mHz	164 ndB	114 ndB	301803	1627730

(1) Values given are for a 4-kSPS data rate with a 8.192-MHz CLKIN frequency.

8.3.9 Internal Test Signals

The ADS131M04-Q1 features an internal analog test signal that is useful for troubleshooting and diagnosis. A positive or negative DC test signal can be applied to the channel inputs through the input multiplexer. The multiplexer is controlled through the MUXn[1:0] bits in the CHn_CFG register. The test signals are created by internally dividing the internal reference voltage. The same signal is shared by all channels.

The test signal is nominally 2 / 15 × V_{REF}. The test signal automatically adjusts the voltage level with the gain setting such that the ADC always measures a signal that is 2 / 15 × $V_{Diff\ Max}$. For example, at a gain of 1, this voltage equates to 160 mV. At a gain of 2, this voltage is 80 mV.

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8.3.10 Channel Phase Calibration

The ADS131M04-Q1 allows fine adjustment of the sample phase between channels through the use of channel phase calibration. This feature is helpful when different channels are measuring the outputs of different types of sensors that have different phase responses. For example, in power metrology applications, voltage can be measured by a voltage divider, whereas current is measured using a current transformer that exhibits a phase difference between the input and output signals. The differences in phase between the voltage and current measurement must be compensated to measure the power and related parameters accurately.

The phase setting of the different channels is configured by the PHASEn[9:0] bits in the CHn_CFG register corresponding to the channel whose phase adjustment is desired. The register value is a 10-bit two's complement value corresponding to the number of modulator clock cycles of phase offset compared to a reference phase of 0 degrees.

The mechanism for achieving phase adjustment derives from the ΔΣ architecture. The ΔΣ modulator produces samples continuously at the modulator frequency, f_{MOD}. These samples are filtered and decimated to the output data rate by the digital filter. The ratio between f_{MOD} and the data rate is the oversampling ratio (OSR). Each conversion result corresponds to an OSR number of modulator samples provided to the digital filter. When the different channels of the ADS131M04-Q1 have no programmed phase offset between them, the modulator clock cycles corresponding to the conversion results of the different channels are aligned in the time domain. Figure 8-9 depicts an example scenario where the voltage input to channel 1 has no phase offset from channel 0.

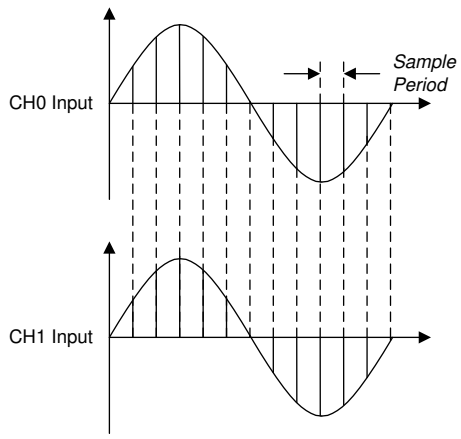

Figure 8-9. Two Channel Outputs With Equal Phase Settings

However, the sample period of one channel can be shifted with respect to another. If the inputs to both channels are sinusoids of the same frequency and the samples for these channels are retrieved by the host at the same time, the effect is that the phase of the channel with the modified sample period appears *shifted*. Figure 8-10 depicts how the period corresponding to the samples are shifted between channels. Figure 8-11 illustrates how the samples appear as having generated a phase shift when they are retrieved by the host.

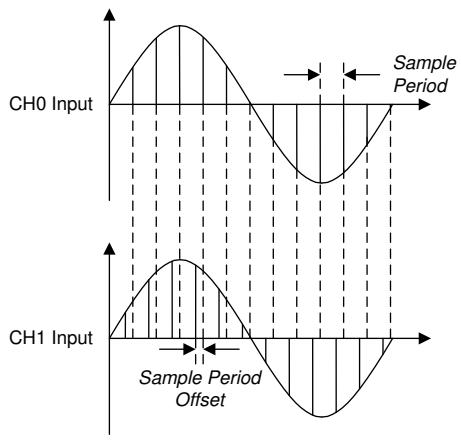

Figure 8-10. Channel 1 With a Positive Sample Phase Shift With Respect to Channel 0

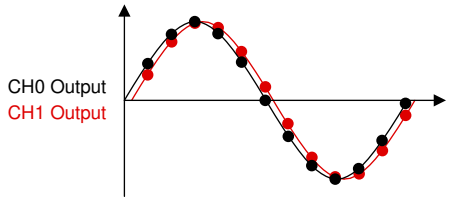

Figure 8-11. Channels 1 and 0 From the Perspective of the Host

The valid setting range is from –OSR / 2 to (OSR / 2) – 1, except for OSRs greater than 1024, where the phase calibration setting is limited to –512 to 511. If a value outside of –OSR / 2 and (OSR / 2) – 1 is programmed, the device internally clips the value to the nearest limit. For example, if the OSR setting is programmed to 128 and the PHASEn[9:0] bits are programmed to 0001100100b corresponding to 100 modulator clock cycles, the device sets the phase of the channel to 63 because that value is the upper limit of phase calibration for that OSR setting. Table 8-5 gives the range of phase calibration settings for various OSR settings.

Table 8-5. Phase Calibration Setting Limits for Different OSR Settings

OSR SETTING	PHASE OFFSET RANGE (t_{MOD})	PHASEn[9:0] BITS RANGE
64	–32 to 31	11 1110 0000b to 00 0001 1111b
128	–64 to 63	11 1100 0000b to 00 0011 1111b
256	–128 to 127	11 1000 0000b to 00 0111 1111b
512	–256 to 255	11 0000 0000b to 00 1111 1111b
1024	–512 to 511	10 0000 0000b to 01 1111 1111b
2048	–512 to 511	10 0000 0000b to 01 1111 1111b
4096	–512 to 511	10 0000 0000b to 01 1111 1111b
8192	–512 to 511	10 0000 0000b to 01 1111 1111b
16384	–512 to 511	10 0000 0000b to 01 1111 1111b

Follow these steps to create a phase shift larger than half the sample period for OSRs less than 2048:

- Create a phase shift corresponding to an integer number of sample periods by modifying the indices between channel data in software
- Use the phase calibration function of the ADS131M04-Q1 to create the remaining fractional sample period phase shift

For example, to create a phase shift of 2.25 samples between channels 0 and 1, create a phase shift of two samples by aligning sample N in the channel 0 output data stream with sample N+2 in the channel 1 output

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data stream in the host software. Make the remaining 0.25 sample adjustment using the ADS131M04-Q1 phase calibration function.

The phase calibration settings of the channels affect the timing of the data-ready interrupt signal, $\overline{\text{DRDY}}$. See the *Data Ready ($\overline{\text{DRDY}}$)* section for more details regarding how phase calibration affects the $\overline{\text{DRDY}}$ signal.

8.3.11 Calibration Registers

The calibration registers allow for the automatic computation of calibrated ADC conversion results from pre-programmed values. The host can rely on the device to automatically correct for system gain and offset after the error correction terms are programmed into the corresponding device registers. The measured calibration coefficients must be store in external non-volatile memory and programmed into the registers each time the ADS131M04-Q1 powers up because the ADS131M04-Q1 registers are volatile.

The offset calibration registers are used to correct for system offset error, otherwise known as *zero error*. Offset error corresponds to the ADC output when the input to the system is zero. The ADS131M04-Q1 corrects for offset errors by subtracting the contents of the OCALn[23:0] register bits in the CHn_OCAL_MSB and CHn_OCAL_LSB registers from the conversion result for that channel before being output. There are separate CHn_OCAL_MSB and CHnOCAL_LSB registers for each channel, which allows separate offset calibration coefficients to be programmed for each channel. The contents of the OCALn[23:0] bits are interpreted by the device as 24-bit two's complement values, which is the same format as the ADC data.

The gain calibration registers are used to correct for system gain error. Gain error corresponds to the deviation of gain of the system from the ideal value. The ADS131M04-Q1 corrects for gain errors by multiplying the ADC conversion result by the value given by the contents of the GCALn[23:0] register bits in the CHn_GCAL_MSB and CHn_GCAL_LSB registers before being output. There are separate CHn_GCAL_MSB and CHn_GCAL_LSB registers for each channel, which allows separate gain calibration coefficients to be programmed for each channel. The contents of the GCALn[23:0] bits are interpreted by the device as 24-bit unsigned values corresponding to linear steps ranging from gains of 0 to $2 – (1 / 2^{23})$. Table 8-6 describes the relationship between the GCALn[23:0] bit values and the gain calibration factor.

Table 8-6. GCALn[23:0] Bit Mapping

GCALn[23:0] VALUE	GAIN CALIBRATION FACTOR
000000h	0
000001h	1.19×10^{-7}
800000h	1
FFFFFEh	$2 – 2.38 \times 10^{-7}$
FFFFFFh	$2 – 1.19 \times 10^{-7}$

The calibration registers do not need to be enabled because they are always in use. The OCALn[23:0] bits have a default value of 000000h resulting in no offset correction. Similarly, the GCALn[23:0] bits default to 800000h resulting in a gain calibration factor of 1.

Figure 8-12 depicts a block diagram illustrating the mechanics of the calibration registers on one channel of the ADS131M04-Q1.

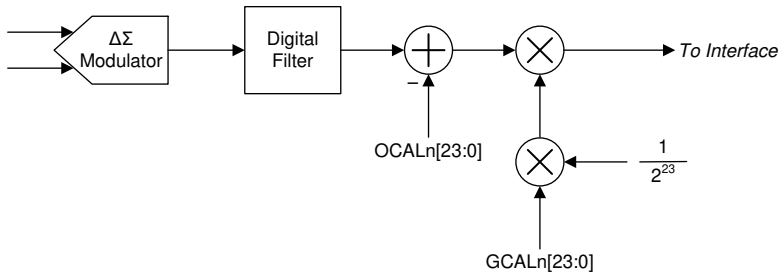

Figure 8-12. Calibration Block Diagram

8.3.12 Communication Cyclic Redundancy Check (CRC)

The ADS131M04-Q1 features a cyclic redundancy check (CRC) engine on both input and output data to mitigate SPI communication errors. The CRC word is 16 bits wide for either input or output CRC. Coverage includes all words in the SPI frame where the CRC is enabled, including padded bits in a 32-bit word size.

CRC on the SPI input is optional and can be enabled and disabled by writing the RX_CRC_EN bit in the MODE register. Input CRC is disabled by default. When the input CRC is enabled, the device checks the provided input CRC against the CRC generated based on the input data. A CRC error occurs if the CRC words do not match. The device does not execute any commands, except for the WREG command, if the input CRC check fails. A WREG command always executes even when the CRC check fails. The device sets the CRC_ERR bit in the STATUS register for all cases of a CRC error. The response on the output in the SPI frame following the frame where the CRC error occurred is that of a NULL command, which means the STATUS register plus the conversion data are output in the following SPI frame. The CRC_ERR bit is cleared when the STATUS register is output.

The output CRC cannot be disabled and always appears at the end of the output frame. The host can ignore the data if the output CRC is not used.

There are two types of CRC polynomials available: CCITT CRC and ANSI CRC (CRC-16). The CRC setting determines the algorithm for both the input and output CRC. The CRC type is programmed by the CRC_TYPE bit in the MODE register. Table 8-7 lists the details of the two CRC types.

The seed value of the CRC calculation is FFFFh.

Table 8-7. CRC Types

CRC TYPE	POLYNOMIAL	BINARY POLYNOMIAL
CCITT CRC	$x^{16} + x^{12} + x^5 + 1$	0001 0000 0010 0001
ANSI CRC	$x^{16} + x^{15} + x^2 + 1$	1000 0000 0000 0101

8.3.13 Register Map CRC

The ADS131M04-Q1 performs a CRC on the register map as a means to check for unintended changes to the registers. Enable the register map CRC by setting the REG_CRC_EN bit in the MODE register. When enabled, the device constantly calculates the register map CRC using each bit in the writable register space. The register addresses covered by the register map CRC on the ADS131M04-Q1 are 02h through 1Ch. The CRC is calculated beginning with the MSB of register 02h and ending with the LSB of register 1Ch using the polynomial selected in the CRC_TYPE bit in the MODE register.

The CRC calculation is initialized with the seed value of FFFFh.

The calculated CRC is a 16-bit value and is stored in the REGMAP_CRC register. The calculation is done using one register map bit per CLKIN period and constantly checks the result against the previous calculation. The REG_MAP bit in the STATUS register is set to flag the host if the register map CRC changes, including changes resulting from register writes. The bit is cleared by reading the STATUS register, or by the STATUS register being output as a response to the NULL command.

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8.4 Device Functional Modes

Figure 8-13 shows a state diagram depicting the major functional modes of the ADS131M04-Q1 and the transitions between them.

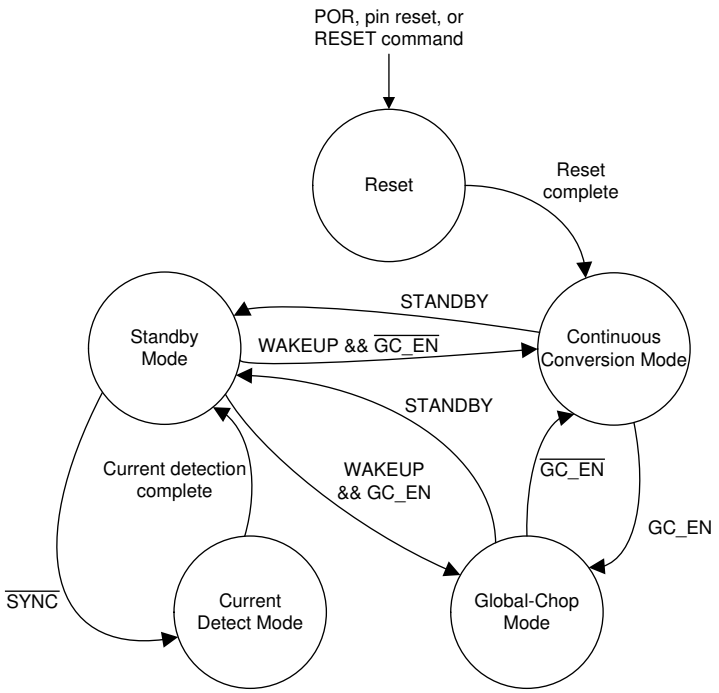

Figure 8-13. State Diagram Depicting Device Functional Modes

8.4.1 Power-Up and Reset

The ADS131M04-Q1 is reset in one of three ways: by a power-on reset (POR), by the $\overline{\text{SYNC}}$/$\overline{\text{RESET}}$ pin, or by a RESET command. After a reset occurs, the configuration registers are reset to the default values and the device begins generating conversion data as soon as a valid MCLK is provided. In all three cases a low to high transition on the $\overline{\text{DRDY}}$ pin indicates that the SPI interface is ready for communication. The device ignores any SPI communication before this point.

8.4.1.1 Power-On Reset

Power-on reset (POR) is the reset that occurs when a valid supply voltage is first applied. The POR process requires t_{POR} from when the supply voltages reach 90% of their nominal value. Internal circuitry powers up and the registers are set to their default state during this time. The $\overline{\text{DRDY}}$ pin transitions from low to high immediately after t_{POR} indicating the SPI interface is ready for communication. The device ignores any SPI communication before this point.

8.4.1.2 $\overline{\text{SYNC}}$/$\overline{\text{RESET}}$ Pin

The $\overline{\text{SYNC}}$/$\overline{\text{RESET}}$ pin is an active low, dual-function pin that generates a reset if the pin is held low longer than $t_{w(RSL)}$. The device maintains a reset state until $\overline{\text{SYNC}}$/$\overline{\text{RESET}}$ is returned high. The host must wait for at least t_{REGACQ} after $\overline{\text{SYNC}}$/$\overline{\text{RESET}}$ is brought high or for the $\overline{\text{DRDY}}$ rising edge before communicating with the device. Conversion data are generated immediately after the registers are reset to their default values, as described in the *Fast Start-Up Behavior* section.

8.4.1.3 RESET Command

The ADS131M04-Q1 can be reset via the SPI RESET command (0011h). The device communicates in frames of a fixed length. See the *SPI Communication Frames* section for details regarding SPI data framing on the ADS131M04-Q1. The RESET command occurs in the first word of the data frame, but the command is not latched by the device until the entire frame is complete. After the response completes channel data and CRC

words are clocked out. Terminating the frame early causes the RESET command to be ignored. Six words are required to complete a frame on the ADS131M04-Q1.

A reset occurs immediately after the command is latched. The host must wait for t_{REGACQ} before communicating with the device to ensure the registers have assumed their default settings. Conversion data are generated immediately after the registers are reset to their default values, as described in the *Fast Start-Up Behavior* section.

8.4.2 Fast Start-Up Behavior

The ADS131M04-Q1 begins generating conversion data shortly after startup as soon as a valid CLKIN signal is provided to the ΔΣ modulators. The fast start-up feature is useful for applications such as circuit breakers powered from the mains that require a fast determination of the input voltage soon after power is applied to the device. Fast start up is accomplished via two mechanisms. First, the device internal power-supply circuitry is designed specifically to enable fast start up. Second, the digital decimation filter dynamically switches from a fast-settling filter to a $sinc^3$ filter when the $sinc^3$ filter has had time to settle.

After the supplies are ramped to 90% of their final values, the device requires t_{POR} for the internal circuitry to settle. The end of t_{POR} is indicated by a transition of $\overline{DRDY}$ from low to high. The transition of $\overline{DRDY}$ from low to high also indicates the SPI interface is ready to accept commands.

The ΔΣ modulators of the ADS131M04-Q1 require CLKIN to toggle after t_{POR} to begin working. The modulators begin sampling the input signal after an initial wait time delay of (256 + 44) × t_{MOD} when CLKIN begins toggling. Therefore, provide a valid clock signal on CLKIN as soon as possible after the supply ramp to achieve the fastest possible startup time.

The data generated by the ΔΣ modulators are fed to the digital filter blocks. The data are provided to both the fast-settling filter and the $sinc^3$ filter paths. The fast-settling filter requires only one data rate period to provide settled data. Meanwhile, the $sinc^3$ filter requires three data rate periods to settle. The fast-settling filter generates the output data for the two interim ADC output samples indicated by $\overline{DRDY}$ transitioning from high to low while the $sinc^3$ filter is settling. The device disables the fast-settling filter and provides conversion data from the $sinc^3$ filter path for the third and following samples. Figure 8-14 shows the behavior of the fast start-up feature when using an external clock that is provided to the device right after the supplies have ramped. Table 8-8 shows the values for the various start-up and settling times relevant to the device start up.

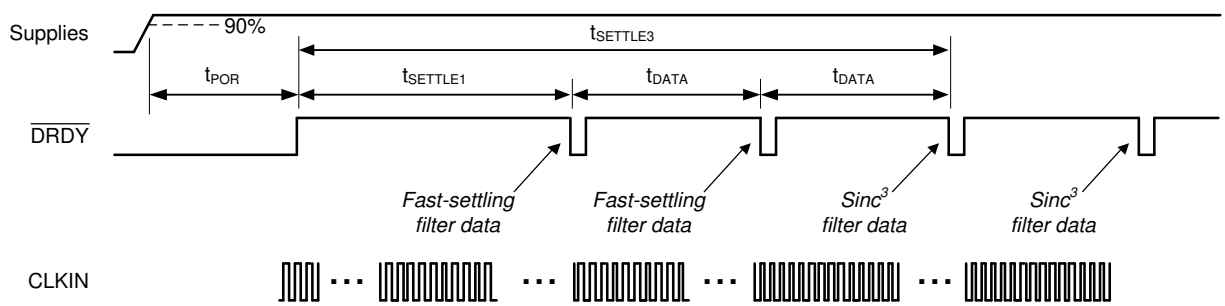

Figure 8-14. Fast Startup Behavior and Settling Times

Table 8-8. Fast Startup Settling Times for Default OSR = 1024

PARAMETER	VALUE (DETAILS) (t_{MOD})	VALUE (t_{MOD})	VALUE AT f_{CLKIN} = 8.192 MHz (ms)
$t_{DATA} = 1/f_{DATA}$	1024	1024	0.250
$t_{SETTLE1}$	256 + 44 + 1024	1324	0.323
$t_{SETTLE3}$	256 + 44 + 3 x 1024	3372	0.823

The fast-settling filter provides conversion data that are significantly noisier than the data that comes from the $sinc^3$ filter path, but allows the device to provide settled conversion data during the longer settling time of the more accurate $sinc^3$ digital filter. If the level of precision provided by the fast-settling filter is insufficient even for

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the first samples immediately following start up, ignore the first two instances of $\overline{DRDY}$ toggling from high to low and begin collecting data on the third instance.

The start-up process following a RESET command or a pin reset using the $\overline{SYNC}/\overline{RESET}$ pin is similar to what occurs after power up. However there is no t_{POR} in the case of a command or pin reset because the supplies are already ramped. After reset, the device waits for the initial wait time delay of (256 + 44) × t_{MOD} before providing modulator samples to the two digital filters. The fast-settling filter is enabled for the first two output samples.

8.4.3 Conversion Modes

There are two ADC conversion modes on the ADS131M04-Q1: continuous-conversion and global-chop mode. Continuous-conversion mode is a mode where ADC conversions are generated constantly by the ADC at a rate defined by f_{MOD} / OSR. Global-chop mode differs from continuous-conversion mode because global-chop periodically chops (or swaps) the inputs, which reduces system offset errors at the cost of settling time between the points when the inputs are swapped. In either continuous-conversion or global-chop mode, there are three power modes that provide flexible options to scale power consumption with bandwidth and dynamic range. The *Power Modes* section discusses these power modes in further detail.

8.4.3.1 Continuous-Conversion Mode

Continuous-conversion mode is the mode in which ADC data are generated constantly at the rate of f_{MOD} / OSR. New data are indicated by a $\overline{DRDY}$ falling edge at this rate. Continuous-conversion mode is intended for measuring AC signals because this mode allows for higher output data rates than global-chop mode.

8.4.3.2 Global-Chop Mode

The ADS131M04-Q1 incorporates a global-chop mode option to reduce offset error and offset drift inherent to the device resulting from mismatch in the internal circuitry to very low levels. When global-chop mode is enabled by setting the GC_EN bit in the GLOBAL_CHOP_CFG register, the device uses the conversion results from two consecutive internal conversions taken with opposite input polarity to cancel the device offset voltage. Conversion *n* is taken with normal input polarity. The device then reverses the internal input polarity for conversion $\overline{n + 1}$. The average of two consecutive conversions (*n* and $\overline{n + 1}$, $\overline{n + 1}$ and *n* + *2* and so on) yields the final offset compensated result.

Figure 8-15 shows a block diagram of the global-chop mode implementation. The combined PGA and ADC internal offset voltage is modeled as V_{OFS}. Only this device inherent offset voltage is reduced by global-chop mode. Offset in the external circuitry connected to the analog inputs is not affected by global-chop mode.

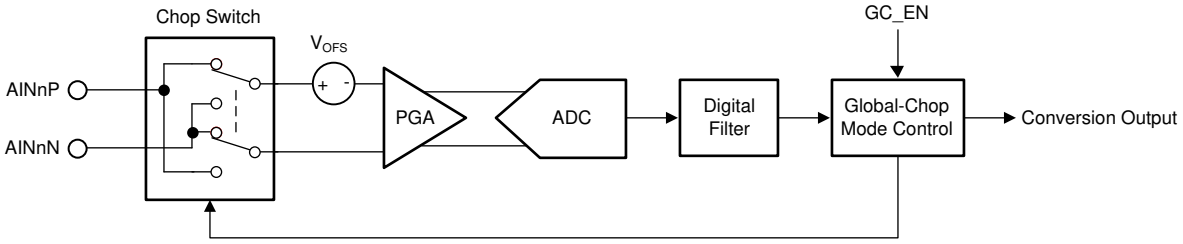

Figure 8-15. Global-Chop Mode Implementation

The conversion period in global-chop mode differs from the conversion time when global-chop mode is disabled (t_{DATA} = OSR x t_{MOD}). Figure 8-16 shows the conversion timing for an ADC channel using global-chop mode.

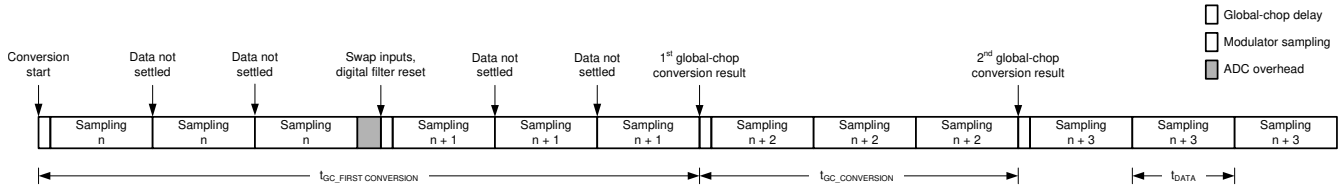

Figure 8-16. Conversion Timing With Global-Chop Mode Enabled

Every time the device swaps the input polarity, the digital filter is reset. The ADC then always takes three internal conversions to produce one settled global-chop conversion result.

The ADS131M04-Q1 provides a programmable delay (t_{GC_DLY}) between the end of the previous conversion period and the beginning of the subsequent conversion period after the input polarity is swapped. This delay allows external input circuitry to settle because the chopping switches interface directly with the analog inputs. The GC_DLY[3:0] bits in the GLOBAL_CHOP_CFG register configure the delay after chopping the inputs. The global-chop delay is selected in terms of modulator clock periods from 2 to 65,536 x t_{MOD}.

The effective conversion period in global-chop mode follows Equation 8. A $\overline{DRDY}$ falling edge is generated each time a new global-chop conversion becomes available to the host.

The conversion process of all ADC channels in global-chop mode is restarted in the following two conditions so that all channels start sampling at the same time:

- Falling edge of the $\overline{SYNC}/\overline{RESET}$ pin
- Change of OSR setting

The conversion period of the first conversion after the ADC channels are reset is considerably longer than the conversion period of all subsequent conversions mentioned in Equation 8, because the device must first perform two fully settled internal conversions with the input polarity swapped. The conversion period for the first conversion in global-chop mode follows Equation 9.

$$t_{GC_CONVERSION} = t_{GC_DLY} + 3 \times OSR \times t_{MOD} \quad (8)$$

$$t_{GC_FIRST_CONVERSION} = t_{GC_DLY} + 3 \times OSR \times t_{MOD} + t_{GC_DLY} + 3 \times OSR \times t_{MOD} + 44 \times t_{MOD} \quad (9)$$

Using global-chop mode reduces the ADC noise shown in Table 7-1 at a given OSR by a factor of $\sqrt{2}$ because two consecutive internal conversions are averaged to yield one global-chop conversion result. The DC test signal cannot be measured in global-chop mode.

Phase calibration is automatically disabled in global-chop mode.

8.4.4 Power Modes

In both continuous-conversion and global-chop mode, there are three selectable power modes that allow scaling of power with bandwidth and performance: high-resolution (HR) mode, low-power (LP) mode, and very-low-power (VLP) mode. The mode is selected by the PWR[1:0] bits in the CLOCK register. See the *Recommended Operating Conditions* table for restrictions on the CLKIN frequency for each power mode.

8.4.5 Standby Mode

Standby mode is a low-power state in which all channels are disabled, and the reference and other non-essential circuitry are powered down. This mode differs from completely powering down the device because the device retains the register settings. Enter standby mode by sending the STANDBY command (0022h). Stop toggling CLKIN when the device is in standby mode to minimize device power consumption. Exit standby mode by sending the WAKEUP command (0033h). After exiting standby mode, the modulators begin sampling the input signal after a modulator settling time of 8 × t_{MOD} when CLKIN begins toggling.

8.4.6 Current-Detect Mode

Current-detect mode is a special mode that is helpful for applications requiring tamper detection when the equipment is in a low-power state. In this mode, the ADS131M04-Q1 collects a configurable number of samples at a nominal data rate of 2.7 kSPS and compares the absolute value of the results to a programmable threshold. If a configurable number of results exceed the threshold, the host is notified via a $\overline{DRDY}$ falling edge and the device returns to standby mode. Enter current-detect mode by providing a negative pulse on $\overline{SYNC}/\overline{RESET}$ with a pulse duration less than $t_{w(RSL)}$ when in standby mode. Current-detect mode can only be entered from standby mode.

The device uses a limited power operating mode to generate conversions in current-detect mode. The conversion results are only used for comparison by the internal digital threshold comparator and are not accessible by the host. The device uses an internal oscillator that enables the device to capture the data without

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the use of the external clock input. Do not toggle CLKIN when in current-detect mode to minimize device power consumption.

Current-detect mode is configured in the CFG, THRSHLD_MSB, and THRSHLD_LSB registers. Enable and disable current-detect mode by toggling the CD_EN bit in the CFG register. The THRSHLD_MSB and THRSHLD_LSB registers contain the CD_THRSH[23:0] bits that represent the digital comparator threshold value during current detection.

The number of samples used for current detection are programmed by the CD_LEN[2:0] bits in the CFG register. The number of samples used for current detection range from 128 to 3584.

The programmable values in CD_NUM[2:0] configure the number of samples that must exceed the threshold for a detection to occur. The purpose of requiring multiple samples for detection is to control noisy values that may exceed the threshold, but do not represent a high enough power level to warrant action by the host. In summary, the conversion result must exceed the value programmed in CD_THRSH[23:0] a number of times as represented by the value stored in CD_NUM[2:0].

The device can be configured to notify the host based on any of the results from individual channels, all channels, or any combination of channels. The CD_ALLCH bit in the CFG register determines how many channels are required to exceed the programmed thresholds to trigger a current detection. When the bit is 1, all enabled channels are required to meet the current detection requirements in order for the host to be notified. If the bit is 0, any enabled channel triggers a current detection notification if the requirements are met. Enable and disable channels using the CHn_EN bits in the CLK register to control which combination of channels must meet the requirements to trigger a current-detection notification.

Figure 8-17 illustrates a flow chart depicting the current-detection process on the ADS131M04-Q1.

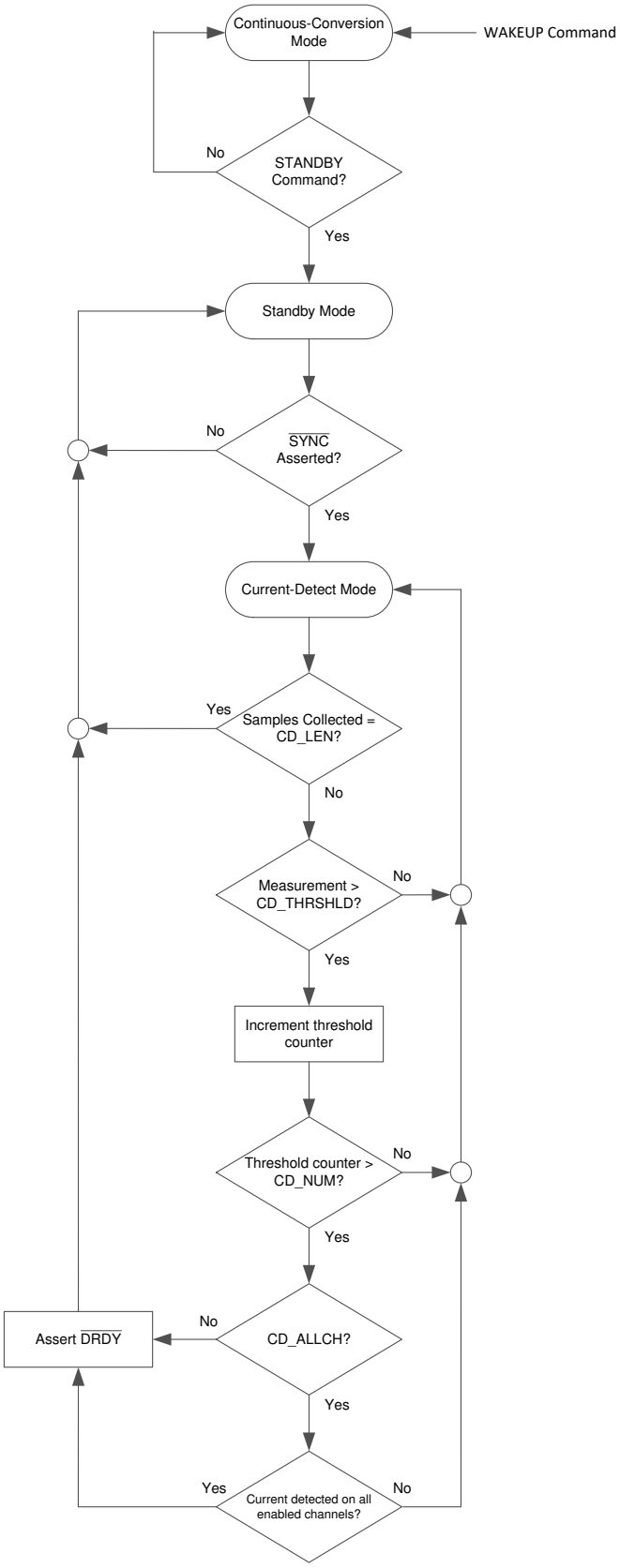

Figure 8-17. Current-Detect Mode Flow Chart

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8.5 Programming

8.5.1 Interface

The ADS131M04-Q1 uses an SPI-compatible interface to configure the device and retrieve conversion data. The device always acts as an SPI peripheral; SCLK and $\overline{CS}$ are inputs to the interface. The interface operates in SPI mode 1 where CPOL = 0 and CPHA = 1. In SPI mode 1, the SCLK idles low and data are launched or changed only on SCLK rising edges; data are latched or read by the controller and peripheral on SCLK falling edges. The interface is full-duplex, meaning data can be sent and received simultaneously by the interface. The device includes the typical SPI signals: SCLK, $\overline{CS}$, DIN (PICO), and DOUT (POCI). In addition, there are two other digital pins that provide additional functionality. The $\overline{DRDY}$ pin serves as a flag to the host to indicate new conversion data are available. The $\overline{SYNC}$/$\overline{RESET}$ pin is a dual-function pin that allows synchronization of conversions to an external event and allows for a hardware device reset.

8.5.1.1 Chip Select ($\overline{CS}$)

The $\overline{CS}$ pin is an active low input signal that selects the device for communication. The device ignores any communication and DOUT is high impedance when $\overline{CS}$ is held high. Hold $\overline{CS}$ low for the duration of a communication frame to ensure proper communication. The interface is reset each time $\overline{CS}$ is taken high.

8.5.1.2 Serial Data Clock (SCLK)

The SCLK pin is an input that serves as the serial clock for the interface. Output data on the DOUT pin transition on the rising edge of SCLK and input data on DIN are latched on the falling edge of SCLK.

8.5.1.3 Serial Data Input (DIN)

The DIN pin is the serial data input pin for the device. Serial commands are shifted in through the DIN pin by the device with each SCLK falling edge when the $\overline{CS}$ pin is low.

8.5.1.4 Serial Data Output (DOUT)

The DOUT pin is the serial data output pin for the device. The device shifts out command responses and ADC conversion data serially with each rising SCLK edge when the $\overline{CS}$ pin is low. This pin assumes a high-impedance state when $\overline{CS}$ is high.

8.5.1.5 Data Ready ($\overline{DRDY}$)

The $\overline{DRDY}$ pin is an active low output that indicates when new conversion data are ready in conversion mode or that the requirements are met for current detection when in current-detect mode. Connect the $\overline{DRDY}$ pin to a digital input on the host to trigger periodic data retrieval in conversion mode.

The timing of $\overline{DRDY}$ with respect to the sampling of a given channel on the ADS131M04-Q1 depends on the phase calibration setting of the channel and the state of the DRDY_SEL[1:0] bits in the MODE register. Setting the DRDY_SEL[1:0] bits to 00b configures $\overline{DRDY}$ to assert when the channel with the largest positive phase calibration setting, or the most lagging, has a new conversion result. When the bits are 01b, the device asserts $\overline{DRDY}$ each time any channel data are ready. Finally, setting the bits to either 10b or 11b configures the device to assert $\overline{DRDY}$ when the channel with the most negative phase calibration setting, or the most leading, has new conversion data. Changing the DRDY_SEL[1:0] bits has no effect on $\overline{DRDY}$ behavior in global-chop mode because phase calibration is automatically disabled in global-chop mode.

The timing of the first $\overline{DRDY}$ assertion after channels are enabled or after a synchronization pulse is provided depends on the phase calibration setting. If the channel that causes $\overline{DRDY}$ to assert has a phase calibration setting less than zero, the first $\overline{DRDY}$ assertion can be less than one sample period from the channel being enabled or the occurrence of the synchronization pulse. However, $\overline{DRDY}$ asserts in the next sample period if the phase setting puts the output timing too close to the beginning of the sample period.

Table 8-9 lists the phase calibration setting boundary at which $\overline{DRDY}$ either first asserts within a sample period, or in the next sample period. If the setting for the channel configured to control $\overline{DRDY}$ assertion is greater than the value listed in Table 8-9 for each OSR, $\overline{DRDY}$ asserts for the first time within a sample period of the channel being enabled or the synchronization pulse. If the phase setting value is equal to or more negative than the value

in Table 8-9, $\overline{\text{DRDY}}$ asserts in the following sample period. See the *Synchronization* section for more information about synchronization.

Table 8-9. Phase Setting First $\overline{\text{DRDY}}$ Assertion Boundary

OSR	PHASE SETTING BOUNDARY	PHASEn[9:0] BIT SETTING BOUNDARY
64	+13	00Dh
128	–19	3EDh
256	–83	3ADh
512	–211	32Dh
1024	–467	22Dh
>1024	None	N/A

The DRDY_HIZ bit in the MODE register configures the state of the $\overline{\text{DRDY}}$ pin when deasserted. By default the bit is 0b, meaning the pin is actively driven high using a push-pull output stage. When the bit is 1b, $\overline{\text{DRDY}}$ behaves like an open-drain digital output. Use a 100-kΩ pullup resistor to pull the pin high when $\overline{\text{DRDY}}$ is not asserted.

The DRDY_FMT bit in the MODE register determines the format of the $\overline{\text{DRDY}}$ signal. When the bit is 0b, new data are indicated by $\overline{\text{DRDY}}$ changing from high to low and remaining low until either all of the conversion data are shifted out of the device, or remaining low and going high briefly before the next time $\overline{\text{DRDY}}$ transitions low. When the DRDY_FMT bit is 1b, new data are indicated by a short negative pulse on the $\overline{\text{DRDY}}$ pin. If the host does not read conversion data after the $\overline{\text{DRDY}}$ pulse when DRDY_FMT is 1b, the device skips a conversion result and does not provide another $\overline{\text{DRDY}}$ pulse until the second following instance when data are ready because of how the pulse is generated. See the *Collecting Data for the First Time or After a Pause in Data Collection* section for more information about the behavior of $\overline{\text{DRDY}}$ when data are not consistently read.

The $\overline{\text{DRDY}}$ pulse is blocked when new conversions complete while conversion data are read. Therefore, avoid reading ADC data during the time where new conversions complete in order to achieve consistent $\overline{\text{DRDY}}$ behavior.

8.5.1.6 Conversion Synchronization or System Reset ($\overline{\text{SYNC}}$/$\overline{\text{RESET}}$)

The $\overline{\text{SYNC}}$/$\overline{\text{RESET}}$ pin is a multifunction digital input pin that serves primarily to allow the host to synchronize conversions to an external process or to reset the device. See the *Synchronization* section for more details regarding the synchronization function. See the *$\overline{\text{SYNC}}$/$\overline{\text{RESET}}$ Pin* section for more details regarding how the device is reset.

8.5.1.7 SPI Communication Frames

SPI communication on the ADS131M04-Q1 is performed in frames. Each SPI communication frame consists of several words. The word size is configurable as either 16 bits, 24 bits, or 32 bits by programming the WLENGTH[1:0] bits in the MODE register.

The ADS131M04-Q1 implements a timeout feature for SPI communication. Enable or disable the timeout using the TIMEOUT bit in the MODE register. When enabled, the entire SPI frame (first SCLK to last SCLK) must complete within 2^{15} CLKIN cycles otherwise the SPI resets. This feature is provided as a means to recover SPI synchronization for cases where $\overline{\text{CS}}$ is tied low.

The interface is full duplex, meaning that the interface is capable of transmitting data on DOUT while simultaneously receiving data on DIN. The input frame that the host sends on DIN always begins with a command. The first word on the output frame that the device transmits on DOUT always begins with the response to the command that was written on the previous input frame. The number of words in a command depends on the command provided. For most commands, there are six words in a frame. On DIN, the host provides the command, the command CRC if input CRC is enabled or a word of zeros if input CRC is disabled, and four additional words of zeros. Simultaneously on DOUT, the device outputs the response from the previous frame command, four words of ADC data representing the four ADC channels, and a CRC word. Figure 8-18 illustrates a typical command frame structure.

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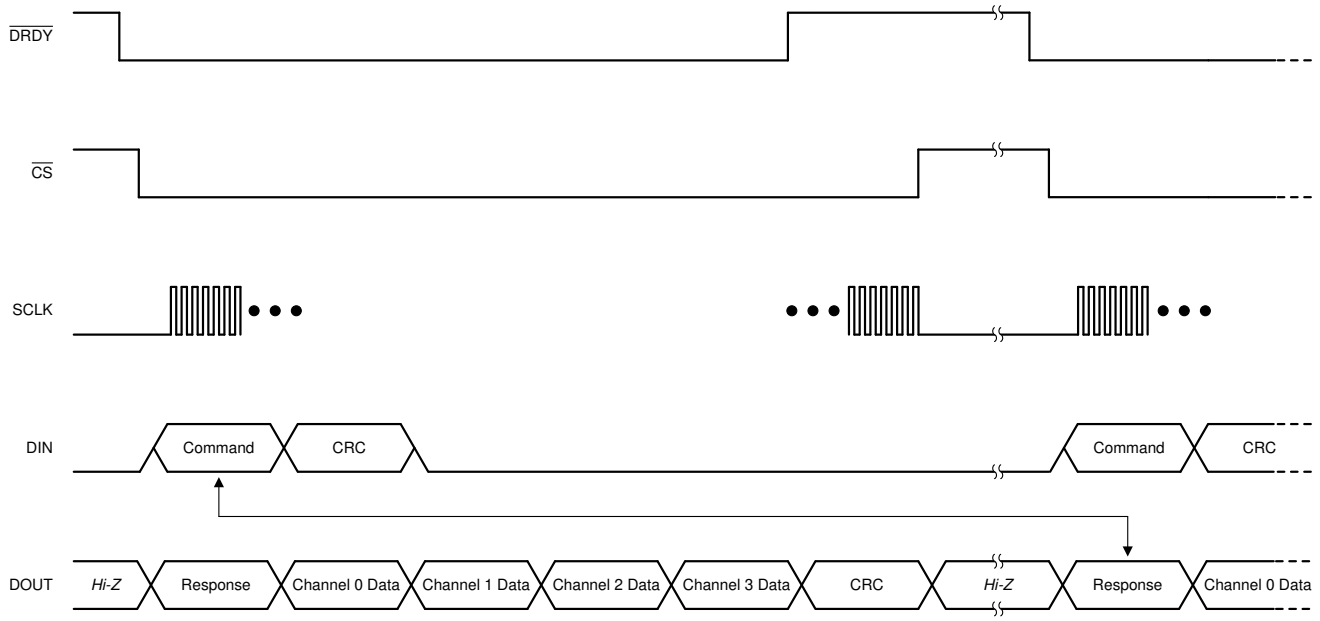

Figure 8-18. Typical Communication Frame

There are some commands that require more than six words. In the case of a read register (RREG) command where more than a single register is read, the response to the command contains the acknowledgment of the command followed by the register contents requested, which may require a larger frame depending on how many registers are read. See the *RREG (101a aaaa annn nnnn)* section for more details on the RREG command.

In the case of a write register (WREG) command where more than a single register is written, the frame extends to accommodate the additional data. See the *WREG (011a aaaa annn nnnn)* section for more details on the WREG command.

See the *Commands* section for a list of all valid commands and their corresponding responses on the ADS131M04-Q1.

Under special circumstances, a data frame can be shortened by the host. See the *Short SPI Frames* section for more information about artificially shortening communication frames.

8.5.1.8 SPI Communication Words

An SPI communication frame with the ADS131M04-Q1 is made of words. Words on DIN can contain commands, register settings during a register write, or a CRC of the input data. Words on DOUT can contain command responses, register settings during a register read, ADC conversion data, or CRC of the output data.

Words can be 16, 24, or 32 bits. The word size is configured by the WLENGTH[1:0] bits in the MODE register. The device defaults to a 24-bit word size. Commands, responses, CRC, and registers always contain 16 bits of actual data. These words are always most significant bit (MSB) aligned, and therefore the least significant bits (LSBs) are zero-padded to accommodate 24- or 32-bit word sizes. ADC conversion data are nominally 24 bits. The ADC truncates eight LSBs when the device is configured for 16-bit communication. There are two options for 32-bit communication available for ADC data that are configured by the WLENGTH[1:0] bits in the MODE register. Either the ADC data can be LSB padded with zeros or the data can be MSB sign extended.

8.5.1.9 ADC Conversion Data

The device provides conversion data for each channel at the data rate. The time when data are available relative to $\overline{\text{DRDY}}$ asserting is determined by the channel phase calibration setting and the DRDY_SEL[1:0] bits in the MODE register when in continuous-conversion mode. All data are available immediately following $\overline{\text{DRDY}}$ assertion in global-chop mode. The conversion status of all channels is available as the DRDY[3:0] bits in the STATUS register. The STATUS register content is automatically output as the response to the NULL command.

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Conversion data are 24 bits. The data LSBs are truncated when the device operates with a 16-bit word size. The LSBs are zero padded or the MSBs sign extended when operating with a 32-bit word size depending on the setting of the WLENGTH[1:0] bits in the MODE register.

Data are given in binary two's complement format. Use Equation 10 to calculate the size of one code (LSB).

$$1\ \text{LSB} = (2.4 / \text{Gain}) / 2^{24} = +\text{FSR} / 2^{23} \tag{10}$$

A positive full-scale input $V_{IN} \geq +\text{FSR} - 1\ \text{LSB} = 1.2 / \text{Gain} - 1\ \text{LSB}$ produces an output code of 7FFFFFh and a negative full-scale input ($V_{IN} \leq -\text{FSR} = -1.2 / \text{Gain}$) produces an output code of 800000h. The output clips at these codes for signals that exceed full-scale.

Table 8-10 summarizes the ideal output codes for different input signals.

Table 8-10. Ideal Output Code versus Input Signal

INPUT SIGNAL, $V_{IN} = V_{AINP} - V_{AINN}$	IDEAL OUTPUT CODE
$\geq \text{FSR}\ (2^{23} - 1) / 2^{23}$	7FFFFFh
$\text{FSR} / 2^{23}$	000001h
0	000000h
$-\text{FSR} / 2^{23}$	FFFFFFh
$\leq -\text{FSR}$	800000h

Figure 8-19 shows the mapping of the analog input signal to the output codes.

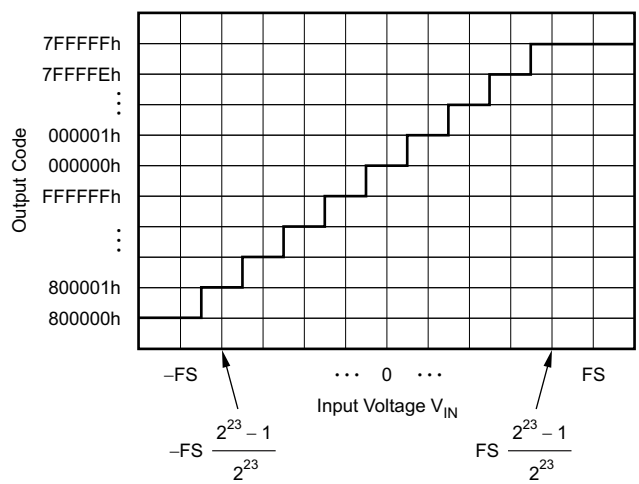

Figure 8-19. Code Transition Diagram

8.5.1.9.1 Collecting Data for the First Time or After a Pause in Data Collection

Take special precaution when collecting data for the first time or when beginning to collect data again after a pause. The internal mechanism that outputs data contains a first-in-first-out (FIFO) buffer that can store two samples of data per channel at a time. The DRDY flag for each channel in the STATUS register remains set until both samples for each channel are read from the device. This condition is not obvious under normal circumstances when the host is reading each consecutive sample from the device. In that case, the samples are cleared from the device each time new data are generated so the DRDY flag for each channel in the STATUS register is cleared with each read. However, both slots of the FIFO are full if a sample is missed or if data are not read for a period of time. Either strobe the $\overline{\text{SYNC}}/\overline{\text{RESET}}$ pin to re-synchronize conversions and clear the FIFOs, or quickly read two data packets when data are read for the first time or after a gap in reading data. This process ensures predictable $\overline{\text{DRDY}}$ pin behavior. See the *Synchronization* section for information about the synchronization feature. These methods do not need to be employed if each channel data was read for each output data period from when the ADC was enabled.

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Figure 8-20 depicts an example of how to collect data after a period of the ADC running, but where no data are being retrieved. In this instance, the $\overline{\text{SYNC}}$/$\overline{\text{RESET}}$ pin is used to clear the internal FIFOs and realign the ADS131M04-Q1 output data with the host.

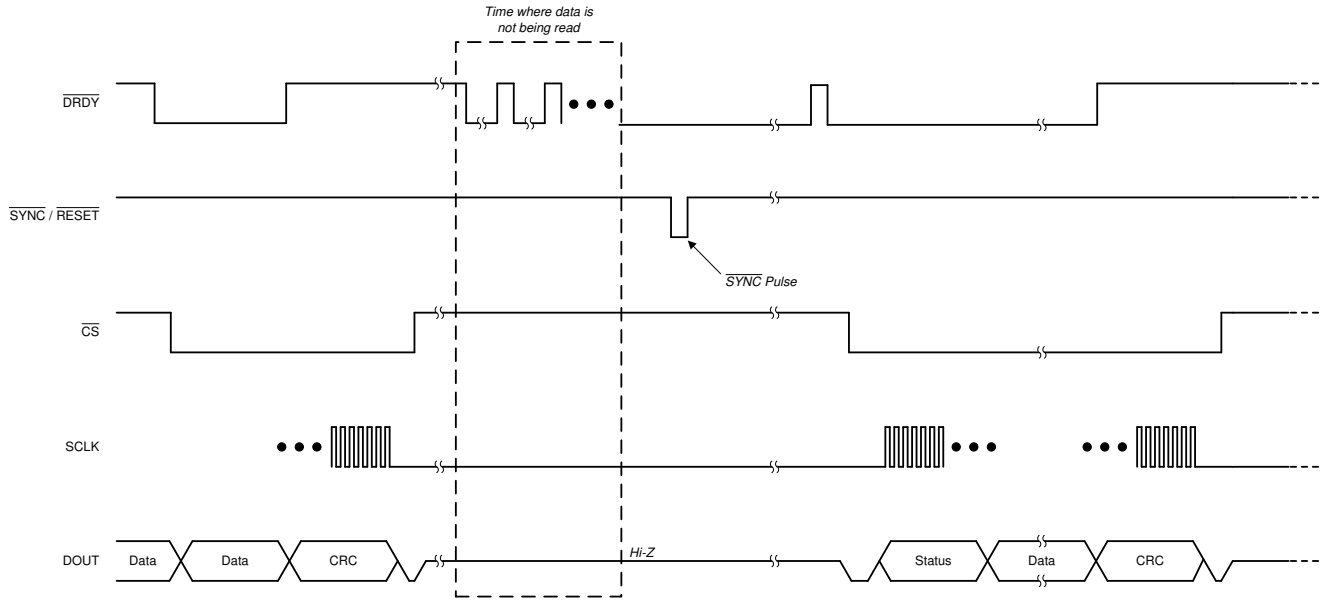

Figure 8-20. Collecting Data After a Pause in Data Collection Using the $\overline{\text{SYNC}}$/$\overline{\text{RESET}}$ Pin

Another functionally equivalent method for clearing the FIFO after a pause in collecting data is to begin by reading two samples in quick succession. Figure 8-21 depicts this method. This example shows when the DRDY_FMT bit in the MODE register is set to 0b indicating $\overline{\text{DRDY}}$ is a level output. There is a very narrow pulse on $\overline{\text{DRDY}}$ immediately after the first set of data are shifted out of the device. This pulse may be too narrow for some microcontrollers to detect. Therefore, do not rely upon this pulse but instead immediately read out the second data set after the first data set. The host operates synchronous to the device after the second word is read from the device.

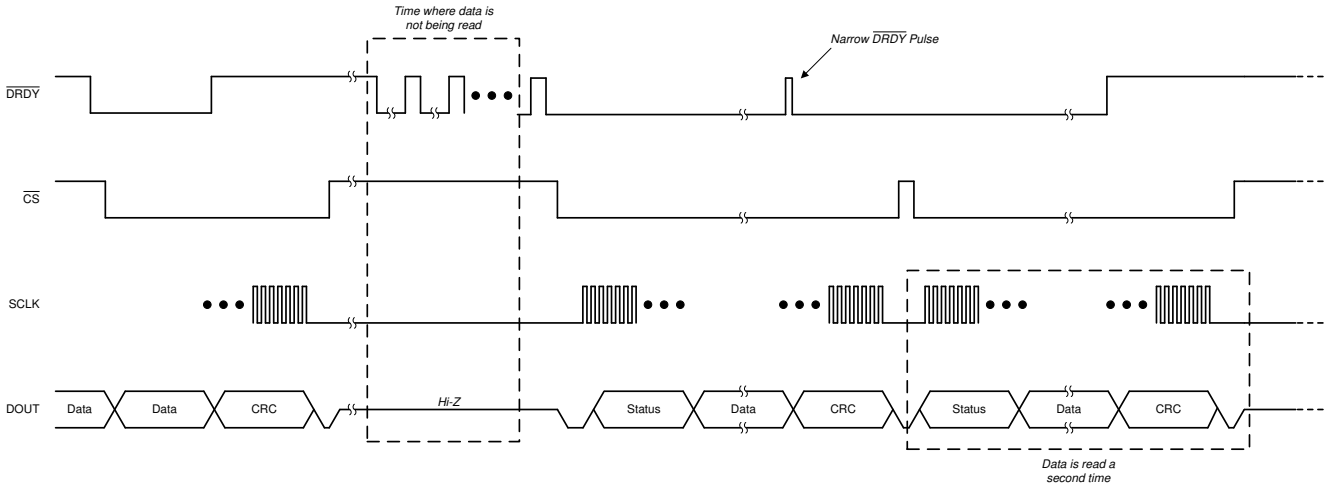

Figure 8-21. Collecting Data After a Pause in Data Collection by Reading Data Twice

8.5.1.10 Commands

Table 8-11 contains a list of all valid commands, a short description of their functionality, their binary command word, and the expected response that appears in the following frame.

Table 8-11. Command Definitions

COMMAND	DESCRIPTION	COMMAND WORD	RESPONSE
NULL	No operation	0000 0000 0000 0000	STATUS register
RESET	Reset the device	0000 0000 0001 0001	1111 1111 0010 0100
STANDBY	Place the device into standby mode	0000 0000 0010 0010	0000 0000 0010 0010
WAKEUP	Wake the device from standby mode to conversion mode	0000 0000 0011 0011	0000 0000 0011 0011
LOCK	Lock the interface such that only the NULL, UNLOCK, and RREG commands are valid	0000 0101 0101 0101	0000 0101 0101 0101
UNLOCK	Unlock the interface after the interface is locked	0000 0110 0101 0101	0000 0110 0101 0101
RREG	Read *nnn nnnn* plus 1 registers beginning at address *a aaaa a*	101*a aaaa annn nnnn*	*dddd dddd dddd dddd* or 111*a aaa annn nnnn* (1)
WREG	Write *nnn nnnn* plus 1 registers beginning at address *a aaaa a*	011*a aaaa annn nnnn*	010*a aaaa ammm mmmm* (2)

(1) When *nnn nnnn* is 0, the response is the requested register data *dddd dddd dddd dddd*. When *nnn nnnn* is greater than 0, the response begins with 111*a aaaa annn nnnn*, followed by the register data.
(2) In this case *mmm mmmm* represents the number of registers that are actually written minus one. This value may be less than *nnn nnnn* in some cases.

8.5.1.10.1 NULL (0000 0000 0000 0000)

The NULL command is the *no-operation* command that results in no registers read or written, and the state of the device remains unchanged. The intended use case for the NULL command is during ADC data capture. The command response for the NULL command is the contents of the STATUS register. Any invalid command also gives the NULL response.

8.5.1.10.2 RESET (0000 0000 0001 0001)

The RESET command resets the ADC to the register defaults. The command is latched by the device at the end of the frame. A reset occurs immediately after the command is latched. The host must wait for t_{REGACQ} after reset before communicating with the device to ensure the registers have assumed their default settings. The device sends an acknowledgment of FF24h when the ADC is properly RESET. The device responds with 0011h if the command word is sent but the frame is not completed and therefore the device is not reset. See the *RESET Command* section for more information regarding the operation of the reset command. Figure 8-22 illustrates a properly sent RESET command frame.

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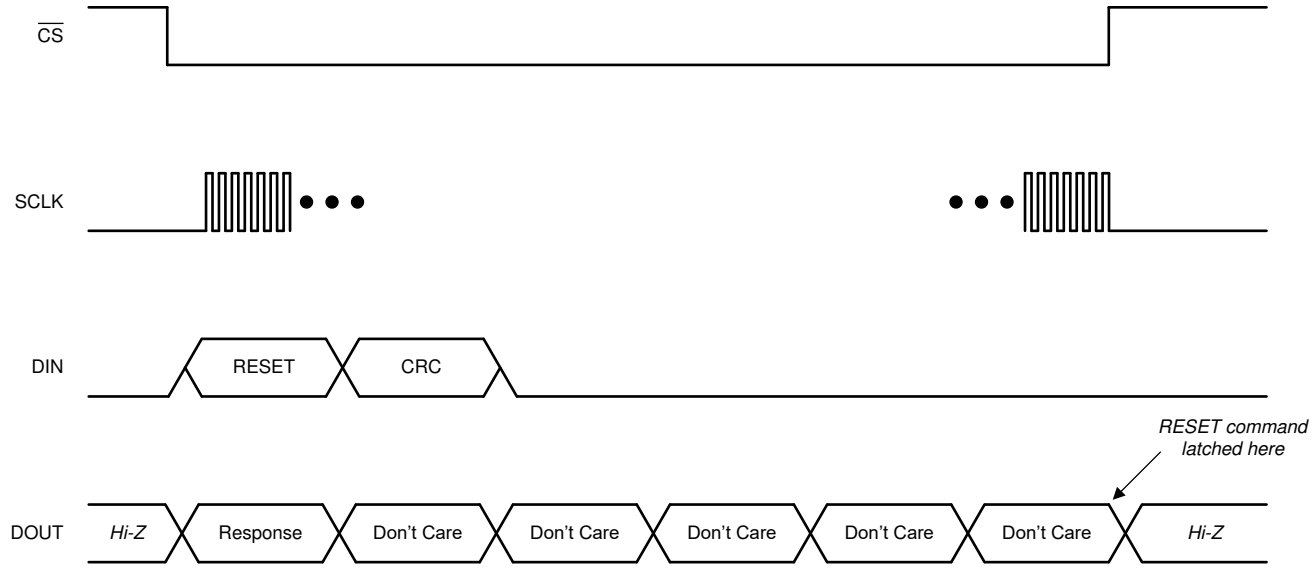

Figure 8-22. RESET Command Frame

8.5.1.10.3 STANDBY (0000 0000 0010 0010)

The STANDBY command places the device in a low-power standby mode. The command is latched by the device at the end of the frame. The device enters standby mode immediately after the command is latched. See the *Standby Mode* section for more information. This command has no effect if the device is already in standby mode.

8.5.1.10.4 WAKEUP (0000 0000 0011 0011)

The WAKEUP command returns the device to conversion mode from standby mode. This command has no effect if the device is already in conversion mode.

8.5.1.10.5 LOCK (0000 0101 0101 0101)

The LOCK command locks the interface, preventing the device from accidentally latching unwanted commands that can change the state of the device. When the interface is locked, the device only responds to the NULL, RREG, and UNLOCK commands. The device continues to output conversion data even when locked.

8.5.1.10.6 UNLOCK (0000 0110 0101 0101)

The UNLOCK command unlocks the interface if previously locked by the LOCK command.

8.5.1.10.7 RREG (101*a aaaa annn nnnn*)

The RREG is used to read the device registers. The binary format of the command word is 101*a aaaa annn nnnn*, where *a aaaa a* is the binary address of the register to begin reading and *nnn nnnn* is the unsigned binary number of consecutive registers to read minus one. There are two cases for reading registers on the ADS131M04-Q1. When reading a single register (*nnn nnnn* = 000 0000b), the device outputs the register contents in the command response word of the following frame. If multiple registers are read using a single command (*nnn nnnn* > 000 0000b), the device outputs the requested register data sequentially in order of addresses.

8.5.1.10.7.1 Reading a Single Register

Read a single register from the device by specifying *nnn nnnn* as zero in the RREG command word. As with all SPI commands on the ADS131M04-Q1, the response occurs on the output in the frame following the command. Instead of a unique acknowledgment word, the response word is the contents of the register whose address is specified in the command word. Figure 8-23 shows an example of reading a single register.

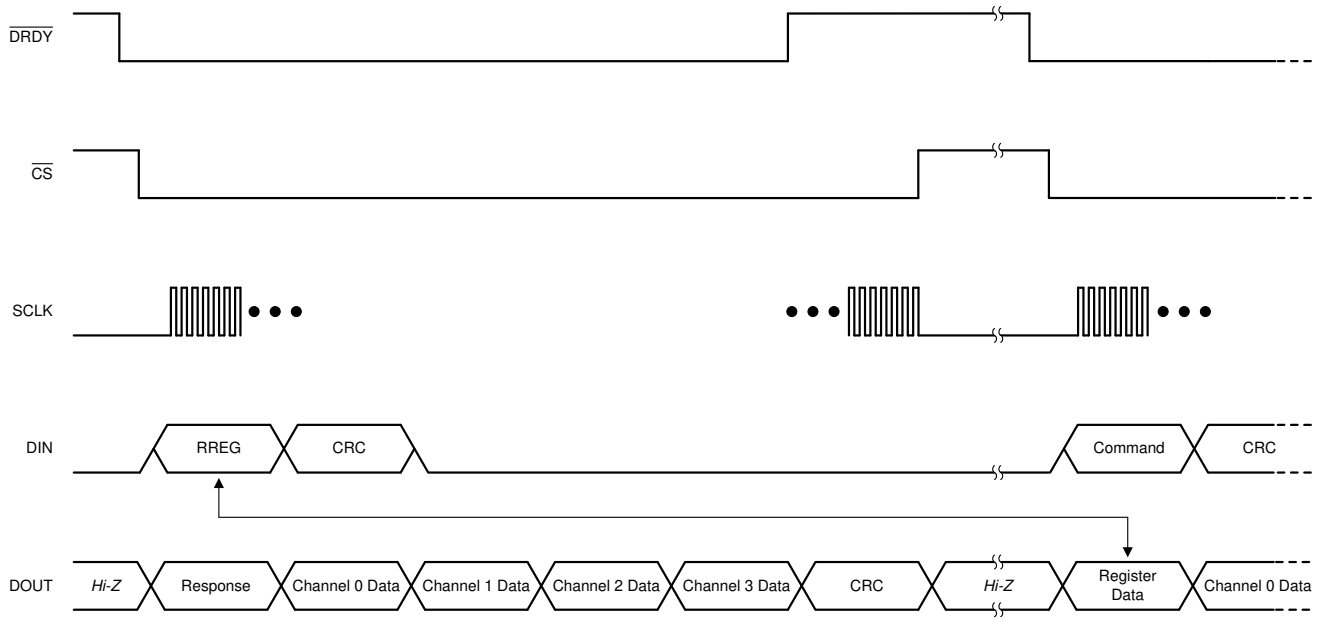

Figure 8-23. Reading a Single Register

8.5.1.10.7.2 Reading Multiple Registers

Multiple registers are read from the device when nnn nnnn is specified as a number greater than zero in the RREG command word. Like all SPI commands on the ADS131M04-Q1, the response occurs on the output in the frame following the command. Instead of a single acknowledgment word, the response spans multiple words in order to shift out all requested registers. Continue toggling SCLK to accommodate outputting the entire data stream. ADC conversion data are not output in the frame following an RREG command to read multiple registers. Figure 8-24 shows an example of reading multiple registers.

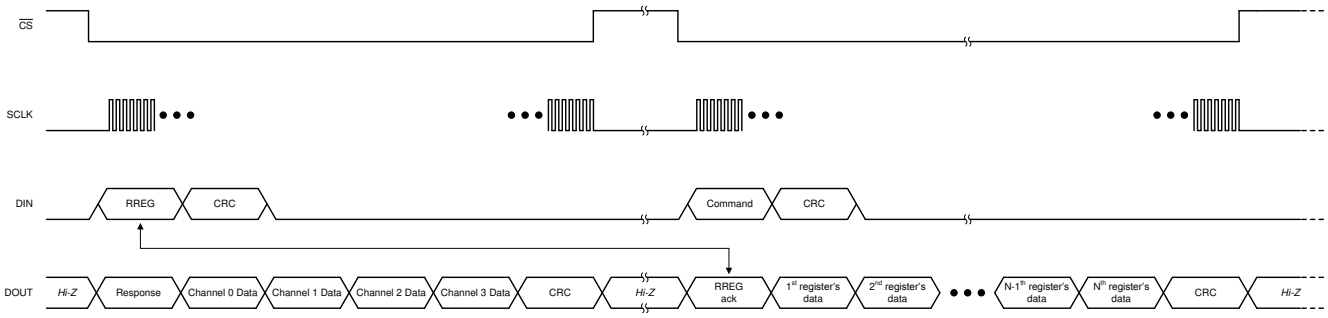

Figure 8-24. Reading Multiple Registers

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8.5.1.10.8 WREG (011a aaaa annn nnnn)

The WREG command allows writing an arbitrary number of contiguous device registers. The binary format of the command word is 011*a aaaa annn nnnn*, where *a aaaa a* is the binary address of the register to begin writing and *nnn nnnn* is the unsigned binary number of consecutive registers to write minus one. Send the data to be written immediately following the command word. Write the intended contents of each register into individual words, MSB aligned.

If the input CRC is enabled, write this CRC after the register data. The registers are written to the device as they are shifted into DIN. Therefore, a CRC error does not prevent an erroneous value from being written to a register. An input CRC error during a WREG command sets the CRC_ERR bit in the STATUS register.

The device ignores writes to read-only registers or to out-of-bounds addresses. Gaps in the register map address space are still included in the parameter *nnn nnnn*, but are not writeable so no change is made to them. The response to the WREG command that occurs in the following frame appears as 010*a aaaa ammm mmmm* where *mmm mmmm* is the number of registers actually written minus one. This number can be checked by the host against *nnn nnnn* to ensure the expected number of registers are written.

Figure 8-25 shows a typical WREG sequence. In this example, the number of registers to write is larger than the number of ADC channels and, therefore, the frame is extended beyond the ADC channels and output CRC word. Ensure all of the ADC data and output CRC are shifted out during each transaction where new data are available. Therefore, the frame must be extended beyond the number of words required to send the register data in some cases.

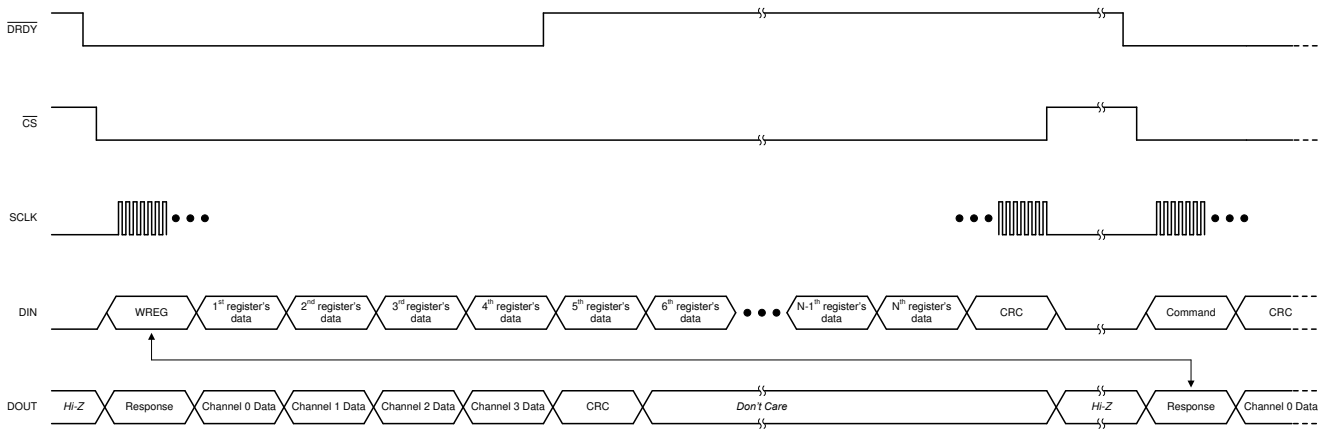

Figure 8-25. Writing Registers

8.5.1.11 Short SPI Frames

The SPI frame can be shortened to only send commands and receive responses if the ADCs are disabled and no ADC data are being output by the device. Read out all of the expected output data words from each sample period if the ADCs are enabled. Reading all of the data output with each frame ensures predictable $\overline{\text{DRDY}}$ pin behavior. If reading out all the data on each output data period is not feasible, see the *Collecting Data for the First Time or After a Pause in Data Collection* section on how to begin reading data again after a pause from when the ADCs were last enabled.

A short frame is not possible when using the RESET command. A full frame must be provided for a device reset to take place when providing the RESET command.

8.5.2 Synchronization

Synchronization can be performed by the host to ensure the ADC conversions are synchronized to an external event. For example, synchronization can realign the data capture to the expected timing of the host if a glitch on the clock causes the host and device to become out of synchronization.

Provide a negative pulse on the $\overline{\text{SYNC}}/\overline{\text{RESET}}$ pin with a duration less than $t_{w(RSL)}$ but greater than a CLKIN period to trigger synchronization. The device internally compares the leading negative edge of the pulse to the internal clock that tracks the data rate. The internal data rate clock has timing equivalent to the $\overline{\text{DRDY}}$ pin if configured to assert with a phase calibration setting of 0b. If the negative edge on $\overline{\text{SYNC}}/\overline{\text{RESET}}$ aligns with the internal data rate clock, the device is determined to be synchronized and therefore no action is taken. If there is misalignment, the digital filters on the device are reset to be synchronized with the $\overline{\text{SYNC}}/\overline{\text{RESET}}$ pulse. Conversions are immediately restarted when the $\overline{\text{SYNC}}/\overline{\text{RESET}}$ pin is toggled in global-chop mode.

The phase calibration settings on all channels are retained during synchronization. Thus, channels with non-zero phase calibration settings generate conversion results less than a data rate period after the synchronization event occurs. However, the results can be corrupted and are not settled until the respective channels have at least three conversion cycles for the $sinc^3$ filter to settle.

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8.6 ADS131M04-Q1 Registers

Table 8-12 lists the ADS131M04-Q1 registers. All register offset addresses not listed in Table 8-12 should be considered as reserved locations and the register contents should not be modified.

Table 8-12. Register Map

ADDRESS	REGISTER	RESET VALUE	BIT 15 / BIT 7	BIT 14 / BIT 6	BIT 13 / BIT 5	BIT 12 / BIT 4	BIT 11 / BIT 3	BIT 10 / BIT 2	BIT 9 / BIT 1	BIT 8 / BIT 0
DEVICE SETTINGS AND INDICATORS (Read-Only Registers)										
00h	ID	24xxh	RESERVED				CHANCNT[3:0]			
			RESERVED							
01h	STATUS	0500h	LOCK	F_RESYNC	REG_MAP	CRC_ERR	CRC_TYPE	RESET	WLENGTH[1:0]	
			RESERVED				DRDY3	DRDY2	DRDY1	DRDY0
GLOBAL SETTINGS ACROSS CHANNELS										
02h	MODE	0510h	RESERVED		REGCRC_EN	RX_CRC_EN	CRC_TYPE	RESET	WLENGTH[1:0]	
			RESERVED			TIMEOUT	DRDY_SEL[1:0]		DRDY_HiZ	DRDY_FMT
03h	CLOCK	0F0Eh	RESERVED				CH3_EN	CH2_EN	CH1_EN	CH0_EN
			RESERVED		TBM	OSR[2:0]			PWR[1:0]	
04h	GAIN1	0000h	RESERVED	PGAGAIN3[2:0]			RESERVED	PGAGAIN2[2:0]		
			RESERVED	PGAGAIN1[2:0]			RESERVED	PGAGAIN0[2:0]		
06h	CFG	0600h	RESERVED			GC_DLY[3:0]				GC_EN
			CD_ALLCH	CD_NUM[2:0]			CD_LEN[2:0]			CD_EN
07h	THRSHLD_MSB	0000h	CD_TH_MSB[15:8]							
			CD_TH_MSB[7:0]							
08h	THRSHLD_LSB	0000h	CD_TH_LSB[7:0]							
			RESERVED				DCBLOCK[3:0]			
CHANNEL-SPECIFIC SETTINGS										
09h	CH0_CFG	0000h	PHASE0[9:2]							
			PHASE0[1:0]		RESERVED			DCBLK0_DIS0	MUX0[1:0]	
0Ah	CH0_OCAL_MSB	0000h	OCAL0_MSB[15:8]							
			OCAL0_MSB[7:0]							
0Bh	CH0_OCAL_LSB	0000h	OCAL0_LSB[7:0]							
			RESERVED							
0Ch	CH0_GCAL_MSB	8000h	GCAL0_MSB[15:8]							
			GCAL0_MSB[7:0]							
0Dh	CH0_GCAL_LSB	0000h	GCAL0_LSB[7:0]							
			RESERVED							
0Eh	CH1_CFG	0000h	PHASE1[9:2]							
			PHASE1[1:0]		RESERVED			DCBLK1_DIS0	MUX1[1:0]	
0Fh	CH1_OCAL_MSB	0000h	OCAL1_MSB[15:8]							
			OCAL1_MSB[7:0]							
10h	CH1_OCAL_LSB	0000h	OCAL1_LSB[7:0]							
			RESERVED							
11h	CH1_GCAL_MSB	8000h	GCAL1_MSB[15:8]							
			GCAL1_MSB[7:0]							
12h	CH1_GCAL_LSB	0000h	GCAL1_LSB[7:0]							
			RESERVED							
13h	CH2_CFG	0000h	PHASE2[9:2]							
			PHASE2[1:0]		RESERVED			DCBLK2_DIS0	MUX2[1:0]	
14h	CH2_OCAL_MSB	0000h	OCAL2_MSB[15:8]							
			OCAL2_MSB[7:0]							
15h	CH2_OCAL_LSB	0000h	OCAL2_LSB[7:0]							
			RESERVED							
16h	CH2_GCAL_MSB	8000h	GCAL2_MSB[15:8]							
			GCAL2_MSB[7:0]							
17h	CH2_GCAL_LSB	0000h	GCAL2_LSB[7:0]							
			RESERVED							

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Table 8-12. Register Map (continued)

ADDRESS	REGISTER	RESET VALUE	BIT 15 / BIT 7	BIT 14 / BIT 6	BIT 13 / BIT 5	BIT 12 / BIT 4	BIT 11 / BIT 3	BIT 10 / BIT 2	BIT 9 / BIT 1	BIT 8 / BIT 0
18h	CH3_CFG	0000h	PHASE3[9:2]							
			PHASE3[1:0]		RESERVED			DCBLK3_DIS0	MUX3[1:0]	
19h	CH3_OCAL_MSB	0000h	OCAL3_MSB[15:8]							
			OCAL3_MSB[7:0]							
1Ah	CH3_OCAL_LSB	0000h	OCAL3_LSB[7:0]							
			RESERVED							
1Bh	CH3_GCAL_MSB	8000h	GCAL3_MSB[15:8]							
			GCAL3_MSB[7:0]							
1Ch	CH3_GCAL_LSB	0000h	GCAL3_LSB[7:0]							
			RESERVED							
REGISTER MAP CRC AND RESERVED REGISTERS										
3Eh	REGMAP_CRC	0000h	REG_CRC[15:8]							
			REG_CRC[7:0]							
3Fh	RESERVED	0000h	RESERVED							
			RESERVED							

Complex bit access types are encoded to fit into small table cells. Table 8-13 shows the codes that are used for access types in this section.

Table 8-13. Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

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8.6.1 ID Register (Address = 0h) [reset = 24xxh]

The ID register is shown in Figure 8-26 and described in Table 8-14.

Return to the Summary Table.

Figure 8-26. ID Register

15	14	13	12	11	10	9	8
RESERVED				CHANCNT[3:0]			
R-0010b				R-0100b			
7	6	5	4	3	2	1	0
RESERVED							
R-xxxxxxxxb							

Table 8-14. ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R	0010b	Reserved Always reads 0010b
11:8	CHANCNT[3:0]	R	0100b	Channel count. Always reads 0100b.
7:0	RESERVED	R	xxxxxxxxb	Reserved Values are subject to change without notice.

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8.6.2 STATUS Register (Address = 1h) [reset = 0500h]

The STATUS register is shown in Figure 8-27 and described in Table 8-15.

Return to the Summary Table.

Figure 8-27. STATUS Register

15	14	13	12	11	10	9	8
LOCK	F_RESYNC	REG_MAP	CRC_ERR	CRC_TYPE	RESET	WLENGTH[1:0]	
R-0b	R-0b	R-0b	R-0b	R-0b	R-1b	R-01b	
7	6	5	4	3	2	1	0
RESERVED				DRDY3	DRDY2	DRDY1	DRDY0
R-0000b				R-0b	R-0b	R-0b	R-0b

Table 8-15. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	LOCK	R	0b	SPI interface lock indicator 0b = Unlocked (default) 1b = Locked
14	F_RESYNC	R	0b	ADC resynchronization indicator. This bit is set each time the ADC resynchronizes. 0b = No resynchronization (default) 1b = Resynchronization occurred
13	REG_MAP	R	0b	Register map CRC fault indicator 0b = No change in the register map CRC (default) 1b = Register map CRC changed
12	CRC_ERR	R	0b	SPI input CRC error indicator 0b = No CRC error (default) 1b = Input CRC error occurred
11	CRC_TYPE	R	0b	CRC type 0b = 16-bit CCITT (default) 1b = 16-bit ANSI
10	RESET	R	1b	Reset status 0b = Not reset 1b = Reset occurred (default)
9:8	WLENGTH[1:0]	R	01b	Data word length 00b = 16 bits 01b = 24 bits (default) 10b = 32 bits; zero padding 11b = 32 bits; sign extension for 24-bit ADC data
7:4	RESERVED	R	0000b	Reserved Always reads 0000b

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Table 8-15. STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	DRDY3	R	0b	Channel 3 ADC data available indicator 0b = No new data available 1b = New data are available
2	DRDY2	R	0b	Channel 2 ADC data available indicator 0b = No new data available 1b = New data are available
1	DRDY1	R	0b	Channel 1 ADC data available indicator 0b = No new data available 1b = New data are available
0	DRDY0	R	0b	Channel 0 ADC data available indicator 0b = No new data available 1b = New data are available

8.6.3 MODE Register (Address = 2h) [reset = 0510h]

The MODE register is shown in Figure 8-28 and described in Table 8-16.

Return to the Summary Table.

Figure 8-28. MODE Register

15	14	13	12	11	10	9	8
RESERVED		REG_CRC_EN	RX_CRC_EN	CRC_TYPE	RESET	WLENGTH[1:0]	
R/W-00b		R/W-0b	R/W-0b	R/W-0b	R/W-1b	R/W-01b	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			TIMEOUT	DRDY_SEL[1:0]		DRDY_HiZ	DRDY_FMT
R/W-000b			R/W-1b	R/W-00b		R/W-0b	R/W-0b

Table 8-16. MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R/W	00b	Reserved Always write 00b
13	REG_CRC_EN	R/W	0b	Register map CRC enable 0b = Register CRC disabled (default) 1b = Register CRC enabled
12	RX_CRC_EN	R/W	0b	SPI input CRC enable 0b = Disabled (default) 1b = Enabled
11	CRC_TYPE	R/W	0b	SPI input and output, register map CRC type 0b = 16-bit CCITT (default) 1b = 16-bit ANSI
10	RESET	R/W	1b	Reset Write 0b to clear this bit in the STATUS register 0b = No reset 1b = Reset occurred (default by definition)
9:8	WLENGTH[1:0]	R/W	01b	Data word length selection 00b = 16 bits 01b = 24 bits (default) 10b = 32 bits; LSB zero padding 11b = 32 bits; MSB sign extension
7:5	RESERVED	R/W	000b	Reserved Always write 000b
4	TIMEOUT	R/W	1b	SPI Timeout enable 0b = Disabled 1b = Enabled (default)

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Table 8-16. MODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	DRDY_SEL[1:0]	R/W	00b	$\overline{\text{DRDY}}$ pin signal source selection 00b = Most lagging enabled channel (default) 01b = Logic OR of all enabled channels 10b = Most leading enabled channel 11b = Most leading enabled channel
1	DRDY_HiZ	R/W	0b	$\overline{\text{DRDY}}$ pin state when conversion data are not available 0b = Logic high (default) 1b = High impedance
0	DRDY_FMT	R/W	0b	$\overline{\text{DRDY}}$ signal format when conversion data are available 0b = Logic low (default) 1b = Low pulse with a fixed duration

8.6.4 CLOCK Register (Address = 3h) [reset = *0F0Eh*]

The CLOCK register is shown in Figure 8-29 and described in Table 8-17.

Return to the Summary Table.

Figure 8-29. CLOCK Register

15	14	13	12	11	10	9	8
RESERVED				CH3_EN	CH2_EN	CH1_EN	CH0_EN
R-0000b				R/W-1b	R/W-1b	R/W-1b	R/W-1b
7	6	5	4	3	2	1	0
RESERVED		TBM	OSR[2:0]			PWR[1:0]	
R/W-00b		R/W-0b	R/W-011b			R/W-10b	

Table 8-17. CLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R	0000b	Reserved Always reads 0000b
11	CH3_EN	R/W	1b	Channel 3 ADC enable 0b = Disabled 1b = Enabled (default)
10	CH2_EN	R/W	1b	Channel 2 ADC enable 0b = Disabled 1b = Enabled (default)
9	CH1_EN	R/W	1b	Channel 1 ADC enable 0b = Disabled 1b = Enabled (default)
8	CH0_EN	R/W	1b	Channel 0 ADC enable 0b = Disabled 1b = Enabled (default)
7:6	RESERVED	R/W	00b	Reserved Always write 00b
5	TBM	R/W	0b	Modulator oversampling ratio 64 selection (turbo mode) 0b = OSR set by bits 4:2 (that is, OSR[2:0]) 1b = OSR of 64 is selected
4:2	OSR[2:0]	R/W	011b	Modulator oversampling ratio selection 000b = 128 001b = 256 010b = 512 011b = 1024 (default) 100b = 2048 101b = 4096 110b = 8192 111b = 16384

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Table 8-17. CLOCK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	PWR[1:0]	R/W	10b	Power mode selection 00b = Very-low-power 01b = Low-power 10b = High-resolution (default) 11b = High-resolution

8.6.5 GAIN1 Register (Address = 4h) [reset = 0000h]

The GAIN1 register is shown in Figure 8-30 and described in Table 8-18.

Return to the Summary Table.

Figure 8-30. GAIN1 Register

15	14	13	12	11	10	9	8
RESERVED	PGAGAIN3[2:0]			RESERVED	PGAGAIN2[2:0]		
R/W-0b	R/W-000b			R/W-0b	R/W-000b		
7	6	5	4	3	2	1	0
RESERVED	PGAGAIN1[2:0]			RESERVED	PGAGAIN0[2:0]		
R/W-0b	R/W-000b			R/W-0b	R/W-000b		

Table 8-18. GAIN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0b	Reserved Always write 0b
14:12	PGAGAIN3[2:0]	R/W	000b	PGA gain selection for channel 3 000b = 1 (default) 001b = 2 010b = 4 011b = 8 100b = 16 101b = 32 110b = 64 111b = 128
11	RESERVED	R/W	0b	Reserved Always write 0b
10:8	PGAGAIN2[2:0]	R/W	000b	PGA gain selection for channel 2 000b = 1 (default) 001b = 2 010b = 4 011b = 8 100b = 16 101b = 32 110b = 64 111b = 128
7	RESERVED	R/W	0b	Reserved Always write 0b

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Table 8-18. GAIN1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:4	PGAGAIN1[2:0]	R/W	000b	PGA gain selection for channel 1 000b = 1 (default) 001b = 2 010b = 4 011b = 8 100b = 16 101b = 32 110b = 64 111b = 128
3	RESERVED	R/W	0b	Reserved Always write 0b
2:0	PGAGAIN0[2:0]	R/W	000b	PGA gain selection for channel 0 000b = 1 (default) 001b = 2 010b = 4 011b = 8 100b = 16 101b = 32 110b = 64 111b = 128

8.6.6 RESERVED Register (Address = 5h) [reset = 0000h]

The RESERVED register is shown in Figure 8-31 and described in Table 8-19.

Return to the Summary Table.

Figure 8-31. RESERVED Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-00000000b							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R/W-00000000b							

Table 8-19. RESERVED Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	R/W	00000000 00000000b	Reserved Always write 0000000000000000b

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8.6.7 CFG Register (Address = 6h) [reset = 0600h]

The CFG register is shown in Figure 8-32 and described in Table 8-20.

Return to the Summary Table.

Figure 8-32. CFG Register

15	14	13	12	11	10	9	8
RESERVED			GC_DLY[3:0]				GC_EN
R/W-000b			R/W-0011b				R/W-0b
7	6	5	4	3	2	1	0
CD_ALLCH	CD_NUM[2:0]			CD_LEN[2:0]			CD_EN
R/W-0b	R/W-000b			R/W-000b			R/W-0b

Table 8-20. CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	R/W	000b	Reserved Always write 000b
12:9	GC_DLY[3:0]	R/W	0011b	Global-chop delay selection Delay in modulator clock periods before measurement begins 0000b = 2 0001b = 4 0010b = 8 0011b = 16 (default) 0100b = 32 0101b = 64 0110b = 128 0111b = 256 1000b = 512 1001b = 1024 1010b = 2048 1011b = 4096 1100b = 8192 1101b = 16384 1110b = 32768 1111b = 65536
8	GC_EN	R/W	0b	Global-chop enable 0b = Disabled (default) 1b = Enabled
7	CD_ALLCH	R/W	0b	Current-detect channel selection Channels required to trigger current-detect 0b = Any channel (default) 1b = All channels

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Table 8-20. CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:4	CD_NUM[2:0]	R/W	000b	Number of current-detect exceeded thresholds selection Number of current-detect exceeded thresholds to trigger a detection 000b = 1 (default) 001b = 2 010b = 4 011b = 8 100b = 16 101b = 32 110b = 64 111b = 128
3:1	CD_LEN[2:0]	R/W	000b	Current-detect measurement length selection Current-detect measurement length in conversion periods 000b = 128 (default) 001b = 256 010b = 512 011b = 768 100b = 1280 101b = 1792 110b = 2560 111b = 3584
0	CD_EN	R/W	0b	Current-detect mode enable 0b = Disabled (default) 1b = Enabled

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8.6.8 THRSHLD_MSB Register (Address = 7h) [reset = 0000h]

The THRSHLD_MSB register is shown in Figure 8-33 and described in Table 8-21.

Return to the Summary Table.

Figure 8-33. THRSHLD_MSB Register

15	14	13	12	11	10	9	8
CD_TH_MSB[15:8]							
R/W-00000000b							
7	6	5	4	3	2	1	0
CD_TH_MSB[7:0]							
R/W-00000000b							

Table 8-21. THRSHLD_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CD_TH_MSB[15:0]	R/W	00000000 00000000b	Current-detect mode threshold MSB

8.6.9 THRSHLD_LSB Register (Address = 8h) [reset = 0000h]

The THRSHLD_LSB register is shown in Figure 8-34 and described in Table 8-22.

Return to the Summary Table.

Figure 8-34. THRSHLD_LSB Register

15	14	13	12	11	10	9	8
CD_TH_LSB[7:0]							
R/W-00000000b							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				DCBLOCK			
R-0000b				R/W-0000b			

Table 8-22. THRSHLD_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	CD_TH_LSB[7:0]	R/W	00000000b	Current-detect mode threshold LSB
7:4	RESERVED	R	0000b	Reserved Always write 0000b
3:0	DCBLOCK[3:0]	R/W	0000b	DC block filter setting, see Table 8-4 for details. Value of coefficient *a* 0000b = DC block filter disabled 0001b = 1/4 0010b = 1/8 0011b = 1/16 0100b = 1/32 0101b = 1/64 0110b = 1/128 0111b = 1/256 1000b = 1/512 1001b = 1/1024 1010b = 1/2048 1011b = 1/4096 1100b = 1/8192 1101b = 1/16384 1110b = 1/32768 1111b = 1/65536

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8.6.10 CH0_CFG Register (Address = 9h) [reset = 0000h]

The CH0_CFG register is shown in Figure 8-35 and described in Table 8-23.

Return to the Summary Table.

Figure 8-35. CH0_CFG Register

15	14	13	12	11	10	9	8
PHASE0[9:2]							
R/W-0000000000b							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHASE0[1:0]		RESERVED			DCBLK0_DIS0	MUX0[1:0]	
R/W-0000000000b		R-000b			R/W-0b	R/W-00b	

Table 8-23. CH0_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:6	PHASE0[9:0]	R/W	0000000000b	Channel 0 phase delay Phase delay in modulator clock cycles provided in two's complement format. See Table 8-5 for details.
5:3	RESERVED	R	000b	Reserved Always write 000b
2	DCBLK0_DIS0	R/W	0b	DC block filter for channel 0 disable 0b = Controlled by DCBLOCK[3:0] (default) 1b = Disabled for this channel
1:0	MUX0[1:0]	R/W	00b	Channel 0 input selection 00b = AIN0P and AIN0N (default) 01b = ADC inputs shorted 10b = Positive DC test signal 11b = Negative DC test signal

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8.6.11 CH0_OCAL_MSB Register (Address = Ah) [reset = 0000h]

The CH0_OCAL_MSB register is shown in Figure 8-36 and described in Table 8-24.

Return to the Summary Table.

Figure 8-36. CH0_OCAL_MSB Register

15	14	13	12	11	10	9	8
OCAL0_MSB[15:8]							
R/W-00000000b							
7	6	5	4	3	2	1	0
OCAL0_MSB[7:0]							
R/W-00000000b							

Table 8-24. CH0_OCAL_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	OCAL0_MSB[15:0]	R/W	00000000 00000000b	Channel 0 offset calibration register bits [23:8]

8.6.12 CH0_OCAL_LSB Register (Address = Bh) [reset = 0000h]

The CH0_OCAL_LSB register is shown in Figure 8-37 and described in Table 8-25.

Return to the Summary Table.

Figure 8-37. CH0_OCAL_LSB Register

15	14	13	12	11	10	9	8
OCAL0_LSB[7:0]							
R/W-00000000b							
7	6	5	4	3	2	1	0
RESERVED							
R-00000000b							

Table 8-25. CH0_OCAL_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	OCAL0_LSB[7:0]	R/W	00000000b	Channel 0 offset calibration register bits [7:0]
7:0	RESERVED	R	00000000b	Reserved Always reads 00000000b

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8.6.13 CH0_GCAL_MSB Register (Address = Ch) [reset = 8000h]

The CH0_GCAL_MSB register is shown in Figure 8-38 and described in Table 8-26.

Return to the Summary Table.

Figure 8-38. CH0_GCAL_MSB Register

15	14	13	12	11	10	9	8
GCAL0_MSB[15:8]							
R/W-10000000b							
7	6	5	4	3	2	1	0
GCAL0_MSB[7:0]							
R/W-00000000b							

Table 8-26. CH0_GCAL_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	GCAL0_MSB[15:0]	R/W	1000000000 000000b	Channel 0 gain calibration register bits [23:8]

8.6.14 CH0_GCAL_LSB Register (Address = Dh) [reset = 0000h]

The CH0_GCAL_LSB register is shown in Figure 8-39 and described in Table 8-27.

Return to the Summary Table.

Figure 8-39. CH0_GCAL_LSB Register

15	14	13	12	11	10	9	8
GCAL0_LSB[7:0]							
R/W-00000000b							
7	6	5	4	3	2	1	0
RESERVED							
R-00000000b							

Table 8-27. CH0_GCAL_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	GCAL0_LSB[7:0]	R/W	00000000b	Channel 0 gain calibration register bits [7:0]
7:0	RESERVED	R	00000000b	Reserved Always reads 00000000b

8.6.15 CH1_CFG Register (Address = Eh) [reset = 0000h]

The CH1_CFG register is shown in Figure 8-40 and described in Table 8-28.

Return to the Summary Table.

Figure 8-40. CH1_CFG Register

15	14	13	12	11	10	9	8
PHASE1[9:2]							
R/W-0000000000b							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHASE1[1:0]		RESERVED			DCBLK1_DIS0	MUX1[1:0]	
R/W-0000000000b		R-000b			R/W-0b	R/W-00b	

Table 8-28. CH1_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:6	PHASE1[9:0]	R/W	0000000000b	Channel 1 phase delay Phase delay in modulator clock cycles provided in two's complement format. See Table 8-5 for details.
5:3	RESERVED	R	000b	Reserved Always reads 000b
2	DCBLK1_DIS0	R/W	0b	DC block filter for channel 1 disable 0b = Controlled by DCBLOCK[3:0] (default) 1b = Disabled for this channel
1:0	MUX1[1:0]	R/W	00b	Channel 1 input selection 00b = AIN1P and AIN1N (default) 01b = ADC inputs shorted 10b = Positive DC test signal 11b = Negative DC test signal

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8.6.16 CH1_OCAL_MSB Register (Address = Fh) [reset = 0000h]

The CH1_OCAL_MSB register is shown in Figure 8-41 and described in Table 8-29.

Return to the Summary Table.

Figure 8-41. CH1_OCAL_MSB Register

15	14	13	12	11	10	9	8
OCAL1_MSB[15:8]							
R/W-00000000b							
7	6	5	4	3	2	1	0
OCAL1_MSB[7:0]							
R/W-00000000b							

Table 8-29. CH1_OCAL_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	OCAL1_MSB[15:0]	R/W	00000000 00000000b	Channel 1 offset calibration register bits [23:8]

8.6.17 CH1_OCAL_LSB Register (Address = 10h) [reset = 0000h]

The CH1_OCAL_LSB register is shown in Figure 8-42 and described in Table 8-30.

Return to the Summary Table.

Figure 8-42. CH1_OCAL_LSB Register

15	14	13	12	11	10	9	8
OCAL1_LSB[7:0]							
R/W-00000000b							
7	6	5	4	3	2	1	0
RESERVED							
R-00000000b							

Table 8-30. CH1_OCAL_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	OCAL1_LSB[7:0]	R/W	00000000b	Channel 1 offset calibration register bits [7:0]
7:0	RESERVED	R	00000000b	Reserved Always reads 00000000b

8.6.18 CH1_GCAL_MSB Register (Address = 11h) [reset = 8000h]

The CH1_GCAL_MSB register is shown in Figure 8-43 and described in Table 8-31.

Return to the Summary Table.

Figure 8-43. CH1_GCAL_MSB Register

15	14	13	12	11	10	9	8
GCAL1_MSB[15:8]							
R/W-10000000b							
7	6	5	4	3	2	1	0
GCAL1_MSB[7:0]							
R/W-00000000b							

Table 8-31. CH1_GCAL_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	GCAL1_MSB[15:0]	R/W	1000000000000000b	Channel 1 gain calibration register bits [23:8]

8.6.19 CH1_GCAL_LSB Register (Address = 12h) [reset = 0000h]

The CH1_GCAL_LSB register is shown in Figure 8-44 and described in Table 8-32.

Return to the Summary Table.

Figure 8-44. CH1_GCAL_LSB Register

15	14	13	12	11	10	9	8
GCAL1_LSB[7:0]							
R/W-00000000b							
7	6	5	4	3	2	1	0
RESERVED							
R-00000000b							

Table 8-32. CH1_GCAL_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	GCAL1_LSB[7:0]	R/W	00000000b	Channel 1 gain calibration register bits [7:0]
7:0	RESERVED	R	00000000b	Reserved Always reads 00000000b

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8.6.20 CH2_CFG Register (Address = 13h) [reset = 0000h]

The CH2_CFG register is shown in Figure 8-45 and described in Table 8-33.

Return to the Summary Table.

Figure 8-45. CH2_CFG Register

15	14	13	12	11	10	9	8
PHASE2[9:2]							
R/W-0000000000b							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHASE2[2:0]		RESERVED			DCBLK2_DIS0	MUX2[1:0]	
R/W-0000000000b		R-000b			R/W-0b	R/W-00b	

Table 8-33. CH2_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:6	PHASE2[9:0]	R/W	0000000000b	Channel 2 phase delay Phase delay in modulator clock cycles provided in two's complement format. See Table 8-5 for details.
5:3	RESERVED	R	000b	Reserved Always reads 000b
2	DCBLK2_DIS0	R/W	0b	DC block filter for channel 2 disable 0b = Controlled by DCBLOCK[3:0] (default) 1b = Disabled for this channel
1:0	MUX2[1:0]	R/W	00b	Channel 2 input selection 00b = AIN2P and AIN2N (default) 01b = ADC inputs shorted 10b = Positive DC test signal 11b = Negative DC test signal

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8.6.21 CH2_OCAL_MSB Register (Address = 14h) [reset = 0000h]

The CH2_OCAL_MSB register is shown in Figure 8-46 and described in Table 8-34.

Return to the Summary Table.

Figure 8-46. CH2_OCAL_MSB Register

15	14	13	12	11	10	9	8
OCAL2_MSB[15:8]							
R/W-00000000b							
7	6	5	4	3	2	1	0
OCAL2_MSB[7:0]							
R/W-00000000b							

Table 8-34. CH2_OCAL_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	OCAL2_MSB[15:0]	R/W	00000000 00000000b	Channel 2 offset calibration register bits [23:8]

8.6.22 CH2_OCAL_LSB Register (Address = 15h) [reset = 0000h]

The CH2_OCAL_LSB register is shown in Figure 8-47 and described in Table 8-35.

Return to the Summary Table.

Figure 8-47. CH2_OCAL_LSB Register

15	14	13	12	11	10	9	8
OCAL2_LSB[7:0]							
R/W-00000000b							
7	6	5	4	3	2	1	0
RESERVED							
R-00000000b							

Table 8-35. CH2_OCAL_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	OCAL2_LSB[7:0]	R/W	00000000b	Channel 2 offset calibration register bits [7:0]
7:0	RESERVED	R	00000000b	Reserved Always reads 00000000b

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8.6.23 CH2_GCAL_MSB Register (Address = 16h) [reset = 8000h]

The CH2_GCAL_MSB register is shown in Figure 8-48 and described in Table 8-36.

Return to the Summary Table.

Figure 8-48. CH2_GCAL_MSB Register

15	14	13	12	11	10	9	8
GCAL2_MSB[15:8]							
R/W-10000000b							
7	6	5	4	3	2	1	0
GCAL2_MSB[7:0]							
R/W-00000000b							

Table 8-36. CH2_GCAL_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	GCAL2_MSB[15:0]	R/W	1000000000 000000b	Channel 2 gain calibration register bits [23:8]

8.6.24 CH2_GCAL_LSB Register (Address = 17h) [reset = 0000h]

The CH2_GCAL_LSB register is shown in Figure 8-49 and described in Table 8-37.

Return to the Summary Table.

Figure 8-49. CH2_GCAL_LSB Register

15	14	13	12	11	10	9	8
GCAL2_LSB[7:0]							
R/W-00000000b							
7	6	5	4	3	2	1	0
RESERVED							
R-00000000b							

Table 8-37. CH2_GCAL_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	GCAL2_LSB[7:0]	R/W	00000000b	Channel 2 gain calibration register bits [7:0]
7:0	RESERVED	R	00000000b	Reserved Always reads 00000000b

8.6.25 CH3_CFG Register (Address = 18h) [reset = 0000h]

The CH3_CFG register is shown in Figure 8-50 and described in Table 8-38.

Return to the Summary Table.

Figure 8-50. CH3_CFG Register

15	14	13	12	11	10	9	8
PHASE3[9:2]							
R/W-0000000000b							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHASE3[1:0]		RESERVED			DCBLK3_DIS0	MUX3[1:0]	
R/W-0000000000b		R-000b			R/W-0b	R/W-00b	

Table 8-38. CH3_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:6	PHASE3[9:0]	R/W	0000000000b	Channel 3 phase delay Phase delay in modulator clock cycles provided in two's complement format. See Table 8-5 for details.
5:3	RESERVED	R	000b	Reserved Always reads 000b
2	DCBLK3_DIS0	R/W	0b	DC block filter for channel 3 disable 0b = Controlled by DCBLOCK[3:0] (default) 1b = Disabled for this channel
1:0	MUX3[1:0]	R/W	00b	Channel 3 input selection 00b = AIN3P and AIN3N (default) 01b = ADC inputs shorted 10b = Positive DC test signal 11b = Negative DC test signal

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8.6.26 CH3_OCAL_MSB Register (Address = 19h) [reset = 0000h]

The CH3_OCAL_MSB register is shown in Figure 8-51 and described in Table 8-39.

Return to the Summary Table.

Figure 8-51. CH3_OCAL_MSB Register

15	14	13	12	11	10	9	8
OCAL3_MSB[15:8]							
R/W-00000000b							
7	6	5	4	3	2	1	0
OCAL3_MSB[7:0]							
R/W-00000000b							

Table 8-39. CH3_OCAL_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	OCAL3_MSB[15:0]	R/W	00000000 00000000b	Channel 3 offset calibration register bits [23:8]

8.6.27 CH3_OCAL_LSB Register (Address = 1Ah) [reset = 0000h]

The CH3_OCAL_LSB register is shown in Figure 8-52 and described in Table 8-40.

Return to the Summary Table.

Figure 8-52. CH3_OCAL_LSB Register

15	14	13	12	11	10	9	8
OCAL3_LSB[7:0]							
R/W-00000000b							
7	6	5	4	3	2	1	0
RESERVED							
R-00000000b							

Table 8-40. CH3_OCAL_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	OCAL3_LSB[7:0]	R/W	00000000b	Channel 3 offset calibration register bits [7:0]
7:0	RESERVED	R	00000000b	Reserved Always reads 00000000b

8.6.28 CH3_GCAL_MSB Register (Address = 1Bh) [reset = 8000h]

The CH3_GCAL_MSB register is shown in Figure 8-53 and described in Table 8-41.

Return to the Summary Table.

Figure 8-53. CH3_GCAL_MSB Register

15	14	13	12	11	10	9	8
GCAL3_MSB[15:8]							
R/W-10000000b							
7	6	5	4	3	2	1	0
GCAL3_MSB[7:0]							
R/W-00000000b							

Table 8-41. CH3_GCAL_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	GCAL3_MSB[15:0]	R/W	1000000000 000000b	Channel 3 gain calibration register bits [23:8]

8.6.29 CH3_GCAL_LSB Register (Address = 1Ch) [reset = 0000h]

The CH3_GCAL_LSB register is shown in Figure 8-54 and described in Table 8-42.

Return to the Summary Table.

Figure 8-54. CH3_GCAL_LSB Register

15	14	13	12	11	10	9	8
GCAL3_LSB[7:0]							
R/W-00000000b							
7	6	5	4	3	2	1	0
RESERVED							
R-00000000b							

Table 8-42. CH3_GCAL_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	GCAL3_LSB[7:0]	R/W	00000000b	Channel 3 gain calibration register bits [7:0]
7:0	RESERVED	R	00000000b	Reserved Always reads 00000000b

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8.6.30 REGMAP_CRC Register (Address = 3Eh) [reset = 0000h]

The REGMAP_CRC register is shown in Figure 8-55 and described in Table 8-43.

Return to the Summary Table.

Figure 8-55. REGMAP_CRC Register

15	14	13	12	11	10	9	8
REG_CRC[15:8]							
R-0000000000000000b							
7	6	5	4	3	2	1	0
REG_CRC[7:0]							
R-0000000000000000b							

Table 8-43. REGMAP_CRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	REG_CRC[15:0]	R	00000000 00000000b	Register map CRC

8.6.31 RESERVED Register (Address = 3Fh) [reset = 0000h]

The RESERVED register is shown in Figure 8-56 and described in Table 8-44.

Return to the Summary Table.

Figure 8-56. RESERVED Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-00000000b							
7	6	5	4	3	2	1	0
RESERVED							
R/W-00000000b							

Table 8-44. RESERVED Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	R/W	00000000 00000000b	Reserved, Always write 0000000000000000b

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Unused Inputs and Outputs

Leave any unused analog inputs floating or connect them to AGND.

Do not float unused digital inputs because excessive power-supply leakage current can result. Tie all unused digital inputs to the appropriate levels, DVDD or DGND. Leave the $\overline{\text{DRDY}}$ pin unconnected or connect this pin to DVDD using a weak pullup resistor if unused.

9.1.2 Antialiasing

An analog low-pass filter is required in front of each of the channel inputs to prevent out-of-band noise and interferers from coupling into the band of interest. Because the ADS131M04-Q1 is a delta-sigma ADC, the integrated digital filter provides substantial attenuation for frequencies outside of the band of interest up to the frequencies adjacent to f_{MOD}. Therefore, a single-order RC filter provides sufficient antialiasing protection in the vast majority of applications.

Choosing the values of the resistor and capacitor depends on the desired cutoff frequency, limiting source impedance for the ADC inputs, and providing enough instantaneous charge to the ADC input sampling circuit through the filter capacitor. Figure 9-1 shows the recommended filter component values. These recommendations are sufficient for CLKIN frequencies between 2 MHz and 8.2 MHz.

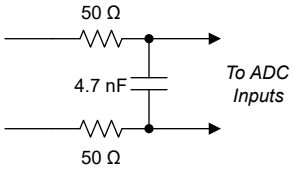

Figure 9-1. Recommended Antialiasing Circuitry

9.1.3 Minimum Interface Connections

Figure 9-2 depicts how the ADS131M04-Q1 can be configured for the minimum number of interface pins. This configuration is useful when using data isolation to minimize the number of isolation channels required or when the microcontroller (MCU) pins are limited.

The CLKIN pin requires an LVCMOS clock that can be either generated by the MCU or created using a local LVCMOS output device. Tie the $\overline{\text{SYNC}}/\overline{\text{RESET}}$ pin to DVDD in hardware if unused. The $\overline{\text{DRDY}}$ pin can be left floating if unused. Connect either $\overline{\text{SYNC}}/\overline{\text{RESET}}$ or $\overline{\text{DRDY}}$ to the MCU to ensure the MCU stays synchronized to ADC conversions. If the MCU provides CLKIN, the CLKIN periods can be counted to determine the sample period rather than forcing synchronization using the $\overline{\text{SYNC}}/\overline{\text{RESET}}$ pin or monitoring the $\overline{\text{DRDY}}$ pin. Synchronization cannot be regained if a bit error occurs on the clock and samples can be missed if the $\overline{\text{SYNC}}/\overline{\text{RESET}}$ or $\overline{\text{DRDY}}$ pins are not used. $\overline{\text{CS}}$ can be tied low in hardware if the ADS131M04-Q1 is the only device on the SPI bus. Ensure the data input and output CRC are enabled and are used to guard against faulty register reads and writes if $\overline{\text{CS}}$ is tied low permanently.

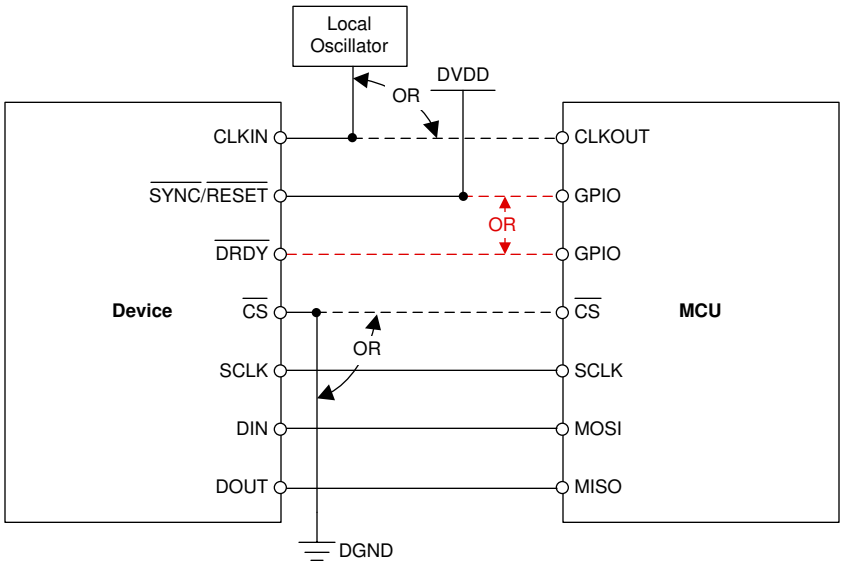

Figure 9-2. Minimum Connections Required to Operate the ADS131M04-Q1

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9.1.4 Multiple Device Configuration

Multiple ADS131M04-Q1 devices can be arranged to capture all signals simultaneously. The same clock must be provided to all devices and the $\overline{\text{SYNC}}$/$\overline{\text{RESET}}$ pins must be strobed simultaneously at least one time to align the sample periods internally between devices. The phase settings of each device can be changed uniquely, but the host must take care to record which channel in the group of devices represents the *zero* phase.

The devices can also share the SPI bus where only the $\overline{\text{CS}}$ pins for each device are unique. Each device can be addressed sequentially by asserting $\overline{\text{CS}}$ for the device that the host wishes to communicate with. The DOUT pin remains high impedance when the $\overline{\text{CS}}$ pin is high, allowing the DOUT lines to be shared between devices as long as no two devices sharing the bus simultaneously have their $\overline{\text{CS}}$ pins low. Figure 9-3 shows multiple devices configured for simultaneous data acquisition while sharing the SPI bus.

Monitoring the $\overline{\text{DRDY}}$ output of only one of the devices is sufficient because all devices convert simultaneously.

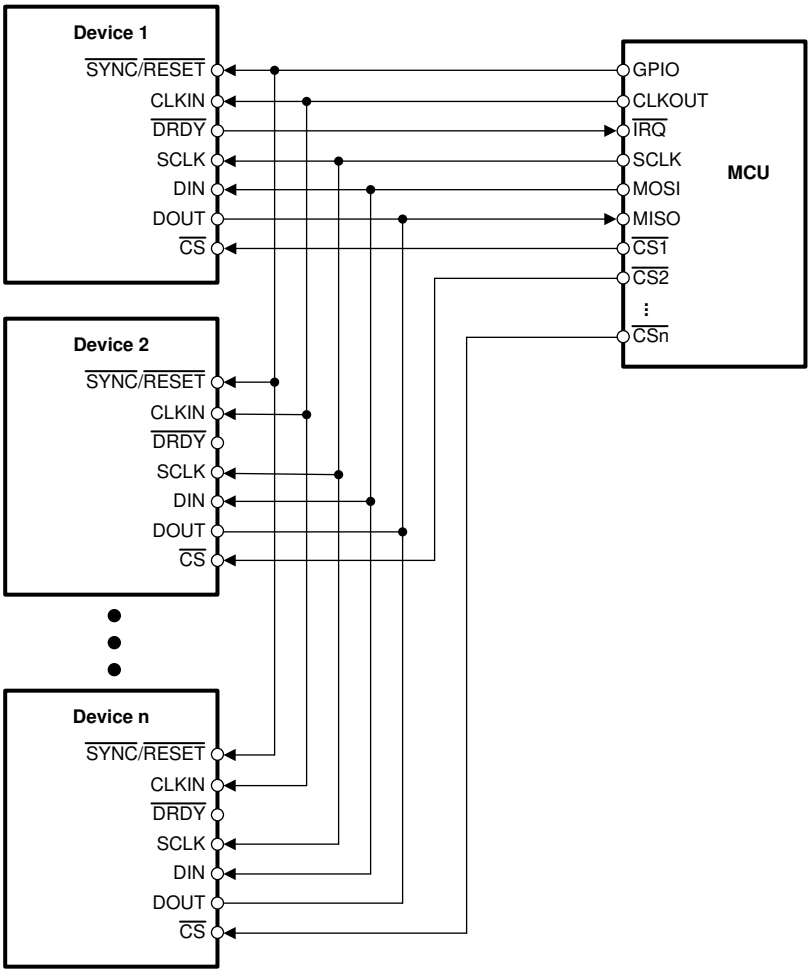

Figure 9-3. Multiple Device Configuration

9.1.5 Troubleshooting

Table 9-1 lists common issues faced when designing with the ADS131M04-Q1 and the corresponding solutions. This list is not comprehensive.

Table 9-1. Troubleshooting Common Issues Using the ADS131M04-Q1

ISSUE	POSSIBLE ROOT CAUSE	POSSIBLE SOLUTION
The $\overline{\text{DRDY}}$ pin is toggling at half the expected frequency.	ADC conversion data are not being read. The two-deep ADC data FIFO overflows and triggers $\overline{\text{DRDY}}$ one time every two ADC data periods.	Read data after each $\overline{\text{DRDY}}$ falling edge after following the recommendations given in the *Collecting Data for the First Time or After a Pause in Data Collection* section.
The F_RESYNC bit is set in the STATUS word even though this bit was already cleared.	The $\overline{\text{SYNC}}$/$\overline{\text{RESET}}$ pin is being toggled asynchronously to CLKIN.	The $\overline{\text{SYNC}}$/$\overline{\text{RESET}}$ pin functions as a constant synchronization check, rather than a *convert start* pin. See the *Synchronization* section for more details on the intended usage of the $\overline{\text{SYNC}}$/$\overline{\text{RESET}}$ pin.
The same ADC conversion data are output twice before changing.	The entire frame is not being sent to the ADC. The ADC does not recognize data as being read.	Read all data words in the output data frame, including those for channels that are disabled.

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9.2 Typical Application

This section describes a typical battery management system (BMS) application circuit using the ADS131M04-Q1. The device serves the following primary functions in this BMS:

- Measure battery current with high resolution and accuracy using a low-side current shunt sensor
- Measure peak currents and detect overcurrent or short-circuit conditions
- Measure battery-pack voltage using a high-voltage resistor divider

Figure 9-4 shows the front-end for the battery management system circuit design.

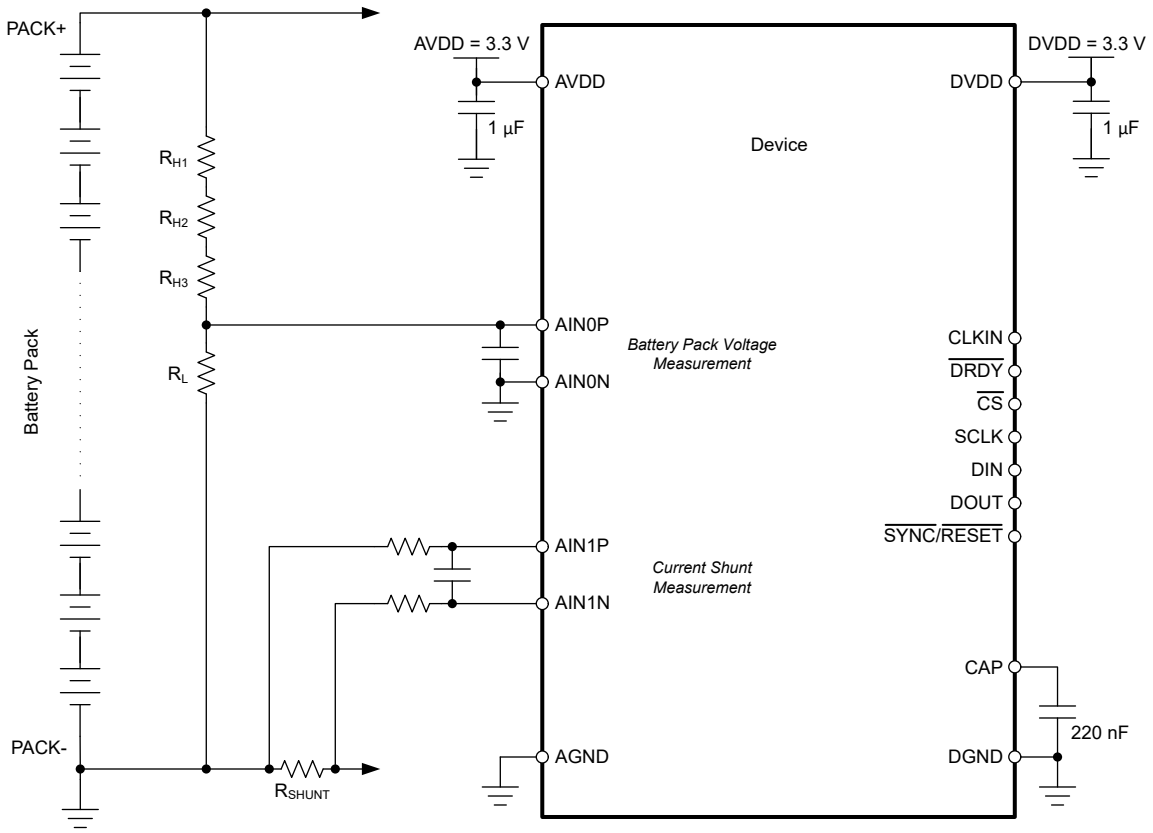

Figure 9-4. ADS131M04-Q1 in a Typical Battery Management System Application

9.2.1 Design Requirements

Table 9-2. Design Requirements

DESIGN PARAMETER	VALUE
Current Measurement	
Current measurement range	±5 kA
Current shunt value	35 µΩ
Update rate	1 ms
Battery-Pack Voltage Measurement	
Voltage measurement range	0 V to 800 V

9.2.2 Detailed Design Procedure

The following sections provide guidelines for selecting the external components and the configuration of the ADS131M04-Q1 for the various measurements in this application example.

9.2.2.1 Current Shunt Measurement

In a typical BMS, the current through the shunt resistor must be measured in both directions for charging and discharging the battery pack. In an overcurrent or short-circuit condition, the current can be as high as I_{BAT_MAX} = ±5 kA in this example application. Therefore, the maximum voltage drop across the shunt is up to V_{SHUNT} = $R_{SHUNT} \times I_{BAT_MAX}$ = 35 µΩ × ±4 kA = ±140 mV.

To measure this shunt voltage, configure channel 1 of the ADS131M04-Q1 for gain = 8, which allows differential voltage measurements of $V_{IN1} = V_{AIN1P} - V_{AIN1N} = \pm V_{REF} / 8 = \pm 1.2\ V / 8 = \pm 150$ mV. The integrated charge pump in the device allows voltage measurements 1.3 V below AGND while using a unipolar analog power supply. This bipolar voltage measurement capability is important because one side of the shunt is connected to the same GND potential as the AGND pin of the ADS131M04-Q1, which means that the absolute voltage that the device must measure is up to 140 mV below AGND.

To enable fast overcurrent detection within 1 ms while providing high accuracy and resolution, operate the ADS131M04-Q1 at 4 kSPS (OSR = 1024, high-resolution mode) using global-chop mode. Global-chop mode enables measurements with minimal offset error over temperature and time. The conversion time using these settings is 0.754 ms according to Equation 9. The input-referred noise is approximately 2.70 $\mu V_{RMS} / \sqrt{2}$ = 1.91 μV_{RMS} following the explanations in the *Noise Measurements* section. Thus, currents as small as 1.91 μV_{RMS} / 35 µΩ = 55 mA can be resolved. The resolution can be further improved by averaging the conversion results over a longer period of time in the microcontroller that interfaces with the ADS131M04-Q1.

9.2.2.2 Battery Pack Voltage Measurement

The 800-V battery-pack voltage is divided down to the voltage range of the ADS131M04-Q1 using a high-voltage resistor divider (R_{H1}, R_{H2}, R_{H3}, and R_L). Gain = 1 is used for channel 0 in this case to allow differential voltage measurements of $V_{IN0} = V_{AIN0P} - V_{AIN0N} = \pm 1.2$ V. The battery-pack voltage measurement is a unipolar, single-ended measurement. Thus, only the voltage range from 0 V to 1.2 V of the ADS131M04-Q1 is used. Equation 11 calculates the resistor divider ratio.

$$V_{IN} / V_{BAT_MAX} = 1.2\ V / 800\ V = R_L / (R_L + R_{H1} + R_{H2} + R_{H3}) \quad (11)$$

The leakage current drawn by the resistor divider must be less than 100 µA in this example to avoid unnecessarily draining the battery. The resistance of the divider must therefore be larger than $R_{TOTAL} \geq V_{BAT_MAX} / I_{LEAKAGE}$ = 800 V / 100 µA = 8 MΩ. The resistor values are chosen as $R_{H1} = R_{H2} = R_{H3}$ = 2.8 MΩ and R_L = 12.4 kΩ. Thus, the maximum voltage across R_L is 1.18 V at V_{BAT_MAX} = 800 V, leaving some headroom to the maximum input voltage of 1.2 V of the ADS131M04-Q1.

The maximum resistance of a single resistor that can be used in an automotive circuit design is often limited to a certain value. Also, the maximum voltage a single resistor can withstand is limited. These reasons are why the high-side resistor of the divider is split into multiple resistors (R_{H1}, R_{H2}, and R_{H3}). Another reason is that in case a single resistor has a short-circuit fault, the remaining resistors still limit the current into the ADS131M04-Q1 analog input pin (AIN0P) to safe levels.

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9.2.3 Application Curve

Figure 9-5 shows the gain error of the current measurement (ADC channel 1) over temperature excluding the error of the shunt. The gain error is calibrated at 25°C.

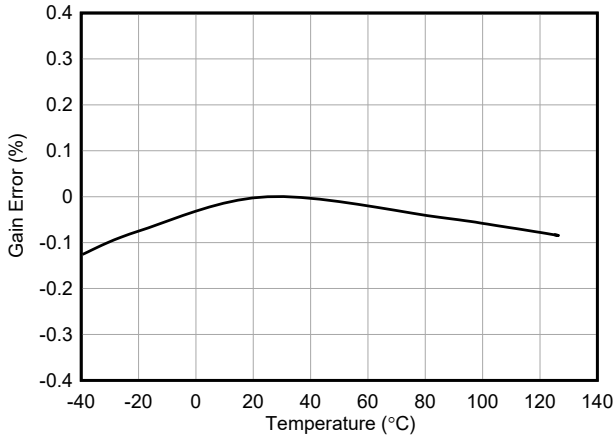

Figure 9-5. Gain Error vs Temperature

9.3 Power Supply Recommendations

9.3.1 CAP Pin Behavior

The ADS131M04-Q1 core digital voltage of 1.8 V is created from an internal LDO from DVDD. The CAP pin outputs the LDO voltage created from the DVDD supply and requires an external bypass capacitor. When operating from DVDD > 2.7 V, place a 220-nF capacitor on the CAP pin to DGND. If DVDD ≤ 2 V, tie the CAP pin directly to the DVDD pin and decouple the star-connected pins using a 100-nF capacitor to DGND.

9.3.2 Power-Supply Sequencing

The power supplies can be sequenced in any order but the analog and digital inputs must never exceed the respective analog or digital power-supply voltage limits.

9.3.3 Power-Supply Decoupling

Good power-supply decoupling is important to achieve optimum performance. AVDD and DVDD must each be decoupled with a 1-µF capacitor. Place the bypass capacitors as close to the power-supply pins of the device as possible with low-impedance connections. Using multilayer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics are recommended for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins can offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes. The analog and digital ground are recommended to be connected together as close to the device as possible.

9.4 Layout

9.4.1 Layout Guidelines

For best performance, dedicate an entire PCB layer to a ground plane and do not route any other signal traces on this layer. However, depending on restrictions imposed by specific end equipment, a dedicated ground plane may not be practical. If ground plane separation is necessary, make a direct connection of the planes at the ADC. Do not connect individual ground planes at multiple locations because this configuration creates ground loops.

Route digital traces away from all analog inputs and associated components in order to minimize interference.

Use C0G capacitors on the analog inputs. Use ceramic capacitors (for example, X7R grade) for the power-supply decoupling capacitors. High-K capacitors (Y5V) are not recommended. Place the required capacitors as close as possible to the device pins using short, direct traces. For optimum performance, use low-impedance connections on the ground-side connections of the bypass capacitors.

When applying an external clock, be sure the clock is free of overshoot and glitches. A source-termination resistor placed at the clock buffer often helps reduce overshoot. Glitches present on the clock input can lead to noise within the conversion data.

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9.4.2 Layout Example

Figure 9-6 shows an example layout of the ADS131M04-Q1 requiring a minimum of two PCB layers. In general, analog signals and planes are partitioned to the left and digital signals and planes to the right.

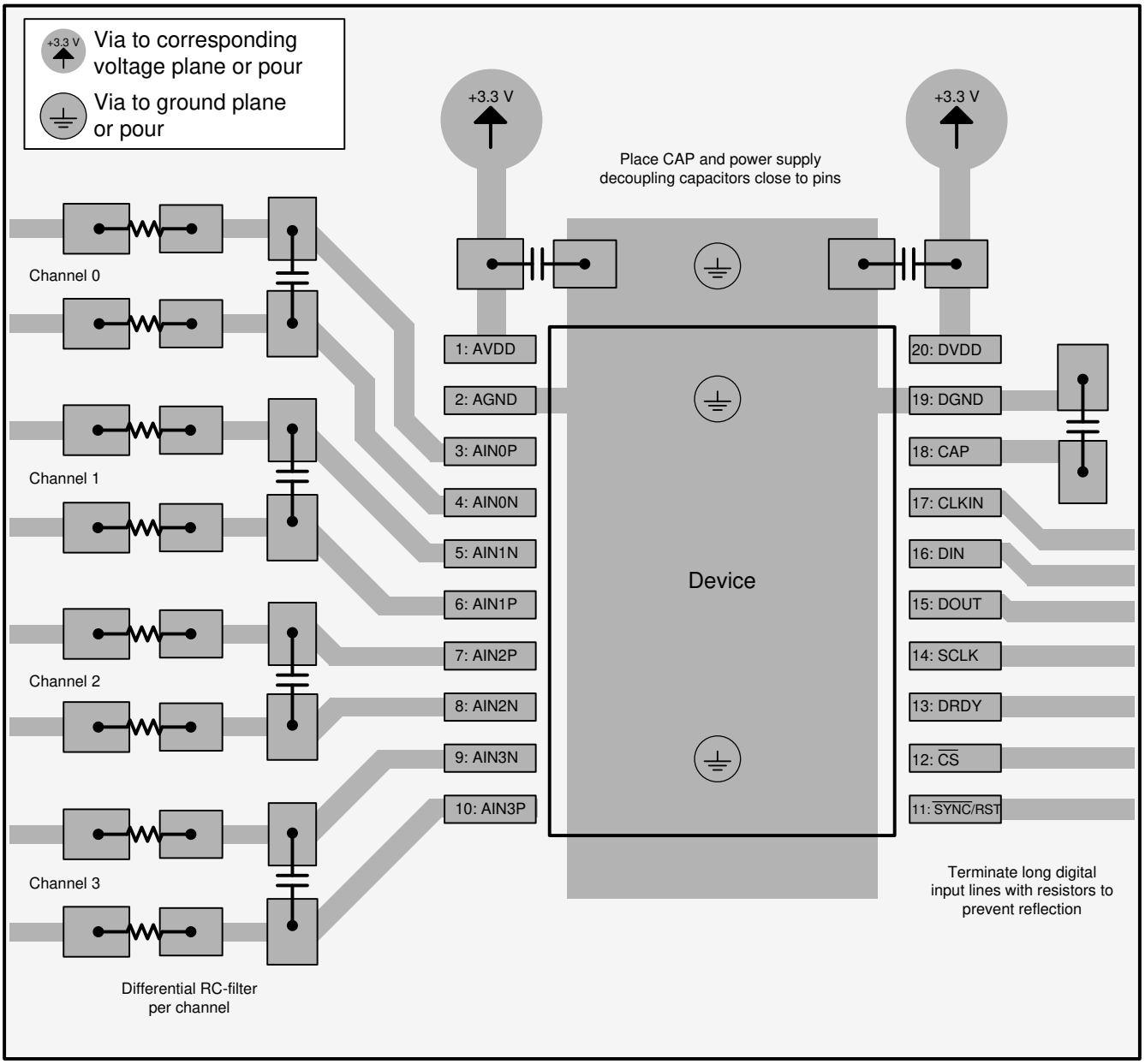

Figure 9-6. Layout Example

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *REF50xx Low-Noise, Very Low Drift, Precision Voltage Reference* data sheet

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS131M04QPWRQ1	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	A131M04Q
ADS131M04QPWRQ1.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	A131M04Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF ADS131M04-Q1 :

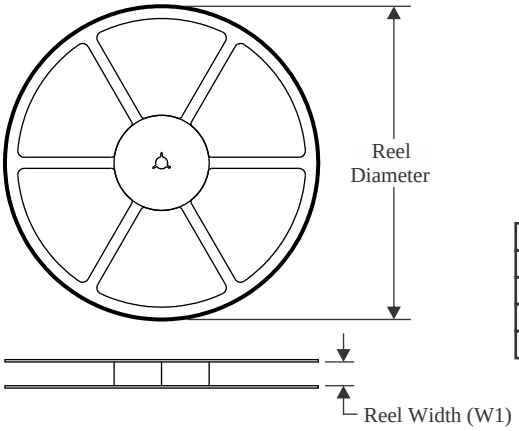
- Catalog : ADS131M04

NOTE: Qualified Version Definitions:

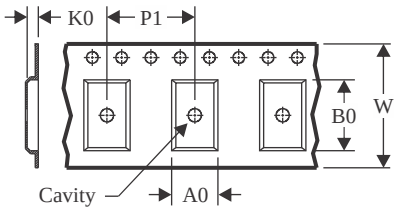
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

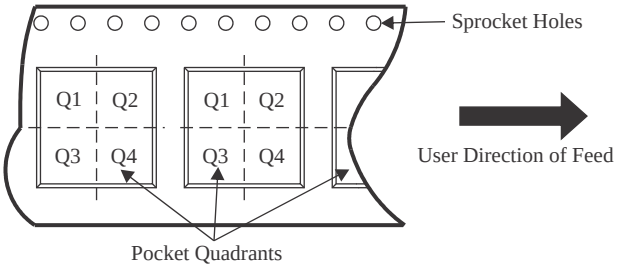


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

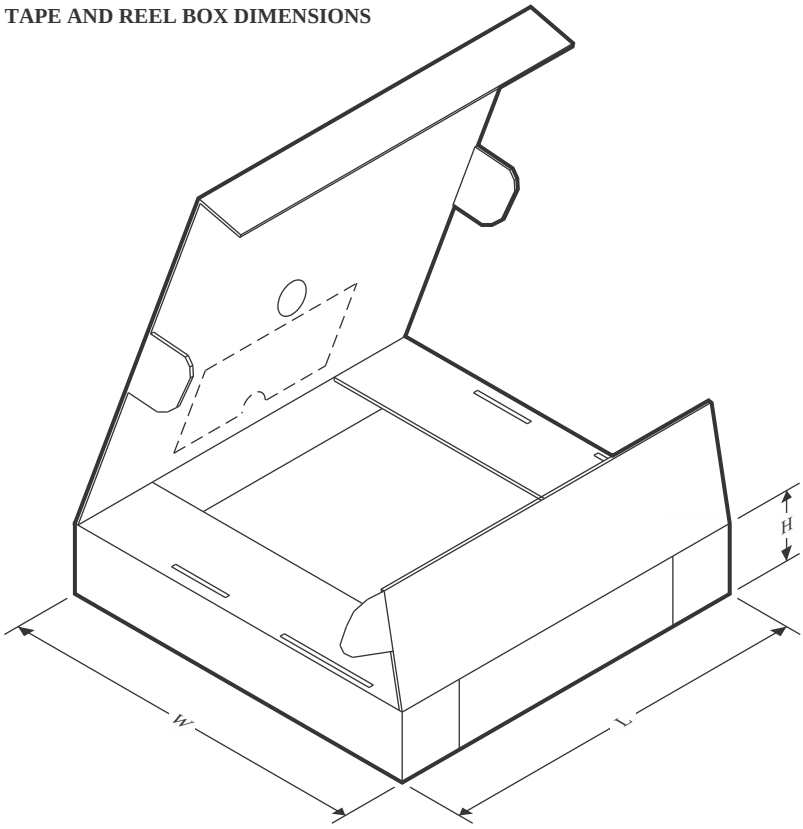
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

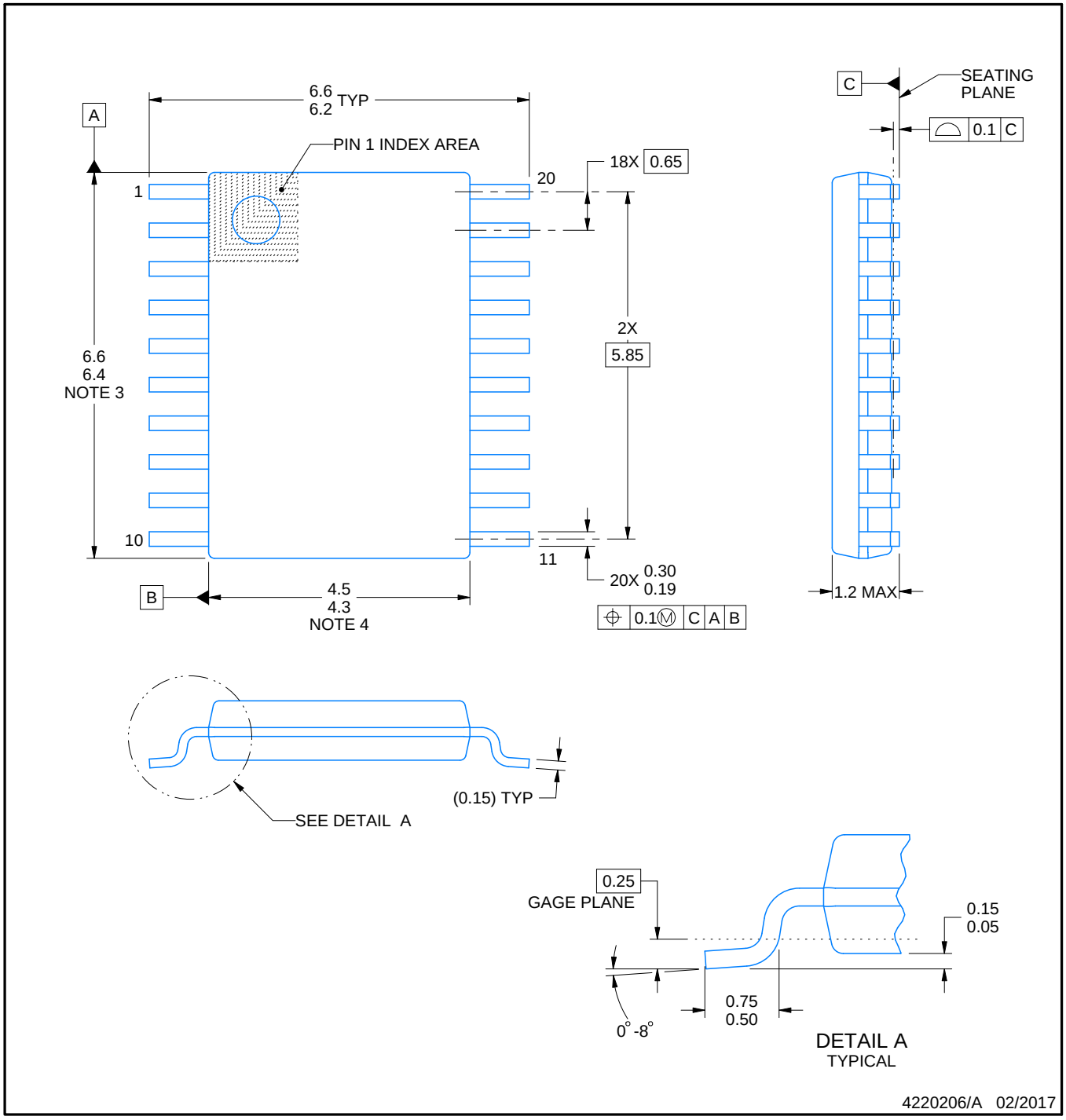
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS131M04QPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



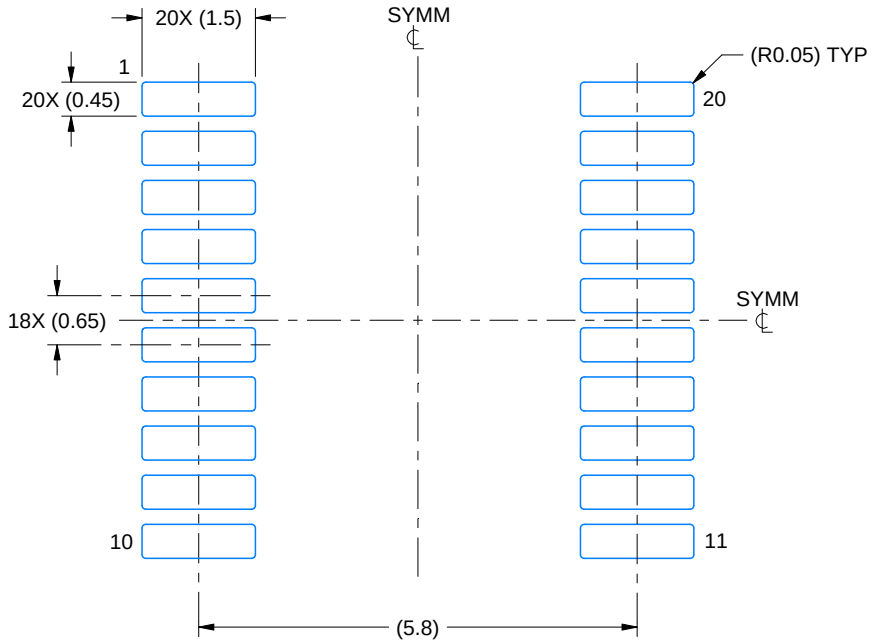
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS131M04QPWRQ1	TSSOP	PW	20	2000	356.0	356.0	35.0



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK DEFINED (PREFERRED)

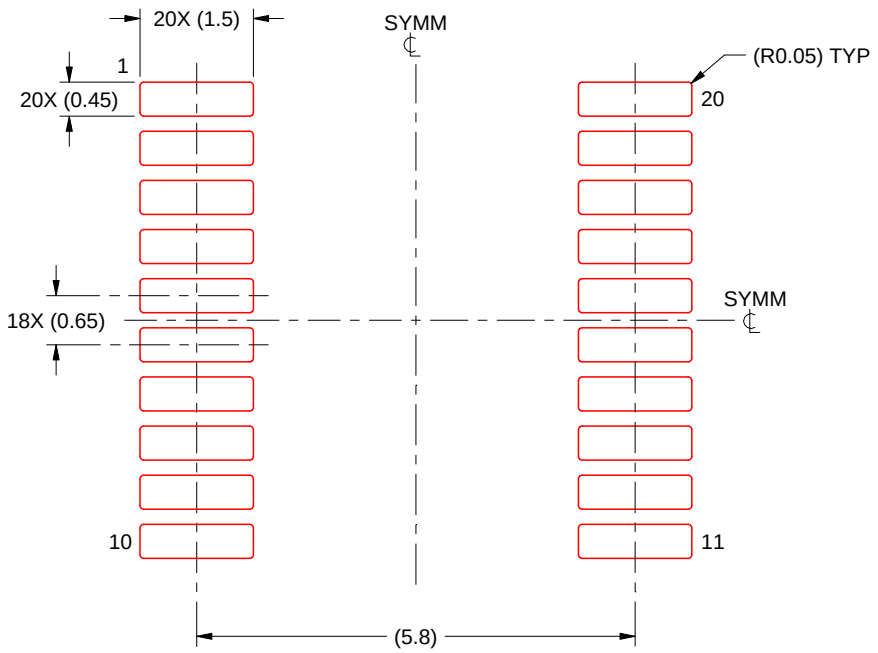
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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