

SCANSTA476 Eight Input IEEE 1149.1 Analog Voltage Monitor

Check for Samples: [SCANSTA476](#)

FEATURES

- Eight Selectable Analog Input Channels
- Analog Full-Scale Input Range 0V to V_{DD}
- Typical Accuracy of 2 mV at Maximum V_{DD}
- Very Low Power Operation
- Small Package Footprint in 16-Lead, 5 x 5 x 0.8 mm WSON
- Single +2.7V to +5.5V Supply Operation
- IEEE 1149.1 (JTAG) Compliant Interface

APPLICATIONS

- Measurement of Point Voltages
- Real-time Signal Monitoring
- System Health Monitoring and Prognostics
- Debug, Environmental Test, Production Test, Field Service
- Supplement In-Circuit Tester (ICT) Access
- Vital in Servers, Computing, Telecommunication and Industrial Equipment
- Essential in Medical, Data Storage, and Networking Equipment

DESCRIPTION

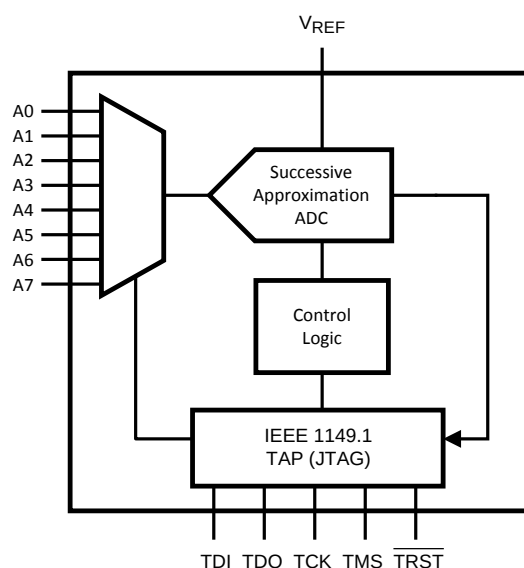
The SCANSTA476 is a low power, Analog Voltage Monitor used for sampling or monitoring up to 8 analog/mixed-signal input channels. Analog Voltage Monitors are valuable during product development, environmental test, production, and field service for verifying and monitoring power supply and reference voltages. In a supervisory role, the 'STA476 is useful for card or system-level health monitoring and prognostics applications.

Instead of requiring an external microcontroller with a GPIO interface, the 'STA476 features a common IEEE 1149.1 (JTAG) interface to select the analog input, initiate a measurement, and access the results - further extending the capabilities of an existing JTAG infrastructure.

The SCANSTA476 uses the V_{REF} input as a reference. This enables the SCANSTA476 to operate with a full-scale input range of 0 to V_{DD} , which can range from +2.7V to +5.5V.

The SCANSTA476 is packaged in a 16-lead non-pullback WSON package that provides an extremely small footprint for applications where space is a critical consideration. This product operates over the industrial temperature range of -40°C to $+85^{\circ}\text{C}$.

Block Diagram



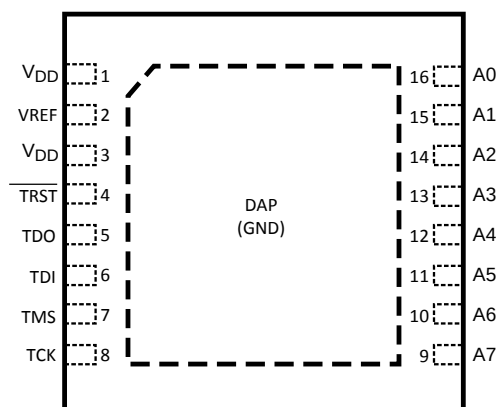
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Connection Diagram



**Figure 1. DAP = GND
(Top View)**

Pin Descriptions

Pin No.	Symbol	Description
ANALOG I/O		
16	A0	Analog input 0. This signal can range from 0V to V _{REF} .
15	A1	Analog input 1. This signal can range from 0V to V _{REF} .
14	A2	Analog input 2. This signal can range from 0V to V _{REF} .
13	A3	Analog input 3. This signal can range from 0V to V _{REF} .
12	A4	Analog input 4. This signal can range from 0V to V _{REF} .
11	A5	Analog input 5. This signal can range from 0V to V _{REF} .
10	A6	Analog input 6. This signal can range from 0V to V _{REF} .
9	A7	Analog input 7. This signal can range from 0V to V _{REF} .
2	V _{REF}	Analog reference voltage input. V _{REF} must be ≤ V _{DD} . This pin should be connected to a quiet source (not directly to V _{DD}) and bypassed to GND with 0.1 μF and 1 μF monolithic capacitors located within 1 cm of the V _{REF} pin.
DIGITAL I/O		
6	TDI	Test Data Input to support IEEE 1149.1 features
5	TDO	Test Data Output to support IEEE 1149.1 features
7	TMS	Test Mode Select to support IEEE 1149.1 features
8	TCK	Test Clock to support IEEE 1149.1 features
4	TRST	Test Reset to support IEEE 1149.1 features
POWER SUPPLY		
1,3	V _{DD}	Positive supply pin. These pins should be connected to a quiet +2.7V to +5.5V source and bypassed to GND with 0.1 μF and 1 μF monolithic capacitors located within 1 cm of the power pin.
See ⁽¹⁾	GND	Ground reference for CMOS circuitry. DAP is the exposed metal contact at the bottom of the WSON package. The DAP is used as the primary GND connection to the device. It should be connected to the ground plane with at least 4 vias for optimal low-noise and thermal performance.

(1) Note that GND is not an actual pin on the package, the GND is connected thru the DAP on the back side of the WSON package.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings ⁽¹⁾⁽²⁾

Supply Voltage V_{DD}		-0.3V to +6.5V
Voltage on Any Analog Pin to GND		-0.3V to $V_{DD}+0.3V$
Voltage on Any Digital Pin to GND		-0.3V to $V_{DD}+0.3V$
Input Current at Any Pin ⁽³⁾		±10 mA
ESD Susceptibility	Human Body Model	8000V
	Machine Model	>250V
Soldering Temperature		Refer to AN-1187 (SNOA401)
Junction Temperature		+150°C
Storage Temperature		-65°C to +150°C
Thermal Resistance, θ_{JA}		42°C/W
Thermal Resistance, θ_{JC}		14.3°C/W

- (1) Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not implied. Exposure to maximum ratings for extended periods may affect device reliability.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
- (3) Except power supply pins.

Recommended Operating Conditions

Operating Temperature Range	-40°C ≤ T_A ≤ +85°C
V_{DD} Supply Voltage	+2.7V to +5.5V
Digital Input Pins Voltage Range	+0V to V_{DD}
Analog Input Pins Voltage Range ⁽¹⁾	+0V to V_{REF}

- (1) For valid measurements, the analog $V_{IN} < V_{REF} \leq V_{DD}$.

SCANSTA476 Electrical Characteristics

The following specifications apply for $V_{DD} = +2.7V$ to 5.5V, $f_{TCK} = 20$ MHz, unless otherwise noted.

Symbol	Parameter	Conditions	Typical	Limits	Units
POWER SUPPLY CHARACTERISTICS					
V _{DD}	Supply Voltage	-40°C ≤ T _A ≤ 85°C		2.7	V (min)
				5.5	V (max)
I _{DD}	Normal Mode (Static)	V _{DD} = +2.7V to +5.5V,	3.5	5.0	mA
	Normal Mode (Operational)	V _{DD} = +2.7V to +5.5V, f _{TCK} = 1 MSPS		5.0	mA (max)
P _D	Power Consumption, Normal Mode (Operational)	V _{DD} = +5.5V, f _{TCK} = 1 MSPS		27.5	mW (max)
ANALOG INPUT CHARACTERISTICS (A0-A7)					
V _{IN}	Analog Input Range	V _{REF} ≤ V _{DD}		0 to V _{REF}	V
V _{REF}	Reference Voltage Range			V _{DD}	V
I _{DCL}	DC Leakage Current		0.1	±10	μA (max)
V _{MEAS}	Analog Input Measurement Accuracy	V _{DD} = +2.7V	1	7.5	mV
		V _{DD} = +5.5V	2	15	
DIGITAL INPUT CHARACTERISTICS (TDI, TMS, TCK, $\overline{\text{TRST}}$)					
V _{IH}	Input High Voltage	V _{DD} = +2.7V to +3.6V		2.0	V (min)
		V _{DD} = +5.5V		2.1	
V _{IL}	Input Low Voltage	V _{DD} = +5V		0.8	V (max)
V _{CL}	Input Clamp Voltage	I _{CL} = -18mA	-0.8	-1.5	V (max)
I _{IN}	Input Current	V _{IN} = 0V or V _{DD}	0.2	±10	μA (max)

SCANSTA476 Electrical Characteristics (continued)

The following specifications apply for $V_{DD} = +2.7V$ to $5.5V$, $f_{TCK} = 20$ MHz, unless otherwise noted.

Symbol	Parameter	Conditions	Typical	Limits	Units
I _{ILR}	Input Current	$\overline{TRST}$, TDI, TMS only		-300	μA (max)
DIGITAL OUTPUT CHARACTERISTICS (TDO)					
V _{OH}	Output High Voltage	I _{OH} = -100 μA, 2.7V ≤ V _{DD} ≤ 5.5V		V _{DD} -0.2	V (min)
		I _{OH} = -4 mA, 3.0V ≤ V _{DD} ≤ 5.5V		2.4	V (min)
		I _{OH} = -4 mA, V _{DD} = 2.7V		2.2	V (min)
V _{OL}	Output Low Voltage	I _{OL} = 100 μA, 2.7V ≤ V _{DD} ≤ 5.5V		0.2	V (max)
		I _{OL} = 4 mA, 2.7V ≤ V _{DD} ≤ 5.5V		0.4	V (max)
I _{OS}	Output Short Circuit Current	V _{OUT} = 0V, V _{DD} = 5.5V		-85	mA (max)
I _{OZ}	TRI-STATE Leakage Current			±10	μA (max)
	Output Coding		Straight (Natural) Binary		
AC ELECTRICAL CHARACTERISTICS					
F _{MAX}	Throughput Rate	TCK = 20MHz		1	MSPS (max)
INPUT TIMING CHARACTERISTICS					
t _{SET}	TDI to TCK (H/L)	See ⁽¹⁾		2.0	ns (min)
t _{HOLD}	TDI to TCK (H/L)	See ⁽¹⁾		1.5	ns (min)
t _{SET}	TMS to TCK (H/L)	See ⁽¹⁾		2.0	ns (min)
t _{HOLD}	TMS to TCK (H/L)	See ⁽¹⁾		2.0	ns (min)
t _W	TCK Pulse Width (H/L)	See ⁽¹⁾		10.0	ns (min)
t _{REC}	Recovery Time $\overline{TRST}$ to TCK	See ⁽¹⁾		2.0	ns (min)
t _W	TRST Pulse Width (L)	See ⁽¹⁾		2.5	ns (min)
F _{MAX}	TCK			20	MHz (min)

(1) Data sheet min/max specification limits are specified by design or statistical analysis.

APPLICATIONS INFORMATION

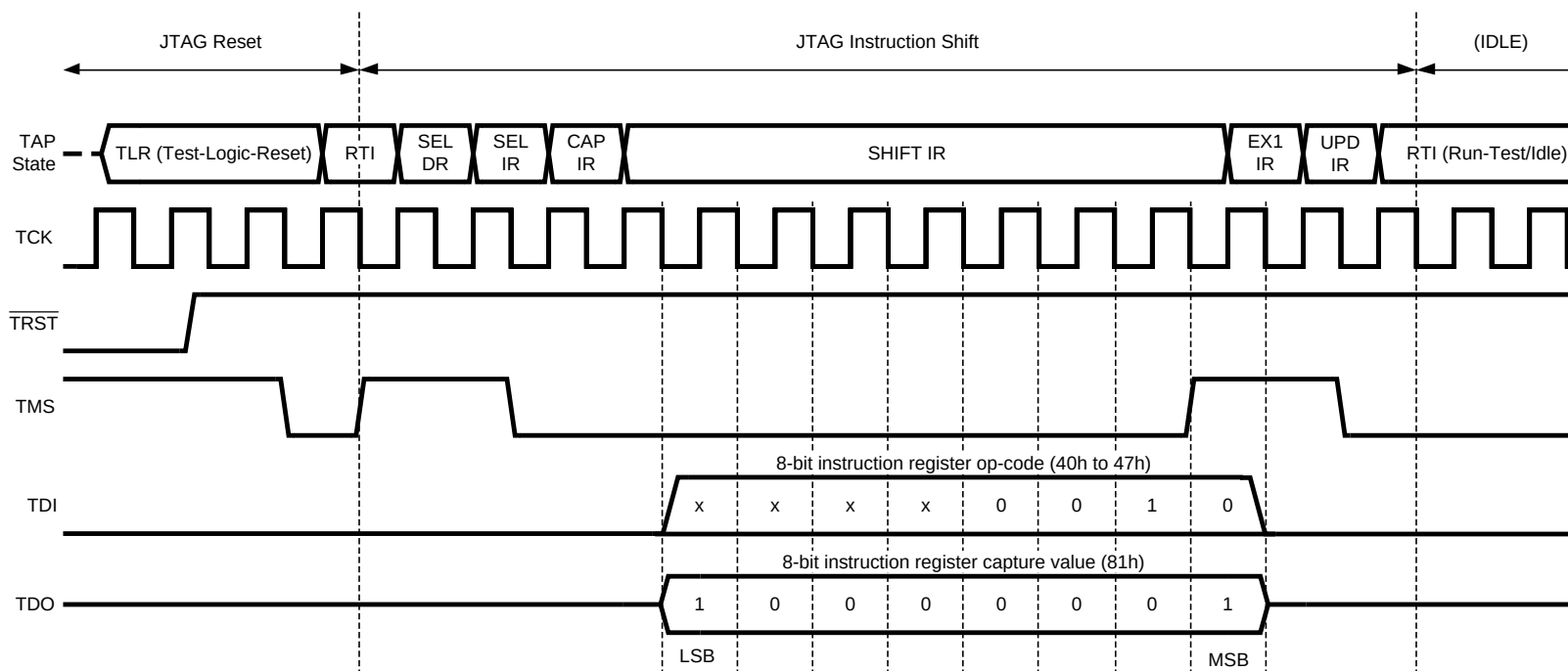
POWER-UP TIMING

The SCANSTA476 typically requires 1 μs to power up, either after first applying V_{DD} , or after an incomplete conversion shift. To return to normal, one "dummy" conversion must be fully completed. After this first dummy conversion, the SCANSTA476 will perform conversions properly.

STARTUP MODE

When the V_{DD} supply is first applied, the SCANSTA476 requires one dummy conversion after start-up.

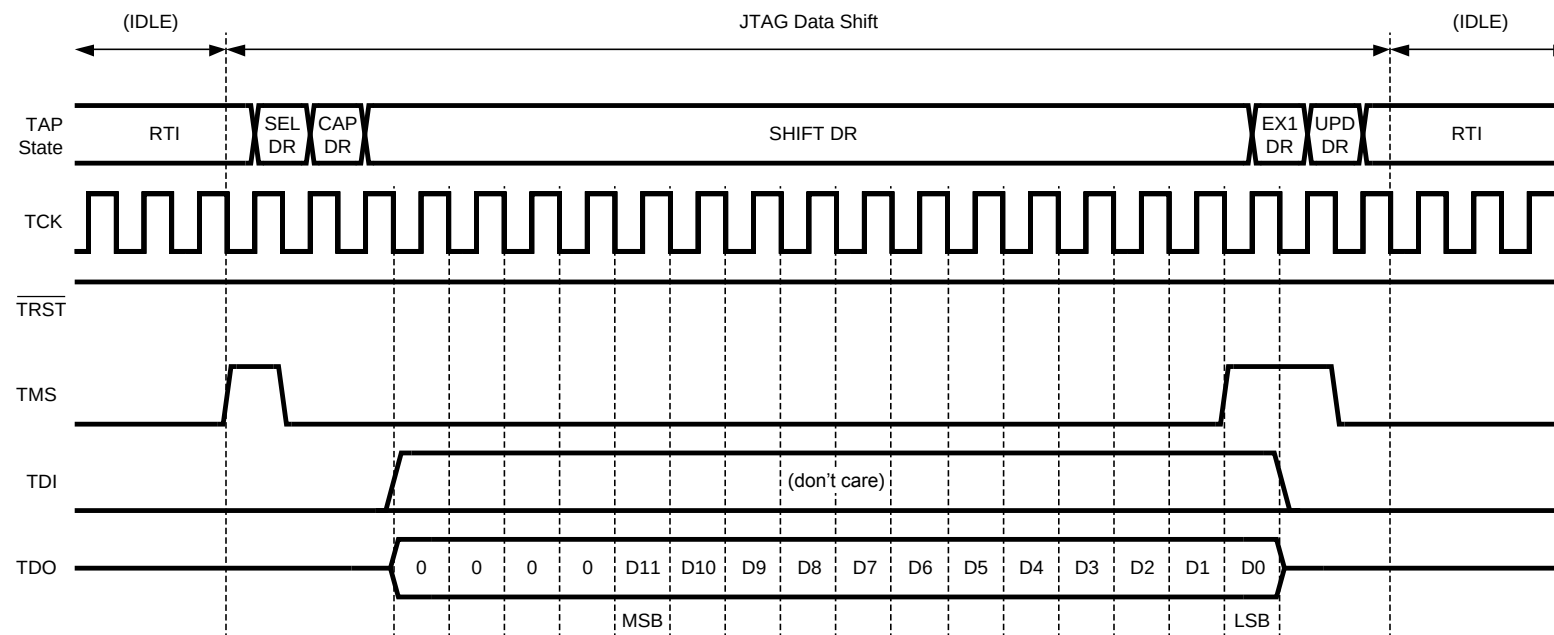
Timing Diagrams



Op-codes 40h to 47h select pins A0 to A7 respectively.

Note the JTAG reset preamble places the JTAG TAP controller in a stable state (RTI). Both the instruction and data shifts start in - and return to - the RTI state

Figure 2. Instruction Shift (Channel Select)



D11 through D0 correspond to the 12-bit sample from the ADC Core.

Note that Data shifts can be run back-to-back for continuous sampling of a single channel, or can be interleaved with instruction shifts for rippling through all 8 channels.

Figure 3. Data Shift (A/D Sample)

REVISION HISTORY

Changes from Revision F (April 2013) to Revision G

Page

- Changed layout of National Data Sheet to TI format [6](#)

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SCANSTA476TSD/NOPB	Active	Production	WSON (NHQ) 16	1000 SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	STA476T
SCANSTA476TSD/NOPB.A	Active	Production	WSON (NHQ) 16	1000 SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	STA476T

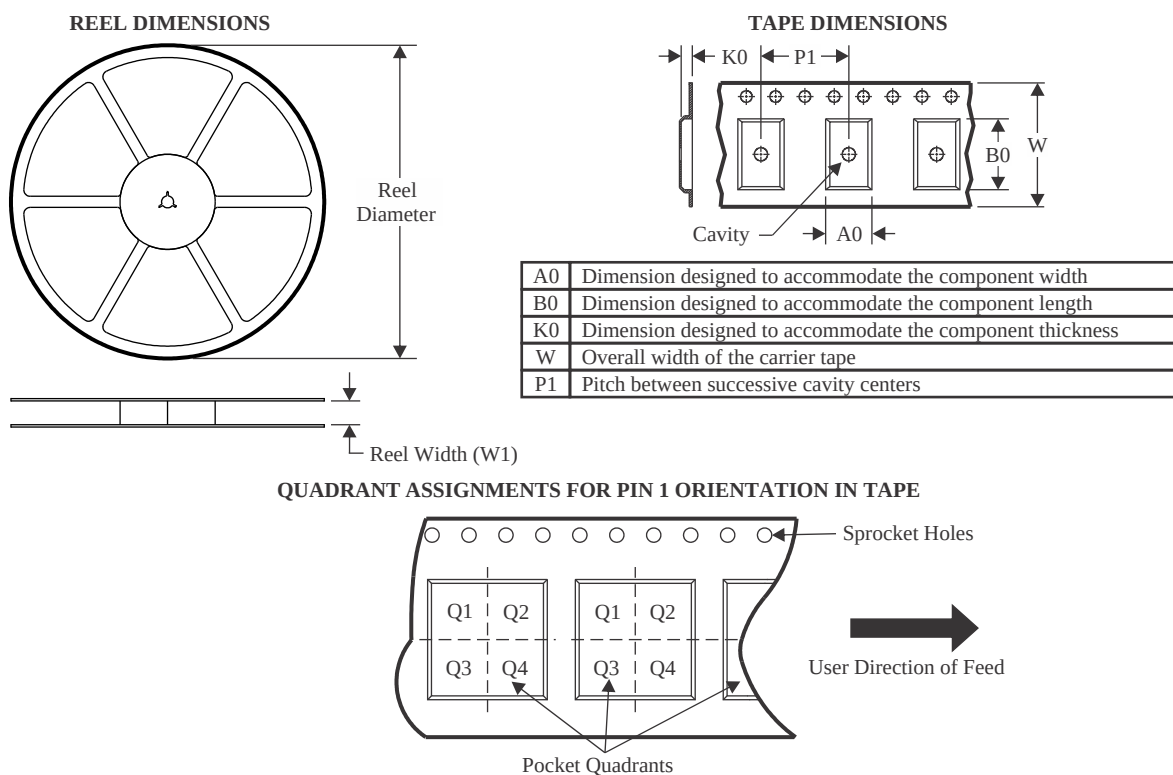
- ⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).
- ⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- ⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- ⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- ⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- ⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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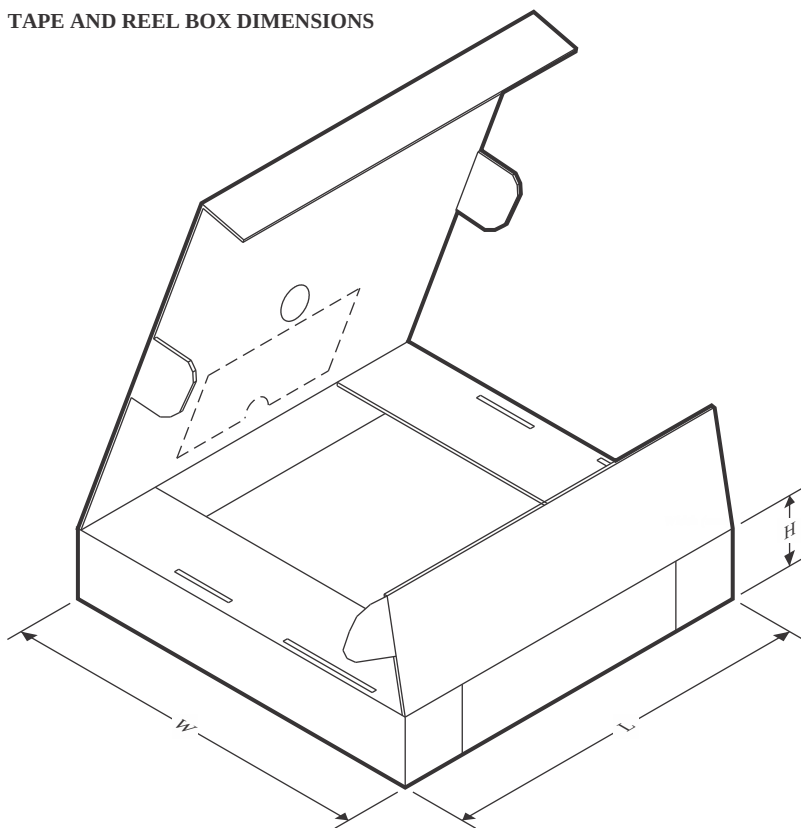
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SCANSTA476TSD/NOPB	WSO	NHQ	16	1000	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SCANSTA476TSD/NOPB	WSON	NHQ	16	1000	208.0	191.0	35.0



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