# 4.5V to 23V Input, 3-A Synchronous Step-Down SWIFT™ Converter with Eco-Mode™

**Check for Samples: TPS54339E**

## FEATURES

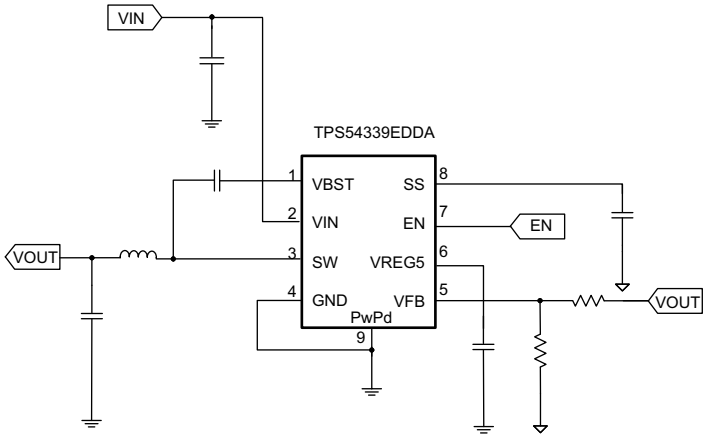
- **D-CAP2™ Mode Enables Fast Transient Response**
- **Low Output Ripple and Allows Ceramic Output Capacitor**
- **Wide $V_{IN}$ Input Voltage Range: 4.5 V to 23 V**
- **Output Voltage Range: 0.76 V to 7.0 V**
- **Highly Efficient Integrated FETs Optimized for Lower Duty Cycle Applications**
  **– 140 mΩ (High Side) and 70 mΩ (Low Side)**
- **High Efficiency, less than 10 µA at shutdown**
- **High Initial Bandgap Reference Accuracy**
- **Adjustable Soft Start**
- **Pre-Biased Soft Start**
- **600-kHz Switching Frequency ($f_{SW}$)**
- **Cycle By Cycle Over Current Limit**
- **Auto-Skip Eco-mode™ for High Efficiency at Light Load**

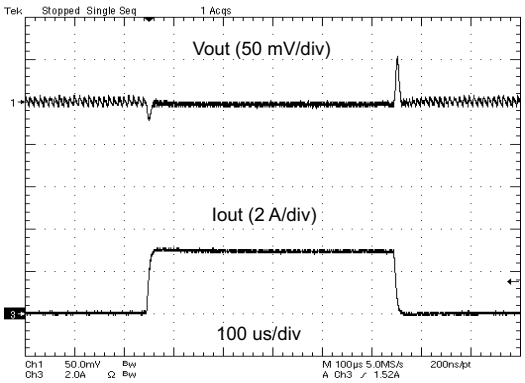
## APPLICATIONS

- **Wide Range of Applications for Low Voltage System**
  - **Digital TV Power Supply**
  - **High Definition Blu-ray Disc™ Players**
  - **Networking Home Terminal**
  - **Digital Set Top Box (STB)**

## DESCRIPTION

The TPS54339E is an adaptive on-time D-CAP2™ mode synchronous buck converter. The TPS54339E enables system designers to complete the suite of various end-equipment power bus regulators with a cost effective, low component count, low standby current solution. The main control loop for the TPS54339E uses the D-CAP2™ mode control that provides a fast transient response with no external compensation components. The adaptive on-time control supports seamless transition between PWM mode at higher load conditions and Eco-mode™ operation at light loads. Eco-mode™ allows the TPS54339E to maintain high efficiency during lighter load conditions. The TPS54339E also has a proprietary circuit that enables the device to adopt to both low equivalent series resistance (ESR) output capacitors, such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors. The device operates from 4.5-V to 18-V VIN input. The output voltage can be programmed between 0.76 V and 7 V. The device also features an adjustable soft start time. The TPS54339E is available in the 8-pin DDA package, and designed to operate from –40°C to 85°C.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION(1)

| $T_A$ | PACKAGE(2) (3) | ORDERABLE PART NUMBER | PIN | TRANSPORT MEDIA |
|---|---|---|---|---|
| –40°C to 85°C | DDA | TPS54339EDDA | 8 | Tube |
| | | TPS54339EDDAR | | Tape and Reel |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) All package options have Cu NIPDAU lead/ball finish.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

| | | VALUE | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| Input voltage range | VIN, EN | –0.3 | 25 | V |
| | VBST | –0.3 | 31 | |
| | VBST (10 ns transient) | –0.3 | 33 | |
| | VBST (vs SW) | –0.3 | 6.5 | |
| | VFB, SS | –0.3 | 6.5 | |
| | SW | –2 | 25 | |
| | SW (10 ns transient) | –3 | 27 | |
| Output voltage range | VREG5 | –0.3 | 6.5 | V |
| | GND | –0.3 | 0.3 | |
| Voltage from GND to thermal pad, $V_{diff}$ | | –0.2 | 0.2 | V |
| Electrostatic discharge | Human Body Model (HBM) | | 2 | kV |
| | Charged Device Model (CDM) | | 500 | V |
| Operating junction temperature, $T_J$ | | –40 | 150 | °C |
| Storage temperature, $T_{stg}$ | | –55 | 150 | |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## THERMAL INFORMATION

| THERMAL METRIC(1) | | TPS54339E DDA (8 PINS) | UNITS |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 46.2 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance | 53.9 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance | 29.7 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 10.0 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 29.6 | |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance | 6.6 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.


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## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range, (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Supply input voltage range | | 4.5 | 23 | V |
| $V_I$ | Input voltage range | VBST | –0.1 | 29 | V |
| | | VBST (10 ns transient) | –0.1 | 32 | |
| | | VBST(vs SW) | –0.1 | 5.7 | |
| | | SS | –0.1 | 5.7 | |
| | | EN | –0.1 | 23 | |
| | | VFB | –0.1 | 5.5 | |
| | | SW | –1.8 | 23 | |
| | | SW (10 ns transient) | –3 | 26 | |
| | | GND | –0.1 | 0.1 | |
| $V_O$ | Output voltage range | VREG5 | –0.1 | 5.7 | V |
| $I_O$ | Output Current range | $I_{VREG5}$ | 0 | 10 | mA |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |
| $T_J$ | Operating junction temperature | | –40 | 150 | °C |

## ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, $V_{IN}$ = 12 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | | |
| $I_{VIN}$ | Operating - non-switching supply current | $V_{IN}$ current, $T_A$ = 25°C, EN = 5V, $V_{FB}$ = 0.8V | | 600 | 1100 | µA |
| $I_{VINSDN}$ | Shutdown supply current | $V_{IN}$ current, $T_A$ = 25°C, EN = 0 V | | 3.0 | 10 | µA |
| **LOGIC THRESHOLD** | | | | | | |
| $V_{ENH}$ | EN high-level input voltage | EN | 1.6 | | | V |
| $V_{ENL}$ | EN low-level input voltage | EN | | | 0.6 | V |
| $R_{EN}$ | EN pin resistance to GND | $V_{EN}$ = 12 V | 200 | 400 | 800 | kΩ |
| **$V_{FB}$ VOLTAGE AND DISCHARGE RESISTANCE** | | | | | | |
| $V_{FBTH}$ | $V_{FB}$ threshold voltage | $T_A$ = 25°C, $V_O$ = 1.05 V, $I_O$ = 10 mA, Eco-mode™ operation | | 772 | | mV |
| | | $T_A$ = 25°C, $V_O$ = 1.05 V, continuous mode operation | 749 | 765 | 781 | mV |
| $I_{VFB}$ | $V_{FB}$ input current | $V_{FB}$ = 0.8 V, $T_A$ = 25°C | | 0 | ±0.1 | µA |
| **$V_{REG5}$ OUTPUT** | | | | | | |
| $V_{VREG5}$ | $V_{REG5}$ output voltage | $T_A$ = 25°C, 6.0 V < $V_{IN}$ < 23 V, 0 < $I_{VREG5}$ < 5 mA | 5.2 | 5.5 | 5.7 | V |
| $I_{VREG5}$ | Output current | $V_{IN}$ = 6 V, $V_{REG5}$ = 4.0 V, $T_A$ = 25°C | 20 | | | mA |
| **MOSFET** | | | | | | |
| $R_{DS(on)h}$ | High side switch resistance | 25°C, $V_{BST}$ - SW = 5.5 V(1) | | 140 | | mΩ |
| $R_{DS(on)l}$ | Low side switch resistance | 25°C(1) | | 70 | | mΩ |
| **CURRENT LIMIT** | | | | | | |
| $I_{ocl}$ | Current limit | L out = 2.2 µH(1) | 3.5 | 4.1 | 5.7 | A |
| **THERMAL SHUTDOWN** | | | | | | |
| $T_{SDN}$ | Thermal shutdown threshold | Shutdown temperature (1) | | 165 | | °C |
| | | Hysteresis (1) | | 40 | | |
| **ON-TIME TIMER CONTROL** | | | | | | |
| $t_{ON}$ | On time | $V_{IN}$ = 12 V, $V_O$ = 1.05 V | | 160 | | ns |
| $t_{OFF(MIN)}$ | Minimum off time | $T_A$ = 25°C, $V_{FB}$ = 0.7 V(1) | | 260 | 310 | ns |

(1) Not production tested.

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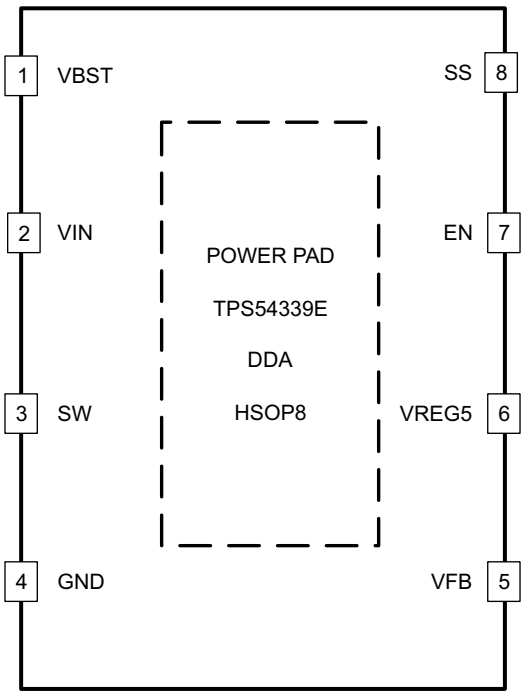
## ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, $V_{IN}$ = 12 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SOFT START** | | | | | | |
| $I_{SSC}$ | SS charge current | $V_{SS}$ = 1.0 V | 4.2 | 6.0 | 7.8 | µA |
| $I_{SSD}$ | SS discharge current | $V_{SS}$ = 0.5 V | 0.8 | 1.5 | | mA |
| **HICCUP AND OVERVOLTAGE PROTECTION** | | | | | | |
| $V_{OVP}$ | Output OVP threshold | OVP Detect (L>H) | | 125% | | |
| $V_{UVP}$ | Output Hiccup threshold | Hiccup detect (H>L) | | 65% | | |
| $T_{UVPDEL}$ | Output Hiccup delay | to Hiccup state | | 6 | | µs |
| $T_{UVPEN}$ | Output Hiccup Enable delay | Relative to soft-start time | | x1.7 | | |
| **UVLO** | | | | | | |
| UVLO | UVLO threshold | Wake up $V_{REG5}$ voltage | 3.45 | 3.75 | 4.05 | V |
| | | Hysteresis $V_{REG5}$ voltage | 0.17 | 0.33 | 0.47 | |

## DEVICE INFORMATION

**DDA PACKAGE**
**(TOP VIEW)**




## PIN FUNCTIONS

| PIN | | DESCRIPTION |
|---|---|---|
| NAME | NO. | |
| VBST | 1 | Supply input for the high-side FET gate drive circuit. Connect 0.1µF capacitor between VBST and SW pins. An internal diode is connected between VREG5 and VBST. |
| VIN | 2 | Input voltage supply pin. |
| SW | 3 | Switch node connection between high-side NFET and low-side NFET. |
| GND | 4 | Ground pin. Power ground return for switching circuit. Connect sensitive SS and VFB returns to GND at a single point. |
| VFB | 5 | Converter feedback input. Connect to output voltage with feedback resistor divider. |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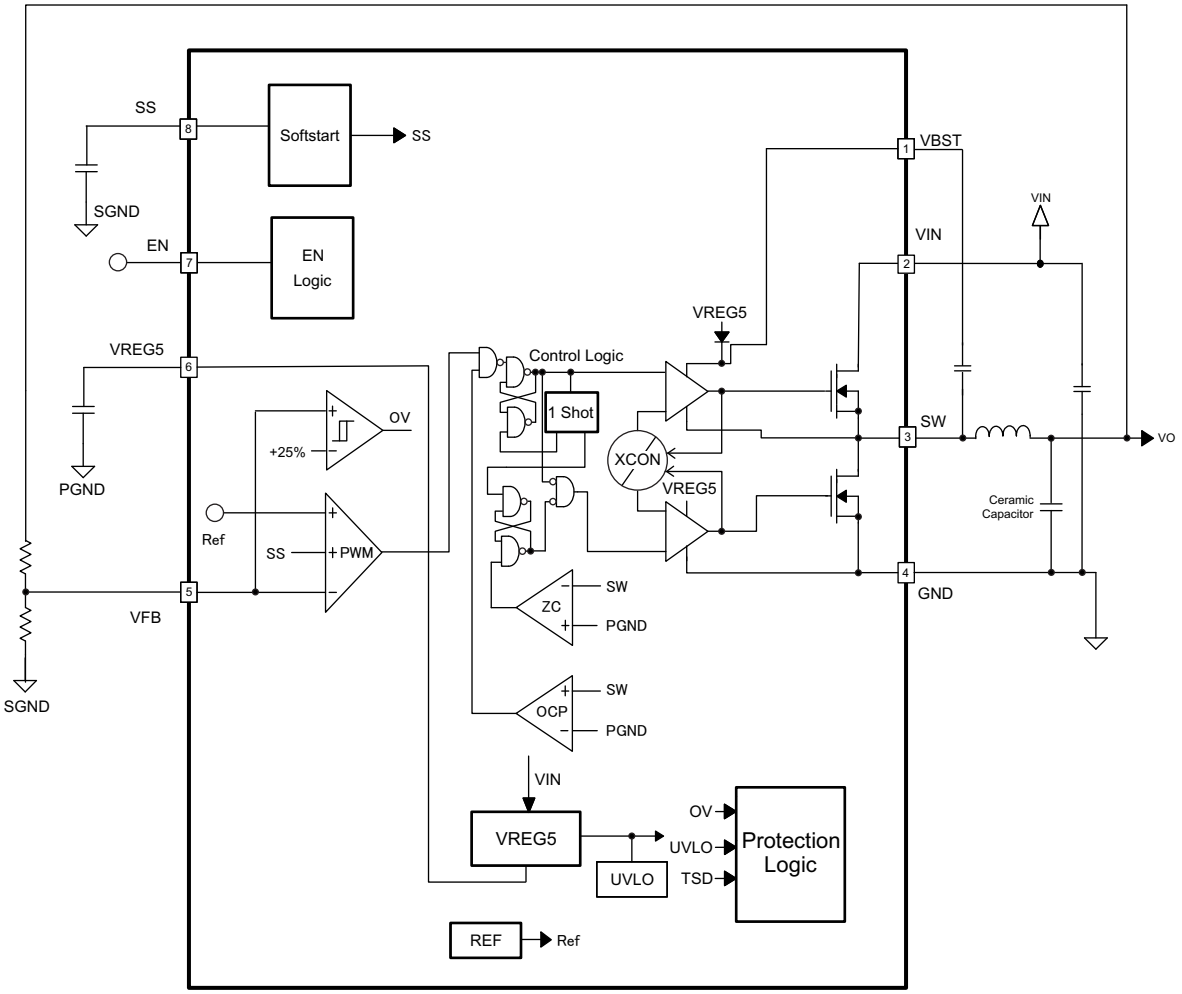
## PIN FUNCTIONS (continued)

| PIN | | DESCRIPTION |
|---|---|---|
| NAME | NO. | |
| VREG5 | 6 | 5.5 V power supply output. A capacitor (typical 0.47 µF) should be connected to GND. VREG5 is not active when EN is low. |
| EN | 7 | Enable input control. EN is active high and must be pulled up to enable the device. |
| SS | 8 | Soft-start control. An external capacitor should be connected to GND. |
| Exposed Thermal Pad | Back side | Thermal pad of the package. Must be soldered to achieve appropriate dissipation. Must be connected to GND. |

## FUNCTIONAL BLOCK DIAGRAM



## OVERVIEW

The TPS54339E is a 3-A synchronous step-down (buck) converter with two integrated N-channel MOSFETs. It operates using D-CAP2™ mode control. The fast transient response of D-CAP2™ control reduces the output capacitance required to meet a specific level of performance. Proprietary internal circuitry allows the use of low ESR output capacitors including ceramic and special polymer types.

## DETAILED DESCRIPTION

### PWM Operation

The main control loop of the TPS54339E is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2™ mode control. D-CAP2™ mode control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one shot timer expires. This one shot is set by the converter input voltage, VIN, and the output voltage, VO, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2™ mode control.

### PWM Frequency and Adaptive On-Time Control

TPS54339E uses an adaptive on-time control scheme and does not have a dedicated on board oscillator. The TPS54339E runs with a pseudo-constant frequency of 600 kHz by using the input voltage and output voltage to set the on-time one-shot timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage; therefore, when the duty ratio is VOUT/VIN, the frequency is constant.

### Auto-Skip Eco-Mode™ Control

The TPS54339E is designed with Auto-Skip Eco-mode™ to increase light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when its zero inductor current is detected. As the load current further decreases the converter run into discontinuous conduction mode. The on-time is kept almost the same as is was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. The transition point to the light load operation $I_{OUT(LL)}$ current can be calculated in Equation 1

$$I_{OUT(LL)} = \frac{1}{2 \cdot L \cdot fsw} \cdot \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{V_{IN}} \tag{1}$$

### Soft Start and Pre-Biased Soft Start

The soft start function is adjustable. When the EN pin becomes high, 6 µA current begins charging the capacitor which is connected from the SS pin to GND. Smooth control of the output voltage is maintained during start up. The equation for the slow start time is shown in Equation 2. VFB voltage is 0.765 V and SS pin source current is 6 µA.

$$t_{SS}(ms) = \frac{C_{SS}(nF) \text{ x } V_{REF} \times 1.1}{I_{SS}(\mu A)} = \frac{C_{SS}(nF) \text{ x } 0.765 \times 1.1}{6} \tag{2}$$

The TPS54339E contains a unique circuit to prevent current from being pulled from the output during startup if the output is pre-biased. When the soft-start commands a voltage higher than the pre-bias level (internal soft start becomes greater than feedback voltage $V_{FB}$), the controller slowly activates synchronous rectification by starting the first low side FET gate driver pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This scheme prevents the initial sinking of the pre-bias output, and ensure that the out voltage ($V_O$) starts and ramps up smoothly into regulation and the control loop is given time to transition from pre-biased start-up to normal mode operation.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### Current Protection

The output overcurrent protection (OCP) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored by measuring the low-side FET switch voltage between the SW pin and GND. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the high-side FET switch, the switch current increases at a linear rate determined by $V_{IN}$, $V_{OUT}$, the on-time and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current Iout. The TPS54339E constantly monitors the low-side FET switch voltage, which is proportional to the switch current, during the low-side on-time. If the measured voltage is above the voltage proportional to the current limit, an internal counter is incremented per each SW cycle and the converter maintains the low-side switch on until the measured voltage is below the voltage corresponding to the current limit at which time the switching cycle is terminated and a new switching cycle begins. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner. If the over current condition exists for 7 consecutive switching cycles, the internal OCL threshold is set to a lower level, reducing the available output current. When a switching cycle occurs where the switch current is not above the lower OCL threshold, the counter is reset and the OCL limit is returned to the higher value.

There are some important considerations for this type of over-current protection. The load current one half of the peak-to-peak inductor current higher than the over-current threshold. Also when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. This may cause the output voltage to fall. When the VFB voltage becomes lower than 65% of the target voltage, the UVP comparator detects it. After 6µs detecting the UVP voltage, device will shut down and re-start after 7 times SS period for Hiccup.

When the over current condition is removed, the output voltage returns to the regulated value. This protection is non-latching.

### Over Voltage Protection

TPS54339E detects over voltage conditions by monitoring the feedback voltage (VFB). This function is enabled after approximately 1.7 x times the soft start time.

When the feedback voltage becomes higher than 125% of the target voltage, the OVP comparator output goes high and both the high-side MOSFET driver and the low-side MOSFET driver turn off. This function is non-latch operation.

### UVLO Protection

Undervoltage lock out protection (UVLO) monitors the voltage of the $V_{REG5}$ pin. When the $V_{REG5}$ voltage is lower than UVLO threshold voltage, the TPS54339E is shut off. This protection is non-latching.

### Thermal Shutdown

TPS54339E monitors the temperature of itself. If the temperature exceeds the threshold value (typically 165°C), the device is shut off. This is non-latch protection.

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## TYPICAL CHARACTERISTICS

VIN = 12 V, $T_A$ = 25°C (unless otherwise noted).

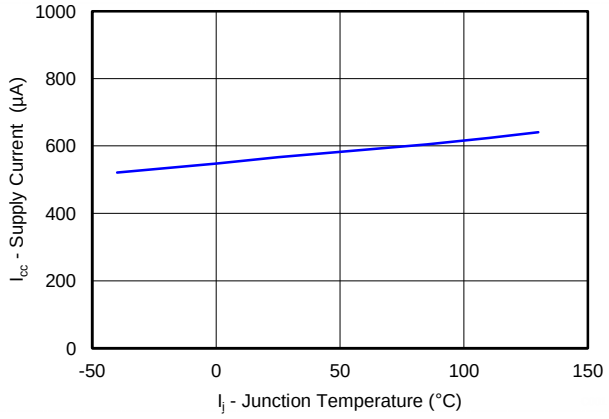


**Figure 1. VIN CURRENT vs JUNCTION TEMPERATURE**

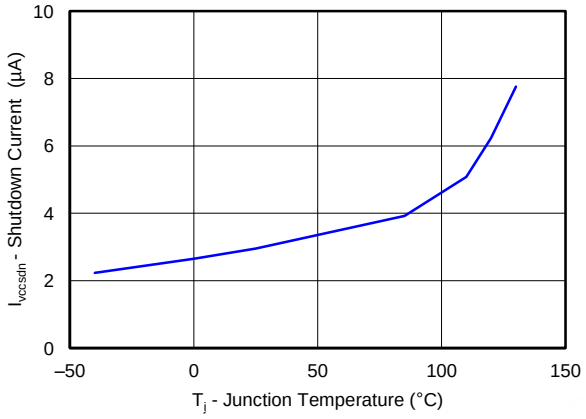


**Figure 2. VIN SHUTDOWN CURRENT vs JUNCTION TEMPERATURE**

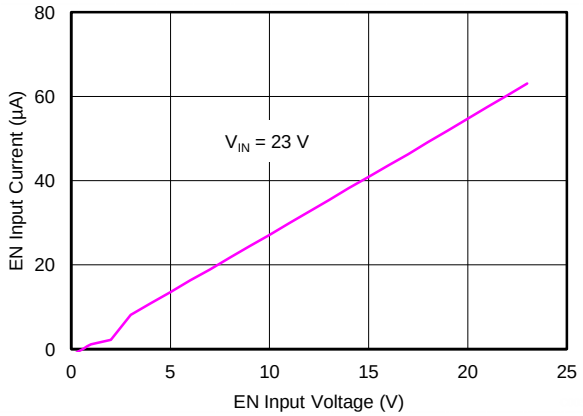


**Figure 3. EN CURRENT vs EN VOLTAGE**

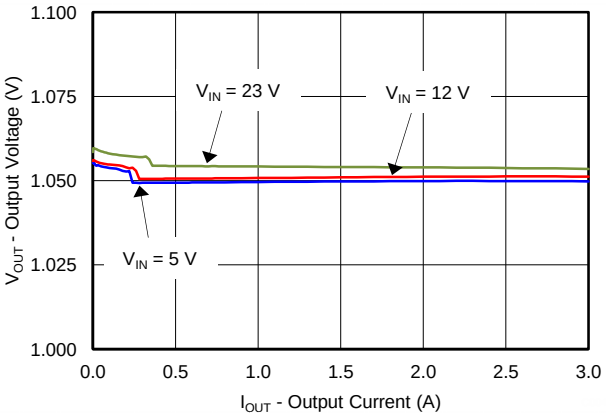


**Figure 4. 1.05-V OUTPUT VOLTAGE vs OUTPUT CURRENT**

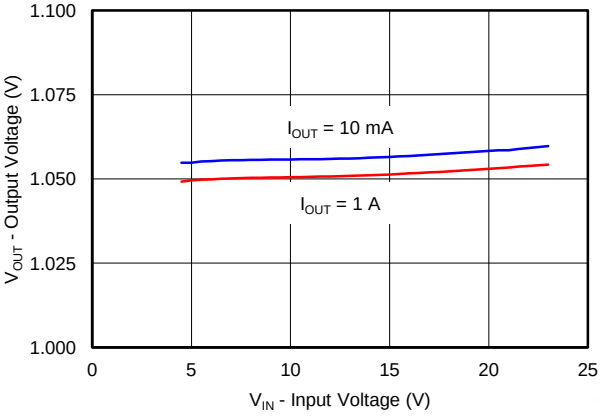


**Figure 5. 1.05-V OUTPUT VOLTAGE vs INPUT VOLTAGE**

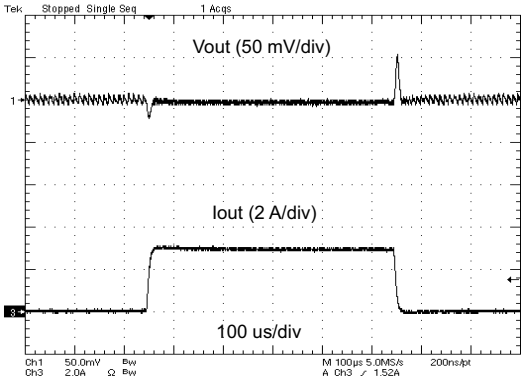


**Figure 6. 1.05-V, LOAD TRANSIENT RESPONSE**


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## TYPICAL CHARACTERISTICS

VIN = 12 V, $T_A$ = 25°C (unless otherwise noted).

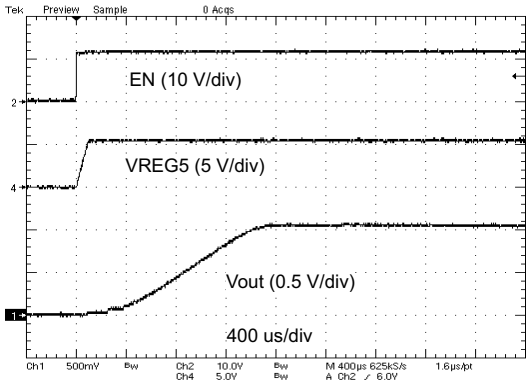


**Figure 7. START-UP WAVE FORM**

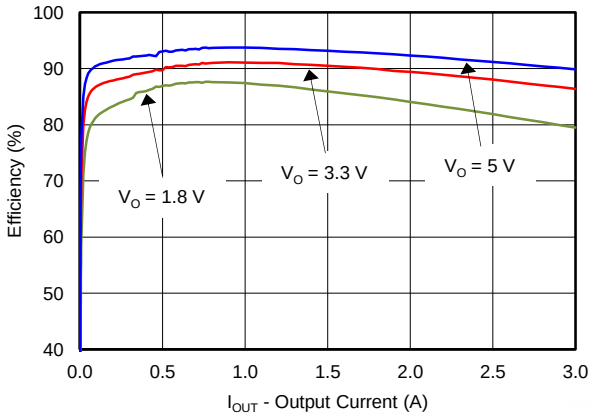


**Figure 8. EFFICIENCY vs OUTPUT CURRENT**

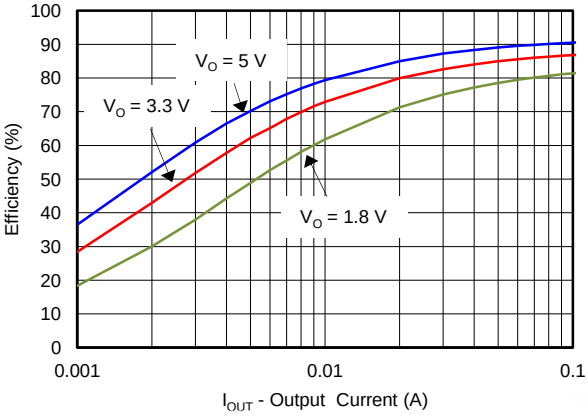


**Figure 9. LIGHT LOAD EFFICIENCY vs OUTPUT CURRENT**

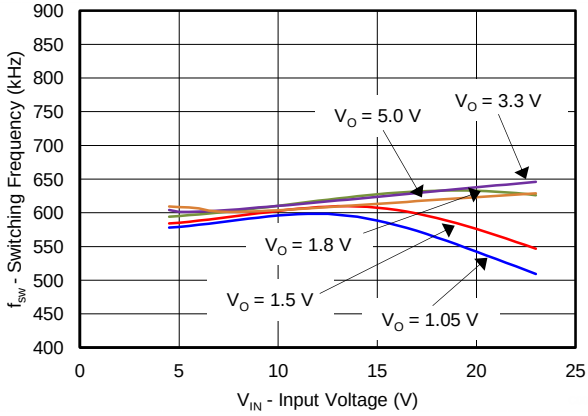


**Figure 10. SWITCHING FREQUENCY vs INPUT VOLTAGE ($I_O$ = 1 A)**

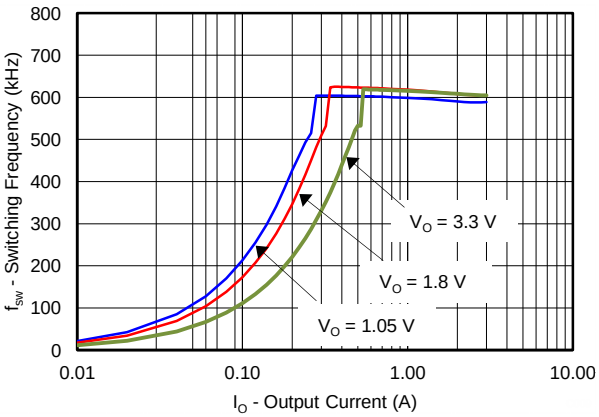


**Figure 11. SWITCHING FREQUENCY vs OUTPUT CURRENT**

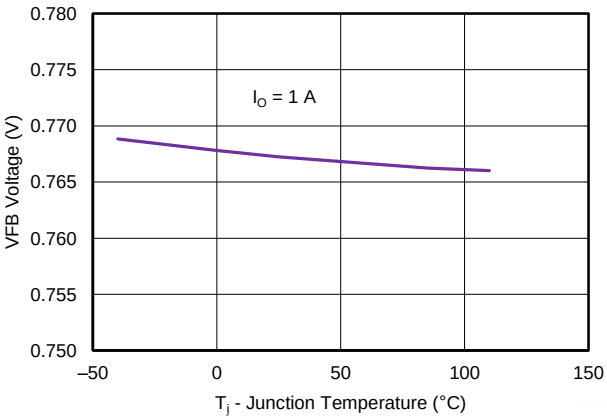


**Figure 12. VFB VOLTAGE vs JUNCTION TEMPERATURE ($I_O$ = 1 A)**

## TYPICAL CHARACTERISTICS (continued)

VIN = 12 V, $T_A$ = 25°C (unless otherwise noted).

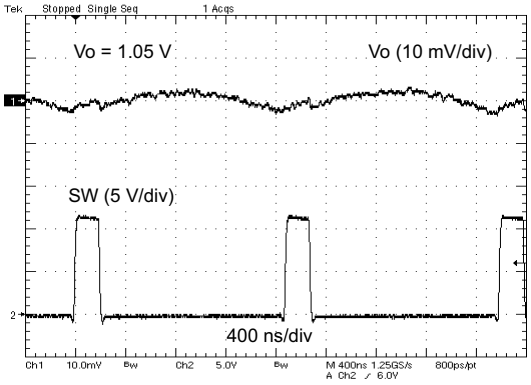


**Figure 13. VOLTAGE RIPPLE AT OUTPUT ($I_O$ = 3A)**

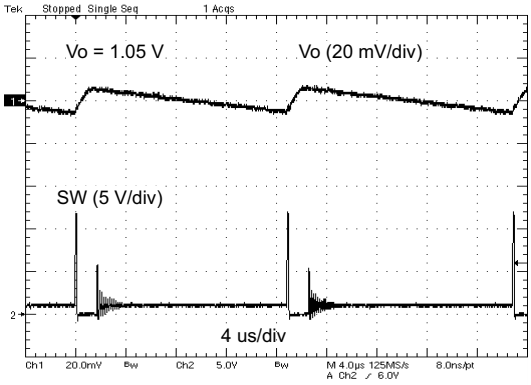


**Figure 14. VOLTAGE RIPPLE AT OUTPUT ($I_O$ = 30 mA)**

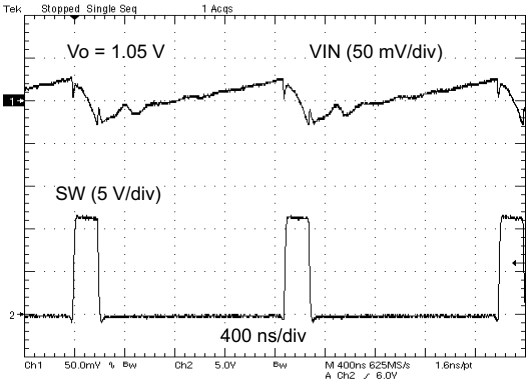


**Figure 15. VOLTAGE RIPPLE AT INPUT ($I_O$ = 3 A)**


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## DESIGN GUIDE

### Step-By-Step Design Procedure

To begin the design process, the user must know a few application parameters:

- Input voltage range
- Output voltage
- Output current
- Output voltage ripple
- Input voltage ripple

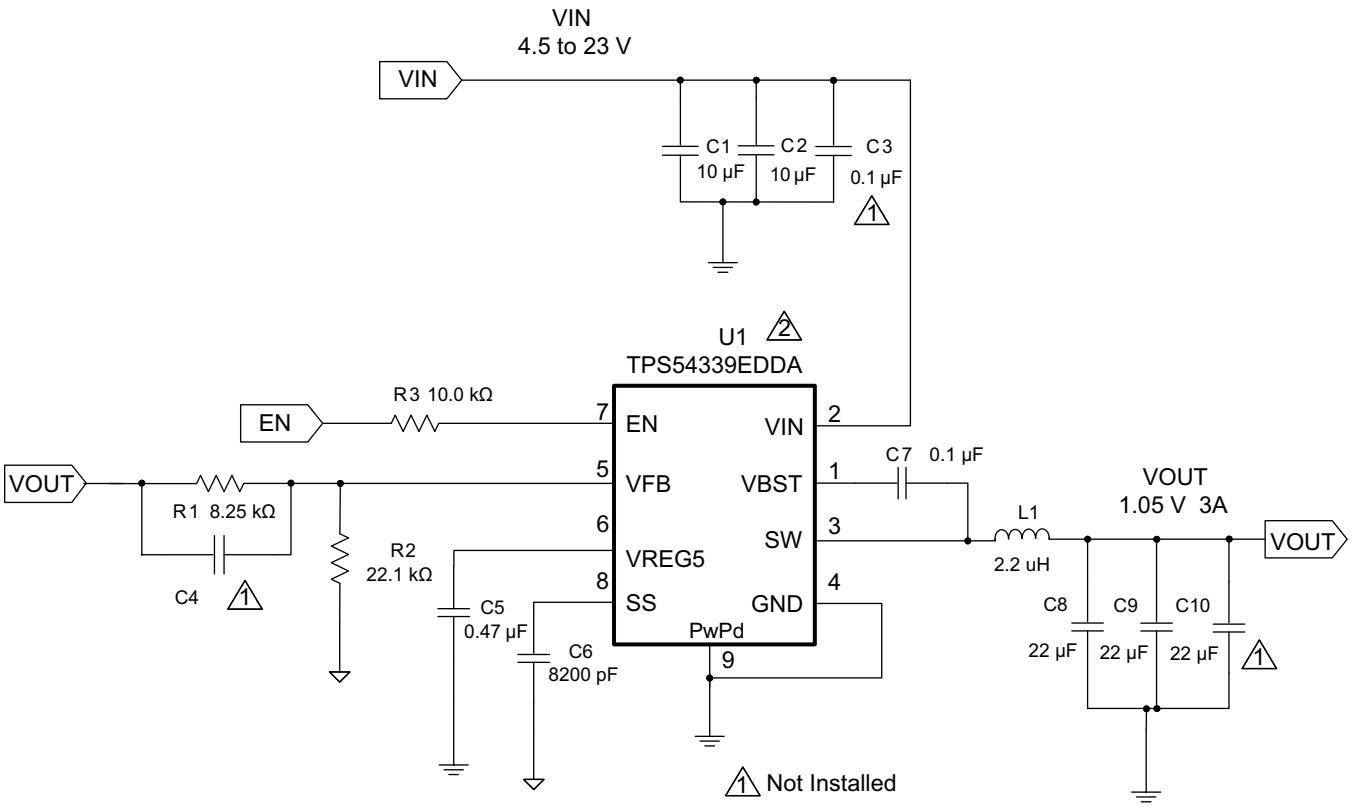


**Figure 16. Shows the schematic diagram for this design example.**

### Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. It is recommended to use 1% tolerance or better divider resistors. Start by using Equation 3 to calculate $V_{OUT}$.

To improve efficiency at light loads consider using larger value resistors, high resistance is more susceptible to noise, and the voltage errors from the VFB input current are more noticeable.

$$V_{OUT} = 0.765 \times \left(1 + \frac{R1}{R2}\right) \tag{3}$$

### Output Filter Selection

The output filter used with the TPS54339E is an LC circuit. This LC filter has double pole at:

$$F_P = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \tag{4}$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS54339E. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. D-CAP2™ introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor selected for the output filter must be selected so that the double pole of Equation 4 is located below the high frequency zero but close enough that the phase boost provided be the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in Table 1

**Table 1. Recommended Component Values**

| Output Voltage (V) | R1 (kΩ) | R2 (kΩ) | C4 (pF)(1) | | | L1 (µH) | | | C8 + C9 (µF) | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Max |
| 1 | 6.81 | 22.1 | 5 | 150 | 220 | 1.5 | 2.2 | 4.7 | 22 | 68 |
| 1.05 | 8.25 | 22.1 | 5 | 150 | 220 | 1.5 | 2.2 | 4.7 | 22 | 68 |
| 1.2 | 12.7 | 22.1 | 5 | | 100 | 1.5 | 2.2 | 4.7 | 22 | 68 |
| 1.5 | 21.5 | 22.1 | 5 | | 68 | 1.5 | 2.2 | 4.7 | 22 | 68 |
| 1.8 | 30.1 | 22.1 | 5 | | 22 | 2.2 | 3.3 | 4.7 | 22 | 68 |
| 2.5 | 49.9 | 22.1 | 5 | | 22 | 2.2 | 3.3 | 4.7 | 22 | 68 |
| 3.3 | 73.2 | 22.1 | 5 | | 22 | 2.2 | 3.3 | 4.7 | 22 | 68 |
| 5 | 124 | 22.1 | 5 | | 22 | 3.3 | | 4.7 | 22 | 68 |
| 6.5 | 165 | 22.1 | 5 | | 22 | 3.3 | | 4.7 | 22 | 68 |

(1) Optional

Since the DC gain is dependent on the output voltage, the required inductor value increases as the output voltage increases. Additional phase boost can be achieved by adding a feed forward capacitor (C4) in parallel with R1. The amount of available phase boost is dependent on the output voltage. Higher output voltages will allow greater phase boost.

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using Equation 5, Equation 6 and Equation 7. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current. Use 600 kHz for $f_{SW}$.

Use 600 kHz for $f_{SW}$. Make sure the chosen inductor is rated for the peak current of Equation 6 and the RMS current of Equation 7.

$$II_{P-P} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}} \tag{5}$$

$$II_{PEAK} = I_O + \frac{II_{P-P}}{2} \tag{6}$$

$$I_{LO(RMS)} = \sqrt{I_O^2 + \frac{1}{12} II_{P-P}^2} \tag{7}$$

For this design example, the calculated peak current is 3.36 A and the calculated RMS current is 3.01 A. The inductor used is a TDK CLF7045T-2R2N with a peak current rating of 5.5 A and an RMS current rating of 4.3 A. For high current designs, TDK SPM6530T-4R7M 4.7µH is also recommended. The SPM6530 series has a higher current rating than the CLF7045 series.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS54339E is intended for use with ceramic or other low ESR capacitors. Recommended values range from 22µF to 68µF. Use Equation 8 to determine the required RMS current rating for the output capacitor.

$$I_{Co(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{SW}} \tag{8}$$

For this design two TDK C3216X5R0J226M 22µF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.21 A and each output capacitor is rated for 4A.

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### Input Capacitor Selection

The TPS54339E requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A ceramic capacitor over 10 µF is recommended for the decoupling capacitor. An additional 0.1 µF capacitor from pin 2 to ground is optional to provide additional high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.

### Bootstrap Capacitor Selection

A 0.1 µF. ceramic capacitor must be connected between the VBST to SW pin for proper operation. It is recommended to use a ceramic capacitor.

### VREG5 Capacitor Selection

A 0.47 µF. ceramic capacitor must be connected between the VREG5 to GND pin for proper operation. It is recommended to use a ceramic capacitor.

## THERMAL INFORMATION

This 8-pin DDA package incorporates an exposed thermal pad that is designed to be directly to an external heartsick. The thermal pad must be soldered directly to the printed board (PCB). After soldering, the PCB can be used as a heartsick. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heartsick structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the exposed thermal pad and how to use the advantage of its heat dissipating abilities, see the Technical Brief, PowerPAD™ Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD™ Made Easy, Texas Instruments Literature No. SLMA004.

The exposed thermal pad dimensions for this package are shown in the following illustration.

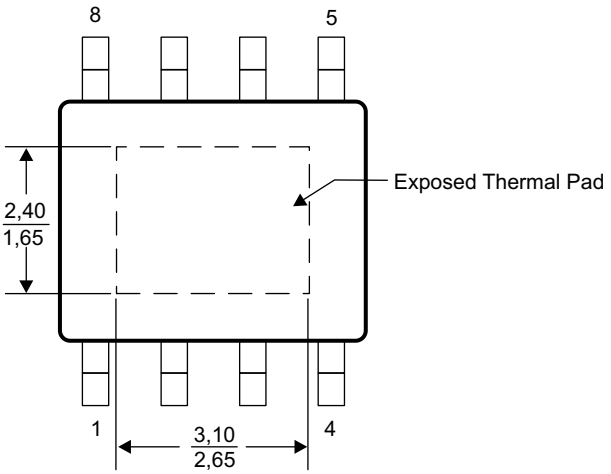


**Figure 17. Thermal Pad Dimensions**

## LAYOUT CONSIDERATIONS

1. Keep the input switching current loop as small as possible.
2. Keep the SW node as physically small and short as possible to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections should be brought from the output to the feedback pin of the device.
3. Keep analog and non-switching components away from switching components.
4. Make a single point connection from the analog ground to power ground.
5. Do not allow switching current to flow under the device.
6. Keep the pattern lines for VIN and PGND broad.
7. Exposed pad of device must be connected to PGND with solder.
8. VREG5 capacitor should be placed near the device, and connected to PGND.
9. Output capacitor should be connected to a broad pattern of the PGND.
10. Voltage feedback loop should be as short as possible, and preferably with ground shield.
11. Lower resistor of the voltage divider which is connected to the VFB pin should be tied to analog ground trace.
12. Providing sufficient via is preferable for VIN, SW and PGND connection.
13. VIN input bypass capacitor and VIN high frequency bypass capacitor must be placed as near as possible to the device.
14. Performance based on four layer printed circuit board.

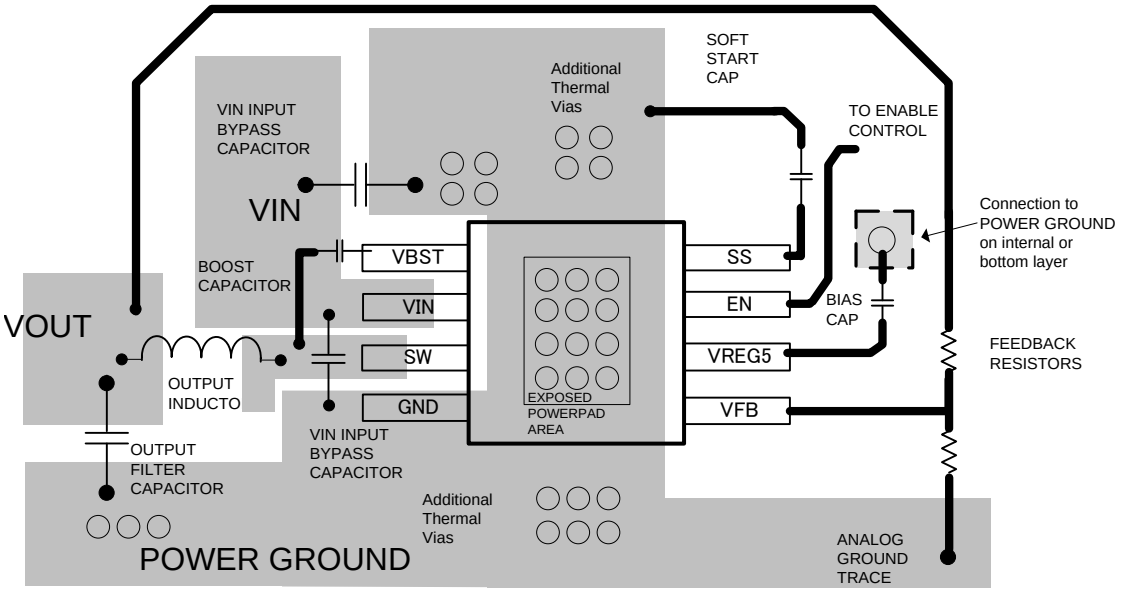


**Figure 18. PCB Layout**


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS54339EDDA | Active | Production | SO PowerPAD (DDA) \| 8 | 75 \| TUBE | Yes | NIPDAU \| SN | Level-2-260C-1 YEAR | -40 to 85 | 54339E |
| TPS54339EDDA.A | Active | Production | SO PowerPAD (DDA) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 54339E |
| TPS54339EDDAR | Active | Production | SO PowerPAD (DDA) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU \| SN | Level-2-260C-1 YEAR | -40 to 85 | 54339E |
| TPS54339EDDAR.A | Active | Production | SO PowerPAD (DDA) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 54339E |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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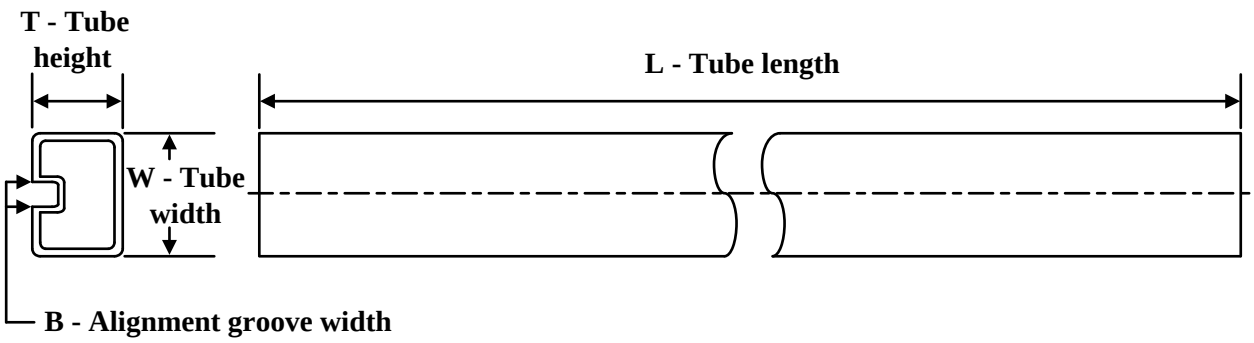
## TUBE

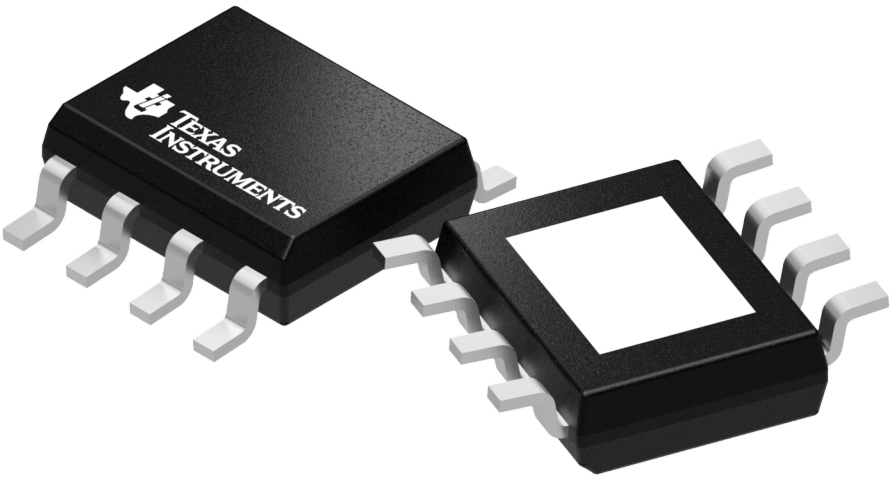



*All dimensions are nominal

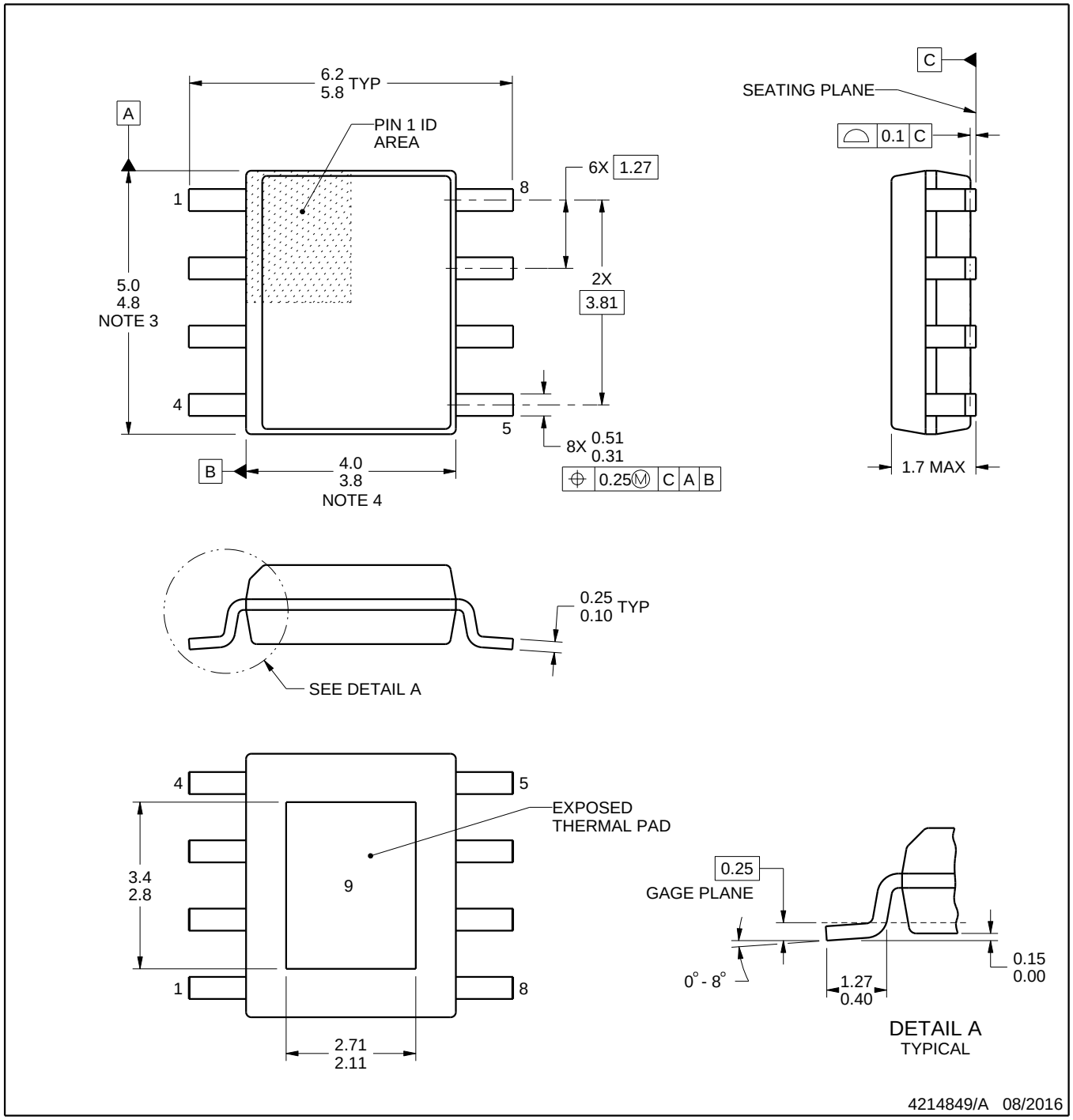
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| TPS54339EDDA | DDA | HSOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TPS54339EDDA | DDA | HSOIC | 8 | 75 | 517 | 7.87 | 635 | 4.25 |
| TPS54339EDDA.A | DDA | HSOIC | 8 | 75 | 517 | 7.87 | 635 | 4.25 |
| TPS54339EDDA.A | DDA | HSOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |

# DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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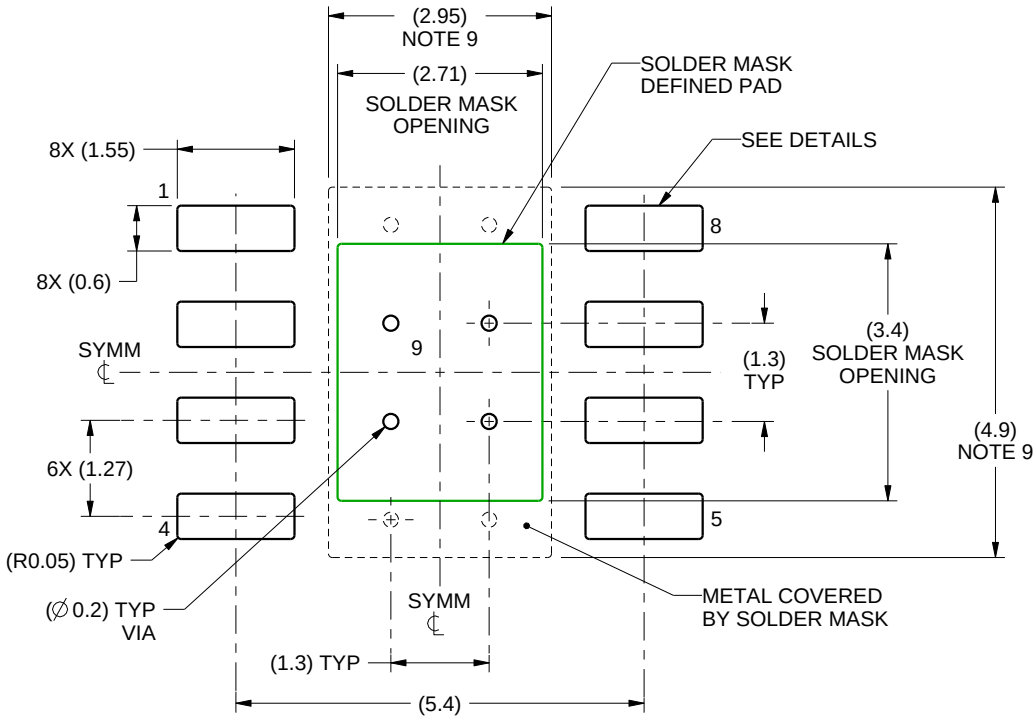
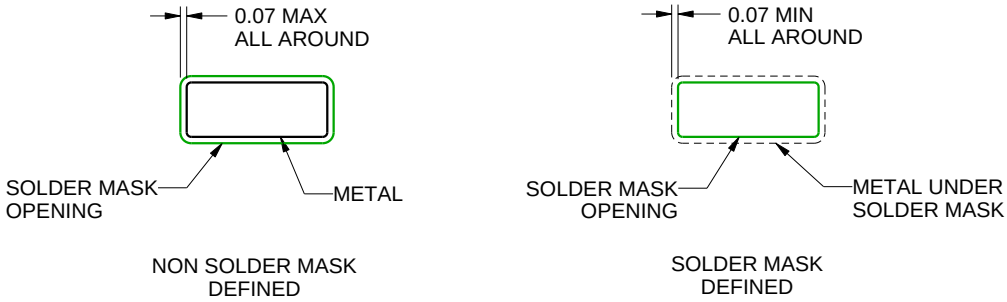
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.




LAND PATTERN EXAMPLE
SCALE:10X

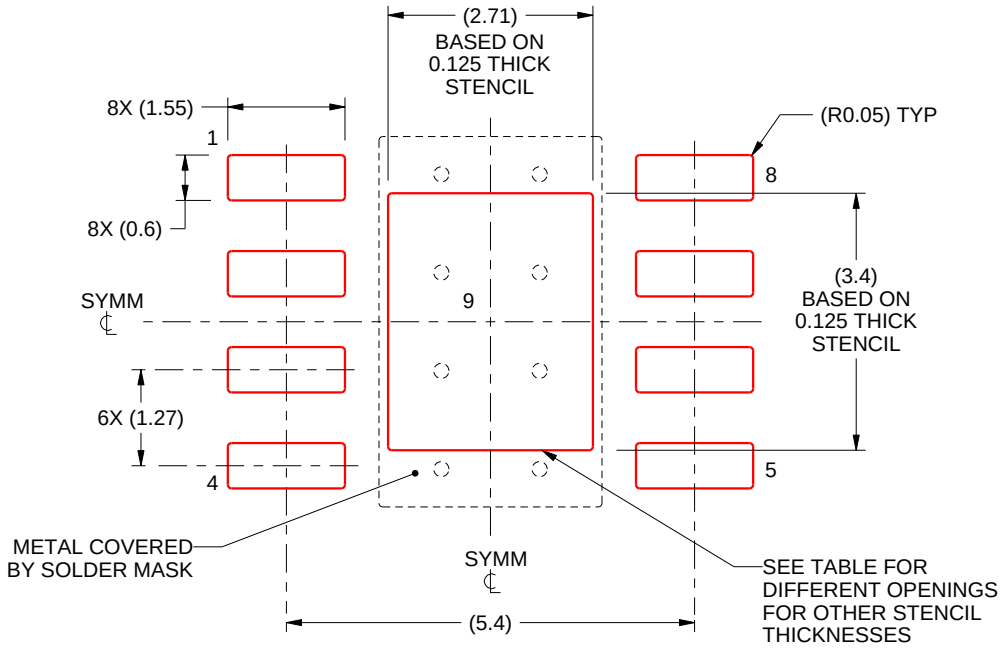



SOLDER MASK DETAILS
PADS 1-8

4214849/A 08/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

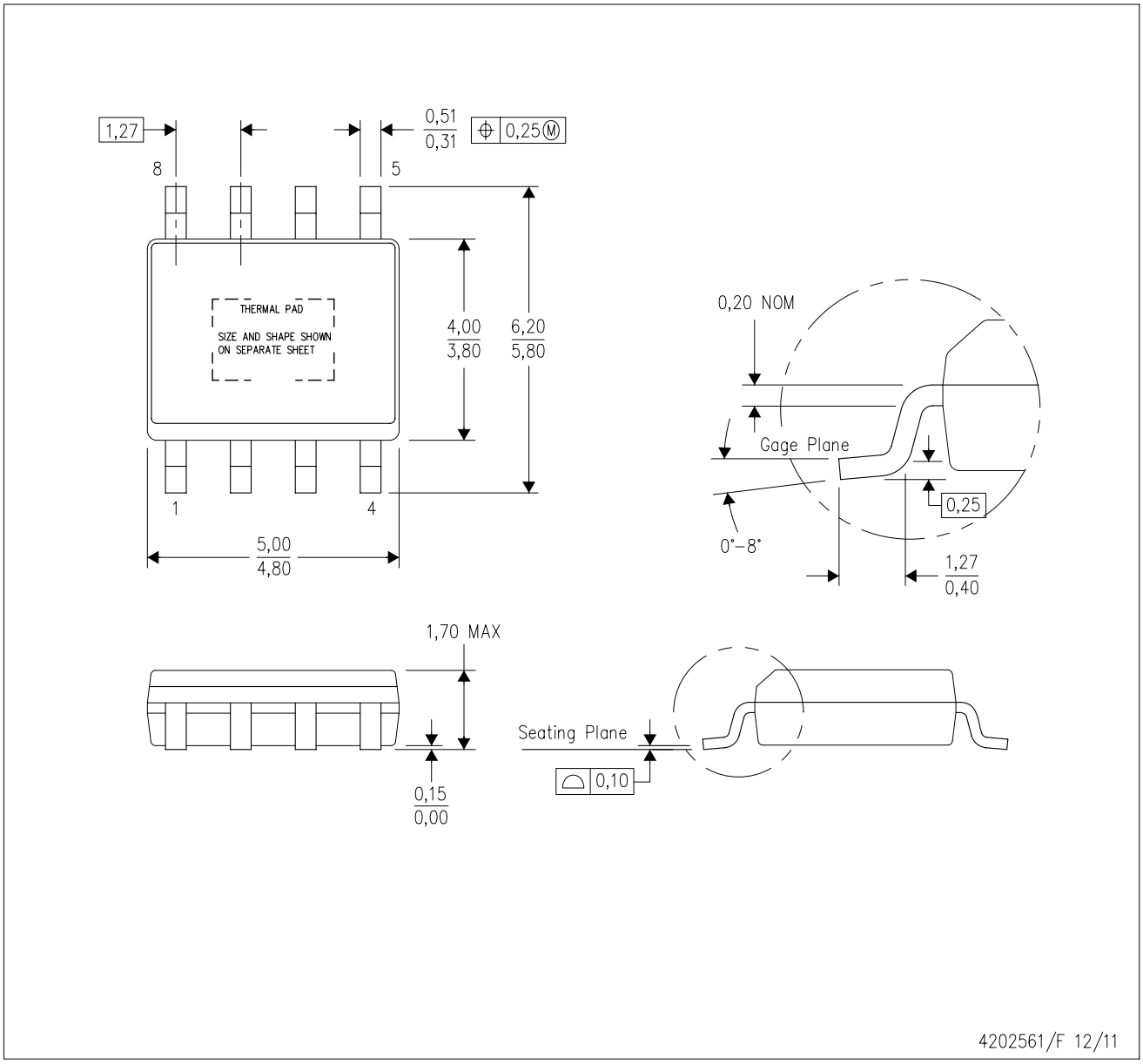
| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|---|---|
| 0.1 | 3.03 X 3.80 |
| 0.125 | 2.71 X 3.40 (SHOWN) |
| 0.150 | 2.47 X 3.10 |
| 0.175 | 2.29 X 2.87 |

4214849/A 08/2016

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

DDA (R-PDSO-G8) PowerPAD™ PLASTIC SMALL-OUTLINE




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS-012 variation BA

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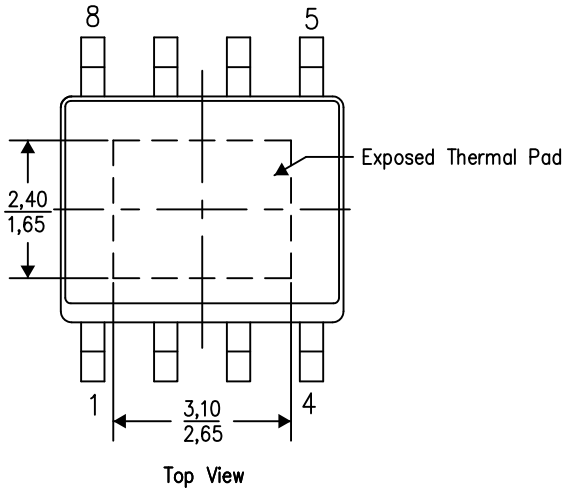
DDA (R-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Exposed Thermal Pad Dimensions

4206322-6/L 05/12

NOTE: A. All linear dimensions are in millimeters

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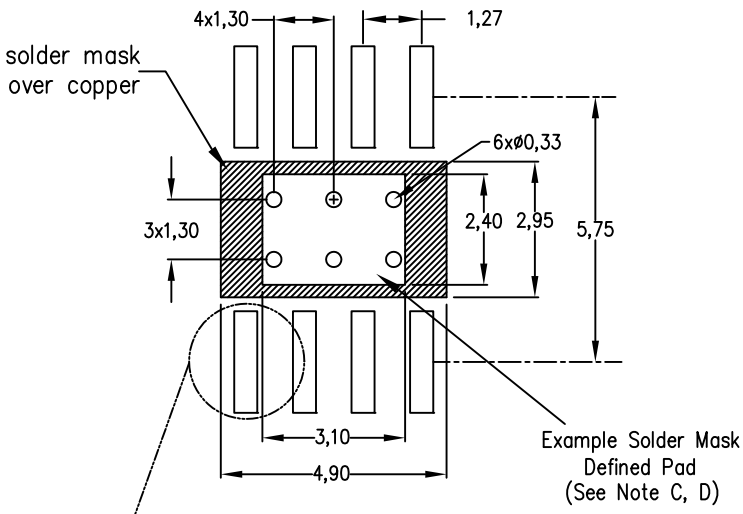
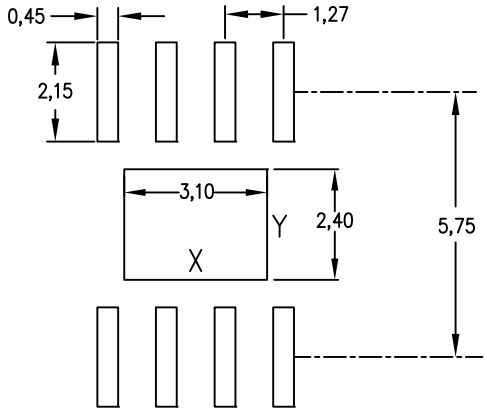
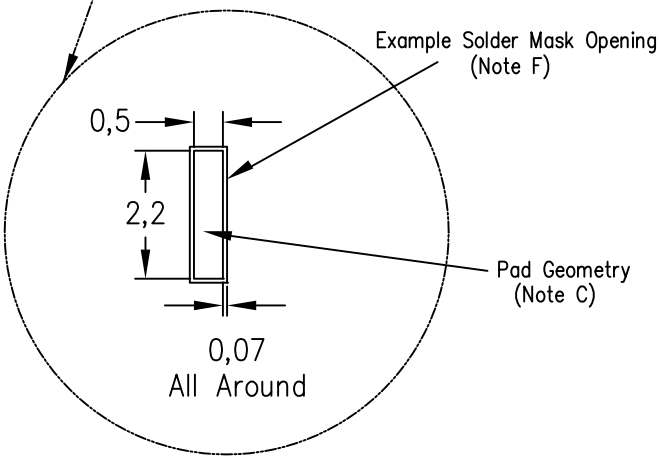
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE




| Center Power Pad Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 3.3 | 2.6 |
| 0.127mm | 3.1 | 2.4 |
| 0.152mm | 2.9 | 2.2 |
| 0.178mm | 2.8 | 2.1 |

4208951–6/D 04/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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