DLP670S 0.67 2716 × 1600 DMD

1 Features

- High resolution 2716 × 1600 array
  - >4.3 million micromirrors
  - 0.67-inch micromirror array diagonal
  - 5.4-micron micromirror pitch
  - ±17.5° micromirror tilt angle (relative to flat surface)
  - Designed for bottom illumination
  - Integrated micromirror driver circuitry
- Designed for use with broadband visible light (420 nm–700 nm)
  - Window transmission 97% (single pass, through two window surfaces)
  - Micromirror reflectivity 88%
  - Array diffraction efficiency 84% (@f/2.4)
  - Array fill factor 93%
- Four 16-bit, low voltage differential signaling (LVDS), double data rate (DDR) input-data buses
- Driven by dual DLPC900 digital controllers
  - Up to 9523-Hz 1-bit patterns/second
  - Equivalent to 41.3 gigabits/second pixel data rate in a prestored pattern mode
  - Up to 1190-Hz, 8-bit gray pattern rate (prestored patterns with illumination modulation)
  - Up to 247-Hz, 8-bit pattern rate (external video pattern input)

2 Applications

- Industrial
  - 3D scanners for machine vision
  - 3D touchless metrology and quality control
  - 3D printing
- Medical
  - Ophthalmology
  - 3D scanners for limb and skin measurement
  - Hyperspectral scanning and imaging
- Displays
  - 3D imaging microscopes
  - Intelligent and adaptive lighting

3 Description

Featuring over 4.3 million micromirrors, the DLP670S digital micromirror device (DMD) is a spatial light modulator (SLM) that modulates the amplitude, direction, and phase of incoming light. This DMD coupled with its four 2xLVDS input data buses enables the display of high-resolution patterns at very fast pattern rates. The high resolution and fast pattern rates offered by the DLP670S make it well-suited to support a wide variety of industrial, medical, and advanced imaging applications. Reliable function and operation of the DLP670S is enabled in conjunction with dual DLPC900 digital controllers. This dedicated chipset provides flexible and easy-to-program patterns at the high pattern rates necessary to meet the requirements of a variety of end-equipment solutions.

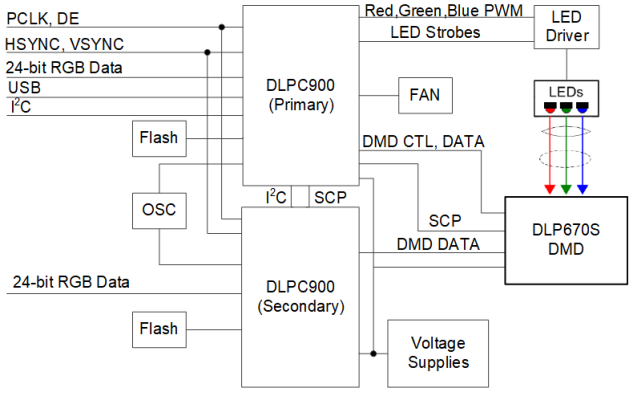
The high resolution provides a direct benefit to the scanning of larger objects in 3D machine vision applications.

Get started with TI DLP® advanced light-control technology page to learn how to get started with the DLP670S. The DLP advanced light control resources on TI.com accelerate time to market, which include evaluation modules, reference designs, optical modules manufacturers, and DLP design network partners.

Table 3-1. Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DLP670S(1)	FYR (350)	35 mm × 32 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



DLP670S Simplified Schematic

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4 Revision History

Changes from Revision * (November 2020) to Revision A (June 2022)	Page
• This document is updated to the latest Texas Instruments and industry data sheet standards	1
• Updated the ESD ratings per the latest standards	13
• Corrected Note (6) LVCMOS Interface	13
• Changed SCP specifications to reflect 'Rise/Fall Time'	17
• Corrected figure Figure 6-3	17

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5 Pin Configuration and Functions

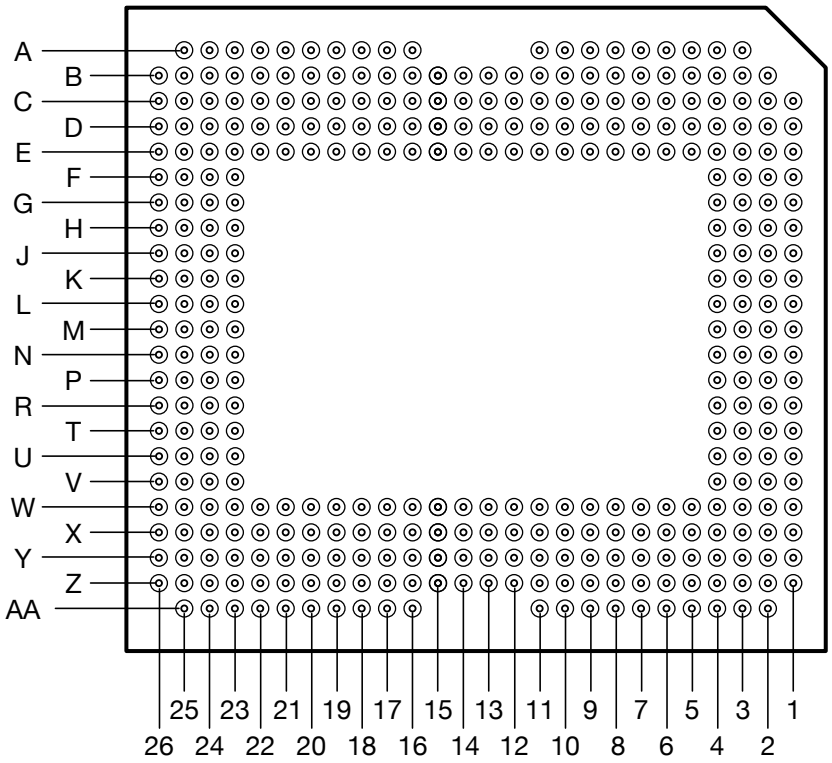

Figure 5-1. FYR Package 350-Pin CPGA Bottom View

CAUTION

To ensure reliable, long-term operation of the DLP670S DMD, it is critical to properly manage the layout and operation of the signals identified in the table below. For specific details and guidelines, refer to Section 10.1 before designing the board.

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Table 5-1. Pin Functions[1]

PIN[2]		TYPE (I/O/P)	SIGNAL	DATA RATE[4]	INTERNAL TERM[5]	DESCRIPTION	TRACE (mils)[6]
NAME	NO.						
DATA INPUTS							
D_AN(0)	C7	Input	2xLVDS	DDR	Differential	LVDS pair for Data Bus A (15:0)	563
D_AP(0)	C8						
D_AN(1)	D4						
D_AP(1)	E4						
D_AN(2)	C5						
D_AP(2)	C4						
D_AN(3)	D6						
D_AP(3)	C6						
D_AN(4)	D8						
D_AP(4)	D7						
D_AN(5)	D3						
D_AP(5)	E3						
D_AN(6)	B3						
D_AP(6)	C3						
D_AN(7)	E11						
D_AP(7)	E10						
D_AN(8)	E6						
D_AP(8)	E5						
D_AN(9)	B10						
D_AP(9)	C10						
D_AN(10)	B8						
D_AP(10)	B9						
D_AN(11)	C13						
D_AP(11)	C14						
D_AN(12)	D15						
D_AP(12)	E15						
D_AN(13)	B12						
D_AP(13)	B13						
D_AN(14)	B15						
D_AP(14)	B16						
D_AN(15)	C16						
D_AP(15)	C17						

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Table 5-1. Pin Functions[1] (continued)

PIN[2]		TYPE (I/O/P)	SIGNAL	DATA RATE[4]	INTERNAL TERM[5]	DESCRIPTION	TRACE (mils)[6]
NAME	NO.						
D_BN(0)	Y8	Input	2xLVDS	DDR	Differential	LVDS pair for Data Bus B (15:0)	563
D_BP(0)	Y7						
D_BN(1)	X4						
D_BP(1)	W4						
D_BN(2)	Z3						
D_BP(2)	Y3						
D_BN(3)	X6						
D_BP(3)	Y6						
D_BN(4)	X8						
D_BP(4)	X7						
D_BN(5)	X3						
D_BP(5)	W3						
D_BN(6)	W15						
D_BP(6)	X15						
D_BN(7)	W11						
D_BP(7)	W10						
D_BN(8)	W6						
D_BP(8)	W5						
D_BN(9)	AA9						
D_BP(9)	AA10						
D_BN(10)	Z8						
D_BP(10)	Z9						
D_BN(11)	Y13						
D_BP(11)	Y14						
D_BN(12)	Z10						
D_BP(12)	Y10						
D_BN(13)	Z12						
D_BP(13)	Z13						
D_BN(14)	Z15						
D_BP(14)	Z16						
D_BN(15)	Y16						
D_BP(15)	Y17						

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Table 5-1. Pin Functions[1] (continued)

PIN[2]		TYPE (I/O/P)	SIGNAL	DATA RATE[4]	INTERNAL TERM[5]	DESCRIPTION	TRACE (mils)[6]
NAME	NO.						
D_CN(0)	C18	Input	2xLVDS	DDR	Differential	LVDS pair for Data Bus C (15:0)	563
D_CP(0)	C19						
D_CN(1)	A20						
D_CP(1)	A19						
D_CN(2)	L23						
D_CP(2)	K23						
D_CN(3)	C23						
D_CP(3)	B23						
D_CN(4)	G23						
D_CP(4)	H23						
D_CN(5)	H24						
D_CP(5)	G24						
D_CN(6)	B18						
D_CP(6)	B19						
D_CN(7)	C21						
D_CP(7)	B21						
D_CN(8)	D23						
D_CP(8)	E23						
D_CN(9)	D25						
D_CP(9)	C25						
D_CN(10)	L24						
D_CP(10)	K24						
D_CN(11)	K25						
D_CP(11)	J25						
D_CN(12)	B24						
D_CP(12)	A24						
D_CN(13)	D26						
D_CP(13)	C26						
D_CN(14)	G25						
D_CP(14)	F25						
D_CN(15)	K26						
D_CP(15)	J26						

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Table 5-1. Pin Functions[1] (continued)

PIN[2]		TYPE (I/O/P)	SIGNAL	DATA RATE[4]	INTERNAL TERM[5]	DESCRIPTION	TRACE (mils)[6]
NAME	NO.						
D_DN(0)	Y18	Input	2xLVDS	DDR	Differential	LVDS pair for Data Bus D (15:0)	563
D_DP(0)	Y19						
D_DN(1)	AA20						
D_DP(1)	AA19						
D_DN(2)	N23						
D_DP(2)	P23						
D_DN(3)	Y23						
D_DP(3)	Z23						
D_DN(4)	U23						
D_DP(4)	T23						
D_DN(5)	T24						
D_DP(5)	U24						
D_DN(6)	Z18						
D_DP(6)	Z19						
D_DN(7)	Y21						
D_DP(7)	Z21						
D_DN(8)	X23						
D_DP(8)	W23						
D_DN(9)	X25						
D_DP(9)	Y25						
D_DN(10)	N24						
D_DP(10)	P24						
D_DN(11)	P25						
D_DP(11)	R25						
D_DN(12)	Z24						
D_DP(12)	AA24						
D_DN(13)	X26						
D_DP(13)	Y26						
D_DN(14)	U25						
D_DP(14)	V25						
D_DN(15)	P26						
D_DP(15)	R26						
DCLK_AN	B6	Input	LVDS		Differential	LVDS pair for Data Clock A [7]	563
DCLK_AP	B5						
DCLK_BN	Z6	Input	LVDS		Differential	LVDS pair for Data Clock B [7]	563
DCLK_BP	Z5						
DCLK_CN	G26	Input	LVDS		Differential	LVDS pair for Data Clock C [7]	563
DCLK_CP	F26						
DCLK_DN	U26	Input	LVDS		Differential	LVDS pair for Data Clock D [7]	563
DCLK_DP	V26						
DATA CONTROL INPUTS							
SCTRL_AN	A10	Input	LVDS	DDR	Differential	LVDS pair for Serial Control (Sync) A[7]	563
SCTRL_AP	A9						

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Table 5-1. Pin Functions[1] (continued)

PIN[2]		TYPE (I/O/P)	SIGNAL	DATA RATE[4]	INTERNAL TERM[5]	DESCRIPTION	TRACE (mils)[6]
NAME	NO.						
SCTRL_BN	Y4	Input	LVDS	DDR	Differential	LVDS pair for Serial Control (Sync) B[7]	563
SCTRL_BP	Y5						
SCTRL_CN	E24	Input	LVDS	DDR	Differential	LVDS pair for Serial Control (Sync) C[7]	563
SCTRL_CP	D24						
SCTRL_DN	W24	Input	LVDS	DDR	Differential	LVDS pair for Serial Control (Sync) D[7]	563
SCTRL_DP	X24						
DAD CONTROL INPUTS							
RESET_ADDR(0)	R3	Input	LVCMOS		Pulldown	Reset Driver Address Select. Bond pad connects to an internal pulldown circuit.[7]	
RESET_ADDR(1)	R4						
RESET_ADDR(2)	T3						
RESET_ADDR(3)	U2						
RESET_MODE(0)	P4	Input	LVCMOS		Pulldown	Reset Driver Mode Select. Bond pad connects to an internal pulldown circuit.[7]	
RESET_MODE(1)	V3						
RESET_OEZ	R2	Input	LVCMOS		Pullup	Active Low. Output Enable signal for internal Reset Driver circuitry. Bond Pad connects to an internal pullup circuit.[7]	
RESET_SEL(0)	P3	Input	LVCMOS		Pulldown	Reset Driver Level Select. Bond pad connects to an internal pulldown circuit.[7]	
RESET_SEL(1)	V2						
RESET_STROBE	W8	Input	LVCMOS		Pulldown	Rising edge on RESET_STROBE latches in the control signals. Bond pad connects to an internal pulldown circuit.[7]	
RESETZ	U4	Input	LVCMOS		Pullup	Active Low. Places reset circuitry in known VOFFSET state. Bond pad connects to an internal pulldown circuit.[7]	
SCP CONTROL							
SCPCLK	W17	Input	LVCMOS		Pulldown	Serial Communications Port Clock. SCPCLK is only active when SCPENZ goes low. Bond pad connects to an internal pulldown circuit.[7]	
SCPDI	W18	Input	LVCMOS	SDR	Pulldown	Serial Communications Port Data. Synchronous to the Rising Edge of SCPCLK. Bond pad connects to an internal pulldown circuit.[7]	
SCPENZ	X18	Input	LVCMOS		Pulldown	Active Low Serial Communications Port Enable. Bond pad connects to an internal pulldown circuit.[7]	
SCPDO	W16	Output	LVCMOS	SDR		Serial Communications Port output	
EXTERNAL REGULATOR SIGNALS							
EN_BIAS	J4	Output	LVCMOS			Active High. Enable signal for external VBIAS regulator	
EN_OFFSET	H3	Output	LVCMOS			Active High. Enable signal for external VOFFSET regulator	

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Table 5-1. Pin Functions[1] (continued)

PIN[2]		TYPE (I/O/P)	SIGNAL	DATA RATE[4]	INTERNAL TERM[5]	DESCRIPTION	TRACE (mils)[6]
NAME	NO.						
EN_RESET	J3	Output	LVCMOS			Active High. Enable signal for external VRESET regulator	
PG_BIAS	K3	Input	LVCMOS			Active low fault from external V_{BIAS} regulator[7]	
PG_OFFSET	F2	Input	LVCMOS			Active low fault from external V_{OFFSET} regulator[7]	
PG_RESET	F3	Input	LVCMOS			Active low fault from external V_{RESET} regulator[7]	
OTHER SIGNALS							
RESET_IRQZ	U3	Output	LVCMOS			Active Low. Output Interrupt to DLP controller (ASIC)	
TEMP_PLUS	E16	Input	Analog			Temperature Sensor Diode Anode[3]	
TEMP_MINUS	E17	Input	Analog			Temperature Sensor Diode Cathode [3]	
POWER							
V_{BIAS}	A5, A6, A7, AA5, AA6, AA7	Power	Analog			Power supply for Positive Bias level of micromirror reset signal	
V_{CC}	A8, B2, C1, D1, D10, D12, D19, E1, E19, E20, E21, F1, K1, L1, M1, N1, P1,V1, W1, W19, W20, W21, X1, X10, X12, X19, Y1, Z1, Z2, AA2, AA8,	Power	Analog			Power supply for low voltage CMOS logic. Power supply for normal high voltage at micromirror address electrodes. Power supply for Offset level during the power-down sequence	
V_{CCI}	A11, A16, A17, A18, A21, A22, A23, AA11, AA16, AA17, AA18, AA21, AA22, AA23,	Power	Analog			Power supply for low voltage CMOS LVDS interface	
V_{OFFSET}	A3, A4, A25, B26, L26, M26, N26, Z26, AA3, AA4, AA25	Power	Analog			Power supply for high voltage CMOS logic. Power supply for stepped high voltage at micromirror address electrodes. Power supply for Offset level of MBRST(15:0)	
V_{RESET}	G1, H1, J1, R1, T1, U1	Power	Analog			Power supply for Negative Reset level of micromirror reset signal	

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Table 5-1. Pin Functions[1] (continued)

PIN[2]		TYPE (I/O/P)	SIGNAL	DATA RATE[4]	INTERNAL TERM[5]	DESCRIPTION	TRACE (mils)[6]
NAME	NO.						
V_{SS} (Ground)	B4, B7, B11, B14, B17, B20, B22, B25, C2, C9, C20, C22, C24, D2, D5, D9, D11, D14, D18, D20, D21, D22, E2, E7, E9, E22, E25, E26, F4, F23, F24, H2, H4, H25, H26, J23, J24, K2, L2, L3, L4, L25, M2, M3, M4, M23, M24, M25, N2, N3, N25, P2,R23, R24, T2, T4, T25, T26, V4, V23, V24, W2, W7, W9, W22, W25, W26, X2, X5, X9, X11, X14, X20, X21, X22, Y2, Y9, Y20, Y22, Y24, Z4, Z7, Z11, Z14, Z17, Z20, Z22, Z25	Ground				Common Return for all power	
RESERVED SIGNALS							
RESERVED_PFE	E18	Ground	LVCMOS			Do Not Connect on the printed circuit board (PCB)	
RESERVED_TM	G4	Ground	LVCMOS			Do Not Connect on the printed circuit board (PCB)	
RESERVED_TP0	E8	Input	Analog			Do Not Connect on the printed circuit board (PCB)	
RESERVED_TP1	J2	Input	Analog			Do Not Connect on the printed circuit board (PCB)	
RESERVED_TP2	G2	Input	Analog			Do Not Connect on the printed circuit board (PCB)	
RESERVED_BA	N4	Output	LVCMOS			Do Not Connect on the printed circuit board (PCB)	
RESERVED_BB	K4	Output	LVCMOS			Do Not Connect on the printed circuit board (PCB)	
RESERVED_BC	X17	Output	LVCMOS			Do Not Connect on the printed circuit board (PCB)	
RESERVED_BD	D17	Output	LVCMOS			Do Not Connect on the printed circuit board (PCB)	

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Table 5-1. Pin Functions[1] (continued)

PIN[2]		TYPE (I/O/P)	SIGNAL	DATA RATE[4]	INTERNAL TERM[5]	DESCRIPTION	TRACE (mils)[6]
NAME	NO.						
NO CONNECT	C11, C12, C15, D13, D16, E12, E13, E14, W13, W12, W14, X13, X16, Y11, Y12, Y15,	NC				For TI Test Purposes only, Do Not Connect on the printed circuit board (PCB)	

(1) The DLP670S DMD is a component of a DLP® chipset. Reliable function and operation of the DLP670S DMD requires that it be used in conjunction with the other components of the applicable DLP® chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology is the TI technology and devices for operating or controlling a DLP® DMD.
(2) The following power supplies are required for all DMD operating modes: VSS, VBIAS, VCC, VCCI, VOFFSET, and VRESET.
(3) VSS must be connected for proper DMD operation.
(4) DDR = Double Data Rate, SDR = Single Data Rate, Refer to the Timing Requirements for specifications and relationships.
(5) Internal term = CMOS level internal termination. Refer to Recommended Operating Conditions for differential termination specification.
(6) Dielectric Constant for the DMD FYR (S610) ceramic package is approximately 9.6. For the package trace lengths shown: Propagation Speed = 11.8 / sqrt(9.6) = 3.808 in/ns. Propagation Delay = 0.262 ns/in = 10.315 ps/mm.
(7) These signals are very sensitive to noise or intermittent power connections, which can cause irreversible DMD micromirror array damage or, to a lesser extent, image disruption. Consider this precaution during DMD board design and manufacturer handling of the DMD sub-assemblies.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
SUPPLY VOLTAGES				
V_{CC}	Supply voltage for LVCMOS core logic(2)	–0.5	2.3	V
V_{CCI}	Supply voltage for LVDS receivers(2)	–0.5	2.3	V
V_{OFFSET}	Supply voltage for HVCMOS and micromirror electrode(2) (3)	–0.5	11	V
V_{BIAS}	Supply voltage for micromirror electrode(2)	–0.5	19	V
V_{RESET}	Supply voltage for micromirror electrode(2)	–15	–0.3	V
$\lvert V_{CC} - V_{CCI} \rvert$	Supply voltage delta (absolute value)(4)		0.3	V
$\lvert V_{BIAS} - V_{OFFSET} \rvert$	Supply voltage delta (absolute value)(5)		11	V
$\lvert V_{BIAS} - V_{RESET} \rvert$	Supply voltage delta (absolute value)(6)		34	V
INPUT VOLTAGES				
	Input voltage for all other LVCMOS input pins(2)	–0.5	V_{CC} + 0.5	V
	Input voltage for all other LVDS input pins(2) (6)	–0.5	V_{CCI} + 0.5	V
$\lvert V_{ID} \rvert$	Input differential voltage (absolute value)(6)		500	mV
I_{ID}	Input differential current(7)		6.25	mA
CLOCKS				
f_{CLOCK}	Clock frequency for LVDS interface: DCLK_A, DCLK_B, DCLK_C, DCLK_D		400	MHz
ENVIRONMENTAL				
T_{ARRAY} and T_{WINDOW}	Array temperature: operational(8)	0	90	°C
	Array temperature: non-operational(8)	–40	90	°C
$\lvert T_{DELTA} \rvert$	Absolute temperature delta between any point on the window edge and the ceramic test point TP1 (9)		30	°C
T_{DP}	Dew point temperature, operating and non–operating (noncondensing)		81	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are referenced to common ground V_{SS}. V_{BIAS}, V_{CC}, V_{CCI}, V_{OFFSET}, and V_{RESET} power supplies are all required for proper DMD operation. V_{SS} must also be connected.
(3) V_{OFFSET} supply transients must fall within specified voltages.
(4) Exceeding the recommended allowable voltage difference between V_{CC} and V_{CCI} may result in excessive current draw.
(5) Exceeding the recommended allowable voltage difference between V_{BIAS} and V_{OFFSET} may result in excessive current draw.
(6) Exceeding the recommended allowable voltage difference between V_{BIAS} and V_{RESET} may result in excessive current draw.
(7) LVDS differential inputs must not exceed the specified limit or damage may result to the internal termination resistors.
(8) The highest temperature of the active array (as calculated in Section 7.6) or of any location along the window edge as defined in Figure 7-1. The locations of thermal test points TP2, TP3, TP4, and TP5 in Figure 7-1 are intended to measure the highest window edge temperature. If a particular application causes another location on the window edge to be at a higher temperature, use that location.
(9) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in Figure 7-1. The window test points TP2, TP3, TP4, and TP5 shown in Figure 7-1 are intended to result in the worst case delta. If a particular application causes another location on the window edge to result in a larger delta temperature, use that location.

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6.2 Storage Conditions

Applicable for the DMD as a component or non-operating in a system

		MIN	MAX	UNIT
T_{DMD}	DMD storage temperature	– 40	80	°C
T_{DP-AVG}	Average dew point temperature, (non-condensing) (1)		28	°C
T_{DP-ELR}	Elevated dew point temperature range , (non-condensing) (2)	28	36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range		24	Months

(1) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
(2) Limit the Exposure to dew point temperatures in the elevated range during storage and operation to less than a total cumulative time of CT_{ELR}.

6.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by Section 6.4. No level of performance is implied when operating the device above or below Section 6.4 limits.

		MIN	NOM	MAX	UNIT
VOLTAGE SUPPLY					
V_{CC}	LVCMOS logic supply voltage(1)	1.65	1.8	1.95	V
V_{CCI}	LVCMOS LVDS Interface supply voltage(1)	1.65	1.8	1.95	V
V_{OFFSET}	Mirror electrode and HVCMOS voltage(1) (2)	9.5	10	10.5	V
V_{BIAS}	Mirror electrode voltage(1)	17.5	18	18.5	V
V_{RESET}	Mirror electrode voltage(1)	–14.5	–14	–13.5	V
$\lvert V_{CC} - V_{CCI} \rvert$	Supply voltage delta (absolute value)(3)		0	0.3	V
$\lvert V_{BIAS} - V_{OFFSET} \rvert$	Supply voltage delta (absolute value)(4)			10.5	V
$\lvert V_{BIAS} - V_{RESET} \rvert$	Supply voltage delta (absolute value)(5)			33	V
LVCMOS INTERFACE					
$V_{IH(DC)}$	DC input high voltage(6)	0.7 × V_{CC}		V_{CC} + 0.3	V
$V_{IL(DC)}$	DC input low voltage(6)	–0.3		0.3 × V_{CC}	V
$V_{IH(AC)}$	AC input high voltage(6)	0.8 × V_{CC}		V_{CC} + 0.3	V
$V_{IL(AC)}$	AC input low voltage(6)	–0.3		0.2 × V_{CC}	V
t_{PWRDNZ}	PWRDNZ pulse width(7)	10			ns
SCP INTERFACE					
f_{SCPCLK}	SCP clock frequency(8)			500	kHz
t_{SCP_PD}	Propagation delay, Clock to Q, from rising–edge of SCPCLK to valid SCPDO(9)	0		900	ns
$t_{SCP_NEG_ENZ}$	Time between falling–edge of SCPENZ and the first rising edge of SCPCLK	2			µs
$t_{SCP_POS_ENZ}$	Time between falling–edge of SCPCLK and the rising edge of SCPENZ	2			µs
t_{SCP_DS}	SCPDI Clock Setup time (before SCPCLK falling edge)(9)	800			ns
t_{SCP_DH}	SCPDI Hold time (after SCPCLK falling edge)(9)	900			ns
$t_{SCP_PW_ENZ}$	SCPENZ inactive pulse width (high level)	2			µs

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6.4 Recommended Operating Conditions (continued)

Over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by Section 6.4. No level of performance is implied when operating the device above or below Section 6.4 limits.

		MIN	NOM	MAX	UNIT
LVDS INTERFACE					
f_{CLOCK}	Clock frequency for LVDS interface (all channels), DCLK(10)			400	MHz
$\|V_{ID}\|$	Input differential voltage (absolute value)(11)	150	300	440	mV
V_{CM}	Common mode voltage(11)	1100	1200	1300	mV
V_{LVDS}	LVDS voltage(11)	880		1520	mV
t_{LVDS_RSTZ}	Time required for LVDS receivers to recover from PWRDNZ			2000	ns
Z_{IN}	Internal differential termination resistance	80	100	120	Ω
Z_{LINE}	Line differential impedance (PWB/trace)	90	100	110	Ω
ENVIRONMENTAL					
T_{ARRAY}	Array temperature, long-term operational(12) (13) (14) (15)	10		40 to 70(14)	°C
	Array temperature, short-term operational(13) (16)	0		10	°C
T_{WINDOW}	Window temperature — operational(17)			85	°C
$\|T_{DELTA}\|$	Absolute Temperature delta between any point on the window edge and the ceramic test point TP1(17) (18)			14	°C
$T_{DP\text{-}AVG}$	Average dew point temperature (non-condensing)(19)			28	°C
$T_{DP\text{-}ELR}$	Elevated dew point temperature range (non-condensing)(20)	28		36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range			24	Months
ILL_{θ}	Illumination marginal ray angle(21)			55	deg
For Illumination Source Between 420 nm and 700 nm					
ILL_{VIS}	Illumination power density on array(22)			31	W/cm^2
ILL_{VISTP}	Illumination total power on array			39.3	W
For Illumination Source <420 nm and >700 nm					
ILL_{IR}	Illumination Wavelengths > 700 nm			10	mW/cm^2
ILL_{UV}	Illumination Wavelengths < 420 nm(12)			10	mW/cm^2

(1) All voltages are referenced to common ground VSS. VBIAS, VCC, VCCI, VOFFSET, and VRESET power supplies are all required for proper DMD operation. VSS must also be connected.
(2) VOFFSET supply transients must fall within specified max voltages.
(3) To prevent excess current, the supply voltage delta |VCCI – VCC| must be less than specified limit. See Section 9, Figure 9-1, and Table 9-1.
(4) To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than specified limit. See Section 9, Figure 9-1, and Table 9-1.
(5) To prevent excess current, the supply voltage delta |VBIAS – VRESET| must be less than specified limit. See Section 9, Figure 9-1, and Table 9-1.
(6) Tester Conditions for VIH and VIL.
- Frequency = 60-MHz Maximum Rise Time = 2.5 ns @ (20% – 80%)
- Frequency = 60-MHz Maximum Fall Time = 2.5 ns @ (80% – 20%)

(7) PWRDNZ input pin resets the SCP and disables the LVDS receivers. PWRDNZ input pin overrides SCPENZ input pin and tristates the SCPDO output pin.
(8) The SCP clock is a gated clock. Duty cycle must be 50% ± 10%. The SCP parameter is related to the frequency of DCLK.
(9) See Figure 6-2.
(10) See the LVDS Timing Requirements in Section 6.8 and Figure 6-6.
(11) See Figure 6-5 LVDS Waveform Requirements.
(12) Simultaneous exposure of the DMD to the maximum Section 6.4 for temperature and UV illumination reduces device lifetime.
(13) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1) shown in Figure 7-1 and the package thermal resistance Section 7.6.
(14) Per Figure 6-1, the maximum operational array temperature must be derated based on the micromirror landed duty cycle that the DMD experiences in the end application. See Section 7.7 for a definition of micromirror landed duty cycle.
(15) Long-term is defined as the usable life of the device.
(16) Array temperatures beyond those specified as long-term are recommended for short-term conditions only (power-up). Short-term is defined as cumulative time over the usable life of the device and is less than 500 hours.

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(17) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in Figure 7-1. The window test points TP2, TP3, TP4 and TP5 shown in Figure 7-1 are intended to result in the worst case delta temperature. If a particular application causes another location on the window edge to result in a larger delta temperature, use that location.
(18) DMD is qualified at the maximum temperature specified. Operation of the DMD outside of these limits has not been tested.
(19) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
(20) Limit exposure to dew point temperatures in the elevated range during storage and operation to less than a total cumulative time of CT_{ELR}.
(21) The maximum marginal ray angle of the incoming illumination light at any point in the micromirror array, including the pond of micromirrors (POM), cannot exceed 55 degrees from the normal to the device array plane. The device window aperture has not necessarily been designed to allow incoming light at higher maximum angles to pass to the micromirrors, and the device performance has not been tested nor qualified at angles exceeding this. Illumination light exceeding this angle outside the micromirror array (including POM) contributes to thermal limitations described in this document, and may negatively affect lifetime.
(22) The maximum optical power that can be incident on the DMD is limited by the maximum optical power density and the micromirror array temperature.

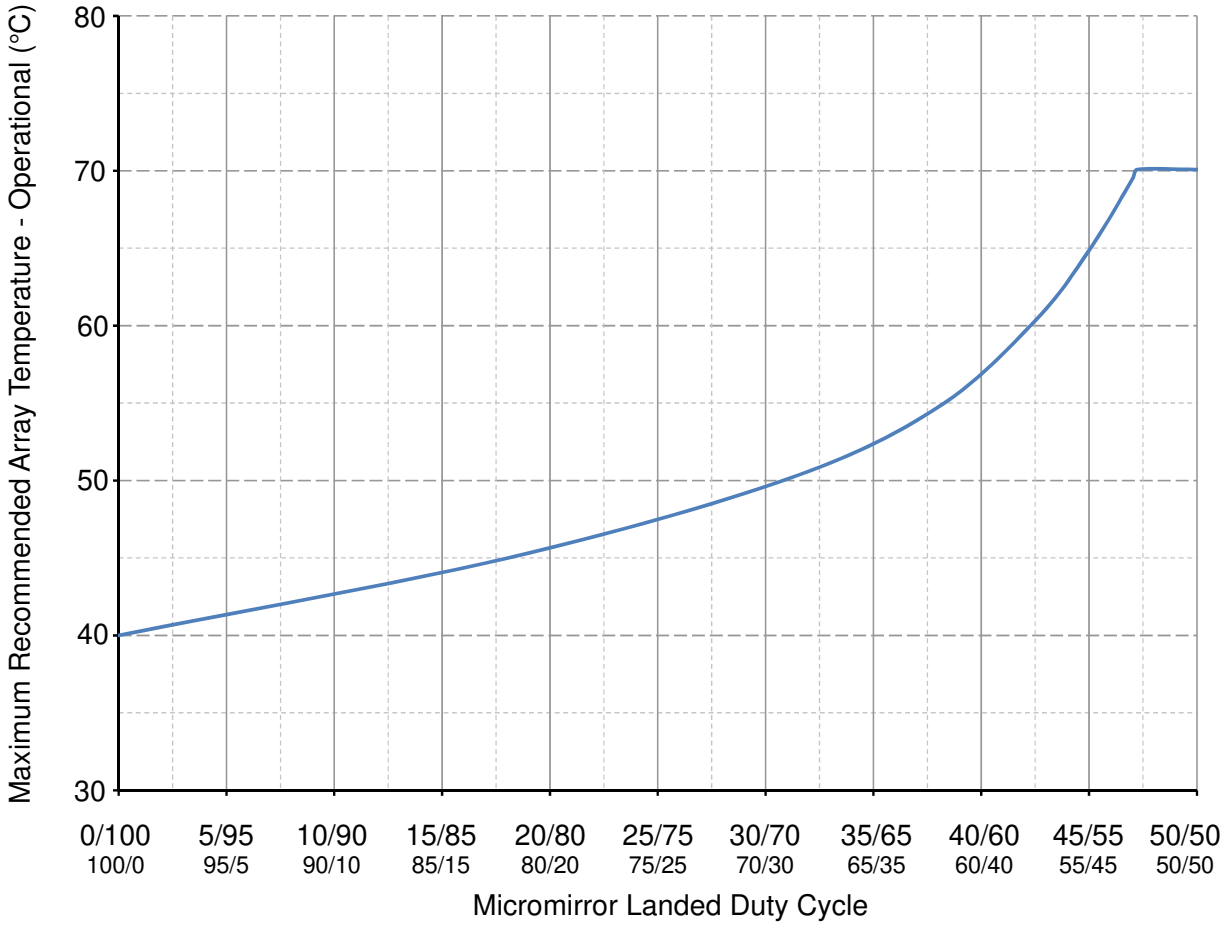

Figure 6-1. Max Recommended Array Temperature—Derating Curve

6.5 Thermal Information

THERMAL METRIC	DLP670S FYR Package 350 PINS	UNIT
Thermal resistance, active area to test point 1 (TP1)(1)	0.60	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the package within the temperature range specified in Section 6.4. The total heat load on the DMD is largely driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems must be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

6.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT VOLTAGES						
V_{OH}	High level output voltage	V_{CC} = 1.8 V, I_{OH} = –2 mA	0.8 × V_{CC}			V
V_{OL}	Low level output voltage	V_{CC} = 1.95 V, I_{OL} = 2 mA			0.2 × V_{CC}	V
CURRENTS						
I_{OZ}	High impedance output current	V_{CC} = 1.95 V	–40		25	µA
I_{IL}	Low level input current	V_{CC} = 1.95 V, VI = 0	–1			µA
I_{IH}	High level input current(1)	V_{CC} = 1.95 V, VI = V_{CC}			110	µA
I_{CC}	Supply current VCC	V_{CC} = 1.95 V			1200	mA
I_{CCI}	Supply current VCCI	V_{CCI} = 1.95 V			330	mA
I_{OFFSET}	Supply current VOFFSET(2)	V_{OFFSET} = 10.5 V			13	mA
I_{BIAS}	Supply current VBIAS(2) (3)	V_{BIAS} = 18.5 V			–4	mA
I_{RESET}	Supply current VRESET(3)	V_{RESET} = –14.5 V			9	mA
SUPPLY POWER						
P_{TOTAL}	Total Supply Power Dissipation				3320	mW

(1) Applies to LVCMOS pins only. Excludes LVDS pins and test pad pins.
(2) To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than the specified limit in Section 6.4.
(3) To prevent excess current, the supply voltage delta |VBIAS – VRESET| must be less than specified limit in Section 6.4.

6.7 Capacitance at Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{I_lvds}	LVDS Input Capacitance 2xLVDS	f = 1 MHz			20	pF
$C_{I_nonlvds}$	Non-LVDS Input capacitance	f = 1 MHz			20	pF
C_{I_tdiode}	Temp Diode Input capacitance	f= 1 MHz			30	pF
C_O	Output Capacitance	f = 1 MHz			20	pF

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6.8 Timing Requirements

			MIN	NOM	MAX	UNIT
SCP(1)						
t_r	Rise time	20% to 80% reference points			30	ns
t_f	Fall time	80% to 20% reference points			30	ns
LVDS(2)						
t_r	Rise slew rate	20% to 80% reference points	0.7	1		V/ns
t_f	Fall slew rate	80% to 20% reference points	0.7	1		V/ns
t_C	Clock Cycle	DCLK_A, LVDS pair	2.5			ns
t_C	Clock Cycle	DCLK_B, LVDS pair	2.5			ns
t_C	Clock Cycle	DCLK_C, LVDS pair	2.5			ns
t_C	Clock Cycle	DCLK_D, LVDS pair	2.5			ns
t_W	Pulse Width	DCLK_A LVDS pair	1.19	1.25		ns
t_W	Pulse Width	DCLK_B LVDS pair	1.19	1.25		ns
t_W	Pulse Width	DCLK_C LVDS pair	1.19	1.25		ns
t_W	Pulse Width	DCLK_D LVDS pair	1.19	1.25		ns
t_{Su}	Setup Time	D_A(15:0) before DCLK_A, LVDS pair	0.325			ns
t_{Su}	Setup Time	D_B(15:0) before DCLK_B, LVDS pair	0.325			ns
t_{Su}	Setup Time	D_C(15:0) before DCLK_C, LVDS pair	0.325			ns
t_{Su}	Setup Time	D_D(15:0) before DCLK_D, LVDS pair	0.325			ns
t_{Su}	Setup Time	SCTRL_A before DCLK_A, LVDS pair	0.325			ns
t_{Su}	Setup Time	SCTRL_B before DCLK_B, LVDS pair	0.325			ns
t_{Su}	Setup Time	SCTRL_C before DCLK_C, LVDS pair	0.325			ns
t_{Su}	Setup Time	SCTRL_D before DCLK_D, LVDS pair	0.325			ns
t_h	Hold Time	D_A(15:0) after DCLK_A, LVDS pair	0.145			ns
t_h	Hold Time	D_B(15:0) after DCLK_B, LVDS pair	0.145			ns
t_h	Hold Time	D_C(15:0) after DCLK_C, LVDS pair	0.145			ns
t_h	Hold Time	D_D(15:0) after DCLK_D, LVDS pair	0.145			ns
t_h	Hold Time	SCTRL_A after DCLK_A, LVDS pair	0.145			ns
t_h	Hold Time	SCTRL_B after DCLK_B, LVDS pair	0.145			ns
t_h	Hold Time	SCTRL_C after DCLK_C, LVDS pair	0.145			ns
t_h	Hold Time	SCTRL_D after DCLK_D, LVDS pair	0.145			ns
LVDS(2)						
t_{SKEW}	Skew Time	Channel B relative to Channel A(3) (4), LVDS pair	–1.25		+1.25	ns
t_{SKEW}	Skew Time	Channel D relative to Channel C(5) (6), LVDS pair	–1.25		+1.25	ns

(1) See Figure 6-3 for Rise Time and Fall Time for SCP.
(2) See Figure 6-5 for Timing Requirements for LVDS.
(3) Channel A (Bus A) includes the following LVDS pairs: DCLK_AN and DCLK_AP, SCTRL_AN and SCTRL_AP, D_AN(15:0) and D_AP(15:0).
(4) Channel B (Bus B) includes the following LVDS pairs: DCLK_BN and DCLK_BP, SCTRL_BN and SCTRL_BP, D_BN(15:0) and D_BP(15:0).
(5) Channel C (Bus C) includes the following LVDS pairs: DCLK_CN and DCLK_CP, SCTRL_CN and SCTRL_CP, D_CN(15:0) and D_CP(15:0).
(6) Channel D (Bus D) includes the following LVDS pairs: DCLK_DN and DCLK_DP, SCTRL_DN and SCTRL_DP, D_DN(15:0) and D_DP(15:0).

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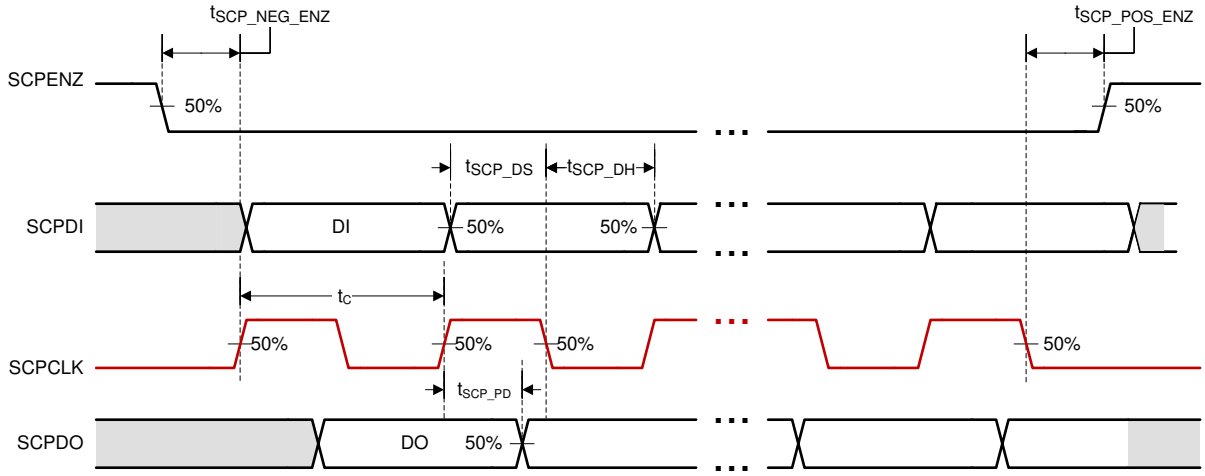

Figure 6-2. SCP Timing Requirements

A. See Section 6.4 for f_{SCPCLK}, t_{SCP_DS}, t_{SCP_DH} and t_{SCP_PD} specifications.
B. SCPCLK falling–edge capture for SCPDI.
C. SCPCLK rising–edge launch for SCPDO.
D. See Equation 1.

$$f_{SCPCLK} = \frac{1}{t_C} \quad (1)$$

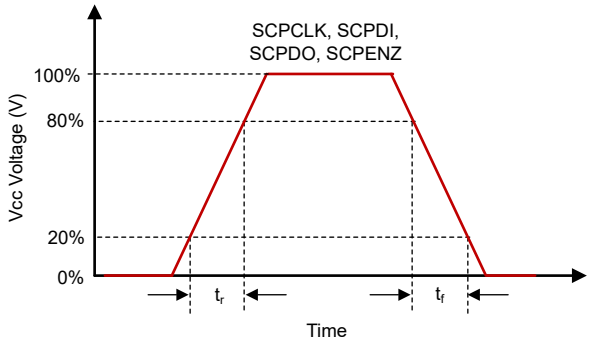

Figure 6-3. SCP Requirements for Rise and Fall

See Section 6.8 for t_r and t_f specifications and conditions.

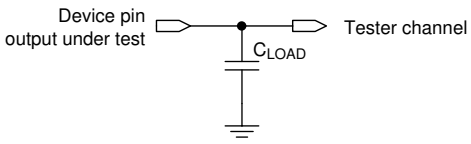

Figure 6-4. Test Load Circuit for Output Propagation Measurement

For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. System designers must use IBIS or other simulation tools to correlate the timing reference load to a system environment.

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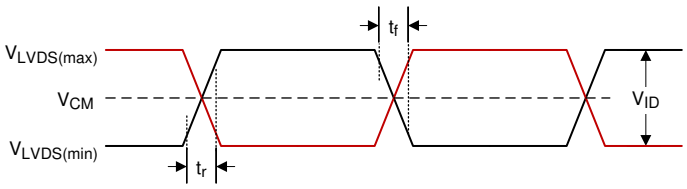

A. See Equation 2 and Equation 3 .

Figure 6-5. LVDS Waveform Requirements

$$V_{LVDS\,(max)} = V_{CM\,(max)} + \left|\frac{1}{2} \times V_{ID\,(max)}\right| \quad (2)$$

$$V_{LVDS\,(min)} = V_{CM\,(min)} - \left|\frac{1}{2} \times V_{ID\,(max)}\right| \quad (3)$$

See Section 6.4 for V_{CM}, V_{ID}, and V_{LVDS} specifications and conditions.

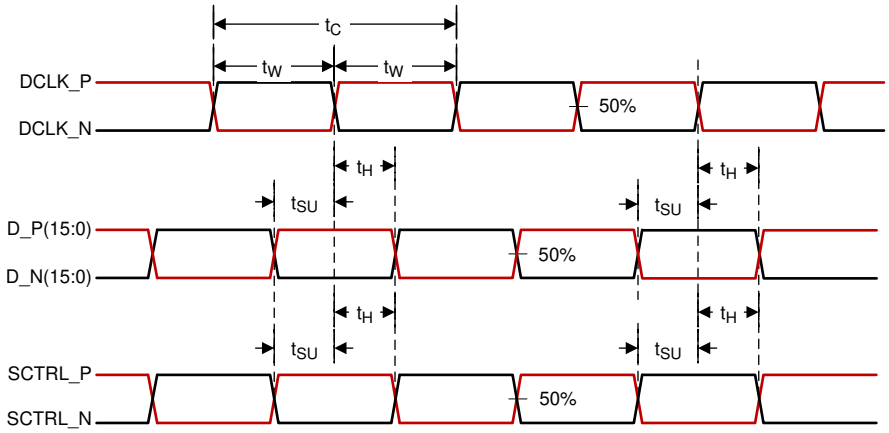

Figure 6-6. Timing Requirements

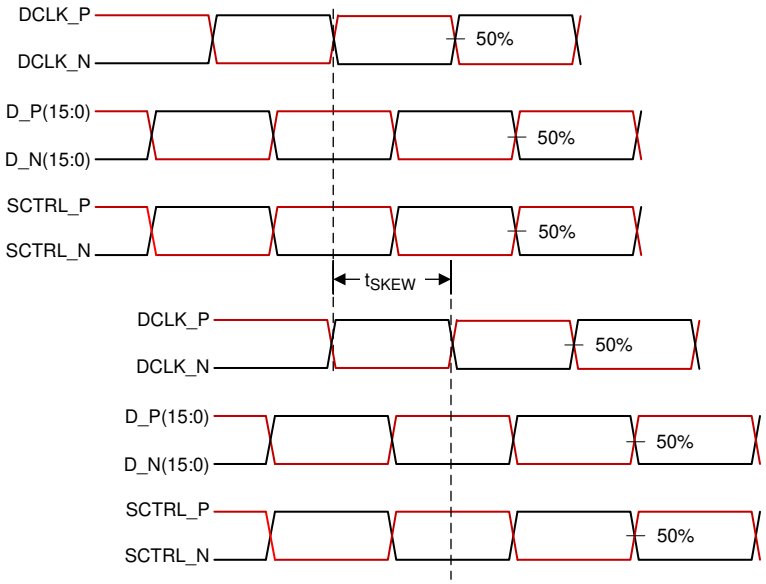

Figure 6-7. LVDS Interface Channel Skew Definition

See Section 6.8 for timing requirements and LVDS pairs per channel (bus) defining D_P(15:0) and D_N(15:0).

6.9 Typical Characteristics

When the DMD is controlled by the DLPC900, the digital controller has four modes of operation:

A. Video mode

B. Video pattern mode

C. Pre-stored pattern mode

D. Pattern on-the-fly mode

In video mode (A), the 24-bit frames displayed on the DMD are the same as the 24-bit video input source and frame rates. In video pattern mode (B), the V_{SYNC} rates displayed on the DMD are linked to the incoming video source V_{SYNC} rates but the overall pattern rates depend upon the configured bit depth. In modes B, C, and D, the pattern rates depend on the bit depth as shown in Table 6-1.

Table 6-1. DLP670S Pattern Rate versus Bit Depth using DLPC900

BIT DEPTH	VIDEO PATTERN MODE (Hz)	PRE-STORED or PATTERN ON-THE-FLY MODE (Hz)
1	2880	9523
2	1440	2915
3	960	2283
4	720	1302
5	480	769
6	480	672
7	360	500
8	247	247

6.10 System Mounting Interface Loads

Table 6-2. System Mounting Interface Loads

PARAMETER	MIN	NOM	MAX	UNIT
When loads are applied to the electrical and thermal interface area				
Maximum load to be applied to the electrical interface area(1)			111	N

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Table 6-2. System Mounting Interface Loads (continued)

PARAMETER	MIN	NOM	MAX	UNIT
Maximum load to be applied to the thermal interface area(1)			111	N
When a load is applied to only the electrical interface area				
Maximum load to be applied to the electrical interface area(1)			222	N
Maximum load to be applied to the thermal interface area(1)			0	N

(1) Apply the load uniformly in the corresponding areas shown in Figure 6-8.

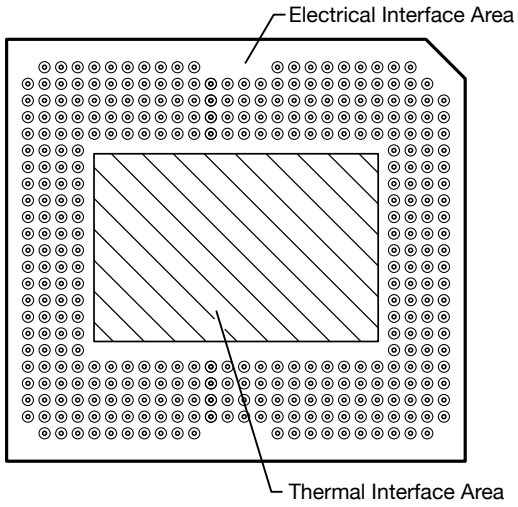

Figure 6-8. System Mounting Interface Loads

6.11 Micromirror Array Physical Characteristics

Table 6-3. Micromirror Array Physical Characteristics

PARAMETER DESCRIPTION		VALUE	UNIT
Number of active columns(1)	M	2716	micromirrors
Number of active rows (1)	N	1600	micromirrors
Micromirror (pixel) pitch (1)	P	5.4	µm
Micromirror active array width (1)	Micromirror pitch × number of active columns	14.6664	mm
Micromirror active array height (1)	Micromirror pitch × number of active rows	8.6400	mm
Micromirror active border (All four sides)(2)	Pond of micromirrors (POM)	20	micromirrors / side

(1) See Figure 6-9.
(2) The structure and qualities of the border around the active array includes a band of partially functional micromirrors referred to as the pond of mirrors (POM). These micromirrors are structurally and electrically prevented from tilting toward the bright or ON state but still require an electrical bias to tilt toward the OFF state.

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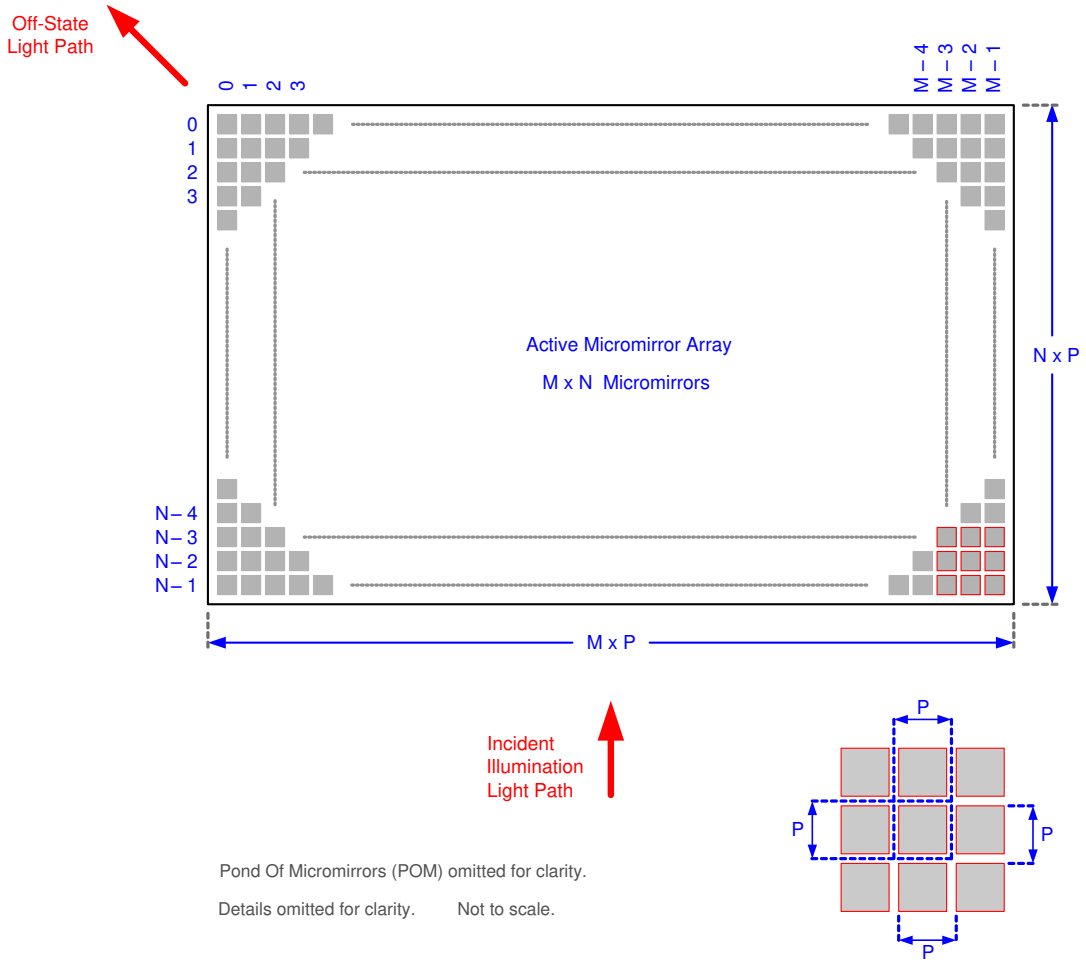

Figure 6-9. Micromirror Array Physical Characteristics

Refer to *Section 6.11* table for M, N, and P specifications.

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6.12 Micromirror Array Optical Characteristics

Table 6-4. Micromirror Array Optical Characteristics

PARAMETER	TEST CONDITION	MIN	NOM	MAX	UNIT
Mirror tilt angle (1) (2) (3) (4)	Landed State	15.6	17.5	18.4	degrees
Micromirror crossover time (5)	Typical Performance		1	3	µS
Micromirror switching time (6)	Typical Performance	10			
Number of out-of-specification micromirrors (7)	Adjacent micromirrors			0	micromirrors
	Non-Adjacent micromirrors			10	
DMD Photopic Efficiency(8)	420 nm – 700 nm		65%		

(1) Measured relative to the plane formed by the overall micromirror array
(2) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.
(3) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable nonuniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations, system contrast variations, and optical power variations.
(4) When the micromirror array is landed (not parked), the tilt direction of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of 1 results in a micromirror landing in the ON State direction. A binary value of 0 results in a micromirror landing in the OFF State direction. See Figure 6-10.
(5) The time required for a micromirror to nominally transition from one landed state to the opposite landed state.
(6) The minimum time between successive transitions of a micromirror.
(7) An out-of-specification micromirror is defined as a micromirror that is unable to transition between the two landed states within the specified micromirror switching time.
(8) Efficiency numbers assume 35-degree illumination angle, F/2.4 illumination and collection cones, uniform source spectrum, and uniform pupil illumination.

- Window Transmission 94% (double Pass, Through Two Window Surfaces)
- Micromirror Reflectivity 88%
- Array Diffraction Efficiency 84% (@f/2.4)
- Array Fill Factor 93%

Efficiency numbers assume 100% electronic mirror duty cycle and do not include optical overfill loss. Note that this number is specified under conditions described above and deviations from the specified conditions result in decreased efficiency.

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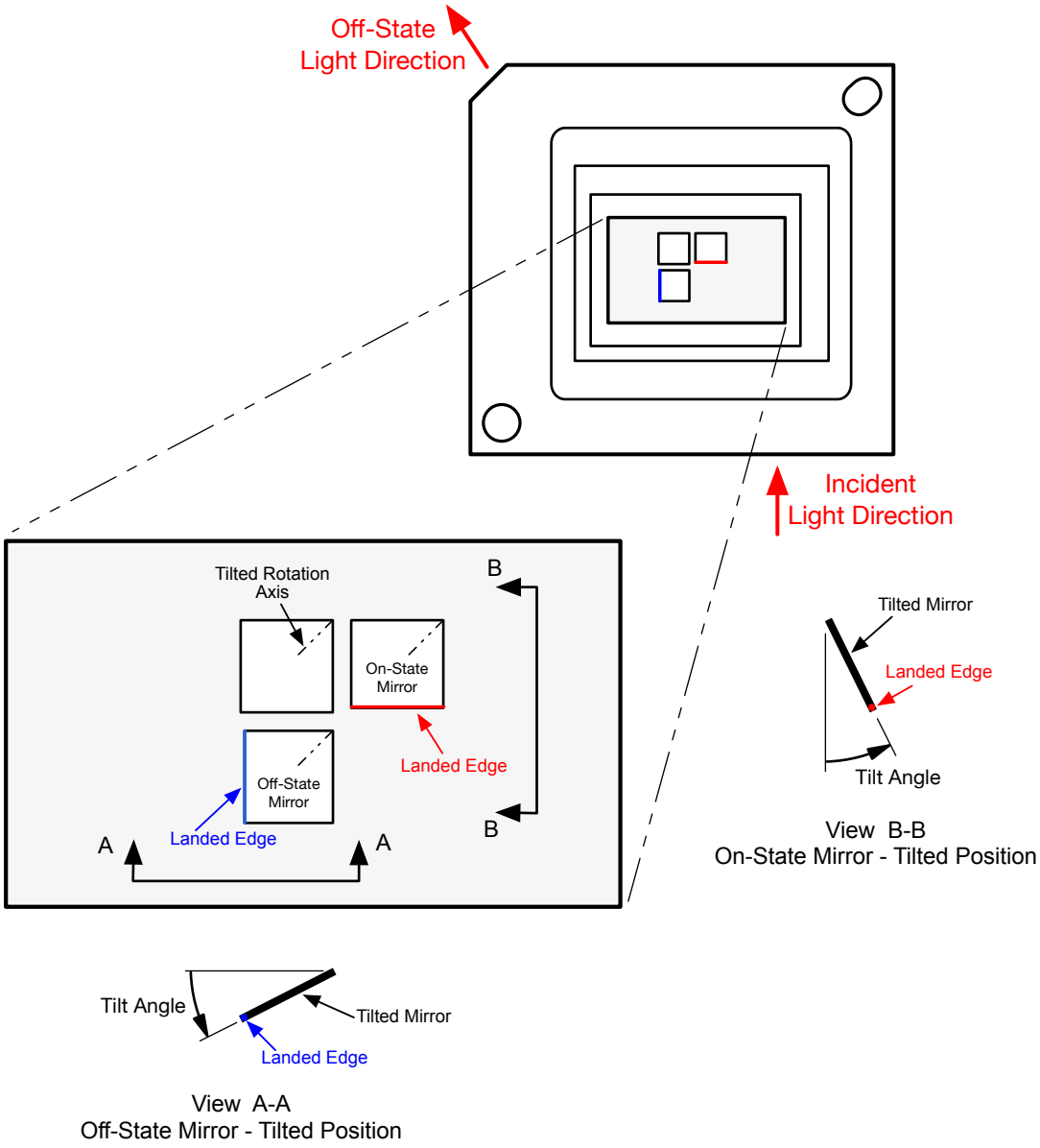

Figure 6-10. Micromirror Landed Orientation and Tilt

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6.13 Window Characteristics

Table 6-5. DMD Window Characteristics

PARAMETER(1)	CONDITIONS	MIN	NOM	MAX	UNIT
Window material	Corning Eagle XG				
Window refractive index	at wavelength 546.1 nm		1.5119		
Window aperture	See Note (2)				
Illumination overfill	Refer to Section 7.5.3				
Window transmittance, single–pass through both surfaces and glass (3)	Minimum within the wavelength range 420 nm to 680 nm. Applies to all angles 0° to 30° AOI.	97%			
	Average over the wavelength range 420 nm to 680 nm. Applies to all angles 30° to 45° AOI.	97%			

(1) See Section 7.5 for more information.
(2) For details on the size and location of the window aperture, see the Mechanical ICD in the Mechanical, Packaging, and Orderable Information section of this data sheet.
(3) See the TI *Wavelength Transmittance Considerations for DLP® DMD Window Application Note*.

6.14 Chipset Component Usage Specification

Reliable function and operation of the DLP670S DMD requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology is the TI technology and devices for operating or controlling a DLP DMD.

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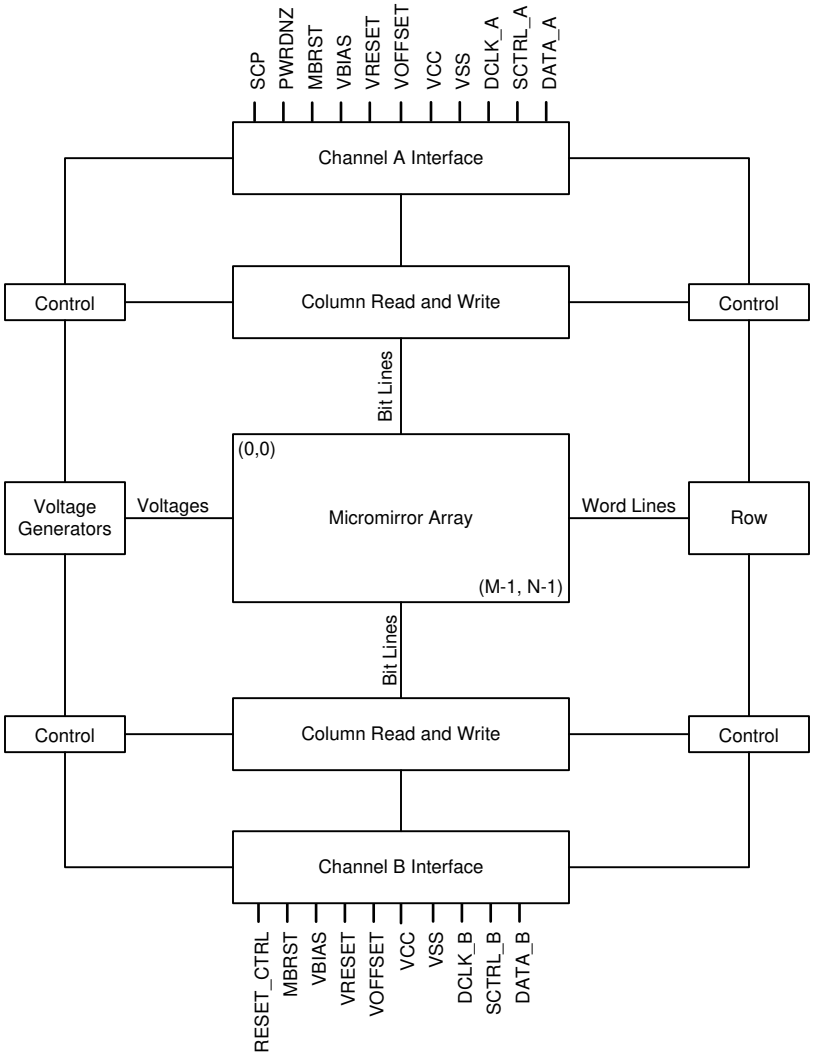
7 Detailed Description

7.1 Overview

The DLP670S DMD is a 0.67-inch diagonal spatial light modulator which consists of an array of highly reflective aluminum micromirrors. The DMD is an electrical input, optical output micro-electrical-mechanical system (MEMS). The input data electrical interface is Low Voltage Differential Signaling (LVDS). The DMD consists of a two-dimensional array of 1-bit CMOS memory cells. The array is organized in a grid of M memory cell columns by N memory cell rows. Refer to the Section 7.2 . The positive or negative deflection angle of the micromirrors can be individually controlled by changing the address voltage of underlying CMOS addressing circuitry and micromirror reset signals (MBRST).

The DMD is one part of a chipset comprising of the DLP670S DMD and the DLPC900 Controller. To ensure reliable operation, the DLPC900 Controller must always be used to control the DLP670S DMD.

7.2 Functional Block Diagram



Channels C and D not shown. For pin details on Channels A, B, C, and D, refer to Section 5 and LVDS Interface section of Section 6.8.
RESET_CTRL is used in applications when an external reset signal is required.

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7.3 Feature Description

7.3.1 Power Interface

The DMD requires five DC voltages: DMD_P3P3V, DMD_P1P8V, VOFFSET, VRESET, and VBIAS. DMD_P3P3V is a filtered version of the 3.3-V (P3P3V) supply received over the cables from the DLPC900 Controller Board. DMD_P3P3V is used on the DMD Board to create the other DMD voltages (DMD_P1P8V, VOFFSET, VRESET, and VBIAS) required for proper DMD operation. TI provides a DMD board reference design on TI.com to enable customers to see how these voltages are created as well and how the DMD board design is accomplished.

7.3.2 Timing

The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be considered. Figure 6-4 shows an equivalent test load circuit for the output under test. Timing reference loads are not intended as a precise representation of any particular system environment or depiction of the actual load presented by a production test. System designers must use IBIS or other simulation tools to correlate the timing reference load to a system environment. The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

7.4 Device Functional Modes

DMD functional modes are controlled by the DLPC900 Controller. See the DLPC900 Controller data sheet or contact a TI applications engineer.

7.5 Optical Interface and System Image Quality

Note

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, the projected image quality and the optical performance are contingent on compliance to the optical system operating conditions described in the following sections.

7.5.1 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area needs to be the same. This angle cannot exceed the nominal device micromirror tilt angle unless appropriate apertures are added in the illumination and projection pupils to block out flat-state and stray light from the projection lens. The micromirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the micromirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle, objectionable artifacts may occur in the projected image border region or active area.

7.5.2 Pupil Match

TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the projected image's border region and active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

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7.5.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view, and is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create reflections from the edge of the window aperture opening that may corrupt the intended projected image. Design the illumination optical system to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system optical architecture, overfill light may have to be further reduced below the suggested 10% level in order for the projected image to be acceptable.

7.6 Micromirror Array Temperature Calculation

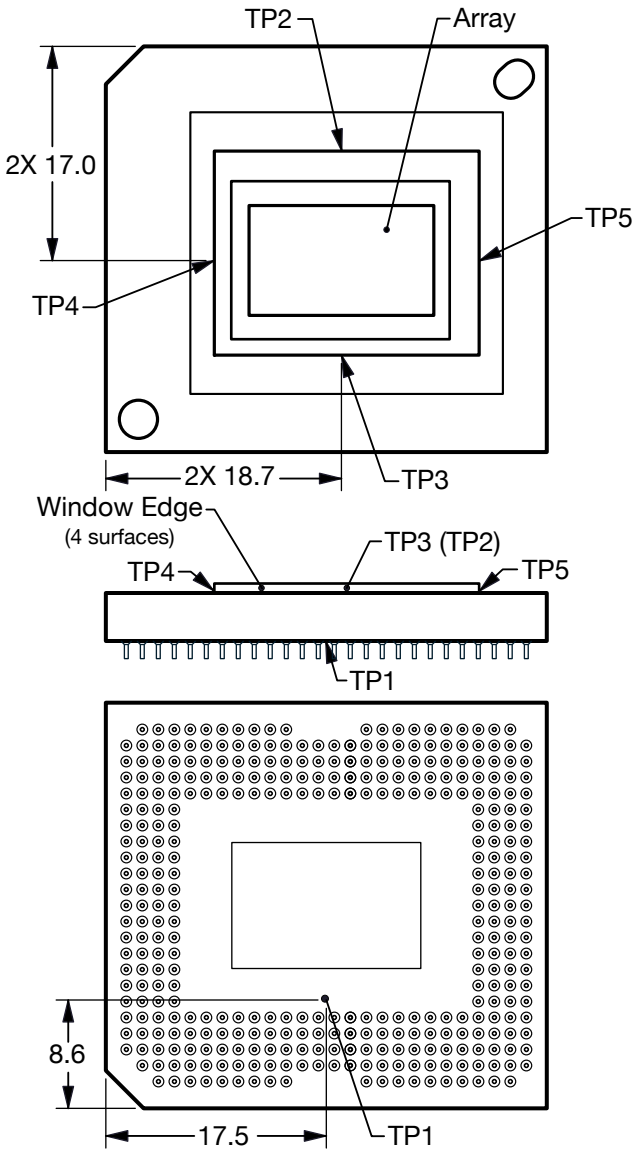

Figure 7-1. DMD Thermal Test Points

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Micromirror array temperature can be computed analytically from measurement points on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load. The relationship between micromirror array temperature and the reference ceramic temperature is provided by the following equations:

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY\text{-}TO\text{-}CERAMIC})$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION}$$

where

- T_{ARRAY} = Computed array temperature (°C)
- $T_{CERAMIC}$ = Measured ceramic temperature (°C) (measured at TP1 location)
- $R_{ARRAY\text{-}TO\text{-}CERAMIC}$ = Thermal resistance of package specified in Thermal Information from array to ceramic TP1 (°C/Watt)
- Q_{ARRAY} = Total DMD power on the array (W) (electrical + absorbed)
- $Q_{ELECTRICAL}$ = Nominal electrical power (W)
- $Q_{ILLUMINATION}$ = Illumination power absorbed (W)

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates, and operating frequencies. A nominal electrical power dissipation to use when calculating array temperature is 3.32 W. The absorbed power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. The factors used in determining the illumination power absorbed is shown in each of the examples below. Examples are included where the optical power has been determined by measuring the illumination power density, total illumination power, and screen lumens. The examples assume illumination distribution is 83.7% on the active array and 16.3% on the area outside the array.

7.6.1 Micromirror Array Temperature Calculation using Illumination Power Density

The equations below are valid for each DMD in a single chip or multi-chip DMD system.

- $Q_{ILLUMINATION}$ = ($Q_{INCIDENT}$ × DMD average thermal absorptivity) (W)
- $Q_{INCIDENT}$ = $ILL_{DENSITY}$ × ILL_{AREA} (W)
- $ILL_{DENSITY}$ = measured illumination optical power density at DMD (W/cm^2)
- ILL_{AREA} = illumination area on DMD (cm^2)
- DMD average thermal absorptivity = 0.40

$Q_{ELECTRICAL}$ = 3.32 W

Array size = 14.6664 mm × 8.6400 mm = 1.267 cm^2

$ILL_{DENSITY}$ = 31 W/cm^2 (measured)

$T_{CERAMIC}$ = 50.0 °C (measured)

ILL_{AREA} = 1.267 cm^2 / (83.7%) = 1.512 cm^2

$Q_{INCIDENT}$ = 31 W/cm^2 × 1.512 cm^2 =46.9 W

Q_{ARRAY} = 3.32 W + (46.9 W × 0.40) = 22.1 W

T_{ARRAY} = 50.0 °C + (22.1 W × 0.60 °C/W) = 63.3 °C

7.6.2 Micromirror Array Temperature Calculation using Total Illumination Power

The equations below are valid for each DMD in a single chip or multi-chip DMD system.

- $Q_{ILLUMINATION}$ = ($Q_{INCIDENT}$ × DMD average thermal absorptivity) (W)
- $Q_{INCIDENT}$ = measured total illumination optical power at DMD (W)
- DMD average thermal absorptivity = 0.40

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$Q_{ELECTRICAL}$ = 3.32 W

$Q_{INCIDENT}$ = 46.9 W (measured)

$T_{CERAMIC}$ = 50.0 °C (measured)

Q_{ARRAY} = 3.32 W + (46.9 W × 0.40) = 22.1 W

T_{ARRAY} = 50.0 °C + (22.1 W × 0.60 °C/W) = 63.3 °C

7.6.3 Micromirror Array Temperature Calculation using Screen Lumens

The equations below are valid for a single chip DMD system with spectral efficiency of 300 lumens/Watt.

- $Q_{ILLUMINATION}$ = SL × C_{L2W} (W)
- SL = measured ANSI screen lumens (lm)
- C_{L2W} = Conversion constant for screen lumens to power absorbed on DMD (Watts/Lumen)

$Q_{ELECTRICAL}$ = 3.32 W

C_{L2W} = 0.00266 W/lm

SL = 7000 lm (measured)

$T_{CERAMIC}$ = 50.0 °C (measured)

Q_{ARRAY} = 3.32 W + (0.00266 W/lm × 7000 lm) = 21.94 W

T_{ARRAY} = 50.0 °C + (21.94 W × 0.60 °C/W) = 63.2 °C

7.7 Micromirror Landed-On/Landed-Off Duty Cycle

7.7.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the On state versus the amount of time the same micromirror is landed in the Off state.

As an example, a landed duty cycle of 100/0 indicates that the referenced pixel is in the On state 100% of the time and in the Off state 0% of the time. Additionally, a landed duty cycle of 0/100 indicates that the pixel is in the Off state 100% of the time and in the On state 0% of the time. Likewise, 50/50 indicates that the pixel is On 50% of the time and Off 50% of the time.

Note

When assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (On or Off), the two numbers (percentages) always add to 100.

7.7.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD usable life.

Note that it is the symmetry or asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

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7.7.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD temperature and landed duty cycle interact to affect the DMD usable life, and this interaction can be exploited to reduce the impact that an asymmetrical landed duty cycle has on the DMD usable life. This is quantified in the derating curve shown in Figure 6-1. The importance of this curve is that:

- All points along this curve represent the same usable life.
- All points above this curve represent lower usable life (and the further away from the curve, the lower the usable life).
- All points below this curve represent higher usable life (and the further away from the curve, the higher the usable life).

In practice, this curve specifies the maximum operating DMD temperature that the DMD operates at for a given long-term average landed duty cycle.

7.7.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the Landed Duty Cycle of a given pixel follows from the input image content being displayed by that specific pixel regardless if the illumination is turned on or off.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel experiences a 100/0 Landed Duty Cycle during that time period. Likewise, when displaying pure-black, the pixel experiences a 0/100 Landed Duty Cycle.

If the use case involves inputting grayscale (8-bit) input images, between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the Landed Duty Cycle tracks one-to-one with the grayscale value, as shown in Table 7-1.

Table 7-1. Grayscale Value and Landed Duty Cycle

Grayscale Value	Landed Duty Cycle
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

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Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and blue) for the given pixel as well as the color cycle time for each primary color, where “color cycle time” is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

During a given period of time, the landed duty cycle of a given pixel can be calculated as follows:

- Landed Duty Cycle = (Red_Cycle_% × Red_Scale_Value) + (Green_Cycle_% × Green_Scale_Value) + (Blue_Cycle_% × Blue_Scale_Value)

Where

- Red_Cycle_%, Green_Cycle_%, and Blue_Cycle_%, represent the percentage of the frame time that Red, Green, and Blue are displayed (respectively) to achieve the desired white point. (1)

For example, assume that the red, green, and blue color cycle times are 50%, 20%, and 30% respectively (in order to achieve the desired white point), then the Landed Duty Cycle for various combinations of red, green, blue color intensities are as shown in Table 7-2 and Table 7-3.

Table 7-2. Example Landed Duty Cycle for Full-Color, Color Percentage

Red Cycle Percentage	Green Cycle Percentage	Blue Cycle Percentage
50%	20%	30%

Table 7-3. Example Landed Duty Cycle for Full-Color

Red Scale Value	Green Scale Value	Blue Scale Value	Landed Duty Cycle
0%	0%	0%	0/100
100%	0%	0%	50/50
0%	100%	0%	20/80
0%	0%	100%	30/70
12%	0%	0%	6/94
0%	35%	0%	7/93
0%	0%	60%	18/82
100%	100%	0%	70/30
0%	100%	100%	50/50
100%	0%	100%	80/20
12%	35%	0%	13/87
0%	35%	60%	25/75
12%	0%	60%	24/76
100%	100%	100%	100/0

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The DMD is a spatial light modulator, which reflects incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data being used.

The DLP670S DMD is controlled by two DLPC900 controllers. The DMD itself receives bit planes through a 2xLVDS input data bus and, when input control commands dictate, activates the controls which update the mechanical state of the DMD mirrors. In combination with the DLPC900 Controllers, the chipset enables four unique modes of system level operation:

- Video Mode - 24 bit video signals presented to inputs of the DLPC900 Controllers appear on the DMD. The DMD mirrors are updated in a PWM fashion to construct the 24 bit video data. This mode is similar to standard DLP Display projector use cases.
- Video Pattern Mode - the user can define periods of time for specific patterns to be displayed on the DMD. Those patterns are provided via the input video interface and are constrained to input video timing parameters. This mode is optimal for when the data to be presented is not known in advance of operation, or input data needs to be streamed or updated based on real-time processing conditions.
- Pre-stored Pattern Mode - the user can define the patterns in advance and build the pattern data into an on-board flash memory. Upon power up, the DLPC900 controllers immediately start reading and displaying those patterns. This mode is typically used in applications where the patterns to be used are known in advance and the patterns can all fit in the external flash memory. This mode typically provides the fastest pattern update rates.
- Pattern-on-the-Fly Pattern Mode - the user can download and update pattern data over the DLPC900 input USB data interface. This allows an external processor to modify and update patterns based on external processing decisions. This mode also provides streaming capability similar to the Video Pattern Mode except that the user will need to take into account delays involved with USB transmission of pattern data and control information.

The DLP670S provides solutions for many varied applications including structured light (3-D machine vision), 3-D printing, information projection, and lithography.

The DLP670S contains the most recent breakthrough micromirror technology called the TRP pixel. With a smaller pixel pitch of 5.4 µm and increased tilt angle of 17.5 degrees nominal, TRP chipsets enable higher resolution in a smaller form factor while maintaining high optical efficiency. DLP chipsets are a great fit for any system that requires high resolution and high output projection imaging.

8.2 Typical Application

3D machine vision is a typical embedded system applications for the DLP670S DMD. In this application, two DLPC900 devices control the pattern data being imaged from a DLP670S DMD onto the object being measured while an external camera system monitors the projected patterns as they appear on the object. An external microprocessor can then geometrically determine all 3D points of the object using the knowledge of the projected pattern provided to the object, the actual distorted pattern as captured by the camera, and the angle between the projector line-of-sight and the camera line-of-sight. This type of application diagram is shown in Figure 8-1. In this configuration, the DLPC900 controller supports a 24-bit parallel RGB video input from an external source computer or processor. The video input FPGA splits each 2716 x 1600 image frame into a left half and a right half with the left half feeding the primary DLPC900 and the right half feeding the secondary DLPC900. Each half consists of 1358 columns x 1600 rows plus any horizontal and vertical blanking at half the pixel clock rate. This system configuration supports still and motion video as well as sequential pattern modes.

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For more information, refer to the DLPC900 digital controller data sheet found on the DLPC900 Product Folder listed under Section 11.3.1.

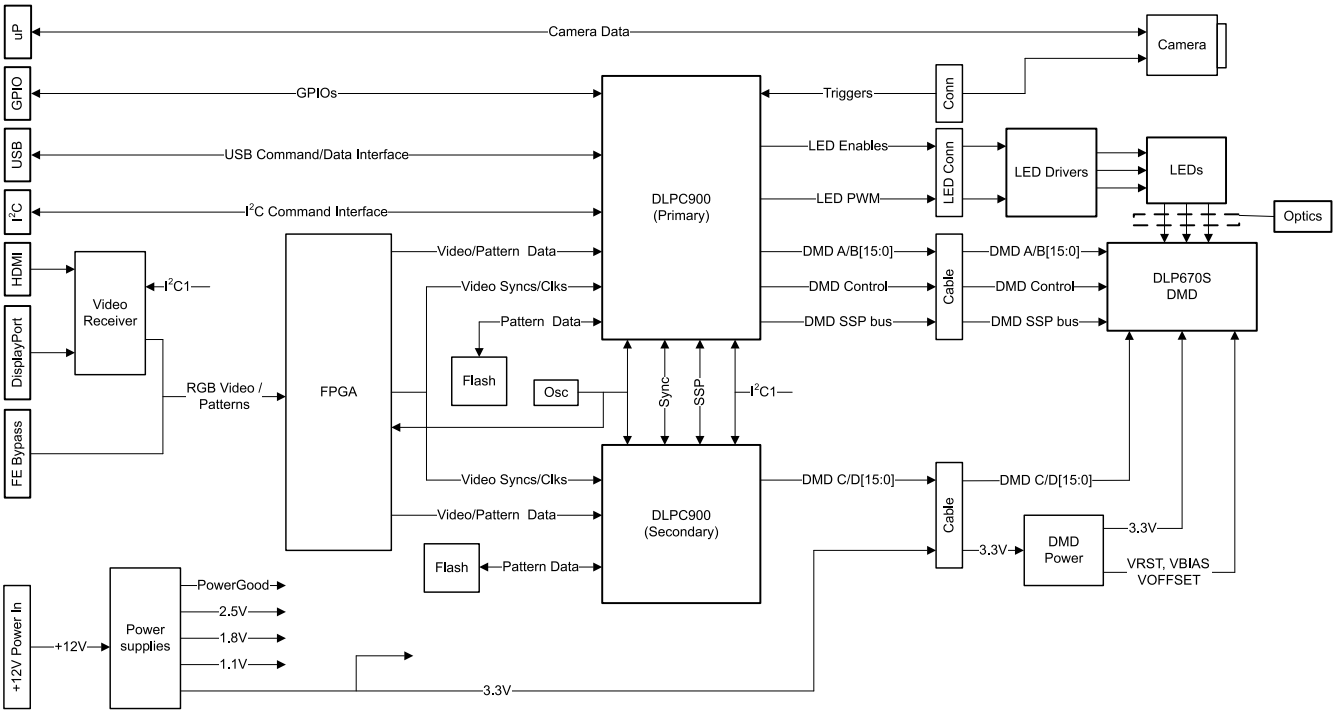

Figure 8-1. Typical DLP670S Application Diagram

8.2.1 Design Requirements

At the high level, typical DLP670S DMD systems include an illumination source (Lamp, LED, or Laser), an optical light engine containing both illumination and projection optics, mechanics, electronic components, power supplies, cooling systems, and software. The designer must first choose an illumination source and design the optical engine taking into consideration the optical relationship from the illumination source to the DMD, and from the DMD to the location of the projected image. The designer must then understand the electronic components of a DLP670S DMD system, part of which includes one or more PCBs which contain the DMD and Controllers. In the TI DLP670S based evaluation module design, the DLPC900 Controller board provides power, bit plane data, and control information to the DMD mounted on the DLP670S DMD board. The DLPC900 Controller board also interfaces to the user system, accepting image data based on user provided timing (software or hardware triggered) and providing that data in bit plane format to the DMD to be projected on the imaging target.

8.2.2 Detailed Design Procedure

A TI evaluation module design exists which shows how to connect the DLPC900 controller to the DMD. In creating a new board specific to a customer application, layout guidelines need to be followed to achieve a functional and reliable projection system. To complete the system, an optical module or light engine is required that contains the DLP670S DMD, associated illumination sources, optical elements, and necessary mechanical components. Care must be taken to understand and implement wise design decisions regarding the engineering aspects of illumination and projection optics, digital and analog electronics, software, and mechanical and thermal design principles.

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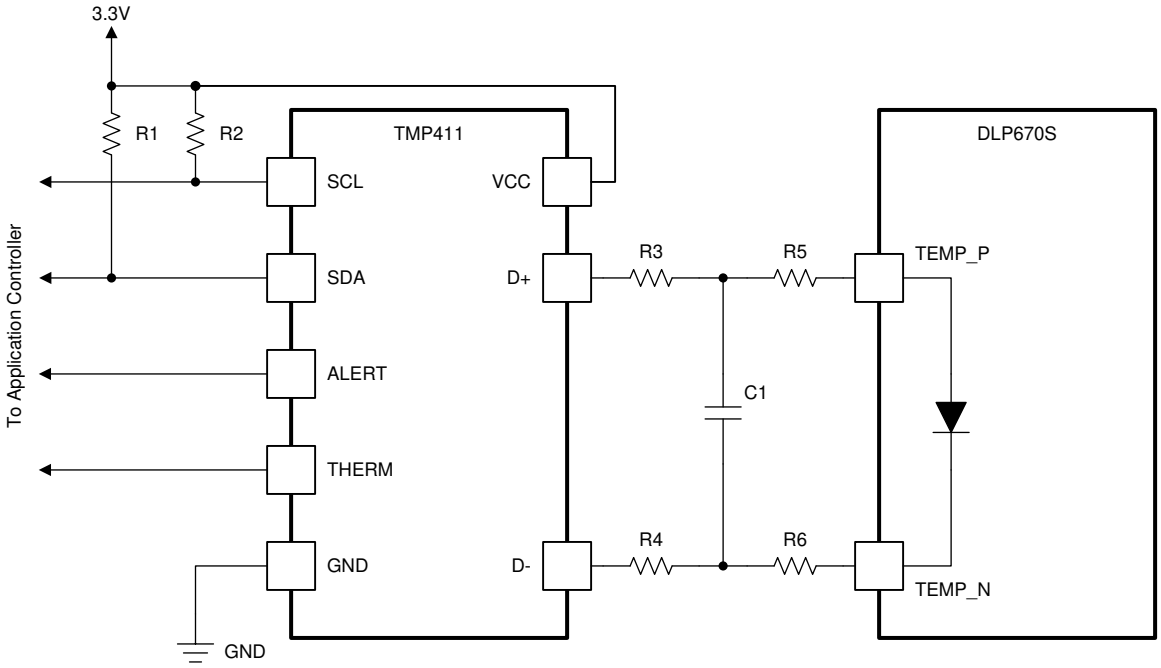
8.3 DMD Die Temperature Sensing

The DMD features a built-in thermal diode that measures the temperature at one corner of the die outside the micromirror array. The DMD thermal diode pins E16 and E17 can be connected to the TMP411 temperature sensor as shown in Figure 8-2, and an external processor can interface with the TMP411 temperature sensor over I^2C bus to allow monitoring of the DMD temperature. This temperature data can be leveraged to incorporate additional functionality in the overall system design such as adjusting illumination power, cooling fan speeds, TEC current inputs, and so forth, all with the idea of maintaining appropriate temperature control of the DMD.



A. Details omitted for clarity, see the DLPLCR67EVM evaluation module design for connections.
B. See the TMP411 datasheet for system board layout recommendation.
C. See the TMP411 datasheet and the DLPLCR67EVM design for suggested component values for R1, R2, R3, R4, and C1.
D. R5 = 0 Ω. R6 = 0 Ω. 0-Ω resistors need to be located close to the DMD package pins.

Figure 8-2. TMP411 Sample Schematic

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9 Power Supply Recommendations

The following power supplies are all required to operate the DMD:

- VSS
- VCC
- VCCI
- VBIAS
- VOFFSET
- VRESET

DMD power-up and power-down sequencing is very important. Sequencing is controlled by the DLPC900 Controller and through the DMD power supply design.

CAUTION

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to any of the prescribed power-up and power-down requirements may affect device reliability. See Figure 9-1 in Section 9.2 .

VBIAS, VCC, VCCI, VOFFSET, and VRESET power supplies must be coordinated during power-up and power-down operations. Failure to meet any of the below requirements results in a significant reduction in the DMD reliability and lifetime. Common ground VSS must also be connected.

9.1 DMD Power Supply Power-Up Procedure

- During power-up, VCC and VCCI must always start and settle before VOFFSET plus Delay1 specified in Table 9-1, VBIAS, and VRESET voltages are applied to the DMD.
- During power-up, it is a strict requirement that the voltage delta between VBIAS and VOFFSET must be within the specified limit shown in Section 6.4.
- During power-up, there is no requirement for the relative timing of VRESET with respect to VBIAS.
- Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements specified in Section 6.1, in Section 6.4, and in Figure 9-1.
- During power-up, LVCMOS input pins must not be driven high until after VCC and VCCI have settled at operating voltages listed in Section 6.4.

9.2 DMD Power Supply Power-Down Procedure

- During power-down, VCC and VCCI must be supplied until after VBIAS, VRESET, and VOFFSET are discharged to within the specified limit of ground. See Table 9-1.
- During power-down, it is a strict requirement that the voltage delta between VBIAS and VOFFSET must be within the specified limit shown in Section 6.4.
- During power-down, there is no requirement for the relative timing of VRESET with respect to VBIAS.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements specified in Section 6.1, in Section 6.4 , and in Figure 9-1.
- During power-down, LVCMOS input pins must be less than specified in Section 6.4.

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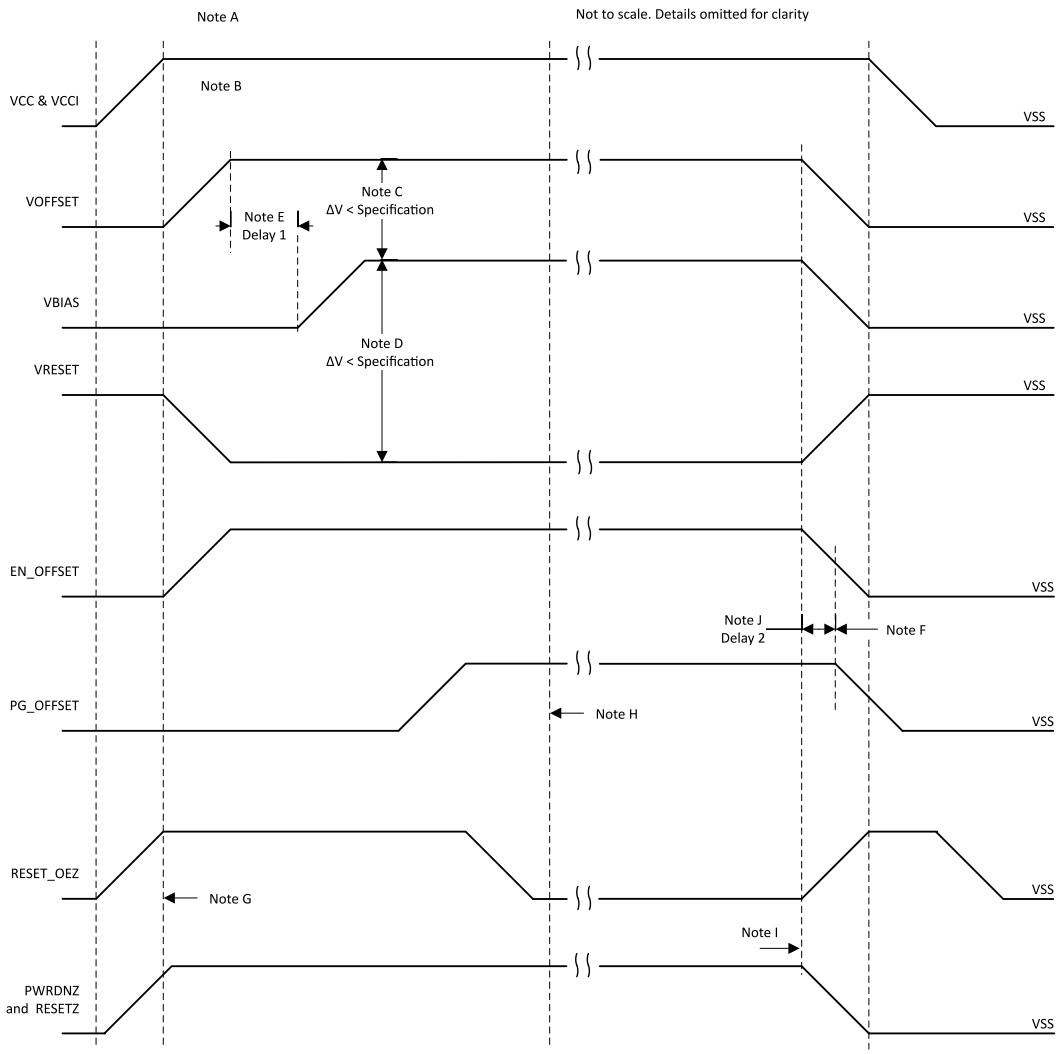

Figure 9-1. DMD Power Supply Requirements

A. See Section 6.4 , and the Pin Functions Table 5-1.
B. To prevent excess current, the supply voltage delta |VCCI – VCC| must be less than specified limit in Section 6.4.
C. To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than specified in Section 6.4.
D. To prevent excess current, the supply voltage delta |VBIAS – VRESET| must be less than specified limit in Section 6.4.
E. VBIAS must power up after VOFFSET has powered up, per the Delay1 specification in Table 9-1.
F. PG_OFFSET must turn off after EN_OFFSET has turned off, per the Delay2 specification in Table 9-1.
G. DLP controller software enables the DMD power supplies to turn on after RESET_OEZ is at logic high.
H. DLP controller software initiates the global VBIAS command.
I. After the DMD micromirror park sequence is complete, the DLP controller software initiates a hardware power-down that activates PWRDNZ and disables VBIAS, VRESET and VOFFSET.
J. Under power-loss conditions where emergency DMD micromirror park procedures are being enacted by the DLP controller hardware, EN_OFFSET may turn off after PG_OFFSET has turned off. The RESET_OEZ signal goes high prior to PG_OFFSET turning off to indicate the DMD micromirror has completed the emergency park procedures.

Table 9-1. DMD Power-Supply Requirements

Parameter	Description	Min	NOM	Max	Unit
Delay1	Delay from VOFFSET settled at recommended operating voltage to VBIAS power up	1	2		ms
Delay2	PG_OFFSET hold time after EN_OFFSET goes low	100			ns

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9.3 Restrictions on Hot Plugging and Hot Swapping

The DLP670S uses a state-of-the-art pixel node which enables smaller optics, higher resolution, and overall great performance and reliability as long as certain design-for-assembly methods are used. To maximize DMD reliability, Hot plugging or hot swapping DMDs **voids the DMD warranty conditions and must be avoided at all times**.

9.3.1 No Hot Plugging

Avoid hot plugging, the act of connecting the DMD to power supplies or data inputs that are already energized, to ensure maximum reliability of the DMD. Do not add or remove the DMD from a DMD socket unless all input power supplies of the DMD are at a potential equal to the local ground potential (VSS). This applies to a DMD incoming test station, a partially assembled product, a completed product under test, and a product in the field. This also applies to any cables, flex cables, or PCB connections which provide power to the DMD. Provide power as defined in the power-up scenario detailed in Section 9.1. Perform power down as defined in Section 9.2.

9.3.2 No Hot Swapping

To ensure maximum reliability of the DMD, avoid hot swapping, which is removing and replacing the DMD with DMD power supplies or data inputs that are already energized. Never add or remove the DMD from a DMD socket unless all input power supplies of the DMD are at a potential equal to the local ground potential (VSS). This applies to a DMD incoming test station, a partially assembled product, a completed product under test, and a product in the field. This also applies to any cables, flex cables, or PCB connections that provide power to the DMD. Provide power as defined in the power-up scenario detailed in Section 9.1. Perform power-down as defined in Section 9.2 .

9.3.3 Intermittent or Voltage Power Spike Avoidance

When DMD power or data and clock inputs are energized, twisting of the DMD, DMD socket, or DMD board must be avoided when trying to align the DMD within an optical engine. This twisting motion can create power intermittences or voltage spikes exceeding input power and data specifications of the DMD which may ultimately affect the DMD reliability. PCB power, data, clock, and control circuits must be de-energized before making or removing connections, including cables, connectors, probes, and bed-of-nails connections.

PCB and system design considerations must take into account ways to prevent external influence of DMD input power clock, data and control signals. Robust connectors must be used which are resistant to intermittent connections or noise spikes if jostled or vibrated. Connectors must be used which are rated to exceed the number of insertion or removal cycles expected in the application. External electromagnetic emitters must not be placed nearby these sensitive circuits unless adequate EMI shielding is properly used. Sufficient bulk decoupling and component decoupling capacitance as well as appropriate PCB layout techniques must be available for all electrical components within the DMD based "system" such that ground bounce does not occur. See the section on Section 10.1 for more layout information.

10 Layout

10.1 Layout Guidelines

10.1.1 Critical Signal Guidelines

The DLP670S DMD is one device in a chipset controlled by the DLPC900 controller. The following guidelines are targeted at designing a functioning PCB using this DLP670S DMD chipset. The DLP670S DMD board must be a high-speed multilayer PCB containing high-speed digital logic utilizing dual edge (DDR) LVDS signals at 400-MHz clock rates. Figure 10-1 shows the DLP670S signals and the recommendations needed from and to the DLPC900 controller devices. The DLPC900 device provides the data and control to the DMD. The TPS65145, LP38513 or equivalent devices supply power to the DMD.

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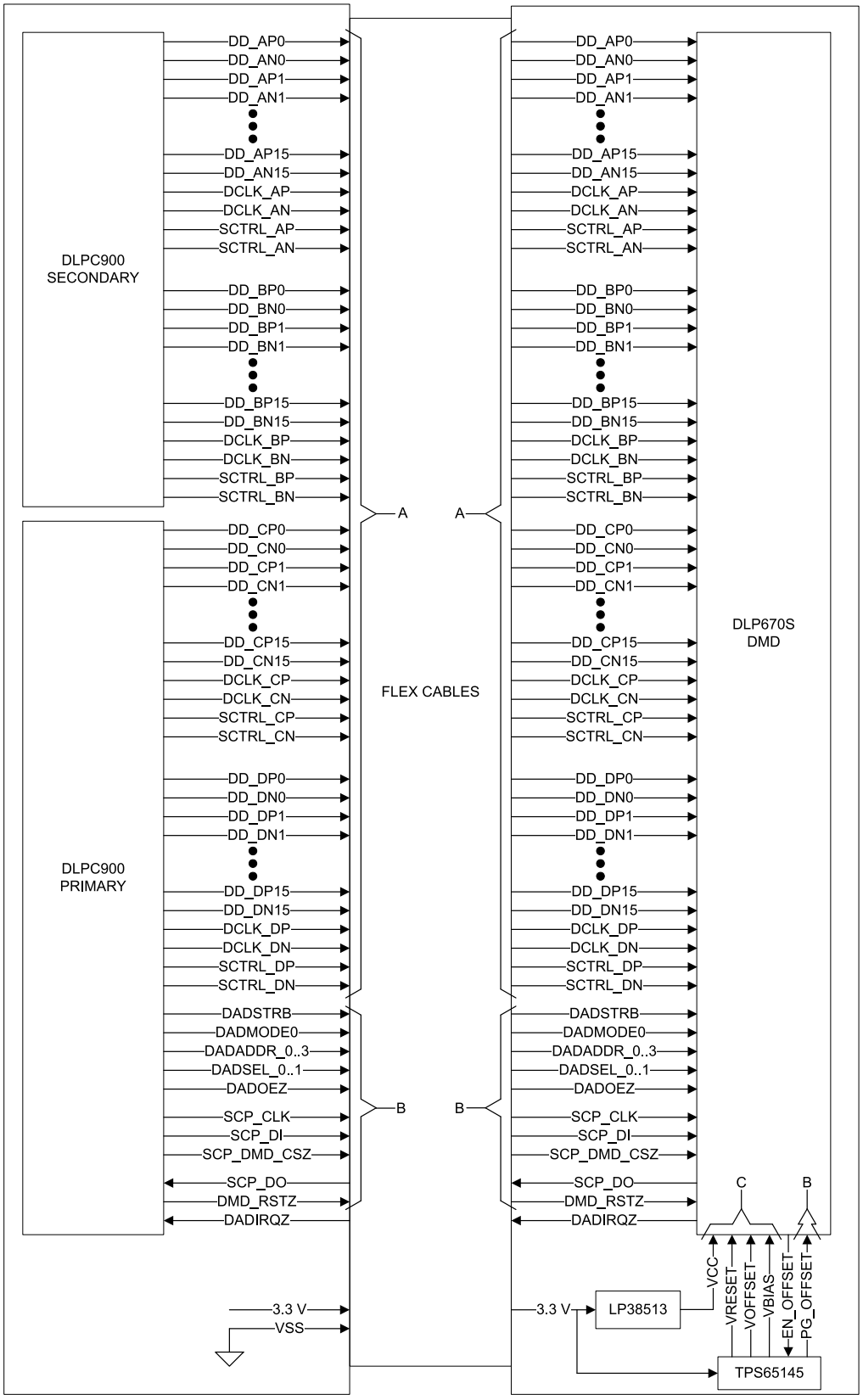

Figure 10-1. DLP670S DMD System Connections

Table 10-1. Layout Restrictions for Figure 10-1

Note	Signal Type	Guideline
A	Differential	Prevent signal noise
		Route 100 ±10-Ω resistor
		Intra-pair (P-to-N) length tolerance is ±12-mils.
		DD and SCTRL must be matched to the DCLK within ±150-mils.
		DCLK_C must be matched to DCLK_D within ±1.25-ns.
		DCLK_A must be matched to DCLK_B within ±1.25-ns.
		Do not switch routing layers except at the beginning and end of trace.
		Signal routing length must not exceed 375-mm.
B	Single-ended	Prevent signal noise
		Route single-ended signals 50 ±5-Ω
		No length match requirement
C	Power	VRESET, VOFFSET, VBIAS, and VCC at the DMD must be kept within the operating limits specified in the data sheet.
		Provide proper amount of decoupling capacitance for each voltage at the DMD

10.1.2 Power Connection Guidelines

The following are recommendations for the power connections to the DMD or DMD PCB:

- Solid planes are **required** for DMD_P3P3V(3.3V), DMD_P1P8V and Ground.
- TI strongly recommends partial power planes are used for VOFFSET, VRESET, and VBIAS.
- VOFFSET, VBIAS, VRESET, VCC, and VCCI power rails must be kept within the specified operating range. *This includes effects from ripple and DC error.*
- To accommodate power supply transient current requirements, adequate decoupling capacitance must be placed as near the DMD VOFFSET, VBIAS, VRESET, VCC, and VCCI pins as possible.
- Do not swap DMDs while the DMD is still powered on (this is called hot swapping). All DMD power supply rails and signals must be 0 volts (not driven) before connecting or disconnecting the DMD physical interface.
- Do not allow power to be applied to the DMD when one or more signal pins are not being driven.
- Decoupling capacitor locations for the DMD must be as close as possible to the DMD. The pads of the capacitors must be connected to at least two or three vias to get a very low impedance to ground as shown in Figure 10-3. Furthermore, the capacitor must be in the flow of the power trace as it goes to the input of the DMD.
- It is extremely important to adhere to the Section 9.1 and Section 9.2 and do not allow the DMD power-supply levels to be outside of the recommended operating conditions specified in the DMD data sheet.

These figures show examples of bypass decoupling capacitor layout.

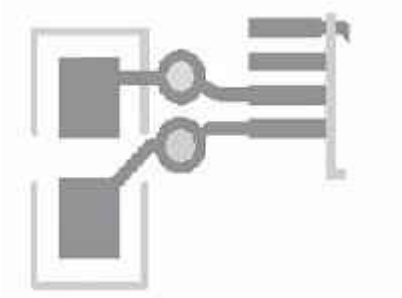

Figure 10-2. Poor Layout

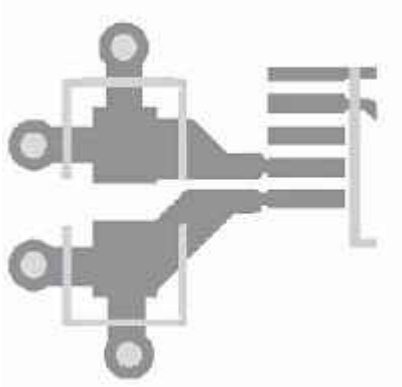

Figure 10-3. Good Layout

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10.1.3 Noise Coupling Avoidance

During operation, it is critical to prevent the coupling of noise or intermittent power connections onto the following signals because irreversible DMD micromirror array damage or lesser effects of image disruption can occur:

- SCTRL_DN, SCTRL_DP
- DCLK_DN, DCLK_DP
- SCPCLK
- SCPDI
- RESET_SEL(0), RESET_SEL(1)
- PG_OFFSET

In this context, the following conditions are considered noise:

- Shorting to another signal
- Shorting to power
- Shorting to ground
- Intermittent connection (includes hot swapping)
- An electrical open condition
- An electrical floating condition
- Inducing electromagnetic interference that is strong enough to affect the integrity of the signals
- Unstable inputs (conditions outside of the specified operating range) to any of the device power rails
- Voltage fluctuations on the device ground pins

10.2 Layout Example

10.2.1 Layers

The layer stack-up and copper weight for each layer is shown in Table 10-2. Small subplanes are allowed on signal routing layers to connect components to major sub-planes on top or bottom layers if necessary.

Table 10-2. Layer Stack-Up

LAYER NO.	LAYER NAME	COPPER WT. (oz.)	COMMENTS
1	Side A — DMD only	1.5	DMD, escapes, low frequency signals, power subplanes
2	Ground	1	Solid ground plane (net GND)
3	Signal	0.5	50-Ω and 100-Ω differential signals
4	Ground	1	Solid ground plane (net GND)
5	DMD_P3P3V	1	+3.3-V power plane (net DMD_P3P3V)
6	Signal	0.5	50-Ω and 100-Ω differential signals
7	Ground	1	Solid ground plane (net GND)
8	Side B - All other Components	1.5	Discrete components, low frequency signals, power subplanes

10.2.2 Impedance Requirements

TI recommends that the board has matched impedance of 50 Ω ±10% for all signals. The exceptions are listed in Figure 10-1 and repeated for convenience in Table 10-3.

Table 10-3. Special Impedance Requirements

Signal Type	Signal Name	Impedance (ohms)
A channel LVDS differential pairs	D_AP(0:15), D_AN(0:15)	100 ±10% differential across each pair
	DCLK_AP, DCLK_AN	
	SCTRL_AP, SCTRL_AN	
B channel LVDS differential pairs	D_BP(0:15), D_BN(0:15)	100 ±10% differential across each pair
	DCLK_BP, DCLK_BN	
	SCTRL_BP, SCTRL_BN	

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Table 10-3. Special Impedance Requirements (continued)

Signal Type	Signal Name	Impedance (ohms)
C channel LVDS differential pairs	D_CP(0:15), D_CN(0:15)	100 ±10% differential across each pair
	DCLK_CP, DCLK_CN	
	SCTRL_CP, SCTRL_CN	
D channel LVDS differential pairs	D_DP(0:15), D_DN(0:15)	100 ±10% differential across each pair
	DCLK_DP, DCLK_DN	
	SCTRL_DP, SCTRL_DN	

10.2.3 Trace Width, Spacing

Unless otherwise specified, TI recommends that all signals follow the 0.005 in./0.005 in. design rule. Minimum trace clearance from the ground ring around the PWB has a 0.1-in. minimum. An analysis of impedance and stack-up requirements determine the actual trace widths and clearances.

10.2.3.1 Voltage Signals

Below are additional voltage supply layout examples from the power planes to the individual DMD pins. In general, power supply trace widths must be as wide as possible to reduce impedances.

Table 10-4. Special Trace Widths, Spacing Requirements

SIGNAL NAME	MINIMUM TRACE WIDTH TO PINS (MIL)	LAYOUT REQUIREMENT
GND	15	Maximize trace width to connecting pin
DMD_P3P3V	15	Maximize trace width to connecting pin
DMD_P1P8V	15	Maximize trace width to connecting pin
VOFFSET	15	Create mini plane from the power generation to the DMD input
VRESET	15	Create mini plane from the power generation to the DMD input
VBIAS	15	Create mini plane from the power generation to the DMD input
All DMD control input/ output connections	10	Use 10 mil etch to connect all signals/voltages to DMD pads

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11 Device and Documentation Support

11.1 Third-Party Products Disclaimer

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11.2 Device Support

11.2.1 Device Nomenclature

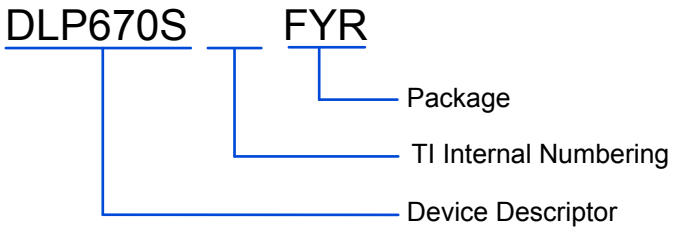

Figure 11-1. Part Number Description

11.2.2 Device Markings

The device markings include both human-readable information and a 2-dimensional matrix code. The human-readable information is described in Figure 11-2. The 2-dimensional matrix code is an alpha-numeric character string that contains the DMD part number, Part 1 of Serial Number, and Part 2 of Serial Number. The first character of the DMD Serial Number (part 1) is the manufacturing year. The second character of the DMD Serial Number (part 1) is the manufacturing month.

Example: DLP670SFYR GHXXXXX LLLLLLM

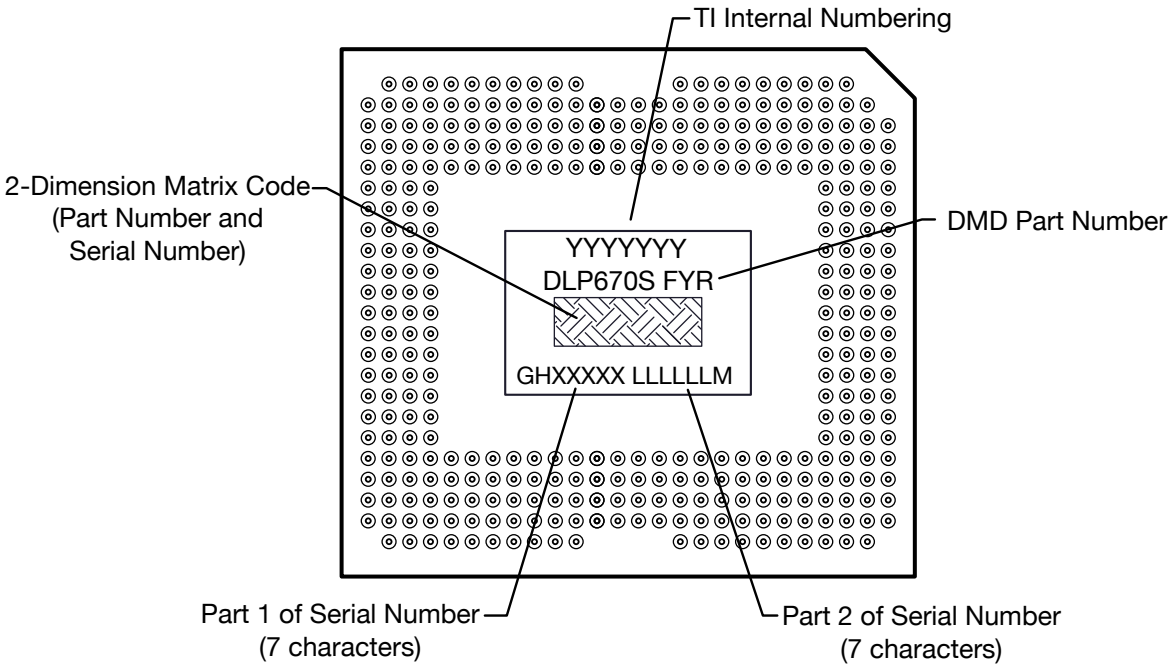

Figure 11-2. DMD Marking Locations

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11.3 Documentation Support

11.3.1 Related Documentation

The following documents contain additional information related to the chipset components used with the DLP670S DMD:

- *DLP670S Product Folder*
- *DLPC900 Product Folder*
- *DLPC900 Programmers Guide*
- *DMD Optical Efficiency for Visible Wavelengths*
- *DMD 101: Introduction to Digital Micromirror Device (DMD) Technology*

11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.8 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DLP670SFYR	Active	Production	CPGA (FYR) | 350	21 | JEDEC TRAY (5+1)	Yes	NI-PD-AU	N/A for Pkg Type	0 to 70	
DLP670SFYR.B	Active	Production	CPGA (FYR) | 350	21 | JEDEC TRAY (5+1)	Yes	NI-PD-AU	N/A for Pkg Type	0 to 70	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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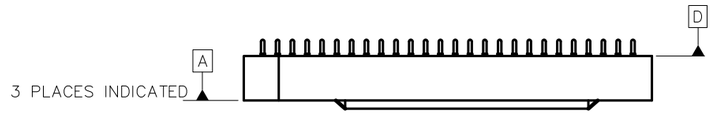
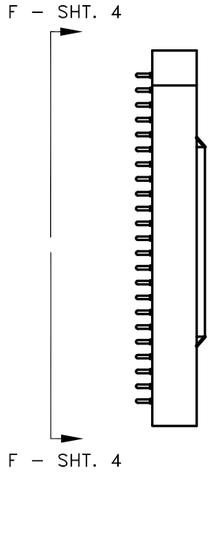
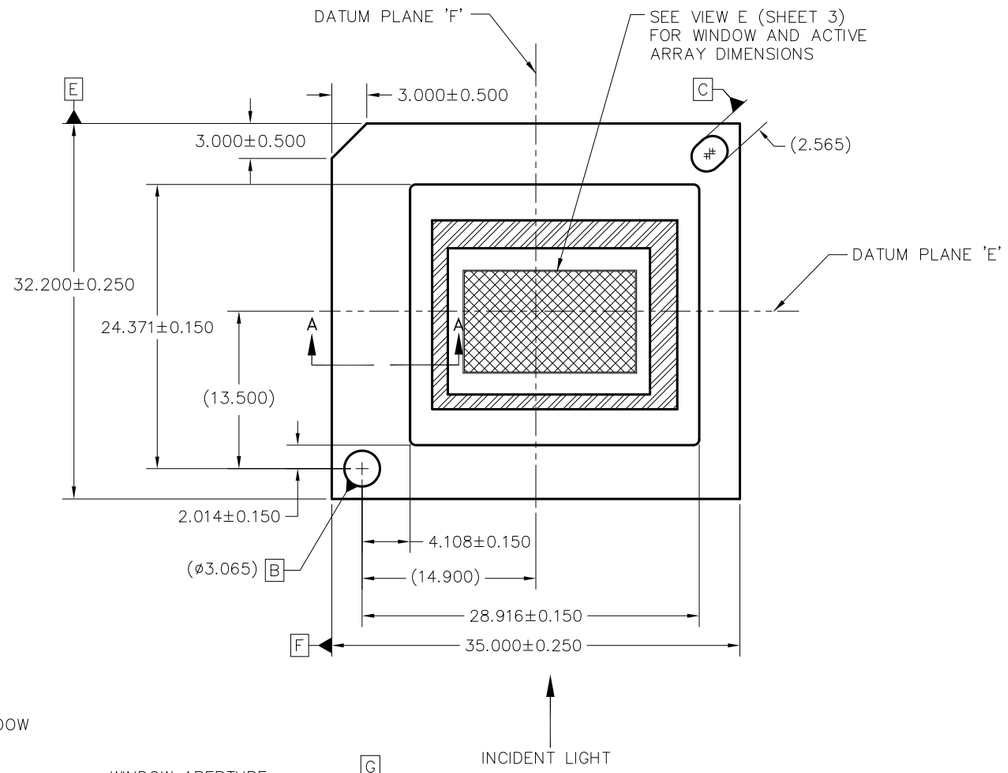
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	ECO 2181188, INITIAL RELEASE	05/07/2019	F. ARMSTRONG

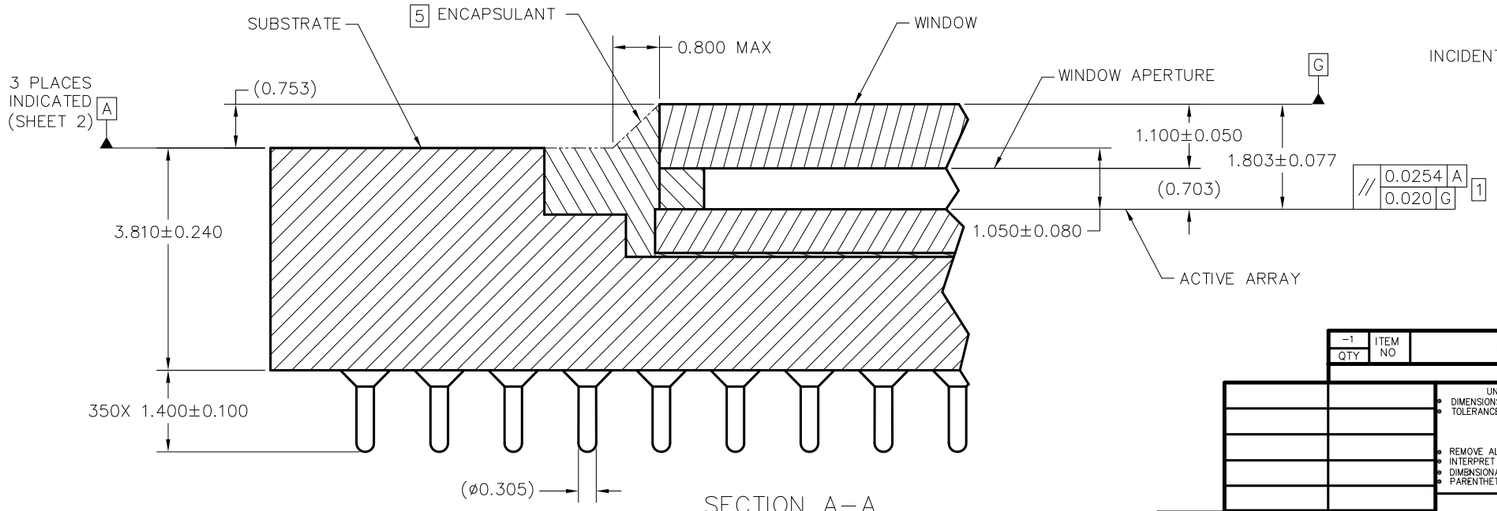
NOTES: UNLESS OTHERWISE SPECIFIED:

1. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY
2. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.8 DEGREES
3. SUBSTRATE SYMBOLIZATION PAD AND PLATING AT BOTTOM OF DATUMS B AND C HOLES ARE ELECTRICALLY CONNECTED TO VSS PLANE WITHIN THE SUBSTRATE
4. BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE AREA
5. MAXIMUM ENCAPSULANT PROFILE SHOWN
6. ENCAPSULANT ALLOWED ON THE SURFACE OF THE CERAMIC IN THE AREA SHOWN IN VIEW B (SHEET 2). ENCAPSULANT SHALL NOT EXCEED 0.200 THICKNESS MAXIMUM.
7. SUBSTRATES PLATED WITH Ni/Au SHALL HAVE THE THREE-DIGIT NUMERICAL MARKING IN THE AREA ABOVE THE SYMBOLIZATION PAD. SUBSTRATES PLATED WITH Ni/Pd/Au SHALL HAVE THE MARKING IN THE AREA BELOW THE SYMBOLIZATION PAD.









SECTION A–A
SCALE 20/1

QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES
		PARTS LIST		

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES: ANGLES ± 1°
  2 PLACE DECIMALS ±0.25
  3 PLACE DECIMALS ±0.50
- REMOVE ALL BURRS AND SHARP EDGES
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5-1994
- DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
- PARENTHETICAL INFO FOR REF ONLY

THIRD ANGLE PROJECTION

NEXT ASSY	USED ON
NONE	0314DA

APPLICATION

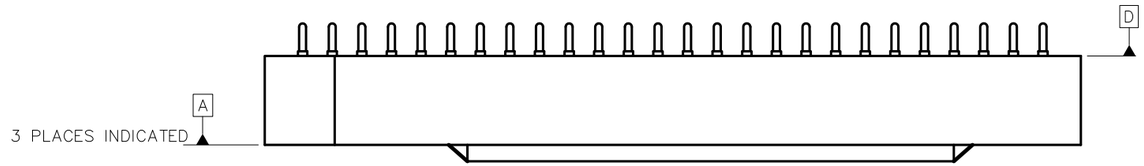
DWN	F. ARMSTRONG	05/07/2019
ENGR	F. ARMSTRONG	05/07/2019
QA	P. KONRAD	05/14/2019
CQE	M. DORAK	05/14/2019

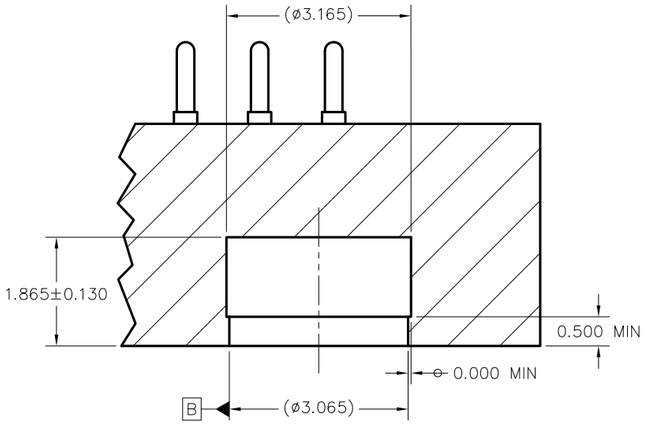
TEXAS INSTRUMENTS
Dallas, Texas

ICD, MECHANICAL, DMD .67 HB MTRP 2XLVDS SERIES 610 (FYR PACKAGE)

SIZE D | DRAWING NO 2516660 | REV A | SCALE 4/1 | SHEET 1 OF 4

ACED1g





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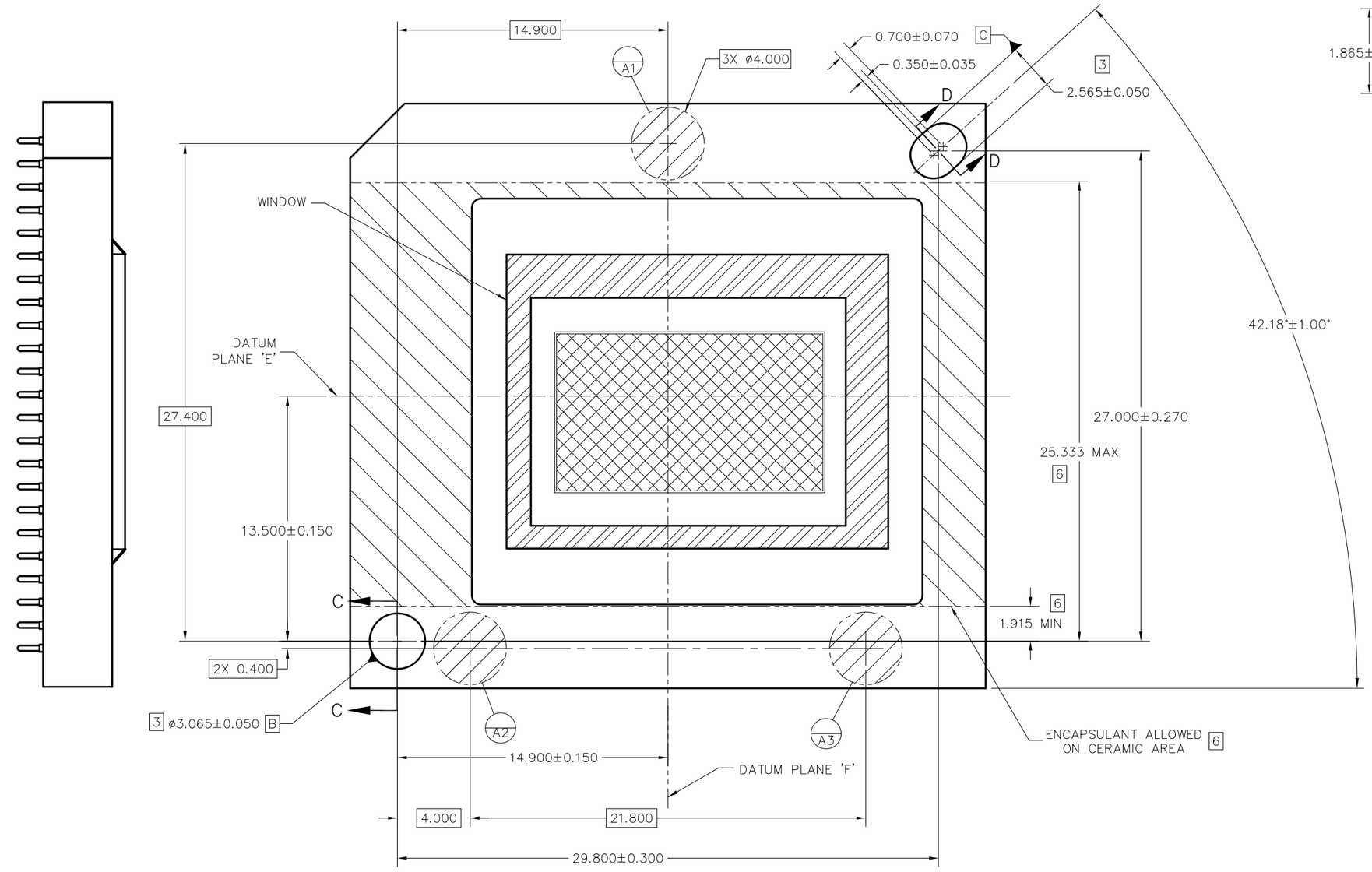
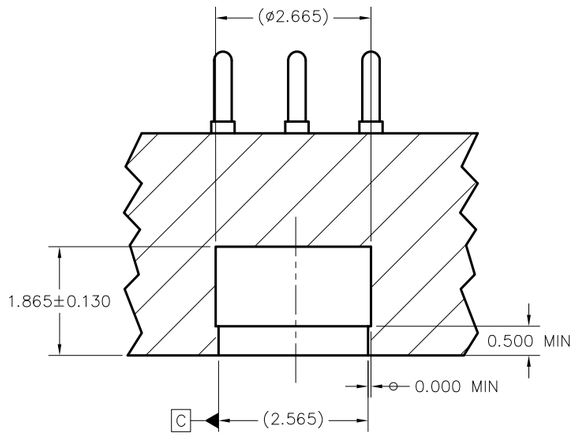
SCALE 16/1



VIEW B
DATUMS AND ENCAPSULANT ALLOWABLE AREA
SCALE 8/1



SECTION D–D
DATUM C
SCALE 16/1

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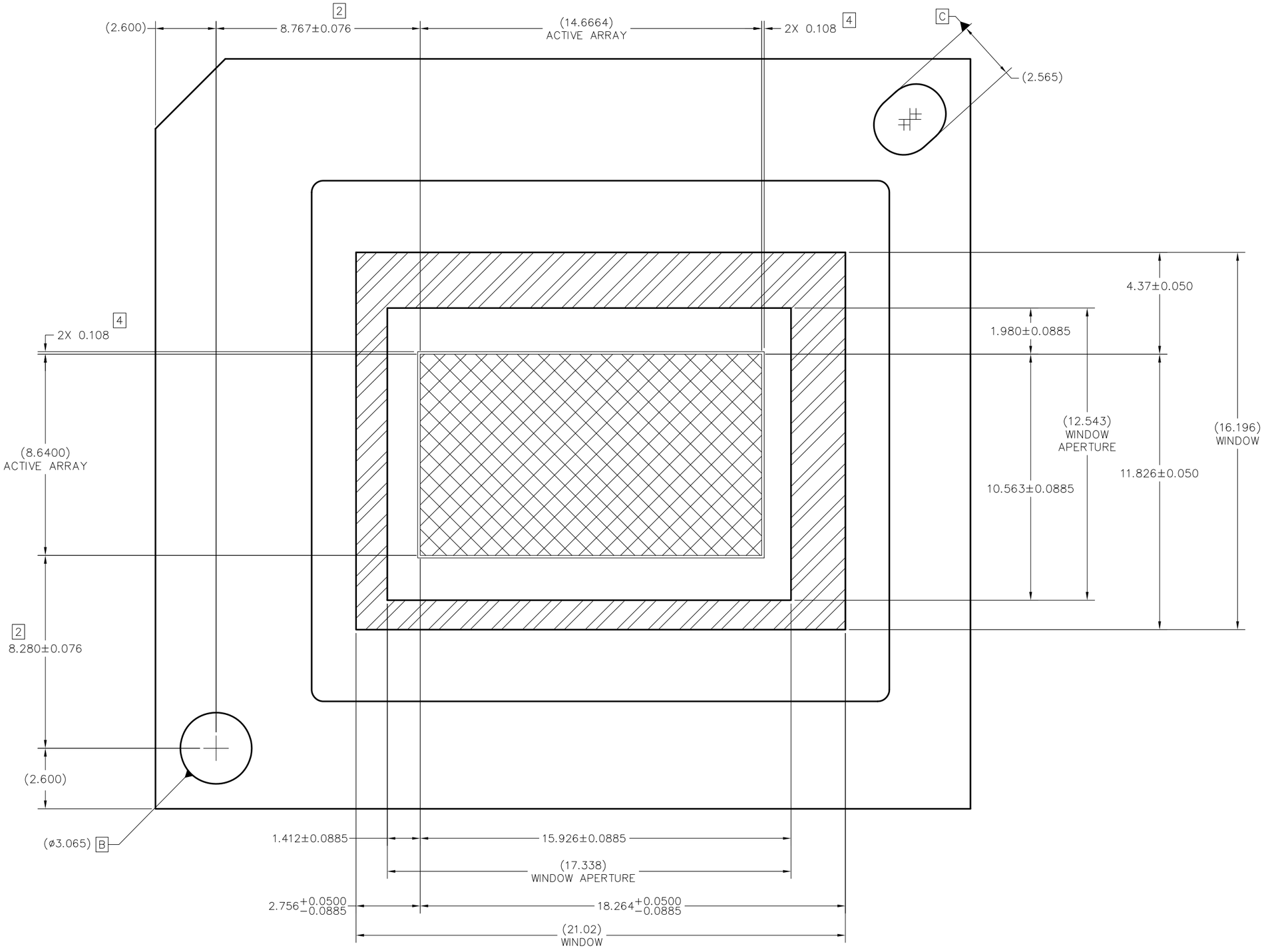
		SCALE 4/1	SHEET 2	

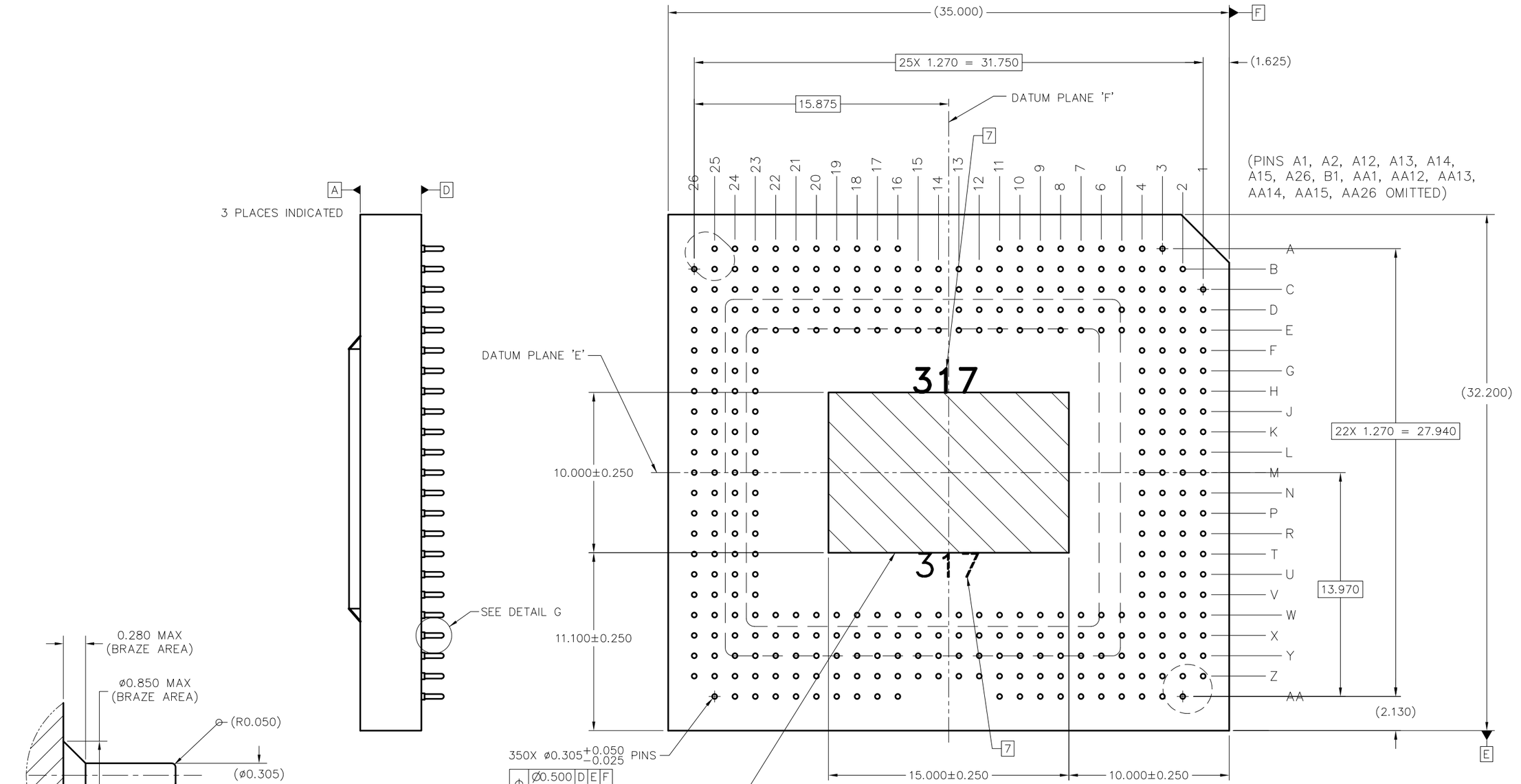
ACED2c



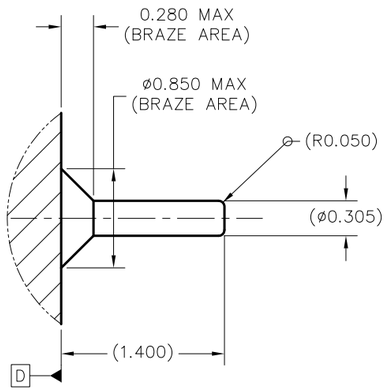
VIEW E (SHEET 1)
DMD WINDOW AND ACTIVE ARRAY
SCALE 12/1

Texas Instruments, Dallas, Texas	DWN DATE	SIZE D	DRAWING NO 2516660	REV A
	ISSUE DATE	SCALE 4/1	SHEET 3	

ACED2c



VIEW F–F (SHEET 1)
PINS AND SYMBOLIZATION PAD
SCALE 8/1



DETAIL G (350 PLACES)
PIN & BRAZE DIMENSIONS
SCALE 40/1

TEXAS INSTRUMENTS Dallas, Texas	DWN DATE / ISSUE DATE	SIZE D	DRAWING NO 2516660 REV A
		SCALE 4/1	SHEET 4

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