# INA241x –5V to 110V, Bidirectional, Ultra-Precise Current Sense Amplifier With Enhanced PWM Rejection

## 1 Features

- Enhanced PWM rejection optimized for systems subject to switching common-mode voltages
  - Supports switching frequencies up to 125kHz
- Wide common-mode voltage:
  - Operational voltage: −5V to 110V
  - Survival voltage: −20V to 120V
- Bidirectional operation
- High small signal bandwidth: 1.1MHz (at all gains)
- Slew rate: 8V/µs
- Step response settling time to 1%: 1µs
- Excellent CMRR
  - 166dB DC-CMRR
  - 104dB AC-CMRR at 100kHz
  - 89dB AC-CMRR at 1MHz
- Accuracy:
  - Gain error (maximum)
    - Version A: ±0.01%, ±1ppm/°C drift
    - Version B: ±0.1%, ±5ppm/°C drift
  - Offset voltage (maximum)
    - Version A: ±10µV, ±0.1µV/°C drift
    - Version B: ±150µV, ±0.5µV/°C drift
- Available gains:
  - INA241A1, INA241B1 : 10V/V
  - INA241A2, INA241B2 : 20V/V
  - INA241A3, INA241B3 : 50V/V
  - INA241A4, INA241B4 : 100V/V
  - INA241A5, INA241B5 : 200V/V
- Package options: SOT23-8, VSSOP-8, SOIC-8,

## 2 Applications

- Motor drives
- Solenoids and actuators
- Injection molding machine
- Cordless power tools
- Medical cordless tools
- Drone propeller speed control

## 3 Description

The INA241x is an ultra-precise, bidirectional current sense amplifier that can measure voltage drops across shunt resistors over a wide common-mode range from –5V to 110V, independent of the supply voltage. The high-precision current measurement is achieved through a combination of low offset voltage (±10µV, maximum), small gain error (±0.01%, maximum) and a high DC CMRR (typical 166dB). The INA241x is designed for high voltage, bidirectional measurements in switching systems that see large common-mode voltage transients at the device inputs. The enhanced PWM rejection circuitry inside the INA241x provides minimal signal disturbance at the output due to the common-mode voltage transitions at the input.

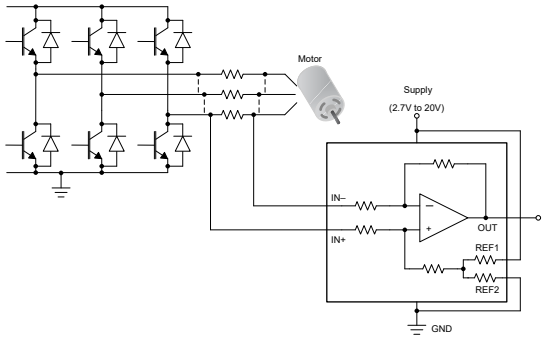
The INA241x operates from a single 2.7V to 20V supply, drawing 2.5mA of supply current. The INA241x is available in five gain options: 10V/V, 20V/V, 50V/V, 100V/V, and 200V/V. Multiple gain options allow for optimization between available shunt resistor values and wide output dynamic range requirements.

The INA241x is specified over operating temperature range of −40°C to 125°C.

**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) |
|---|---|---|
| INA241A<br>INA241B | DDF (SOT-23, 8) | 2.9mm × 2.8mm |
| | DGK (VSSOP, 8) | 3mm × 4.9mm |
| | D (SOIC, 8) | 4.9mm × 6mm |

(1) For all available packages, see the package option addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.




**Typical Application - Inline Motor Control**

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## 4 Device Comparison

**Table 4-1. Device Comparison**

| DEVICE NAME | GAIN |
|---|---|
| INA241A1, INA241B1 | 10V/V |
| INA241A2, INA241B2 | 20V/V |
| INA241A3, INA241B3 | 50V/V |
| INA241A4, INA241B4 | 100V/V |
| INA241A5, INA241B5 | 200V/V |

## 5 Pin Configuration and Functions

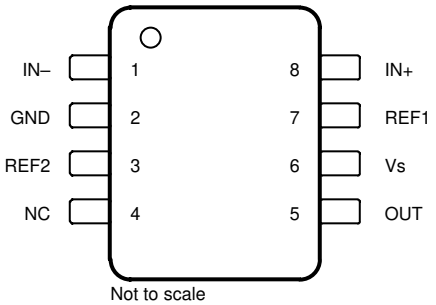



**Figure 5-1. INA241x: DDF Package 8-Pin SOT-23 Top View**

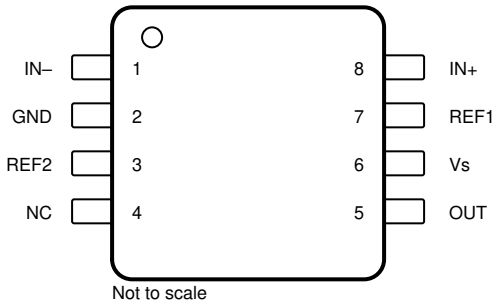



**Figure 5-2. INA241x: D and DGK Package 8-Pin SOIC and 8-Pin VSSOP Top View**

**Table 5-1. Pin Functions: D, DDF and DGK Packages**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| GND | 2 | Ground | Ground. |
| IN+ | 8 | Input | Current-sense amplifier positive input. For high-side applications, connect to bus-voltage side of sense resistor. For low-side applications, connect to load side of sense resistor. |
| IN– | 1 | Input | Current-sense amplifier negative input. For high-side applications, connect to load side of sense resistor. For low-side applications, connect to ground side of sense resistor. |
| NC | 4 | Ground | Reserved. Connect to ground. |
| OUT | 5 | Output | Output voltage. |

**Table 5-1. Pin Functions: D, DDF and DGK Packages (continued)**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| REF1 | 7 | Input | Reference 1 voltage. Connect to voltage potential from 0V to $V_S$; see *Adjusting the Output With the Reference Pins* for connection options. |
| REF2 | 3 | Input | Reference 2 voltage. Connect to voltage potential from 0V to $V_S$; see *Adjusting the Output With the Reference Pins* for connection options. |
| $V_S$ | 6 | Power | Power supply, 2.7V to 20V |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage ($V_S$) | | | 22 | V |
| Analog inputs, $V_{IN+}$, $V_{IN-}$ (2) | Differential ($V_{IN+}$) − ($V_{IN-}$) | −30 | 30 | V |
| | Common-mode | −20 | 120 | V |
| REF1, REF2, NC inputs | | GND − 0.3 | $V_S$ + 0.3 | V |
| Output | | GND – 0.3 | Vs + 0.3 | V |
| $T_A$ | Operating temperature | –55 | 150 | °C |
| $T_J$ | Junction temperature | | 150 | °C |
| $T_{stg}$ | Storage temperature | –65 | 150 | °C |

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) $V_{IN+}$ and $V_{IN–}$ are the voltages at the IN+ and IN– pins, respectively.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±2000 | V |
| | | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CM}$ | Common-mode input range | −5 | 48 | 110 | V |
| $V_S$ | Operating supply range | 2.7 | 5 | 20 | V |
| $T_A$ | Ambient temperature | –40 | | 125 | °C |

## 6.4 Thermal Information

| THERMAL METRIC(1) | | INA241x | | | UNIT |
|---|---|---|---|---|---|
| | | DDF (SOT23) | DGK (VSSOP) | D (SOIC) | |
| | | 8 PINS | 8 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 129.7 | 167.2 | 122.9 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 58 | 58.9 | 54.7 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 52.6 | 88.9 | 68.8 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 2.3 | 8.1 | 12.2 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 52.3 | 87.4 | 67.5 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

## 6.5 Electrical Characteristics

at $T_A$ = 25 °C, $V_S$ = 5V, $V_{SENSE} = V_{IN+} – V_{IN–}$, $V_{CM} = V_{IN–}$ = 48V, and $V_{REF1} = V_{REF2} = V_S$ / 2 (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **INPUT** | | | | | | |
| $V_{CM}$ | Common-mode input range[1] | $V_{IN+}$, $V_{IN–}$ = –5V to 110V, $V_{SENSE}$ = 0mV<br>$T_A$ = –40°C to 125°C | –5 | | 110 | V |
| CMRR | Common-mode rejection ratio, input-referred | $V_{IN+}$, $V_{IN–}$ = –5V to 110V, $V_{SENSE}$ = 0mV<br>$T_A$ = –40°C to 125°C, INA241A | 150 | 166 | | dB |
| | | $V_{IN+}$, $V_{IN–}$ = –5V to 110V, $V_{SENSE}$ = 0mV<br>$T_A$ = –40°C to 125°C, INA241B | 120 | 130 | | |
| | | f = 50kHz | | 105 | | |
| $V_{os}$ | Offset voltage, input-referred | $V_{SENSE}$ = 0mV, INA241A1 | | ±5 | ±20 | µV |
| | | $V_{SENSE}$ = 0mV, INA241A2 | | ±3 | ±15 | |
| | | $V_{SENSE}$ = 0mV, INA241A3, INA241A4 | | ±3 | ±10 | |
| | | $V_{SENSE}$ = 0mV, INA241A5 | | ±2 | ±8 | |
| | | $V_{SENSE}$ = 0mV, INA241B | | ±25 | ±150 | |
| $dV_{os}/dT$ | Offset voltage drift, input-referred | $T_A$ = –40°C to 125°C, INA241A1 | | ±50 | ±250 | nV/°C |
| | | $T_A$ = –40°C to 125°C, INA241A2 | | ±30 | ±150 | |
| | | $T_A$ = –40°C to 125°C, INA241A3, INA241A4, INA241A5 | | ±20 | ±100 | |
| | | $T_A$ = –40°C to 125°C, INA241B | | ±100 | ±500 | |
| PSRR | Power-supply rejection ratio, input-referred | $V_S$ = 2.7V to 20V, $V_{SENSE}$ = 0mV,<br>$V_{REF1} = V_{REF2}$ = 1V,<br>$T_A$ = –40°C to 125°C, INA241A1 | | ±0.2 | ±1 | µV/V |
| | | $V_S$ = 2.7V to 20V, $V_{SENSE}$ = 0mV,<br>$V_{REF1} = V_{REF2}$ = 1V,<br>$T_A$ = –40°C to 125°C, INA241A2 | | ±0.1 | ±0.75 | |
| | | $V_S$ = 2.7V to 20V, $V_{SENSE}$ = 0mV,<br>$V_{REF1} = V_{REF2}$ = 1V,<br>$T_A$ = –40°C to 125°C, INA241A3, INA241A4, INA241A5 | | ±0.06 | ±0.5 | |
| | | $V_S$ = 2.7V to 20V, $V_{SENSE}$ = 0mV,<br>$V_{REF1} = V_{REF2}$ = 1V,<br>$T_A$ = –40°C to 125°C, INA241B | | ±1 | ±10 | |
| $I_B$ | Input bias current | $I_{B+}$, $I_{B–}$, $V_{SENSE}$=0mV | 25 | 35 | 45 | µA |
| | Reference input range | | 0 | | $V_S$ | V |
| **OUTPUT** | | | | | | |
| G | Gain | A1, B1 Devices | | 10 | | V/V |
| | | A2, B2 Devices | | 20 | | V/V |
| | | A3, B3 Devices | | 50 | | V/V |
| | | A4, B4 Devices | | 100 | | V/V |
| | | A5, B5 Devices | | 200 | | V/V |

at $T_A$ = 25 °C, $V_S$ = 5V, $V_{SENSE}$ = $V_{IN+}$ – $V_{IN–}$, $V_{CM}$ = $V_{IN–}$ = 48V, and $V_{REF1}$ = $V_{REF2}$ = $V_S$ / 2 (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $G_{ERR}$ | Gain Error | (GND + 50mV) < $V_{OUT}$ < ($V_S$ - 200mV), INA241A1, INA241A2, INA241A3 | | ±0.002 | ±0.01 | % |
| | | (GND + 50mV) < $V_{OUT}$ < ($V_S$ - 200mV), INA241A4, INA241A5 | | ±0.003 | ±0.015 | |
| | | (GND + 50mV) < $V_{OUT}$ < ($V_S$ - 200mV), INA241B | | ±0.02 | ±0.1 | |
| | Gain Error Drift | $T_A$ = –40°C to +125°C, INA241A1, INA241A2, INA241A3 | | ±0.05 | ±1 | ppm/°C |
| | | $T_A$ = –40°C to +125°C, INA241A4, INA241A5 | | ±0.1 | ±2 | |
| | | $T_A$ = –40°C to +125°C, INA241B | | ±0.2 | ±5 | |
| | Non-Linearity Error | | | ±0.001 | | % |
| | Maximum Capacitive Load | No sustained oscillations, No isolation resistor | | 1 | | nF |
| **VOLTAGE OUTPUT** | | | | | | |
| | Swing to $V_S$ Power Supply Rail | $R_L$ = 10kΩ to GND, $T_A$ = –40°C to +125°C | | $V_S$ – 0.07 | $V_S$ – 0.2 | V |
| | Swing to Ground | $R_L$ = 10kΩ to GND, $V_{SENSE}$ = 0mV, $V_{REF1}$ = $V_{REF2}$ = 0V, $T_A$ = –40°C to +125°C | | 8 | 20 | mV |
| **REFERENCE INPUT** | | | | | | |
| RVRR | Reference voltage rejection ratio, input-referred | $V_{REF1}$ = $V_{REF2}$ = 0.5V to 4.5V, $T_A$ = –40°C to +125°C, INA241A1 | | ±1 | ±2.5 | µV/V |
| | | $V_{REF1}$ = $V_{REF2}$ = 0.5V to 4.5V, $T_A$ = –40°C to +125°C, INA241A2, INA241A3, INA241A4, INA241A5 | | ±0.5 | ±1.5 | |
| | | $V_{REF1}$ = $V_{REF2}$ = 0.5V to 4.5V, $T_A$ = –40°C to +125°C, INA241B, | | ±10 | ±20 | |
| | Reference divider accuracy | $V_{OUT}$ = \|($V_{REF1}$ + $V_{REF2}$)\| / 2 at $V_{SENSE}$ =0mV, $V_{REF1}$ = $V_S$, $V_{REF2}$ = GND $V_{REF1}$ = GND, $V_{REF2}$ = $V_S$ $T_A$ = –40°C to +125°C, INA241A1, INA241A2 | | ±0.002 | ±0.005 | % |
| | | $V_{OUT}$ = \|($V_{REF1}$ + $V_{REF2}$)\| / 2 at $V_{SENSE}$ =0mV, $V_{REF1}$ = $V_S$, $V_{REF2}$ = GND $V_{REF1}$ = GND, $V_{REF2}$ = $V_S$ $T_A$ = –40°C to +125°C, INA241A3, INA241A4, INA241A5 | | ±0.002 | ±0.01 | |
| | | $V_{OUT}$ = \|($V_{REF1}$ + $V_{REF2}$)\| / 2 at $V_{SENSE}$ =0mV, $V_{REF1}$ = $V_S$, $V_{REF2}$ = GND $V_{REF1}$ = GND, $V_{REF2}$ = $V_S$ $T_A$ = –40°C to +125°C, INA241B | | ±0.02 | ±0.15 | |
| **FREQUENCY RESPONSE** | | | | | | |
| BW | Bandwidth | All Gains, −3dB Bandwidth | | 1.1 | | MHz |
| | Settling time | $V_{IN+}$, $V_{IN–}$ = 48V, $V_{OUT}$ = 0.5V to 4.5V, Output settles to 0.5% | | 1.5 | | µs |
| | | $V_{IN+}$, $V_{IN–}$ = 48V, $V_{OUT}$ = 0.5V to 4.5V, Output settles to 1% | | 1 | | µs |
| | | $V_{IN+}$, $V_{IN–}$ = 48V, $V_{OUT}$ = 0.5V to 4.5V, Output settles to 5% | | 0.5 | | µs |
| SR | Slew Rate | Rising | | 8 | | V/µs |

at $T_A$ = 25 °C, $V_S$ = 5V, $V_{SENSE}$ = $V_{IN+}$ – $V_{IN–}$, $V_{CM}$ = $V_{IN–}$ = 48V, and $V_{REF1}$ = $V_{REF2}$ = $V_S$ / 2 (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **NOISE (Input referred)** | | | | | | |
| | Voltage noise density | A1, B1 Devices | | 62 | | nV/√Hz |
| | | A2, B2 Devices | | 49 | | |
| | | A3, B3 Devices | | 39 | | |
| | | A4, B4 Devices | | 36 | | |
| | | A5, B5 Devices | | 28 | | |
| **POWER SUPPLY** | | | | | | |
| $V_S$ | Supply Voltage | | 2.7 | | 20 | V |
| $I_Q$ | Quiescent current | $V_{SENSE}$ = 0mV | | 2.5 | 3 | mA |
| | | $V_{SENSE}$ = 0mV, $T_A$ = –40°C to +125°C | | | 3.2 | mA |
| **TEMPERATURE** | | | | | | |
| $T_A$ | Specified Range | | –40 | | 125 | °C |

(1) Common-mode voltage at both $V_{IN+}$ and $V_{IN-}$ must not exceed the specified common-mode input range.

## 6.6 Typical Characteristics

at $T_A$ = 25°C, $V_S$ = 5V, $V_{SENSE}$ = $V_{IN+}$ – $V_{IN–}$, $V_{CM}$ = $V_{IN–}$ = 48V, and $V_{REF1}$ = $V_{REF2}$ = $V_S$ / 2 (unless otherwise noted)

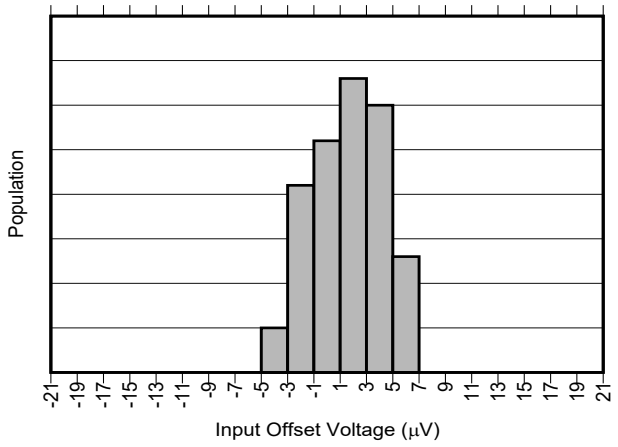



**Figure 6-1. INA241A1 Input Offset Production Distribution**

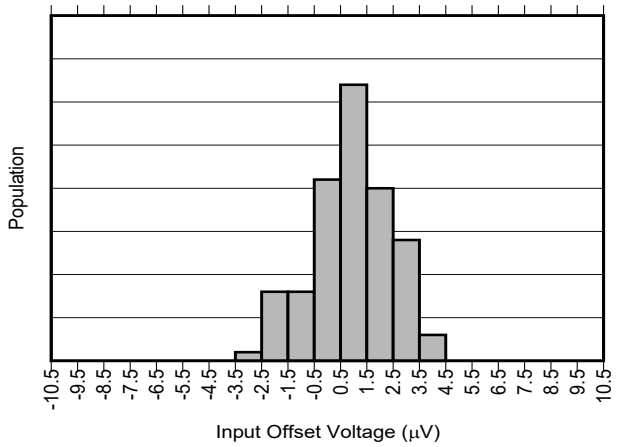



**Figure 6-2. INA241A2 Input Offset Production Distribution**

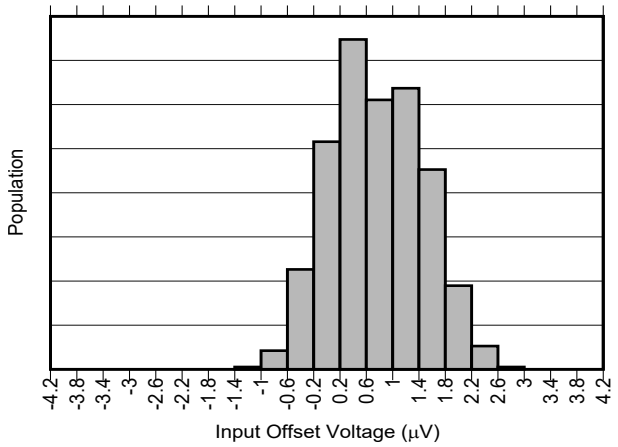



**Figure 6-3. INA241A3 and INA241A4 Input Offset Production Distribution**

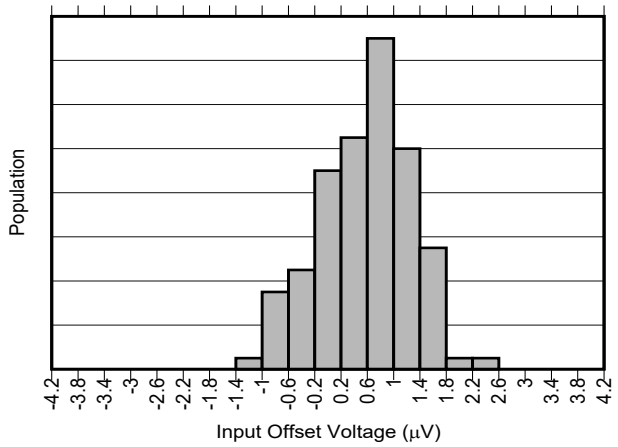



**Figure 6-4. INA241A5 Input Offset Production Distribution**

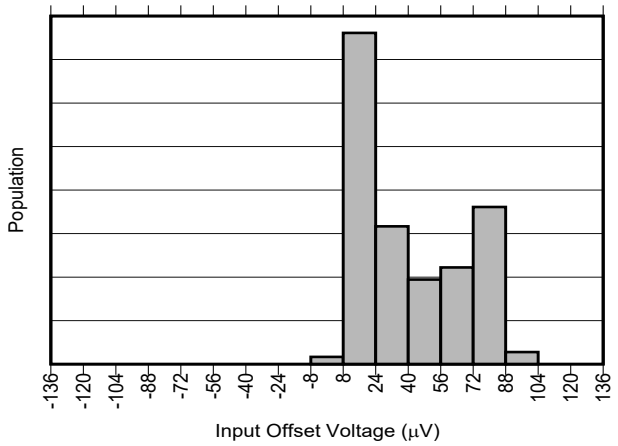



**Figure 6-5. All Gains INA241B Input Offset Production Distribution**

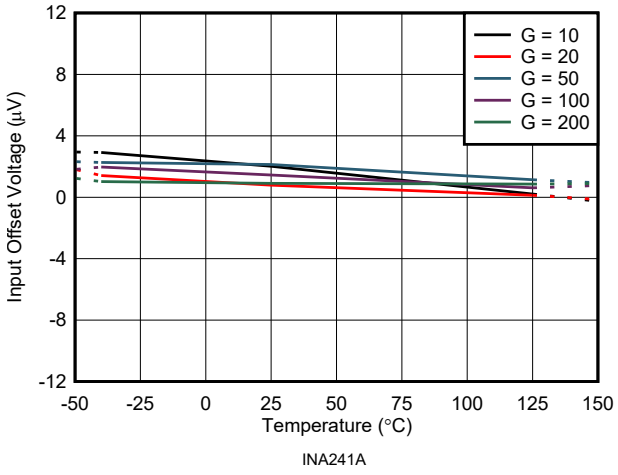



**Figure 6-6. Input Offset Voltage vs Temperature**

## 6.6 Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = 5V, $V_{SENSE}$ = $V_{IN+}$ – $V_{IN–}$, $V_{CM}$ = $V_{IN–}$ = 48V, and $V_{REF1}$ = $V_{REF2}$ = $V_S$ / 2 (unless otherwise noted)

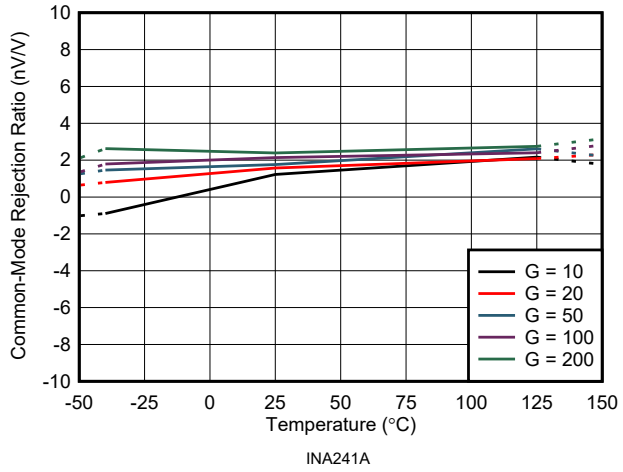



**Figure 6-7. Common-Mode Rejection Ratio vs Temperature**

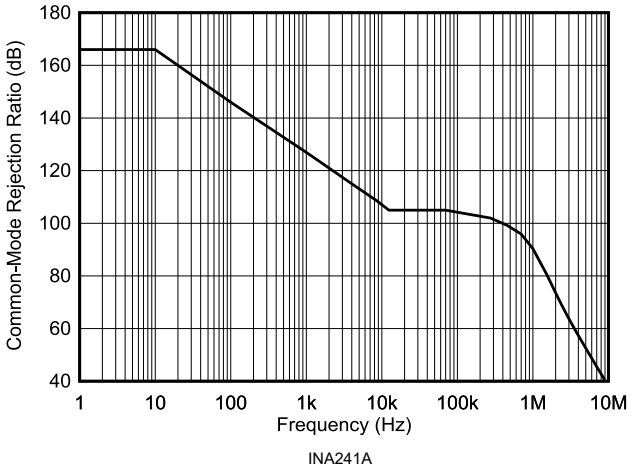



**Figure 6-8. Common-Mode Rejection Ratio vs Frequency**

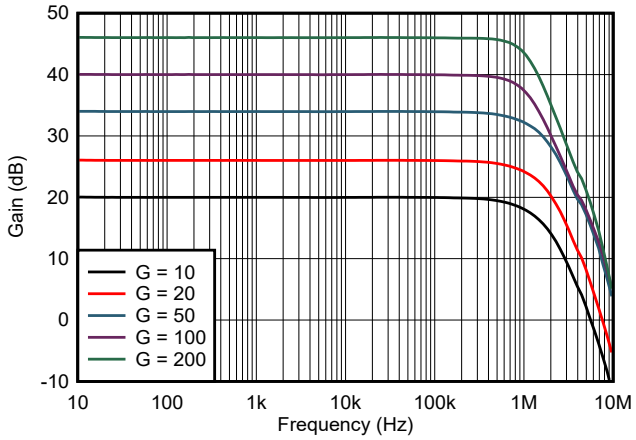



**Figure 6-9. Gain vs Frequency**

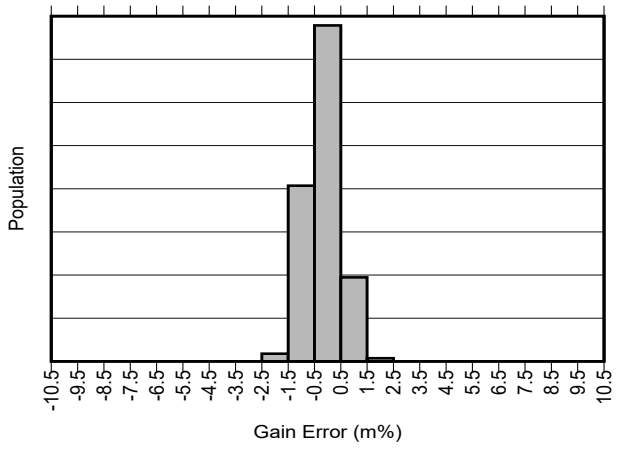



**Figure 6-10. INA241A1, INA241A2 and INA241A3 Gain Error Production Distribution**

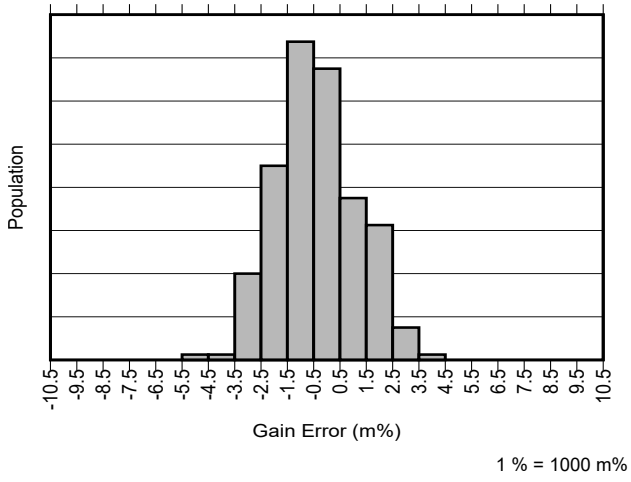



**Figure 6-11. INA241A4 and INA241A5 Gain Error Production Distribution**

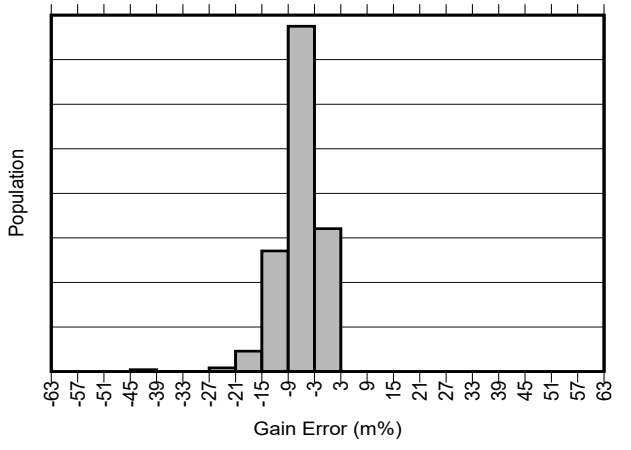



**Figure 6-12. All Gains INA241B Gain Error Production Distribution**

## 6.6 Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = 5V, $V_{SENSE}$ = $V_{IN+}$ – $V_{IN–}$, $V_{CM}$ = $V_{IN–}$ = 48V, and $V_{REF1}$ = $V_{REF2}$ = $V_S$ / 2 (unless otherwise noted)

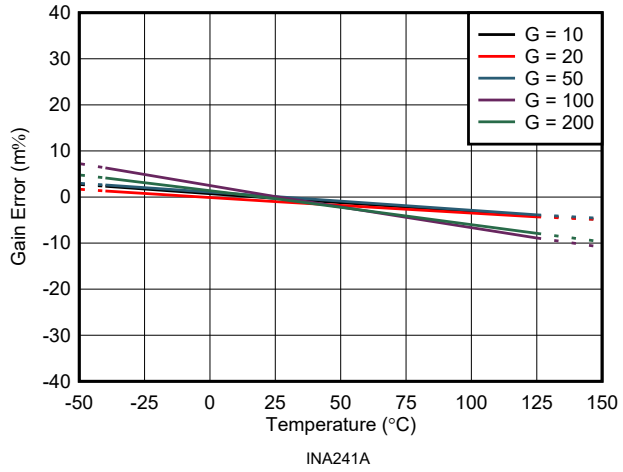



**Figure 6-13. Gain Error vs Temperature**

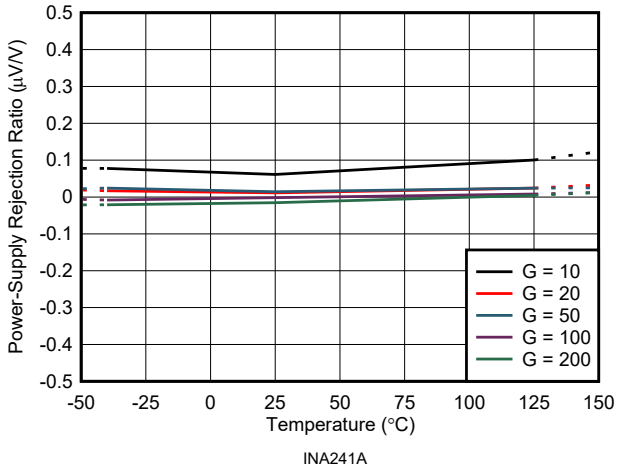



**Figure 6-14. Power-Supply Rejection Ratio vs Temperature**

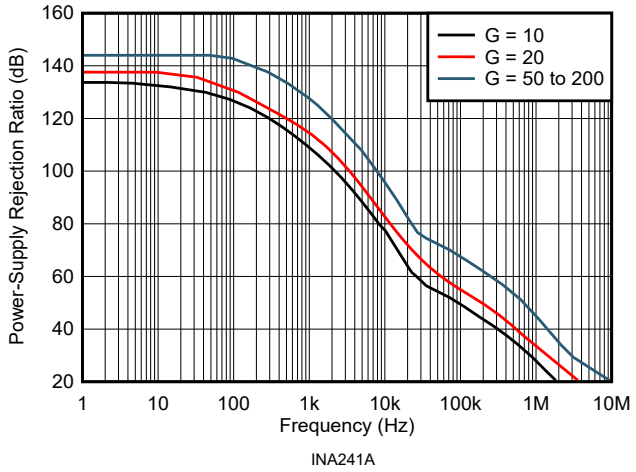



**Figure 6-15. Power-Supply Rejection Ratio vs Frequency**

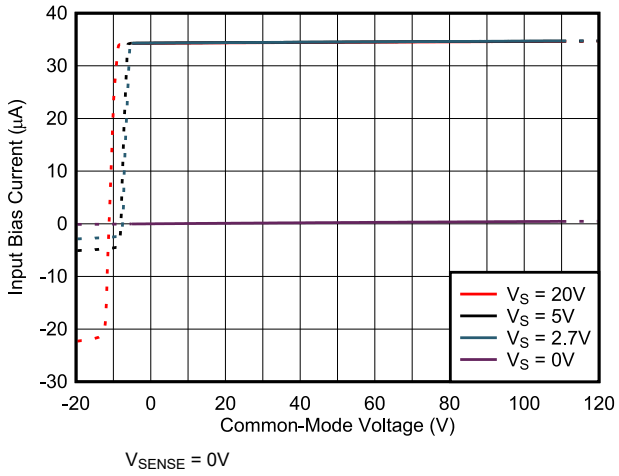



**Figure 6-16. Input Bias Current vs Common-Mode Voltage**

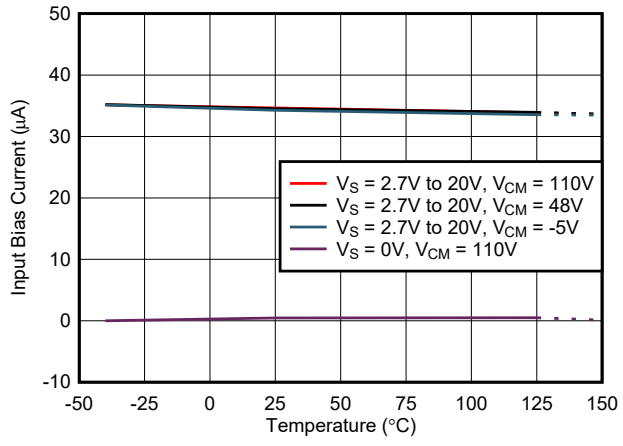



**Figure 6-17. Input Bias Current vs Temperature**

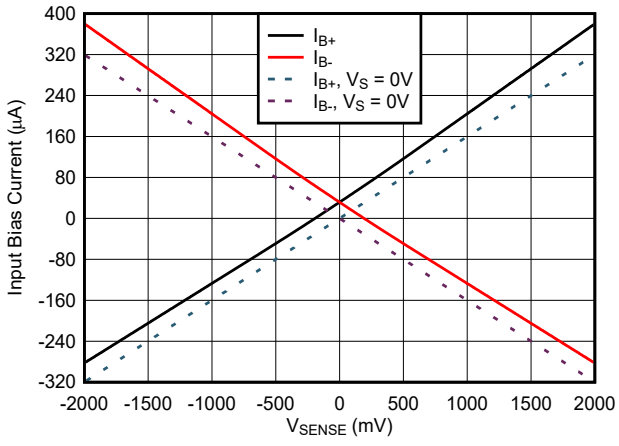



**Figure 6-18. INA241x1 Input Bias Current vs $V_{SENSE}$**

## 6.6 Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = 5V, $V_{SENSE} = V_{IN+} – V_{IN–}$, $V_{CM} = V_{IN–}$ = 48V, and $V_{REF1} = V_{REF2} = V_S / 2$ (unless otherwise noted)

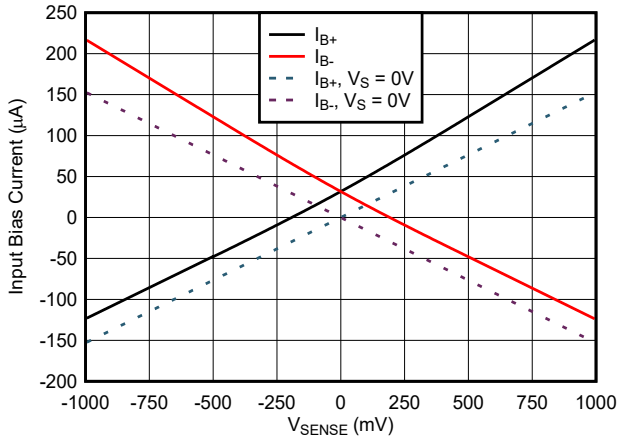



**Figure 6-19. INA241x2 Input Bias Current vs $V_{SENSE}$**

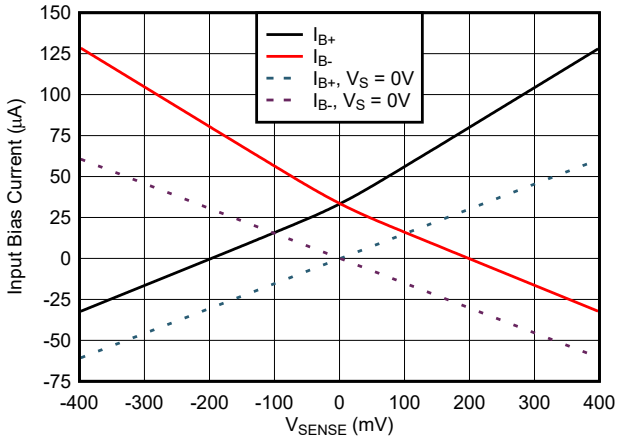



**Figure 6-20. INA241x3 and INA241x4 Input Bias Current vs $V_{SENSE}$**

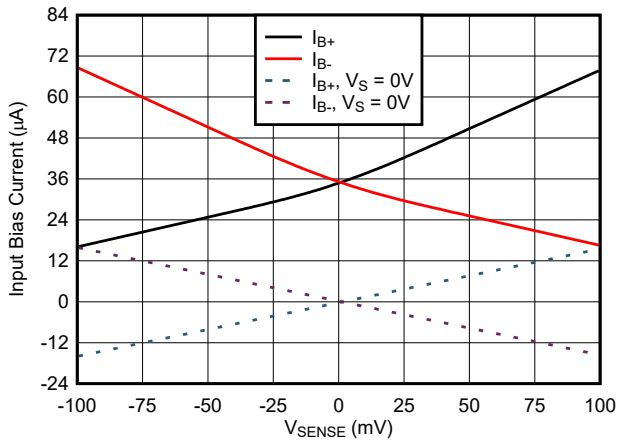



**Figure 6-21. INA241x5 Input Bias Current vs $V_{SENSE}$**

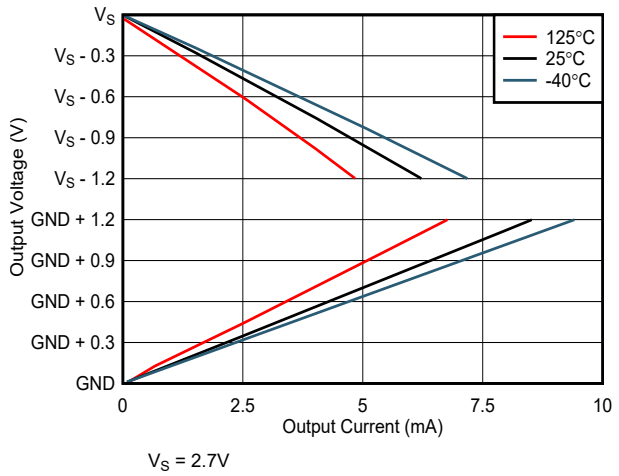



**Figure 6-22. Output Voltage vs Output Current**

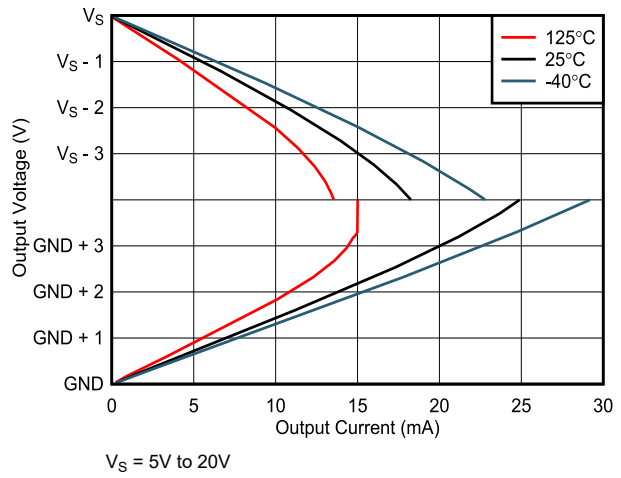



**Figure 6-23. Output Voltage vs Output Current**

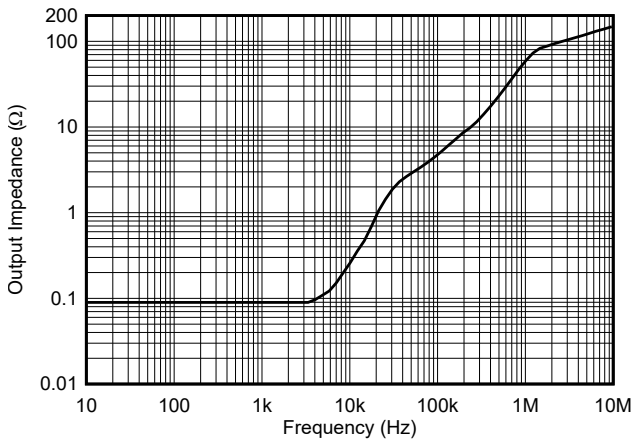



**Figure 6-24. Output Impedance vs Frequency**

## 6.6 Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = 5V, $V_{SENSE} = V_{IN+} – V_{IN–}$, $V_{CM} = V_{IN–}$ = 48V, and $V_{REF1} = V_{REF2} = V_S$ / 2 (unless otherwise noted)

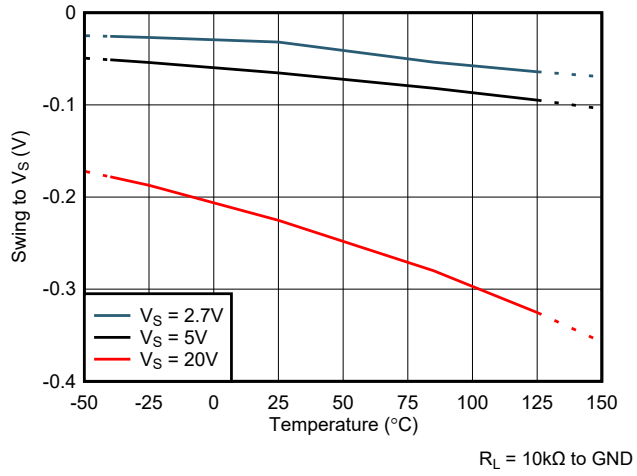



**Figure 6-25. Swing to Supply vs Temperature**

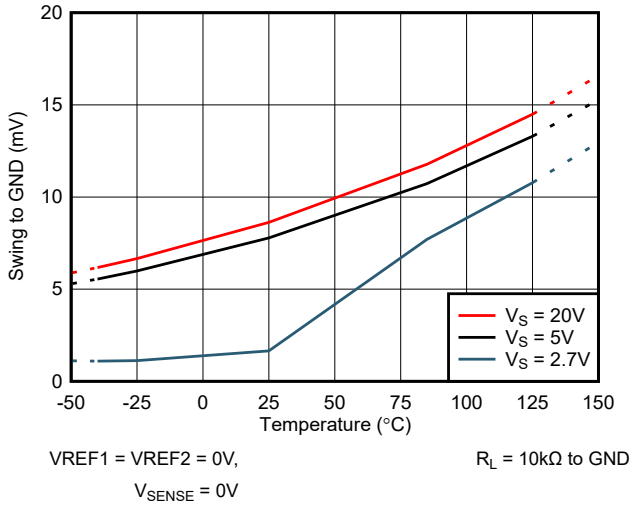



**Figure 6-26. Swing to GND vs Temperature**

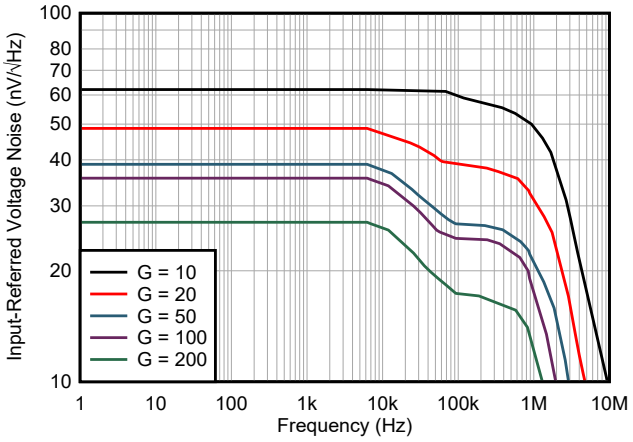



**Figure 6-27. Input Referred Noise vs Frequency**

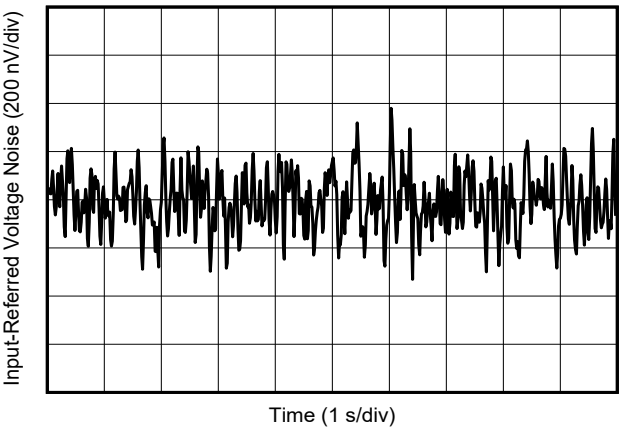



**Figure 6-28. 0.1Hz to 10Hz Voltage Noise**

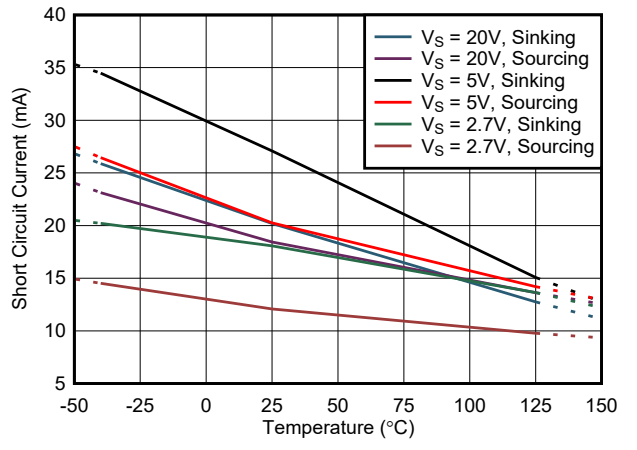



**Figure 6-29. Short-Circuit Current vs Temperature**

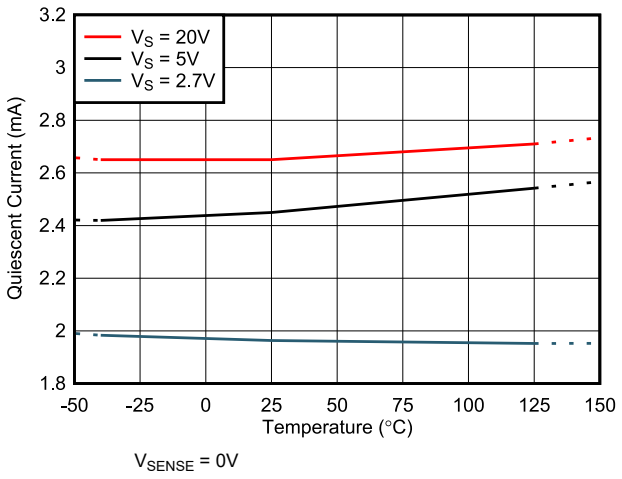
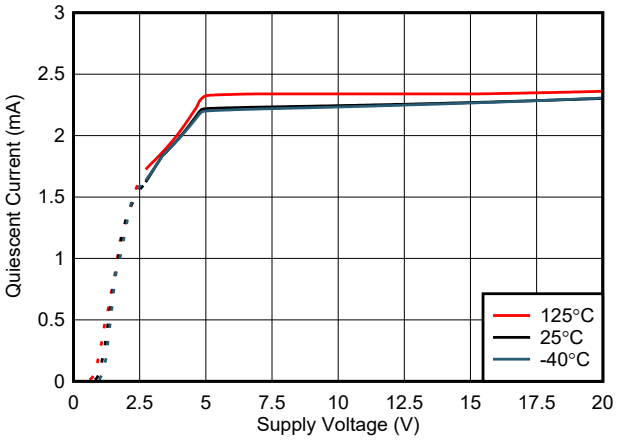



**Figure 6-30. Quiescent Current vs Temperature**

## 6.6 Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = 5V, $V_{SENSE} = V_{IN+} – V_{IN–}$, $V_{CM} = V_{IN–}$ = 48V, and $V_{REF1} = V_{REF2} = V_S / 2$ (unless otherwise noted)




VREF1 = VREF2 = 0V,
$V_{SENSE}$ = 0V

**Figure 6-31. Quiescent Current vs Supply Voltage**

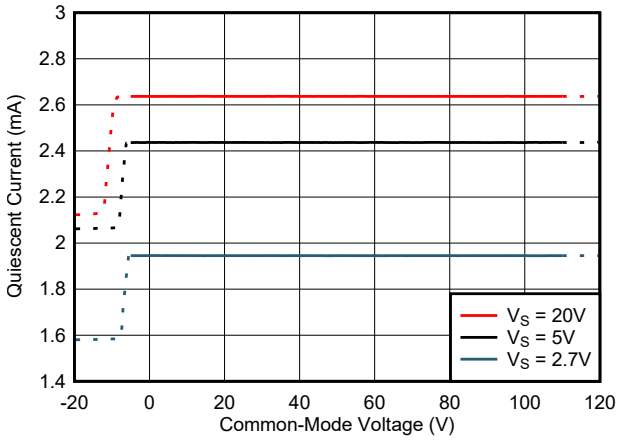
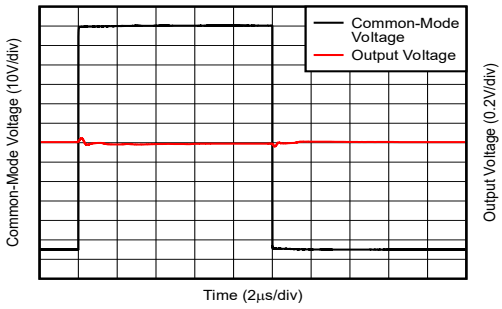



**Figure 6-32. Quiescent Current vs Common-Mode Voltage**




$V_{CM}$ = -5V to 110V,
$V_{SENSE}$ = 0V

**Figure 6-33. Common-Mode Voltage Fast Transient Pulse**

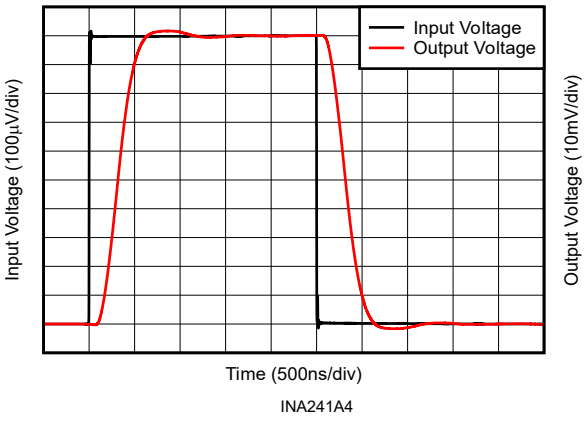



**Figure 6-34. Small Step Response**

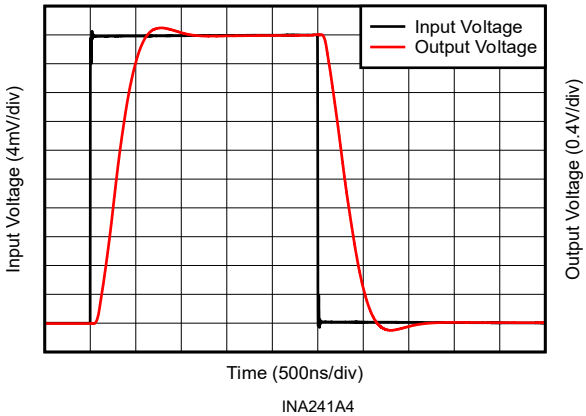



**Figure 6-35. Large Step Response**

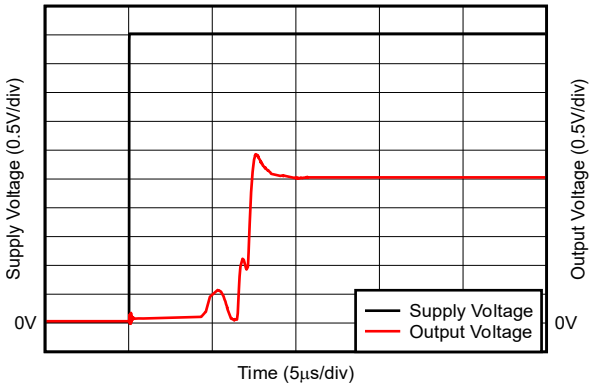



**Figure 6-36. Start-Up Response**

## 6.6 Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = 5V, $V_{SENSE}$ = $V_{IN+}$ – $V_{IN–}$, $V_{CM}$ = $V_{IN–}$ = 48V, and $V_{REF1}$ = $V_{REF2}$ = $V_S$ / 2 (unless otherwise noted)

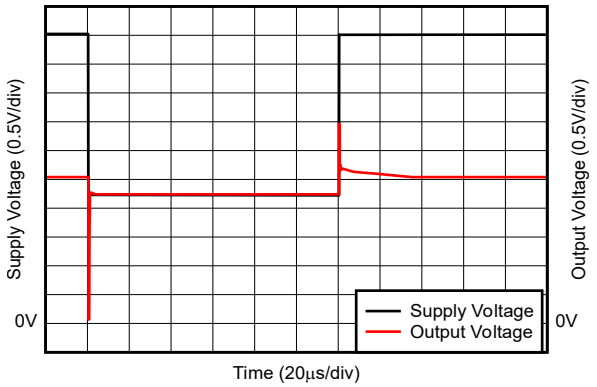


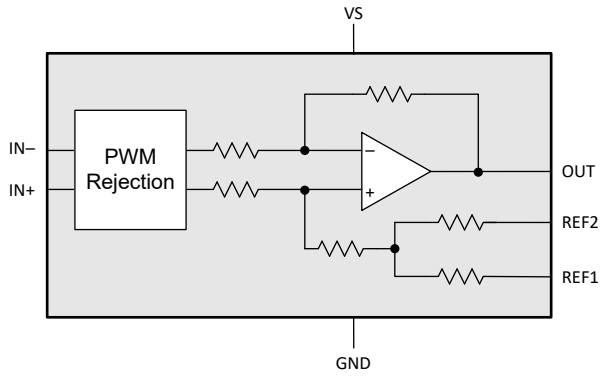

**Figure 6-37. Brownout Recovery**

# 7 Detailed Description

## 7.1 Overview

The INA241x is a high-side, inline, or low-side bidirectional, high-speed current-sense amplifier that offers a wide common-mode range, precision, zero-drift topology, excellent common-mode rejection ratio (CMRR), and features enhanced pulse width modulation (PWM) rejection at the inputs of the device. Enhanced PWM rejection reduces the effect of common-mode transients that can propagate to the output signal that are associated with PWM input signals. Multiple gain versions are available to allow for the optimization of the desired full-scale output voltage based on the target current range expected in the application.

## 7.2 Functional Block Diagram




## 7.3 Feature Description

### *7.3.1 Amplifier Input Common-Mode Signal*

The INA241x supports large input common-mode voltages from –5V to 110V. The internal topology of the INA241x allows the common-mode range to exceed the power-supply voltage ($V_S$). This allows for the INA241x to be used for low-side, inline, and high-side current-sensing applications that extend beyond the supply range of 2.7V to 20V.

#### 7.3.1.1 Enhanced PWM Rejection Operation

The enhanced PWM rejection feature of the INA241x provides increased attenuation of large common-mode ΔV/Δt transients. Large ΔV/Δt common-mode transients associated with PWM signals are employed in applications such as motor or solenoid drive and switching power supplies. The disturbances that can occur at the output of a current sense amplifier from common-mode transients causes erroneous measurements and impose limitations when the output is valid. The INA241x is designed with high common-mode rejection techniques to reduce large ΔV/Δt transients before the system is disturbed. As a result, this makes system design simple with INA241x. The high AC CMRR, in conjunction with signal bandwidth, allows the INA241x to minimize output disturbances and ringing during common-mode transitions when compared against traditional current-sensing amplifiers.

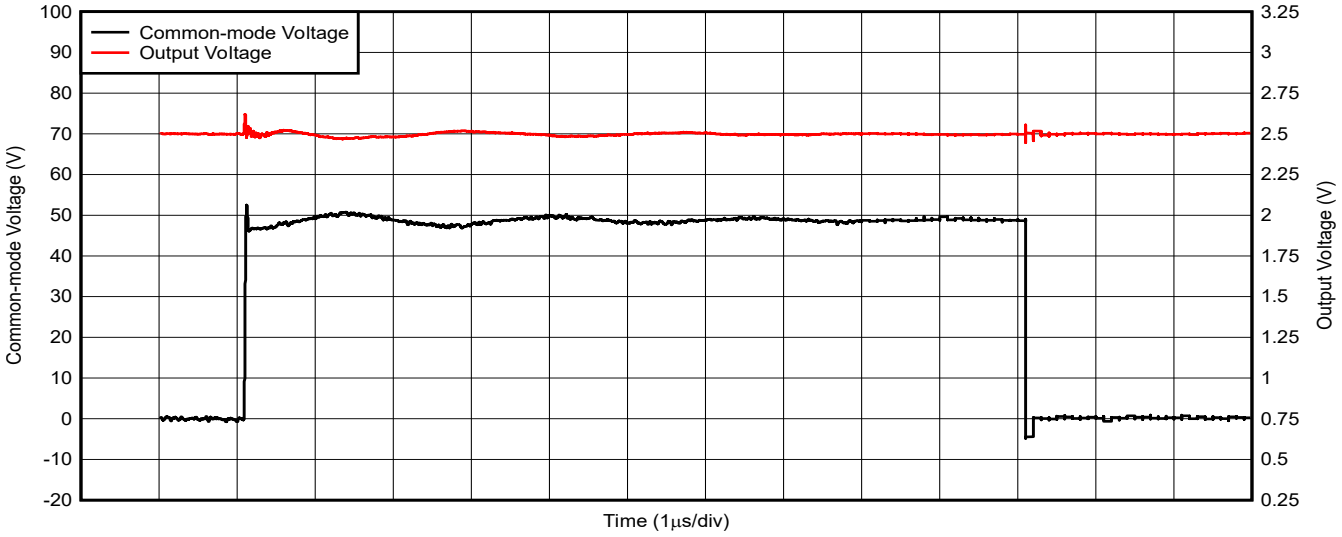



**Figure 7-1. Enhanced PWM Rejection Performance**

Figure 7-1 shows the INA241x PWM enhancement performance. When INA241x senses the large common-mode ΔV/Δt transients, the device holds the output for 1µs, thereby preventing the common-mode disturbance from propagating to the output. If another common-mode transient occurs during the following 3µs, the INA241x relies on high BW and AC CMMR to attenuate the effect of common-mode transient. The enhanced PWM rejection is achieved up to a PWM frequency of 125kHz or if common-mode transient edges are separated by a 3µs interval or more.

#### 7.3.1.2 Input-Signal Bandwidth

The INA241x is available with several gain options including 10V/V, 20V/V, 50V/V, 100V/V, and 200V/V. The unique multistage design enables the amplifier to achieve high bandwidth of 1.1MHz at all gains. This high bandwidth provides the throughput and fast response that is required for the rapid detection and processing of over-current events.

#### 7.3.1.3 Low Input Bias Current

The INA241x inputs draw 35µA (typical) bias current per input pin at common-mode voltages as high as 110V, which enables precision current sensing on applications that require lower current leakage. Unlike many high voltage current sense amplifiers whose input bias currents are proportional to the common-mode voltage, the input bias current of the INA241x remains constant over the entire common-mode voltage range.

#### 7.3.1.4 Low $V_{SENSE}$ Operation

The INA241x features high performance operation across the entire valid $V_{SENSE}$ range. The zero-drift input architecture of the INA241x provides the low offset voltage and low offset drift needed to measure low $V_{SENSE}$ levels accurately across the wide operating temperature of –40°C to +125°C. Low $V_{SENSE}$ operation is particularly beneficial when using low ohmic shunts for low current measurements, as power losses across the shunt are significantly reduced.

#### 7.3.1.5 Wide Fixed Gain Output

The INA241x maximum gain error is ±0.01% at room temperature, with a maximum drift of ±1 ppm/°C over the full temperature range of –40°C to 125°C. The INA241x is available in multiple gain options of 10V/V, 20V/V, 50V/V, 100V/V, and 200V/V, which the system designer must select based on the desired signal-to-noise ratio and other system requirements, such as the dynamic current range and full-scale output voltage target.

#### 7.3.1.6 Wide Supply Range

The INA241x operates with a wide supply range from 2.7V to 20V. While the input common-mode voltage range of the INA241x is independent of the supply voltage, the output voltage is bound by the supply voltage applied to the device. The output voltage can range from as low as 20mV to as high as 200mV below the supply voltage.

## 7.4 Device Functional Modes

### 7.4.1 Adjusting the Output With the Reference Pins

Figure 7-2 shows a test circuit for reference-divider accuracy. The INA241x output is configurable to allow for unidirectional or bidirectional operation.

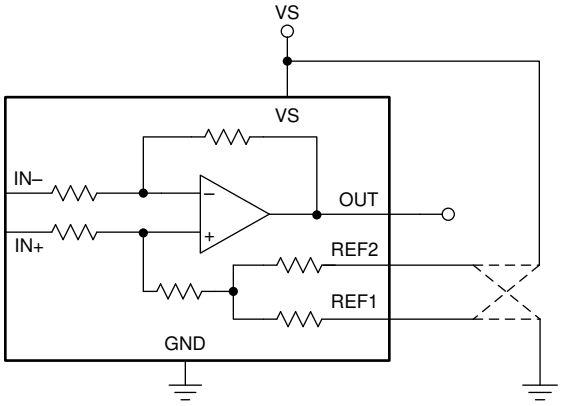



**Figure 7-2. Test Circuit For Reference Divider Accuracy**

The output voltage is set by applying a voltage or voltages to the reference voltage inputs, REF1 and REF2. The reference inputs are connected to an internal gain network. There is no operational difference between the two reference pins. The resistor network connected to the two reference pins are designed with ultra-precision and matching. Output is set accurately at the mid-point voltage between the voltages applied to reference voltage inputs, when current-sense input voltage is 0V as shown in Equation 1. In most bidirectional applications, one reference input is connected to the positive supply and the other reference input is connected to the negative supply (GND pin) to set the output voltage to mid-supply.

$$V_{OUT} = G \times (V_{IN+} - V_{IN-}) + \frac{V_{REF1} + V_{REF2}}{2} \quad (1)$$

### 7.4.2 Reference Pin Connections for Unidirectional Current Measurements

Unidirectional operation allows current measurements through a resistive shunt in one direction. For unidirectional operation, connect the device reference pins together and then to the negative rail (see the *Ground Referenced Output* section) or the positive rail (see the *VS Referenced Output* section). The required differential input polarity depends on the reference input setting. The amplifier output moves away from the referenced rail proportional to the current passing through the external shunt resistor. If the amplifier reference pins are connected to the positive rail, then the input polarity must be negative to move the amplifier output down (towards ground). If the amplifier reference pins are connected to ground, then the input polarity must be positive to move the amplifier output up (towards supply).

The following sections describe how to configure the output for unidirectional operation cases.

#### 7.4.2.1 Ground Referenced Output

When using the INA241x in a unidirectional mode with a ground referenced output, both reference inputs are connected to ground. This configuration takes the output to ground when there is a 0V differential at the input (see Figure 7-3).

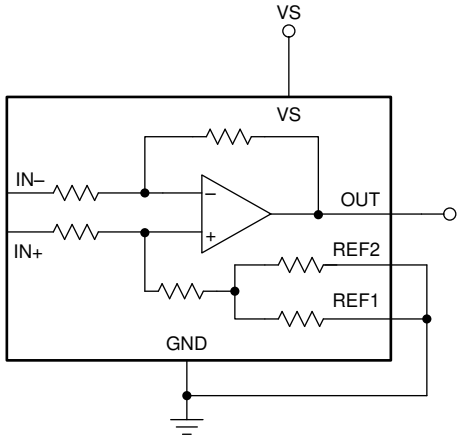



**Figure 7-3. Ground Referenced Output**

#### 7.4.2.2 VS Referenced Output

Unidirectional mode with a VS referenced output is configured by connecting both reference pins to the positive supply. Use this configuration for circuits that require power up and stabilization of the amplifier output signal and other control circuitry before power is applied to the load (see Figure 7-4).

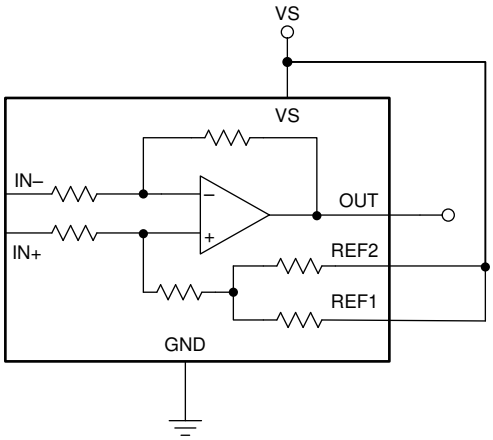



**Figure 7-4. VS Referenced Output**

### *7.4.3 Reference Pin Connections for Bidirectional Current Measurements*

The INA241x measures the differential voltage developed by current flowing through a resistor, commonly referred to as a current-sensing resistor or a current-shunt resistor. The INA241x can operate in either a unidirectional or bidirectional mode based on the voltage potential placed on the reference pins.

The linear range of the output stage is limited to how close the output voltage can approach ground as well the supply voltage as described in the *Specifications*. The selection of the current-sensing resistor along with the current range to be measured, selection of the gain option, as well as the voltage applied to the reference pins must be selected to keep the INA241x within the linear region of operation.

#### 7.4.3.1 Output Set to External Reference Voltage

Connecting both pins together and then to a reference voltage results in an output voltage equal to the reference voltage for the condition of shorted input pins or a 0V differential input. Figure 7-5 shows this configuration. The output voltage decreases below the reference voltage when the IN+ pin is negative relative to the IN– pin and increases when the IN+ pin is positive relative to the IN– pin. This technique is the most accurate way to bias the output to a precise voltage.

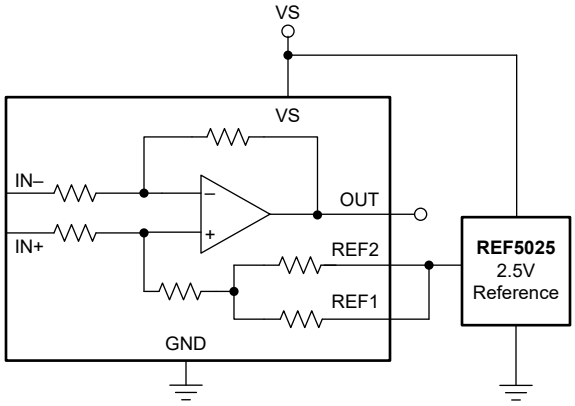



**Figure 7-5. External Reference Output**

#### 7.4.3.2 Output Set to Mid-Supply Voltage

By connecting one reference pin to VS and the other to the GND pin, Figure 7-6 shows that the output is set at half of the supply voltage when there is no differential input. This method creates a ratiometric offset to the supply voltage, where the output voltage remains at VS / 2 for 0V applied to the inputs.

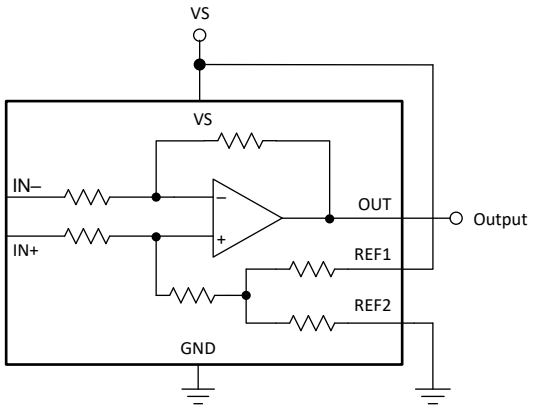



**Figure 7-6. Mid-Supply Voltage Output**

#### 7.4.3.3 Output Set to Mid-External Reference

In this case, Figure 7-7 shows how an external reference can divided by two by connecting one REF pin to ground and the other REF pin to the reference.

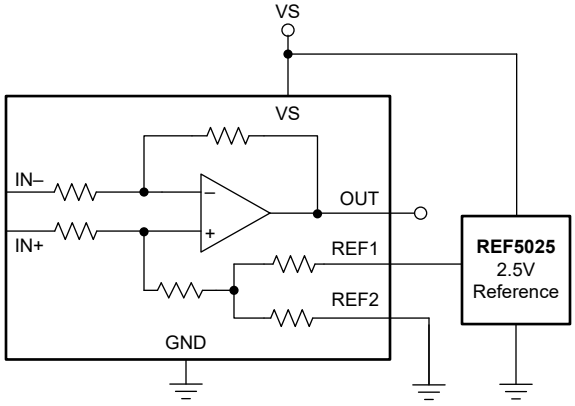



**Figure 7-7. Mid-External Reference Output**

#### 7.4.3.4 Output Set Using Resistor Divider

The INA241x reference pins allow for the mid-point of the output voltage to be adjusted for system circuitry connections to analog to digital converters (ADCs) or other amplifiers. The reference pins are designed to be connected directly to supply, ground, or a low-impedance reference voltage. The reference pins can be connected together and biased using a resistor divider to achieve a custom output voltage. If the amplifier is used in this configuration, as shown in Figure 7-8, use the output as a differential signal with respect to the resistor divider voltage. Use of the amplifier output as a single-ended signal in this configuration is not recommended because the internal impedance shifts can adversely affect device performance specifications. If single-ended measurement is required, TI recommends to use an external op amp to buffer the resistor divider voltage (see Figure 7-9).

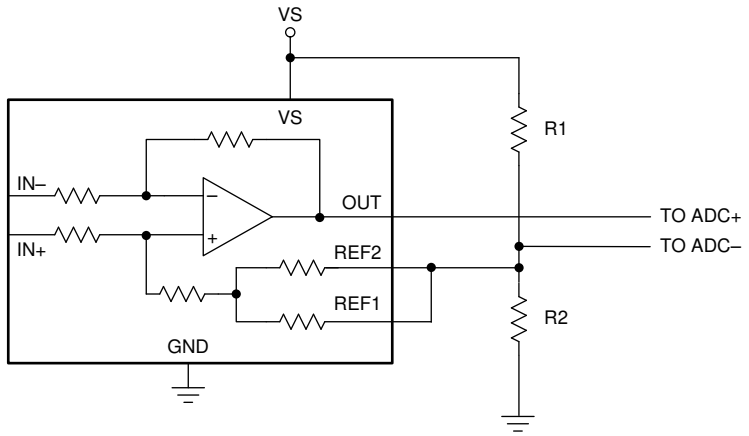



**Figure 7-8. Setting the Reference Using a Resistor Divider**

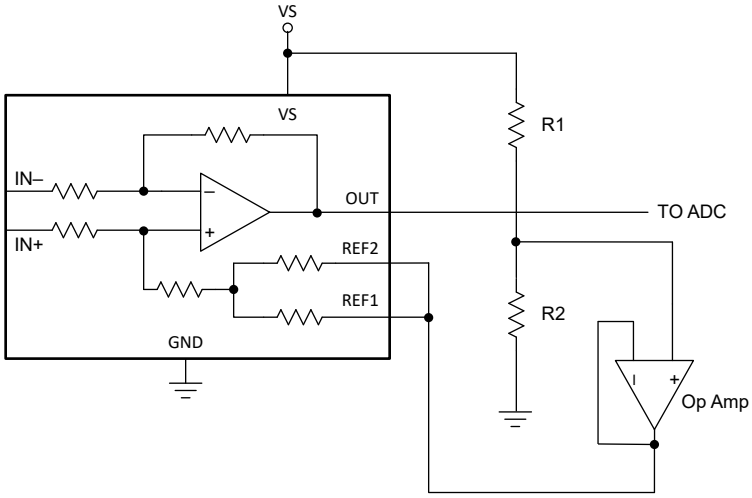



**Figure 7-9. Setting the Reference Using a Resistor Divider and an Op Amp Buffer**

### 7.4.4 High Signal Throughput

With a bandwidth of 1.1MHz at a gain of 20V/V and a slew rate of 8V/µs, the INA241x is specifically designed for detecting and protecting applications from fast inrush currents. As shown in Table 7-1, the INA241x responds in less than 1µs for a system measuring a 75A threshold on a 2mΩ shunt.

**Table 7-1. Response Time**

| PARAMETER | | EQUATION | INA241x AT $V_S$ = 5V |
|---|---|---|---|
| G | Gain | | 20V/V |
| $I_{MAX}$ | Maximum current | | 100A |
| $I_{Threshold}$ | Threshold current | | 75A |
| $R_{SENSE}$ | Current sense resistor value | | 2mΩ |
| $V_{OUT\_MAX}$ | Output voltage at maximum current | $V_{OUT\_MAX} = I_{MAX} \times R_{SENSE} \times G$ | 4V |
| $V_{OUT\_THR}$ | Output voltage at threshold current | $V_{OUT\_THR} = I_{THR} \times R_{SENSE} \times G$ | 3V |
| SR | Slew rate | | 8V/µs |
| $T_{response}$ | Output response time | $T_{response} = V_{OUT\_THR} / SR$ | < 1µs |

## 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

The INA241x amplifies the voltage developed across a current-sensing resistor as current flows through the resistor to the load. The wide input common-mode voltage range and high common-mode rejection of the INA241x make the device usable over a wide range of voltage rails while still maintaining an accurate current measurement.

#### 8.1.1 $R_{SENSE}$ and Device Gain Selection

The accuracy of any current-sense amplifier is maximized by choosing the largest current-sense resistor value possible. A larger value sense resistor maximizes the differential input signal for a given amount of current flow and reduces the error contribution of the offset voltage. However, there are practical limits as to how large the current-sense resistor value can be in a given application because of the physical dimensions of the package, package construction, and maximum power dissipation. Equation 2 gives the maximum value for the current-sense resistor for a given power dissipation budget:

$$R_{SENSE} < \frac{PD_{MAX}}{I_{MAX}^2} \quad (2)$$

where:

- $PD_{MAX}$ is the maximum allowable power dissipation in $R_{SENSE}$.
- $I_{MAX}$ is the maximum current that flows through $R_{SENSE}$.

An additional limitation on the size of the current-sense resistor and device gain is due to the power-supply voltage, $V_S$, and device swing-to-rail limitations. To make sure that the current-sense signal is properly passed to the output, both positive and negative output swing limitations must be examined. Equation 3 provides the maximum values of $R_{SENSE}$ and GAIN to keep the device from exceeding the positive swing limitation.

$$I_{MAX} \times R_{SENSE} \times GAIN < V_{SP} \quad (3)$$

where:

- $I_{MAX}$ is the maximum current that flows through $R_{SENSE}$.
- GAIN is the gain of the current-sense amplifier.
- $V_{SP}$ is the positive output swing of the device as specified in the *Specifications*.

To avoid positive output swing limitations when selecting the value of $R_{SENSE}$, there is always a trade-off between the value of the sense resistor and the gain of the device under consideration. If the sense resistor selected for the maximum power dissipation is too large, then selecting a lower gain device is possible to avoid positive swing limitations.

The negative swing limitation places a limit on how small the sense resistor value can be for a given application. Equation 4 provides the limit on the minimum value of the sense resistor.

$$I_{MIN} \times R_{SENSE} \times GAIN > V_{SN} \quad (4)$$

where:

- $I_{MIN}$ is the minimum current that flows through $R_{SENSE}$.
- GAIN is the gain of the current-sense amplifier.
- $V_{SN}$ is the negative output swing of the device as specified in the *Specifications*.

Table 8-1 shows an example of the different results obtained from using five different gain versions of the INA241x. From the table data, the highest gain device allows a smaller current-shunt resistor and decreased power dissipation in the element.

**Table 8-1. $R_{SENSE}$ Selection and Power Dissipation (1)**

| PARAMETER | | EQUATION | RESULTS AT $V_S$ = 5V | | | | |
|---|---|---|---|---|---|---|---|
| | | | A1, B1 DEVICES | A2, B2 DEVICES | A3, B3 DEVICES | A4, B4 DEVICES | A5, B5 DEVICES |
| G | Gain | | 10V/V | 20V/V | 50V/V | 100V/V | 200V/V |
| $V_{SENSE}$ | Ideal differential input voltage | $V_{SENSE} = V_{OUT} / G$ | 500mV | 250mV | 100mV | 50mV | 25mV |
| $R_{SENSE}$ | Current sense resistor value | $R_{SENSE} = V_{SENSE} / I_{MAX}$ | 50mΩ | 25mΩ | 10mΩ | 5mΩ | 2.5mΩ |
| $P_{SENSE}$ | Current-sense resistor power dissipation | $R_{SENSE} \times I_{MAX}2$ | 5W | 2.5W | 1W | 0.5W | 0.25W |

(1) Design example with 10A full-scale current with maximum output voltage set to 5V.

## 8.2 Typical Application

The INA241x is a bidirectional, current-sense amplifier capable of measuring currents through a resistive shunt with common-mode voltages from –5 V to +110 V.

### 8.2.1 Inline Motor Current-Sense Application

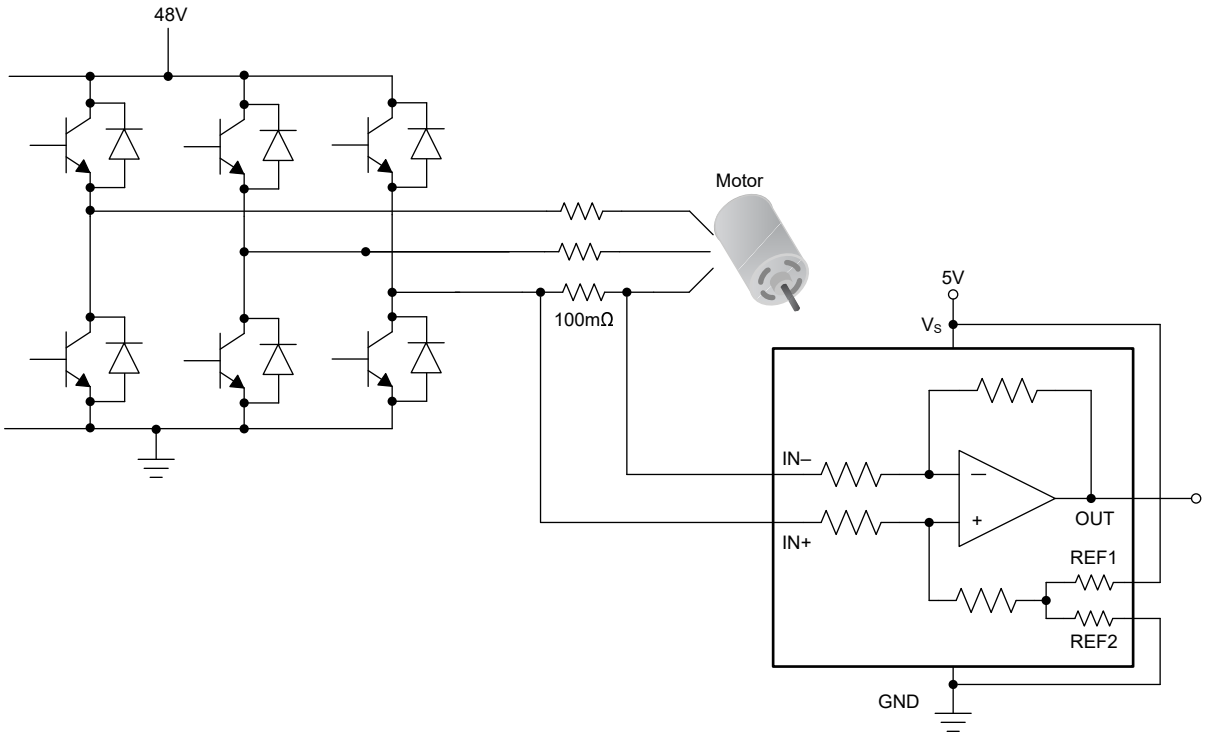



**Figure 8-1. Inline Motor Application Circuit**

#### 8.2.1.1 Design Requirements

Inline current sensing has many advantages in motor control, from torque ripple reduction to real-time motor health monitoring. However, the full-scale PWM voltage requirements for inline current measurements provide challenges to accurately measure the current. Switching frequencies in the 50kHz to 100kHz range create higher ΔV/Δt signal transitions that must be addressed to obtain accurate inline current measurements.

With a superior common-mode rejection capability, high precision, and a high common-mode specification, the INA241x provides performance for a wide range of common-mode voltages.

#### 8.2.1.2 Detailed Design Procedure

For this application, the INA241x measures current in the drive circuitry of a 48V, 4000 RPM motor.

To demonstrate the performance of the device, the INA241A2 with a gain of 20V/V is selected for this design and powered from a 5V supply.

Using the information in the Section 7.4.3.2 section, the reference point is set to mid-scale by splitting the supply with REF1 connected to supply and REF2 connected to ground. This configuration allows for bipolar current measurements. Alternatively, the reference pins can be tied together and driven with an external precision reference.

The current-sensing resistor is sized so that the output of the INA241x is not saturated. A value of 100mΩ is selected to maintain the analog input within the device limits.

#### 8.2.1.3 Application Curve

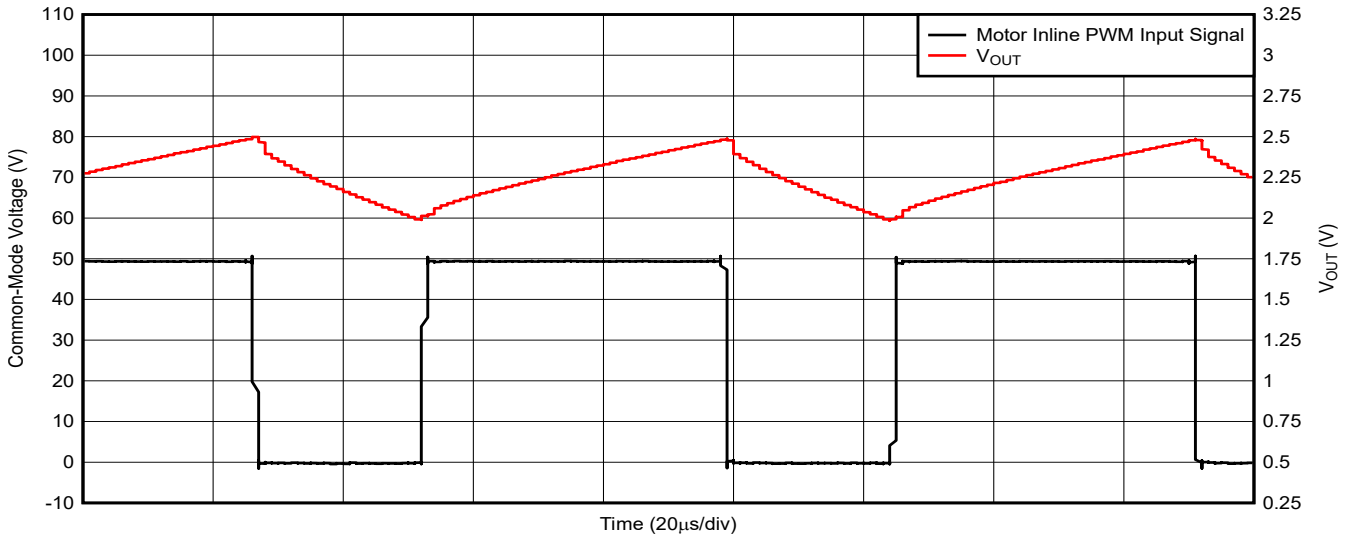



**Figure 8-2. INA241A2 Inline Motor Current-Sense Input and Output Signals**

## 8.3 Power Supply Recommendations

The INA241x makes accurate measurements beyond the connected power-supply voltage ($V_S$) because the inputs (IN+ and IN–) can operate anywhere between –5V and 110V independent of $V_S$. For example, with the $V_S$ power supply equal to 5V, the common-mode voltage of the measured shunt can be as high as 110V.

### *8.3.1 Power Supply Decoupling*

Place the power-supply bypass capacitor as close to the supply and ground pins as possible. TI recommends a bypass capacitor value of 0.1µF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.

## 8.4 Layout

### *8.4.1 Layout Guidelines*

Attention to good layout practices is always recommended.

- Connect the input pins to the sensing resistor using a Kelvin or 4-wire connection. This connection technique makes sure that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current sense resistor, any additional high-current carrying impedance can cause significant measurement errors.
- Place the power-supply bypass capacitor as close to the device power supply and ground pins as possible. The recommended value of this bypass capacitor is 0.1µF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.

### 8.4.2 Layout Examples

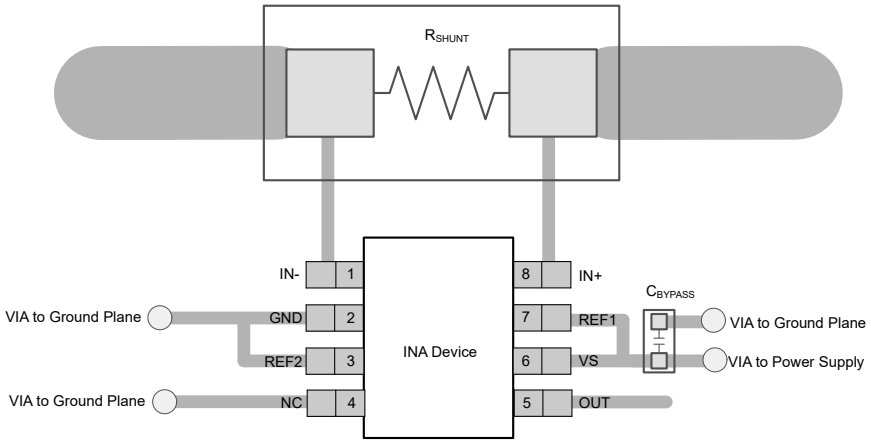



**Figure 8-3. INA241x SOT-23 (DDF), SOIC (D) and VSSOP (DGK) Package Recommended Layout**

# 9 Device and Documentation Support

## 9.1 Documentation Support

### *9.1.1 Related Documentation*

For related documentation see the following: Texas Instruments, *INA296EVM*, EVM user's guide

## 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision C (October 2023) to Revision D (December 2024) | Page |
|---|---|
| • Updated the number format for tables, figures, and cross-references throughout the document | 1 |
| • Deleted DGS package information throughout the document; this package is available in automotive only | 1 |

| Changes from Revision B (July 2023) to Revision C (October 2023) | Page |
|---|---|
| • Deleted the preview note from D package from package information table and throughout the data sheet | 1 |

| Changes from Revision A (August 2022) to Revision B (July 2023) | Page |
|---|---|
| • Added the D and DGS packages to the data sheet | 1 |
| • Changed package information from body size to package size | 1 |
| • Deleted preview note from DGK package from package information table | 1 |
| • Added the D and DGS packages pin configuration | 2 |
| • Added DGS package in recommended layout examples | 25 |

| Changes from Revision * (March 2022) to Revision A (August 2022) | Page |
|---|---|
| • Changed data sheet status from Advanced Information to Production Data | 1 |

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| INA241A1IDDFR | Active | Production | SOT-23-THIN (DDF) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2PH3 |
| INA241A1IDDFR.B | Active | Production | SOT-23-THIN (DDF) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2PH3 |
| INA241A1IDGKR | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2U6B |
| INA241A1IDGKR.B | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2U6B |
| INA241A1IDR | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | I241A1 |
| INA241A1IDR.B | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | I241A1 |
| INA241A2IDDFR | Active | Production | SOT-23-THIN (DDF) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2PI3 |
| INA241A2IDDFR.B | Active | Production | SOT-23-THIN (DDF) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2PI3 |
| INA241A2IDGKR | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2U7B |
| INA241A2IDGKR.B | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2U7B |
| INA241A2IDR | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | I241A2 |
| INA241A2IDR.B | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | I241A2 |
| INA241A3IDDFR | Active | Production | SOT-23-THIN (DDF) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2PJ3 |
| INA241A3IDDFR.B | Active | Production | SOT-23-THIN (DDF) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2PJ3 |
| INA241A3IDGKR | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2U8B |
| INA241A3IDGKR.B | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2U8B |
| INA241A3IDR | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | I241A3 |
| INA241A3IDR.B | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | I241A3 |
| INA241A4IDDFR | Active | Production | SOT-23-THIN (DDF) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2PK3 |
| INA241A4IDDFR.B | Active | Production | SOT-23-THIN (DDF) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2PK3 |
| INA241A4IDGKR | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2U9B |
| INA241A4IDGKR.B | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2U9B |
| INA241A4IDR | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | I241A4 |
| INA241A4IDR.B | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | I241A4 |
| INA241A5IDDFR | Active | Production | SOT-23-THIN (DDF) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2PL3 |
| INA241A5IDDFR.B | Active | Production | SOT-23-THIN (DDF) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2PL3 |
| INA241A5IDGKR | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2UAB |
| INA241A5IDGKR.B | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2UAB |
| INA241A5IDR | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | I241A5 |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| INA241A5IDR.B | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | I241A5 |
| INA241B1IDDFR | Active | Production | SOT-23-THIN (DDF) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2PM3 |
| INA241B1IDDFR.B | Active | Production | SOT-23-THIN (DDF) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2PM3 |
| INA241B1IDGKR | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2UBB |
| INA241B1IDGKR.B | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2UBB |
| INA241B1IDR | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | I241B1 |
| INA241B1IDR.B | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | I241B1 |
| INA241B2IDDFR | Active | Production | SOT-23-THIN (DDF) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2PN3 |
| INA241B2IDDFR.B | Active | Production | SOT-23-THIN (DDF) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2PN3 |
| INA241B2IDGKR | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2UCB |
| INA241B2IDGKR.B | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2UCB |
| INA241B2IDR | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | I241B2 |
| INA241B2IDR.B | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | I241B2 |
| INA241B3IDDFR | Active | Production | SOT-23-THIN (DDF) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2PO3 |
| INA241B3IDDFR.B | Active | Production | SOT-23-THIN (DDF) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2PO3 |
| INA241B3IDGKR | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2UDB |
| INA241B3IDGKR.B | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2UDB |
| INA241B3IDR | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | I241B3 |
| INA241B3IDR.B | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | I241B3 |
| INA241B4IDDFR | Active | Production | SOT-23-THIN (DDF) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2PP3 |
| INA241B4IDDFR.B | Active | Production | SOT-23-THIN (DDF) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2PP3 |
| INA241B4IDGKR | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2UEB |
| INA241B4IDGKR.B | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2UEB |
| INA241B4IDR | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | I241B4 |
| INA241B4IDR.B | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | I241B4 |
| INA241B5IDDFR | Active | Production | SOT-23-THIN (DDF) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2PQ3 |
| INA241B5IDDFR.B | Active | Production | SOT-23-THIN (DDF) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2PQ3 |
| INA241B5IDGKR | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2UFB |
| INA241B5IDGKR.B | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2UFB |
| INA241B5IDR | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | I241B5 |
| INA241B5IDR.B | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | I241B5 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.



**OTHER QUALIFIED VERSIONS OF INA241A, INA241B :**

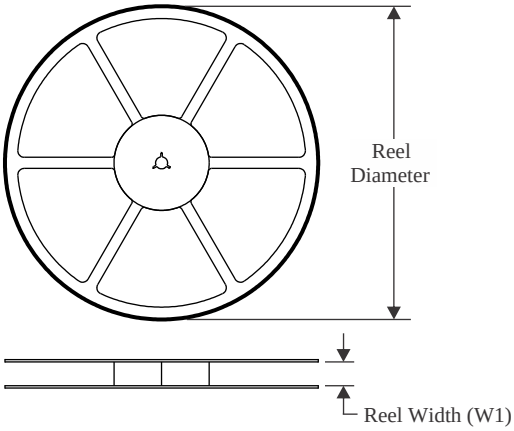
- Automotive : INA241A-Q1, INA241B-Q1

NOTE: Qualified Version Definitions:

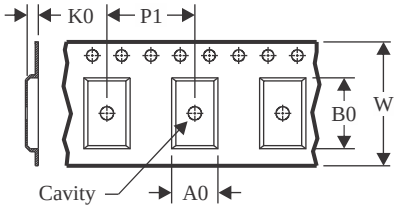
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

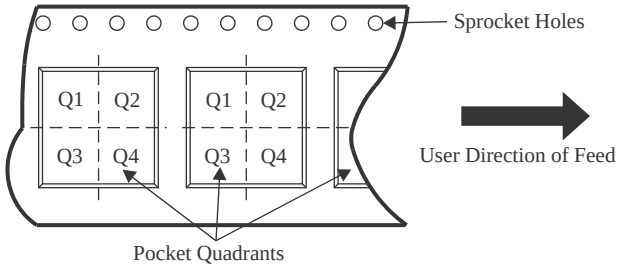



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

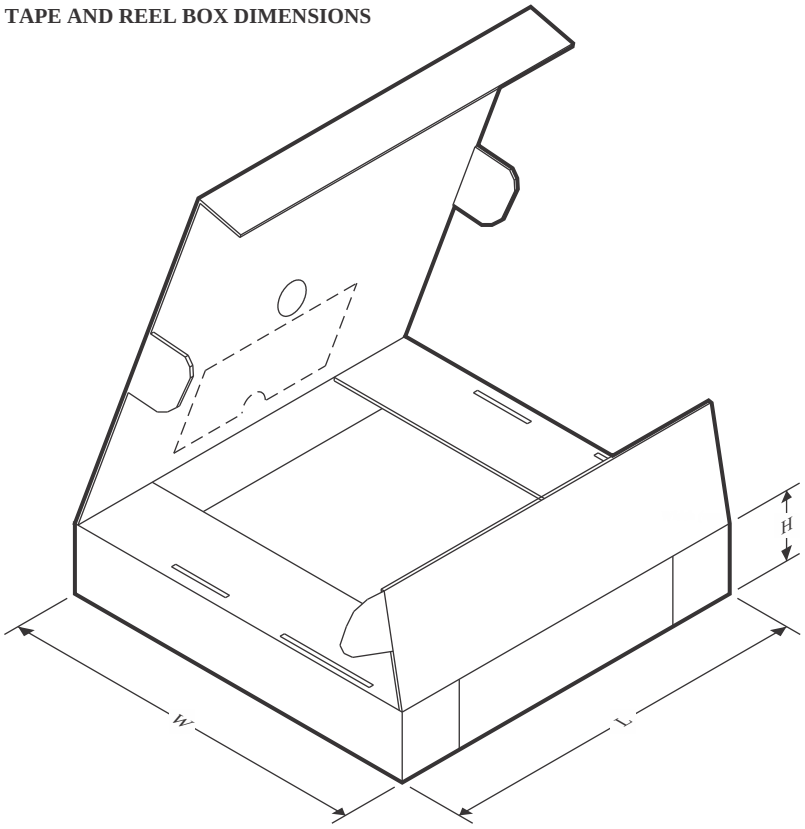



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| INA241A1IDDFR | SOT-23-THIN | DDF | 8 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| INA241A1IDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| INA241A1IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| INA241A2IDDFR | SOT-23-THIN | DDF | 8 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| INA241A2IDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| INA241A2IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| INA241A3IDDFR | SOT-23-THIN | DDF | 8 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| INA241A3IDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| INA241A3IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| INA241A4IDDFR | SOT-23-THIN | DDF | 8 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| INA241A4IDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| INA241A4IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| INA241A5IDDFR | SOT-23-THIN | DDF | 8 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| INA241A5IDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| INA241A5IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| INA241B1IDDFR | SOT-23-THIN | DDF | 8 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| INA241B1IDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| INA241B1IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| INA241B2IDDFR | SOT-23-THIN | DDF | 8 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| INA241B2IDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| INA241B2IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| INA241B3IDDFR | SOT-23-THIN | DDF | 8 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| INA241B3IDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| INA241B3IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| INA241B4IDDFR | SOT-23-THIN | DDF | 8 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| INA241B4IDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| INA241B4IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| INA241B5IDDFR | SOT-23-THIN | DDF | 8 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| INA241B5IDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| INA241B5IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| INA241A1IDDFR | SOT-23-THIN | DDF | 8 | 3000 | 210.0 | 185.0 | 35.0 |
| INA241A1IDGKR | VSSOP | DGK | 8 | 2500 | 356.0 | 356.0 | 35.0 |
| INA241A1IDR | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| INA241A2IDDFR | SOT-23-THIN | DDF | 8 | 3000 | 210.0 | 185.0 | 35.0 |
| INA241A2IDGKR | VSSOP | DGK | 8 | 2500 | 356.0 | 356.0 | 35.0 |
| INA241A2IDR | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| INA241A3IDDFR | SOT-23-THIN | DDF | 8 | 3000 | 210.0 | 185.0 | 35.0 |
| INA241A3IDGKR | VSSOP | DGK | 8 | 2500 | 356.0 | 356.0 | 35.0 |
| INA241A3IDR | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| INA241A4IDDFR | SOT-23-THIN | DDF | 8 | 3000 | 210.0 | 185.0 | 35.0 |
| INA241A4IDGKR | VSSOP | DGK | 8 | 2500 | 356.0 | 356.0 | 35.0 |
| INA241A4IDR | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| INA241A5IDDFR | SOT-23-THIN | DDF | 8 | 3000 | 210.0 | 185.0 | 35.0 |
| INA241A5IDGKR | VSSOP | DGK | 8 | 2500 | 356.0 | 356.0 | 35.0 |
| INA241A5IDR | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| INA241B1IDDFR | SOT-23-THIN | DDF | 8 | 3000 | 210.0 | 185.0 | 35.0 |
| INA241B1IDGKR | VSSOP | DGK | 8 | 2500 | 356.0 | 356.0 | 35.0 |
| INA241B1IDR | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |

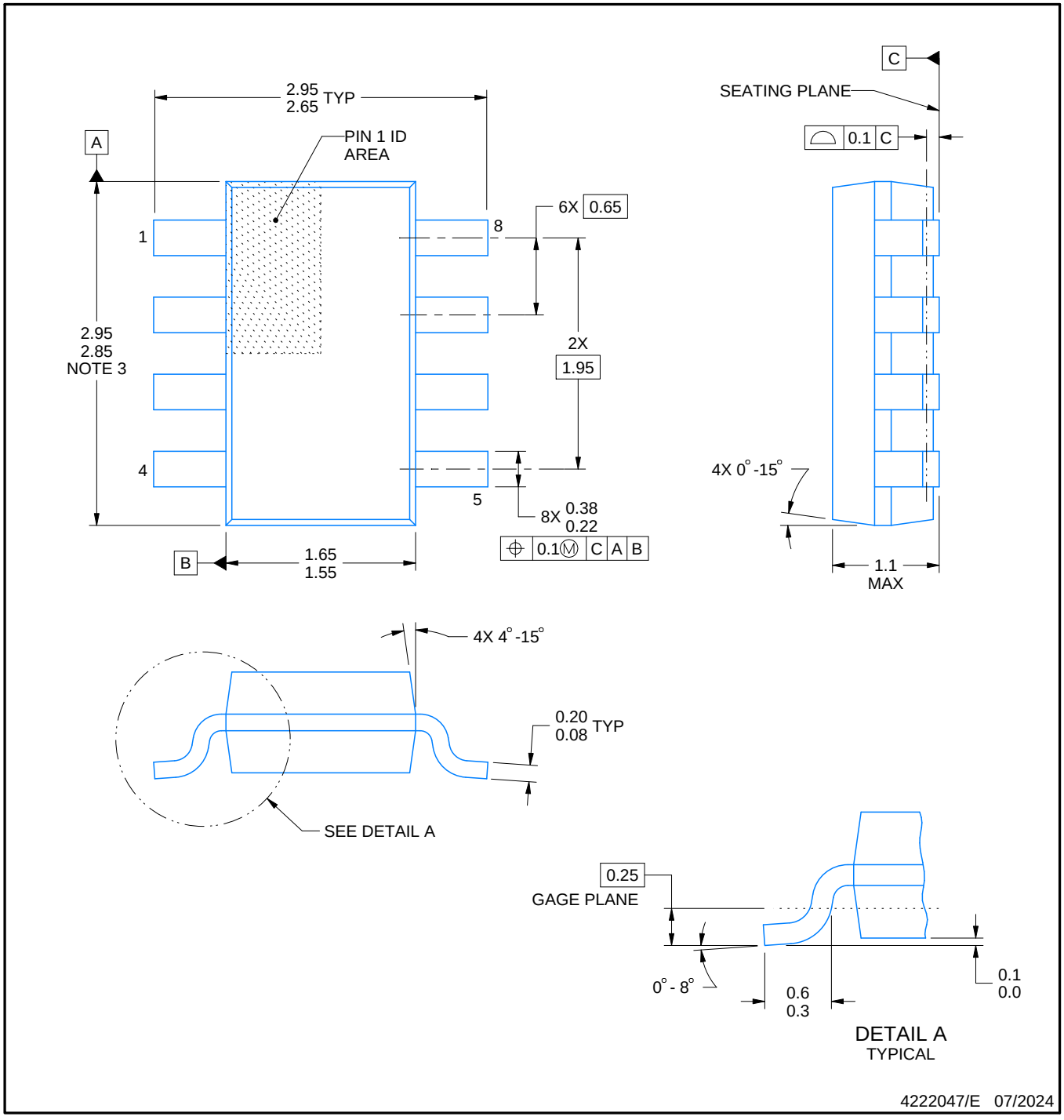
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| INA241B2IDDFR | SOT-23-THIN | DDF | 8 | 3000 | 210.0 | 185.0 | 35.0 |
| INA241B2IDGKR | VSSOP | DGK | 8 | 2500 | 356.0 | 356.0 | 35.0 |
| INA241B2IDR | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| INA241B3IDDFR | SOT-23-THIN | DDF | 8 | 3000 | 210.0 | 185.0 | 35.0 |
| INA241B3IDGKR | VSSOP | DGK | 8 | 2500 | 356.0 | 356.0 | 35.0 |
| INA241B3IDR | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| INA241B4IDDFR | SOT-23-THIN | DDF | 8 | 3000 | 210.0 | 185.0 | 35.0 |
| INA241B4IDGKR | VSSOP | DGK | 8 | 2500 | 356.0 | 356.0 | 35.0 |
| INA241B4IDR | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| INA241B5IDDFR | SOT-23-THIN | DDF | 8 | 3000 | 210.0 | 185.0 | 35.0 |
| INA241B5IDGKR | VSSOP | DGK | 8 | 2500 | 356.0 | 356.0 | 35.0 |
| INA241B5IDR | SOIC | D | 8 | 2500 | 340.5 | 336.1 | 25.0 |

# PACKAGE OUTLINE

## DDF0008A

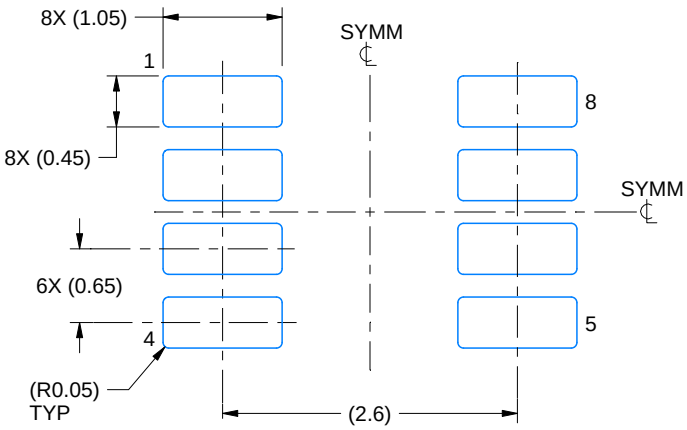
## SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

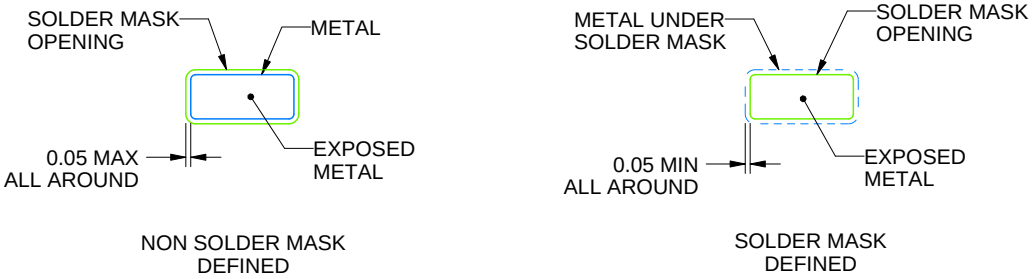



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X




SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

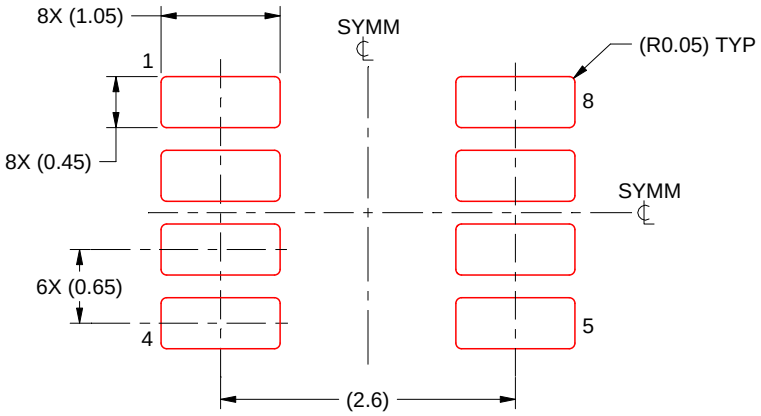
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## DDF0008A

## SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

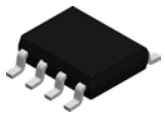



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

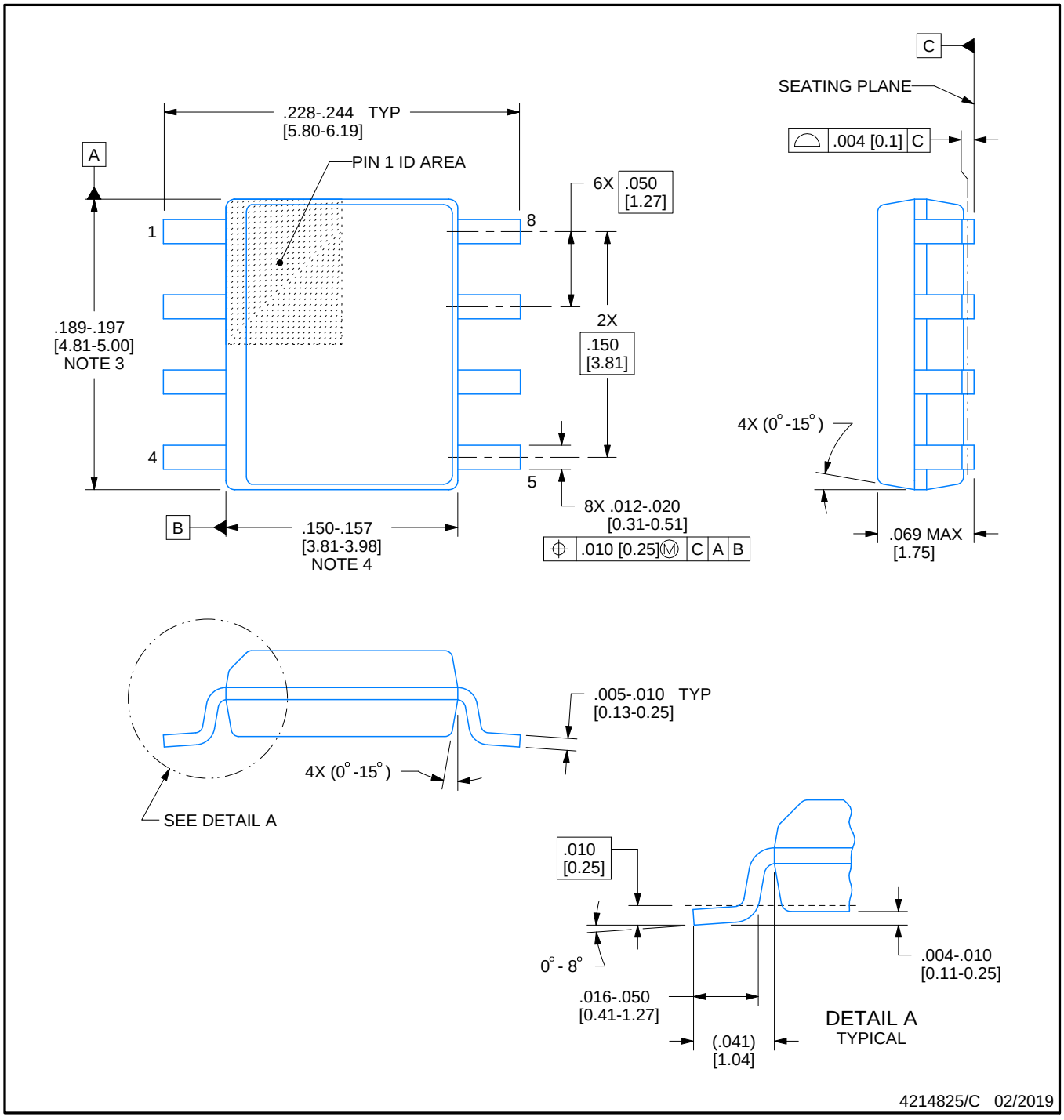


# PACKAGE OUTLINE

## D0008A

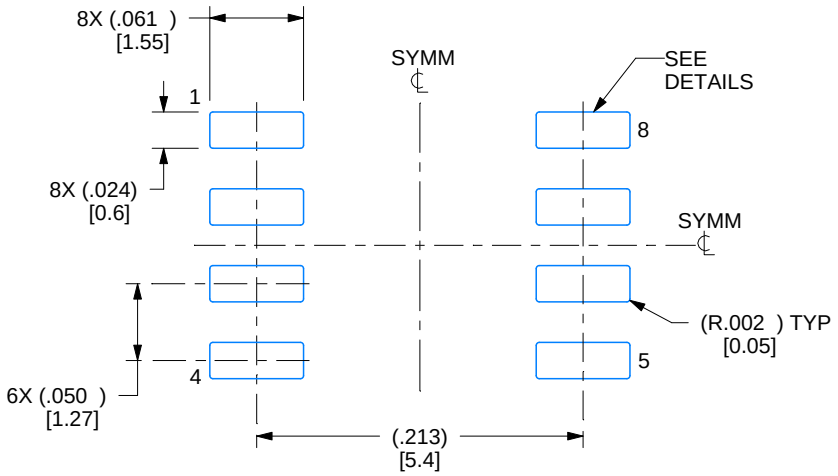
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

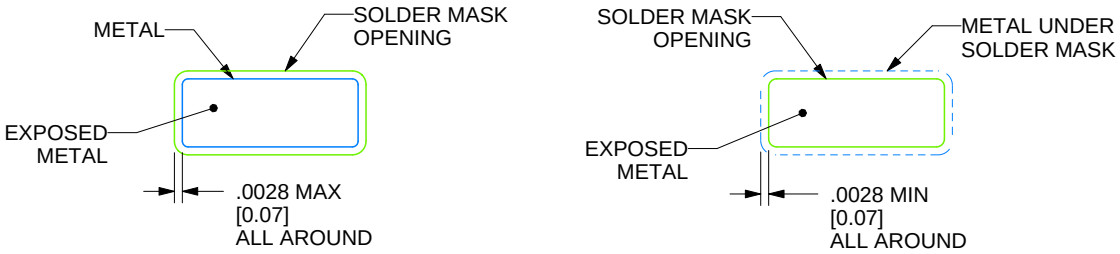



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

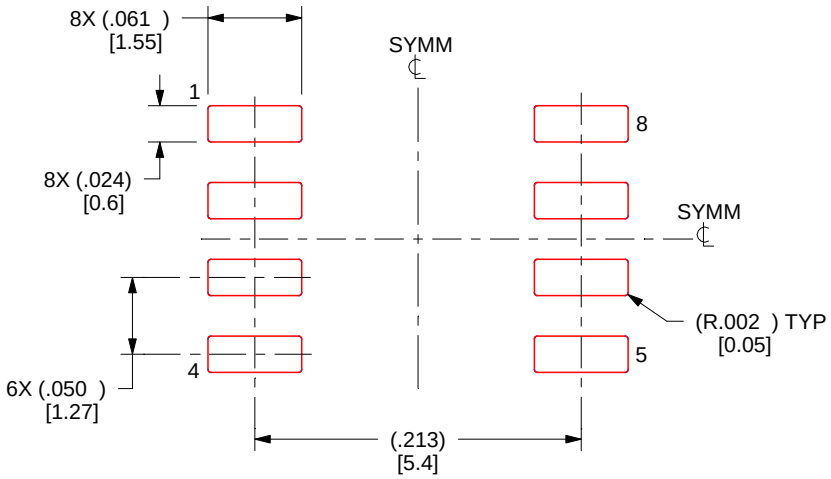
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

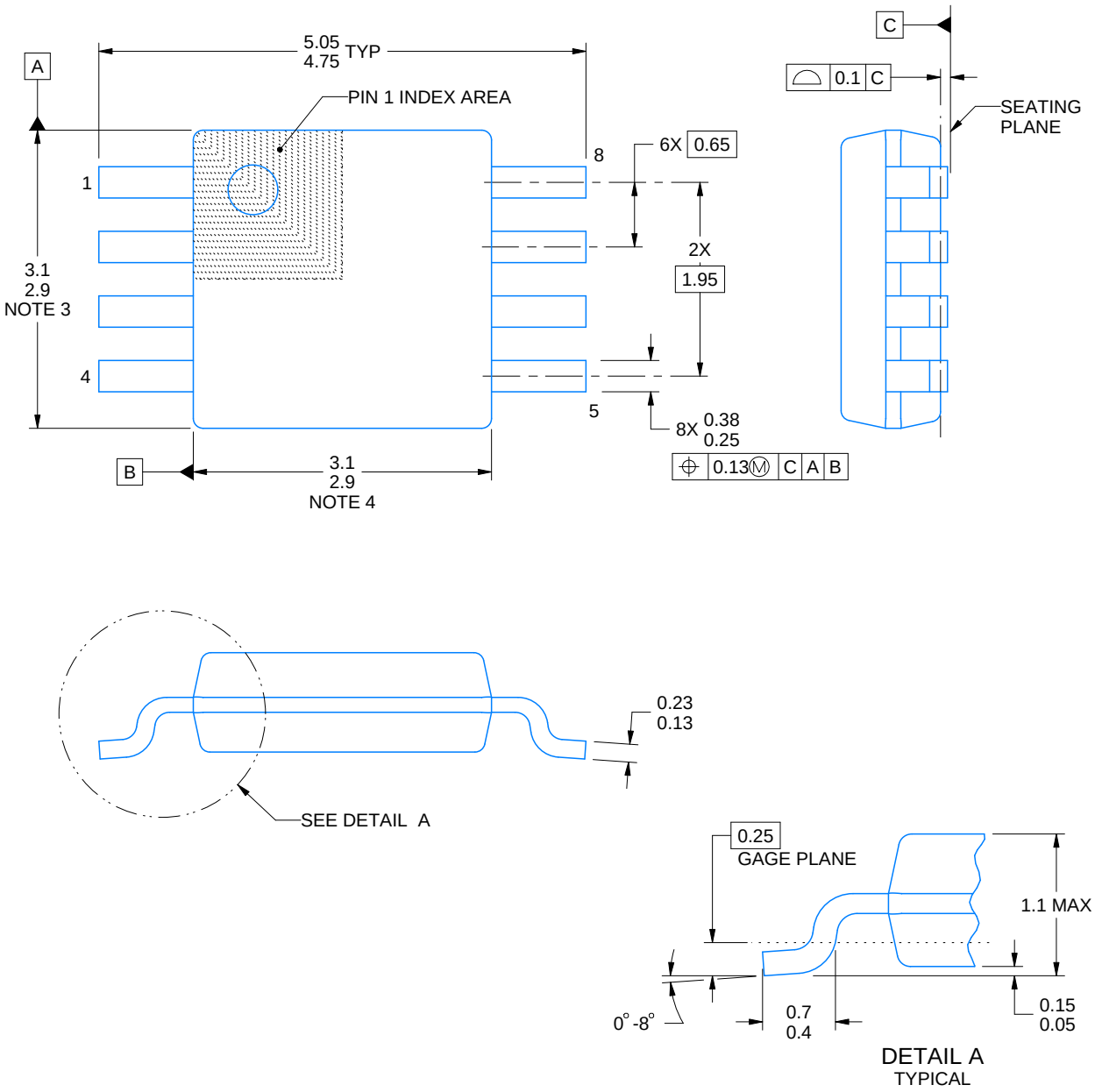
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DGK0008A

## VSSOP - 1.1 mm max height

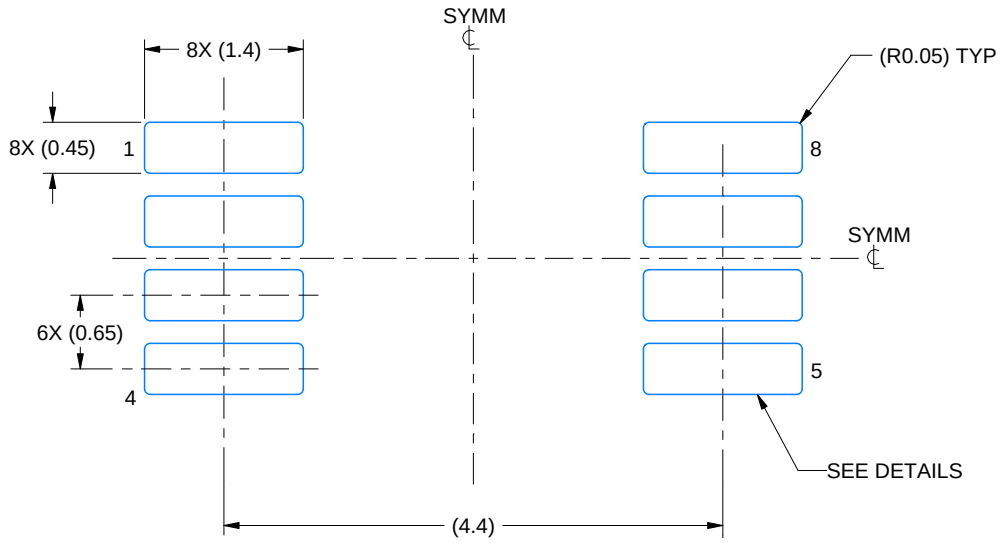
SMALL OUTLINE PACKAGE



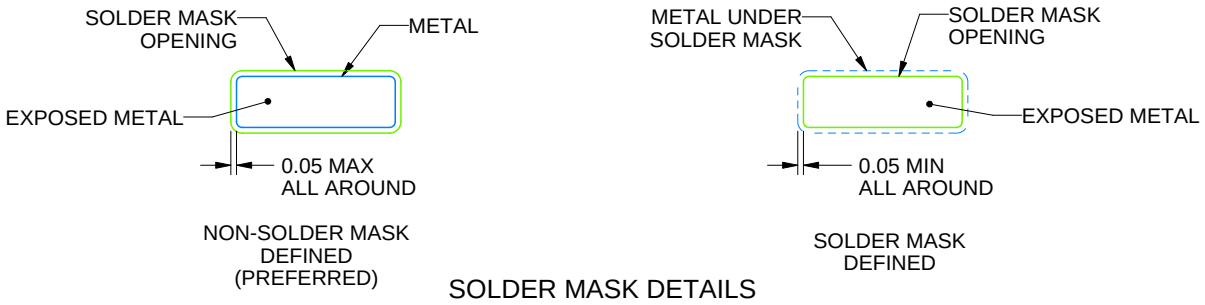

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

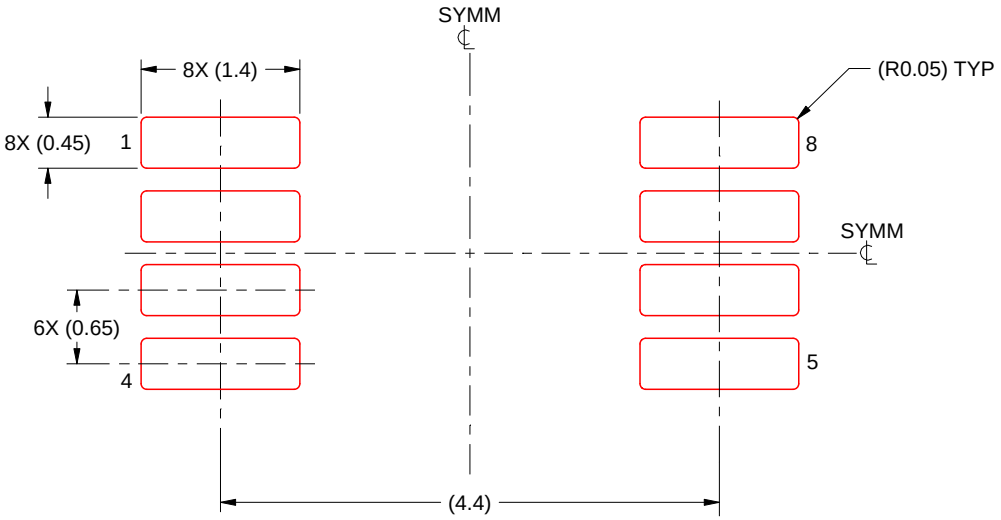



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.




SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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