DRV81008-Q1: 8-channel, 40V, 700mΩ, Fully Protected Low-side Driver

1 Features

- AEC-Q100 qualified for automotive applications
  - Temperature grade 1: –40°C to +125°C, T_A
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- **3V to 40V** Analog supply voltage
  - Cranking capability down to 3V
  - Supports LV124 Automotive standard
- **3V to 5.5V** Digital supply voltage
  - Compatible with 3.3V and 5V microcontrollers
- **42V** minimum drain to the source clamping voltage
- $R_{DS(ON)}$: **700mΩ** typical at 12V, 25 °C
- Current: **330mA** per output at 85 °C, with all channels ON
- **2 parallel inputs** with mapping functionality
- Fail-safe activation in **Limp Home** mode
  - Using nSLEEP and IN pins
- Low-current sleep mode
  - < 3µA for T_J ≤ 85 °C using nSLEEP pin
- 16-bit SPI interface for control and diagnosis
  - Daisy Chain capability
  - Compatible with 8-bit SPI devices
- Supports various **protection features** -
  - Integrated Reverse battery protection
  - Short circuit to ground and battery protection
  - Stable behavior at under voltage conditions
  - Over Current latch OFF
  - Overtemperature warning
  - Thermal shutdown latch OFF
  - Overvoltage protection
  - Loss of battery and loss of ground protection
  - Electrostatic discharge (ESD) protection
- Supports several **diagnostic features** -
  - Diagnostic information via SPI register
  - Over Load detection in ON state
  - Open Load detection in OFF state
  - Input and Output Status Monitor

2 Applications

- Zone Control Module (ZCM)
- Automotive Body Control Module (BCM)
- HVAC Control
- Automotive Lighting
- Gasoline and Diesel Engine
- Vehicle Control Unit (VCU)
- Programmable Logic Controller (PLC)
- Pneumatic Valve
- General purpose relay driver

3 Description

The DRV81008-Q1 is an eight-channel low-side driver with integrated protection and diagnostic features. It is designed to control relays in automotive and industrial applications.

A serial peripheral interface (SPI) with daisy chain capability controls and diagnoses the loads and the device. Two input pins with mapping functionality allow direct PWM control of the outputs. The device supports Limp Home mode for fail-safe activation.

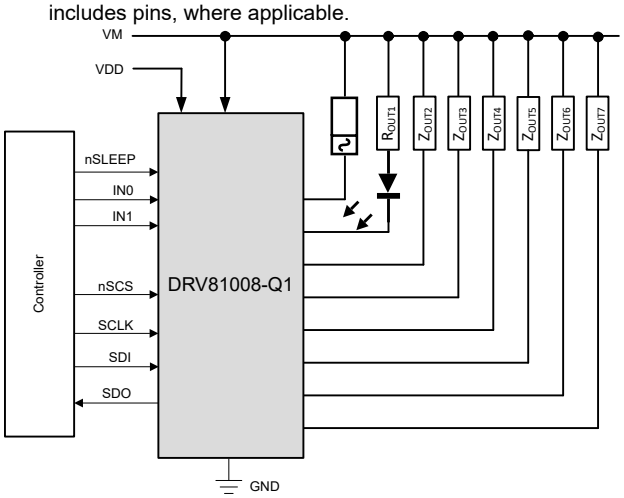
Each low-side switch of the DRV81008-Q1 has 700mΩ ON resistance. The device can support 330mA current per output when all eight channels are ON simultaneously. Integrated clamp circuits on each output dissipates the stored energy during turning OFF inductive loads.

The DRV81008-Q1 supports various protection features such as undervoltage, overvoltage, short circuit, and open load detection. A high level of integration with embedded protection and diagnostic features makes the DRV81008-Q1 an excellent choice for automotive body and powertrain applications, as well as industrial relay control applications.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE (NOM)
DRV81008QPWPRQ1	HTSSOP (24)	7.8mm × 6.4mm	7.7mm × 4.4mm

(1) For more information, see Section 10
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Pin Configuration and Functions....3
5 Specifications....4
5.1 Absolute Maximum Ratings....4
5.2 ESD Ratings....4
5.3 Recommended Operating Conditions....5
5.4 Thermal Information....5
5.5 Electrical Characteristics....6
5.6 Typical Characteristics....10
6 Detailed Description....14
6.1 Overview....14
6.2 Functional Block Diagram....15
6.3 Feature Description....16
7 Application and Implementation....37
7.1 Application Information....37
7.2 Layout....39
8 Device and Documentation Support....41
8.1 Receiving Notification of Documentation Updates....41
8.2 Support Resources....41
8.3 Trademarks....41
8.4 Electrostatic Discharge Caution....41
8.5 Glossary....41
9 Revision History....41
10 Mechanical, Packaging, and Orderable Information....41

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4 Pin Configuration and Functions

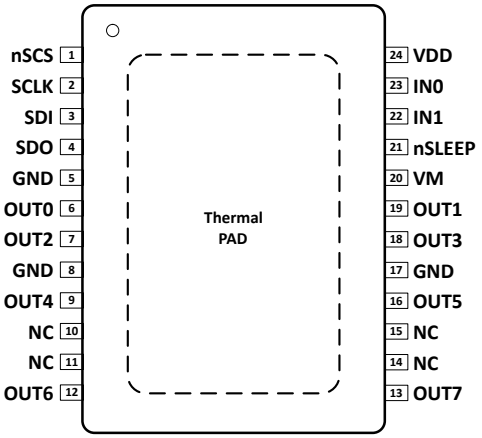

Figure 4-1. 24-Pin HTSSOP (PWP) Top View

Table 4-1. Pin Functions

PIN		TYPE[(1)]	DESCRIPTION
NAME	NO.		
VM	20	P	Analog supply voltage for power stage and protection circuits
VDD	24	P	Digital supply voltage for SPI
GND	5, 8, 17	G	Ground pin
nSCS	1	I	Serial chip select. An active low on this pin enables the serial interface communications. Integrated pull-up to VDD.
SCLK	2	I	Serial clock input. Serial data is shifted out and captured on the corresponding rising and falling edge on this pin. Integrated pull-down to GND.
SDI	3	I	Serial data input. Data is captured on the falling edge of SCLK. Integrated pull-down to GND.
SDO	4	O	Serial data output. Data is shifted out on the rising edge of SCLK.
nSLEEP	21	I	Logic high activates Idle mode. Integrated pull-down to GND.
IN0	23	I	Connected to channel 2 by default and in Limp Home mode. Integrated pull-down to GND.
IN1	22	I	Connected to channel 3 by default and in Limp Home mode. Integrated pull-down to GND.
OUT0	6	O	Drain of low-side FET (channel 0)
OUT2	7	O	Drain of low-side FET (channel 2)
OUT4	9	O	Drain of low-side FET (channel 4)
OUT6	12	O	Drain of low-side FET (channel 6)
OUT7	13	O	Drain of low-side FET (channel 7)
OUT5	16	O	Drain of low-side FET (channel 5)
OUT3	18	O	Drain of low-side FET (channel 3)
OUT1	19	O	Drain of low-side FET (channel 1)
NC	10, 11, 14, 15	-	No connect, internally not bonded
PAD	-	-	Exposed pad. Connect the exposed pad to PCB ground for cooling and EMC.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power

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5 Specifications

5.1 Absolute Maximum Ratings

Over T_J = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise noted)

		MIN	MAX	UNIT
V_M	Analog supply voltage	-0.3	42	V
V_{DD}	Digital supply voltage	-0.3	5.75	V
V_{M_LD}	Supply voltage for load dump protection		42	V
V_{M_SC}	Supply voltage for short circuit protection	0	28	V
$-V_{M_REV}$	Reverse polarity voltage, $T_J(0)$ = 25 °C, t ≤ 2 min, R_L = 70 Ω on all channels	-	18	V
I_{VM}	Current through VM pin, t ≤ 2 min	-10	10	mA
$\|I_L\|$	Load current, single channel	-	I_{L_OCP0}	A
V_{DS}	Voltage at power FET	-0.3	42	V
E_{AS}	Maximum energy dissipation single pulse, $T_J(0)$ = 25 °C, $I_L(0) = 2*I_{L_EAR}$	-	50	mJ
E_{AS}	Maximum energy dissipation single pulse, $T_J(0)$ = 150 °C, $I_L(0)$ = 400 mA	-	25	mJ
E_{AR}	Maximum energy dissipation for repetitive pulses $-I_{L_EAR}$, $2*10^6$ cycles, $T_J(0)$ = 85 °C, $I_L(0) = I_{L_EAR}$	-	10	mJ
V_I	Voltage at IN0, IN1, nSCS, SCLK, SDI pins	-0.3	5.75	V
V_{nSLEEP}	Voltage at nSLEEP pin	-0.3	42	V
V_{SDO}	Voltage at SDO pin	-0.3	V_{DD} + 0.3	V
T_A	Ambient Temperature	-40	125	°C
T_J	Junction Temperature	-40	150	°C
T_{stg}	Storage temperature	-55	150	°C

- *The short circuit protection feature does not support short inductance < 1 µH above 28 V.*
- *Load dump is for a duration of t_{on} = 400 ms; t_{on}/t_{off} = 10%; limited to 100 pulses.*
- *For reverse polarity, $T_J(0)$ = 25 °C, t ≤ 2 min, R_L = 70 Ω on all channels. Device is mounted on a FR4 2s2p board according to JEDEC JESD51-2,-5,-7 at natural convection; the Product (Chip+Package) was simulated on a 76.2 *114.3 *1.5 mm board with 2 inner copper layers (2 * 70 µm Cu, 2 * 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.*
- *For maximum energy dissipation, pulse shape represents inductive switch off: $I_L(t) = I_L(0) \times (1 - t / t_{pulse})$; $0 < t < t_{pulse}$.*
- *Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.*
- *Fault conditions are considered as "outside" normal operating range.*

5.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[(1)]	OUT pins vs. VM or GND	±4000	V
			Other pins	±2000	
		Charged device model (CDM), per AECQ100-011	Corner pins (1, 12, 13, 24)	±750	
			Other pins	±500	

(1) *AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.*

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5.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{M_NOR}	Supply voltage range for normal operation	4	-	40	V
V_{M_LOW}	Lower supply voltage range for extended operation, parameter deviation possible	3	-	4	V
V_{DD}	Logic supply voltage	3	-	5.5	V
V_I	Control and SPI Inputs (nSLEEP, IN0, IN1, nSCS, SCLK, SDI)	0	-	5.5	V
T_A	Ambient temperature	-40	-	125	°C
T_J	Junction temperature	-40	-	150	°C

5.4 Thermal Information

THERMAL METRIC		PWP (HTSSOP) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	13.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.8	°C/W

- *For more information about traditional and new thermal metrics, see the Semiconductor and IC package thermal metrics application report.*
- *°C/W = degrees Celsius per watt.*
- *These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. Power dissipation of 2 W and an ambient temperature of 70°C is assumed. For more information, see these EIA/JEDEC standards:*
  - *JESD51-2, Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
  - *JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
  - *JESD51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
  - *JESD51-9, Test Boards for Area Array Surface Mount Package Thermal Measurements*

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5.5 Electrical Characteristics

V_{DD} = 3 V to 5.5 V, V_M = 4 V to 40 V, T_J = -40 °C to +150 °C (unless otherwise noted)

Typical values: V_{DD} = 5 V, V_M = 13.5 V, T_J = 25 °C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY (V_M, V_{DD})							
V_{M_OP}	VM minimum operating voltage	ENx = 1b, from UVRVM = 1b to V_{DS} ≤ 1 V, R_L = 50 Ω				4	V
V_{DD_OP}	VDD Operating voltage	f_{SCLK} = 5 MHz		3		5.5	V
V_{MDIFF}	Voltage difference between V_M and V_{DD}				200		mV
I_{VM_SLEEP}	Analog supply current in sleep mode	nSLEEP, IN0, IN1 floating, nSCS = VDD	T_J ≤ 85 °C		1	2	µA
			T_J = 150 °C		1	4	µA
I_{VDD_SLEEP}	Logic supply current in sleep mode	nSLEEP, IN0, IN1 floating, nSCS = VDD	T_J ≤ 85 °C		0.2	1	µA
			T_J = 150 °C		0.8	4	µA
I_{SLEEP}	Overall current consumption in Sleep mode	nSLEEP, IN0, IN1 floating, nSCS = VDD	T_J ≤ 85 °C		1.2	3	µA
			T_J = 150 °C		1.8	8	µA
I_{VM_IDLE}	Analog supply current in Idle mode	nSLEEP = logic high, IN0, IN1 floating, f_{SCLK} = 0 MHz, ACT = 0b, ENx = 0b, IOLx = 0b, nSCS = VDD			1.1	1.7	mA
			COR mode, V_M ≤ V_{DD} - 1 V		0.1	0.2	mA
I_{VDD_IDLE}	Logic supply current in Idle mode	nSLEEP = logic high, IN0, IN1 floating, f_{SCLK} = 0 MHz, ACT = 0b, ENx = 0b, nSCS = VDD			0.05	0.1	mA
			COR mode, V_M ≤ V_{DD} - 1 V		1.05	1.6	mA
I_{IDLE}	Overall current consumption in Idle mode	nSLEEP = logic high, IN0, IN1 floating, f_{SCLK} = 0 MHz, ACT = 0b, ENx = 0b, IOLx = 0b, nSCS = VDD			1.1	1.8	mA
I_{VM_ACT}	Analog supply current in Active mode	nSLEEP = logic high, IN0, IN1 floating, f_{SCLK} = 0 MHz, ACT = 1b, IOLx = 0b, nSCS = VDD			2	2.9	mA
			COR mode, V_M ≤ V_{DD} - 1 V		0.1	0.2	mA
I_{VDD_ACT}	Logic supply current in Active mode	nSLEEP = logic high, IN0, IN1 floating, f_{SCLK} = 0 MHz, ACT = 1b, nSCS = VDD			0.05	0.1	mA
			COR mode, V_M ≤ V_{DD} - 1 V		1.95	2.8	mA
I_{ACT}	Overall current consumption in Active mode	nSLEEP = logic high, IN0, IN1 floating, f_{SCLK} = 0 MHz, ACT = 1b, IOLx = 0b, nSCS = VDD			2	3	mA
t_{S2I}	Sleep to Idle delay				200	300	µs
t_{I2S}	Idle to Sleep delay				100	150	µs
t_{I2A}	Idle to Active delay				100	150	µs
t_{A2I}	Active to Idle delay				100	150	µs
t_{S2LH}	Sleep to Limp Home delay				300 + t_{ON}	450 + t_{ON}	µs
t_{LH2S}	Limp Home to Sleep delay				200 + t_{OFF}	300 + t_{OFF}	µs
t_{LH2A}	Limp Home to Active delay				50	100	µs

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5.5 Electrical Characteristics (continued)

V_{DD} = 3 V to 5.5 V, V_M = 4 V to 40 V, T_J = -40 °C to +150 °C (unless otherwise noted)

Typical values: V_{DD} = 5 V, V_M = 13.5 V, T_J = 25 °C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{A2LH}	Active to Limp Home delay				55	100	µs
t_{A2S}	Active to Sleep delay				50	100	µs
CONTROL AND SPI INPUTS (nSLEEP, IN0, IN1, nSCS, SCLK, SDI)							
V_{IL}	Input logic low voltage			0		0.8	V
V_{IH}	Input logic high voltage (nSLEEP, IN0, IN1)			2		5.5	V
V_{IH_SPI}	Input logic high voltage (nSCS, SCLK, SDI)			2		V_{DD}	V
I_{IL}	Input logic low current (all pins except nSCS)	V_I = 0.8 V		8	12	16	µA
I_{IL_nSCS}	nSCS input logic low current	V_{nSCS} = 0.8 V, V_{DD} = 5 V		15	60	85	µA
I_{IH}	Input logic high current (all pins except nSCS)	V_I = 2 V		20	30	40	µA
I_{IH_nSCS}	nSCS input logic high current	V_{nSCS} = 2 V, V_{DD} = 5 V		10	40	65	µA
PUSH-PULL OUTPUT (SDO)							
V_{SDO_L}	Output logic low voltage	I_{SDO} = -1.5 mA		0		0.4	V
V_{SDO_H}	Output logic high voltage	I_{SDO} = 1.5 mA		V_{DD} - 0.4		V_{DD}	V
I_{SDO_OFF}	SDO tristate leakage current	V_{nSCS} = V_{DD}, V_{SDO} = 0 V or V_{DD}		-0.5		0.5	µA
POWER STAGE							
$R_{DS(ON)}$	ON resistance	T_J = 25 °C		0.4	0.7	0.9	Ω
		T_J = 150 °C, I_L = I_{L_EAR} = 220 mA		0.5	1	1.4	
I_{L_NOM}	Nominal load current (all channels active)	T_A = 85 °C, T_J ≤ 150 °C			330	500	mA
		T_A = 105 °C, T_J ≤ 150 °C			260	500	mA
I_{L_NOM}	Nominal load current (half of the channels active)	T_A = 85 °C, T_J ≤ 150 °C			470	500	mA
I_{L_EAR}	Load current for maximum energy dissipation - repetitive (all channels active)	T_A = 85 °C, T_J ≤ 150 °C			220		mA
E_{AR}	Maximum energy dissipation repetitive pulses- 2*I_{L_EAR} (two channels in parallel)	$T_{J(0)}$ = 85 °C, $I_{L(0)}$ = 2*I_{L_EAR}, 2*10^6 cycles, PAR = 1b for affected channels				15	mJ
V_{DS_OP}	Power stage voltage drop at low battery	R_L = 50 Ω supplied by V_M = 4 V			0.05	0.25	V
V_{DS_CL}	Drain to Source Output clamping voltage	I_L = 20 mA		42	46	50	V
I_{L_OFF}	Output leakage current (each channel)	V_{IN} = 0 V or floating, V_{DS} = 28 V, ENx = 0b	T_J ≤ 85 °C		0.1	0.5	µA
			T_J = 150 °C		0.2	1.5	µA
t_{DLY_ON}	Turn-ON delay (from INx pin or bit to V_{OUT} = 90% V_M)	R_L = 50 Ω, V_M = 13.5 V, Active mode or Limp Home mode		2	5.5	9	µs
t_{DLY_OFF}	Turn-OFF delay (from INx pin or bit to V_{OUT} = 10% V_M)	R_L = 50 Ω, V_M = 13.5 V, Active mode or Limp Home mode		3	6	11	µs

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5.5 Electrical Characteristics (continued)

V_{DD} = 3 V to 5.5 V, V_M = 4 V to 40 V, T_J = -40 °C to +150 °C (unless otherwise noted)

Typical values: V_{DD} = 5 V, V_M = 13.5 V, T_J = 25 °C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{ON}	Turn-ON time (from INx pin or bit to V_{OUT} = 10% V_M)	R_L = 50 Ω, V_M = 13.5 V, Active mode or Limp Home mode		10	16	22	µs
t_{OFF}	Turn-OFF time (from INx pin or bit to V_{OUT} = 90% V_M)	R_L = 50 Ω, V_M = 13.5 V, Active mode or Limp Home mode		13	17	24	µs
t_{ON} - t_{OFF}	Turn-ON/OFF matching	R_L = 50 Ω, V_M = 13.5 V, Active mode or Limp Home mode		-10	0	10	µs
SR_{ON}	Turn-ON slew rate, V_{DS} = 70% to 30% V_M	R_L = 50 Ω, V_M = 13.5 V, Active mode or Limp Home mode		0.8	1.2	1.6	V/µs
SR_{OFF}	Turn-OFF slew rate, V_{DS} = 30% to 70% V_M	R_L = 50 Ω, V_M = 13.5 V, Active mode or Limp Home mode		0.8	1.2	1.6	V/µs
t_{SYNC}	Internal reference frequency synchronization time				7	10	µs
PROTECTION							
$V_{M_UVLO_F}$	VM undervoltage shutdown (falling)	ENx = ON, from V_{DS} ≤ 1 V to UVRVM = 1b, R_L = 50 Ω		2.64	2.73	2.82	V
$V_{M_UVLO_R}$	VM undervoltage shutdown (rising)			2.77	2.86	2.95	V
V_{DD_UVLO}	VDD undervoltage shutdown (rising)	V_{SDI} = V_{SCLK} = V_{nSCS} = 0 V, SDO from low to Hi-Z		2.5	2.6	2.7	V
V_{DD_HYS}	VDD undervoltage shutdown hysteresis				120		mV
I_{L_OCP0}	Overcurrent protection threshold, OCP = 0b	T_J = -40 °C		1.4	1.65	2.2	A
		T_J = 25 °C		1.3	1.6	1.9	A
		T_J = 150 °C		1.2	1.45	1.7	A
I_{L_OCP1}	Overcurrent protection threshold, OCP = 0b	T_J = -40 °C		0.7	0.9	1.2	A
		T_J = 25 °C		0.7	0.85	1.1	A
		T_J = 150 °C		0.6	0.8	1	A
I_{L_OCP0}	Overcurrent protection threshold, OCP = 1b	T_J = -40 °C		1.8	2.3	3	A
		T_J = 25 °C		1.8	2.2	2.7	A
		T_J = 150 °C		1.3	2	2.7	A
I_{L_OCP1}	Overcurrent protection threshold, OCP = 1b	T_J = -40 °C		1.2	1.6	2.1	A
		T_J = 25 °C		1.2	1.5	1.9	A
		T_J = 150 °C		1.1	1.4	1.7	A
t_{OCPIN}	Overcurrent threshold switch delay time			70	170	260	µs
t_{OFF_OCP}	Overcurrent shut-down delay time			4	9	14	µs
T_{OTW}	Overtemperature warning			120	140	160	°C
T_{HYS_OTW}	Overtemperature warning hysteresis				12		°C
T_{TSD}	Thermal shut-down temperature			150	175	200	°C
V_{M_AZ}	Over voltage protection	I_{VM} = 10 mA, Sleep mode		42	48	53	V
V_{DS_REV}	Drain Source diode during reverse polarity	I_L = -10 mA, Sleep mode	T_J = 25 °C		650		mV
			T_J = 150 °C		560		mV

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5.5 Electrical Characteristics (continued)

V_{DD} = 3 V to 5.5 V, V_M = 4 V to 40 V, T_J = -40 °C to +150 °C (unless otherwise noted)

Typical values: V_{DD} = 5 V, V_M = 13.5 V, T_J = 25 °C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{RETRY0_LH}	Restart time in Limp Home mode		7	10	13	ms
t_{RETRY1_LH}	Restart time in Limp Home mode		14	20	26	ms
t_{RETRY2_LH}	Restart time in Limp Home mode		28	40	52	ms
t_{RETRY3_LH}	Restart time in Limp Home mode		56	80	104	ms
t_{OSM}	Output Status Monitor comparator settling time				20	µs
V_{DS_OL}	Output Status Monitor threshold voltage		3	3.3	3.6	V
I_{OL}	Output diagnosis current	V_{DS} = 3.3 V, V_M = 5 V to 18 V	20	75	110	µA
I_{OL}	Output diagnosis current	V_{DS} = 3.3 V, V_M = 13.5 V	60	75	85	µA
R_{OL}	Open Load equivalent resistance	V_M = 5 V to 40 V	45		190	kΩ

5.5.1 SPI Timing Requirements

- Not subject to production test, guaranteed by design

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{nSCS_lead}	Enable lead time (falling nSCS to rising SCLK)		200			ns
t_{nSCS_lag}	Enable lag time (falling SCLK to rising nSCS)		200			ns
t_{nSCS_td}	Transfer delay time (rising nSCS to falling nSCS)		250			ns
t_{SDO_en}	Output enable time (falling nSCS to SDO valid)	C_L = 20 pF at SDO pin			200	ns
t_{SDO_dis}	Output disable time (rising nSCS to SDO Hi-z)	C_L = 20 pF at SDO pin			200	ns
f_{SCLK}	Serial clock frequency				5	MHz
t_{SCLK_P}	Serial clock period		200			ns
t_{SCLK_H}	Serial clock logic high time		75			ns
t_{SCLK_L}	Serial clock logic low time		75			ns
t_{SDI_su}	Data setup time (required time SDI to falling SCLK)		20			ns
t_{SDI_h}	Data hold time (falling SCLK to SDI)		20			ns
t_{SDO_v}	Output data valid time with capacitive load	C_L = 20 pF at SDO pin			100	ns

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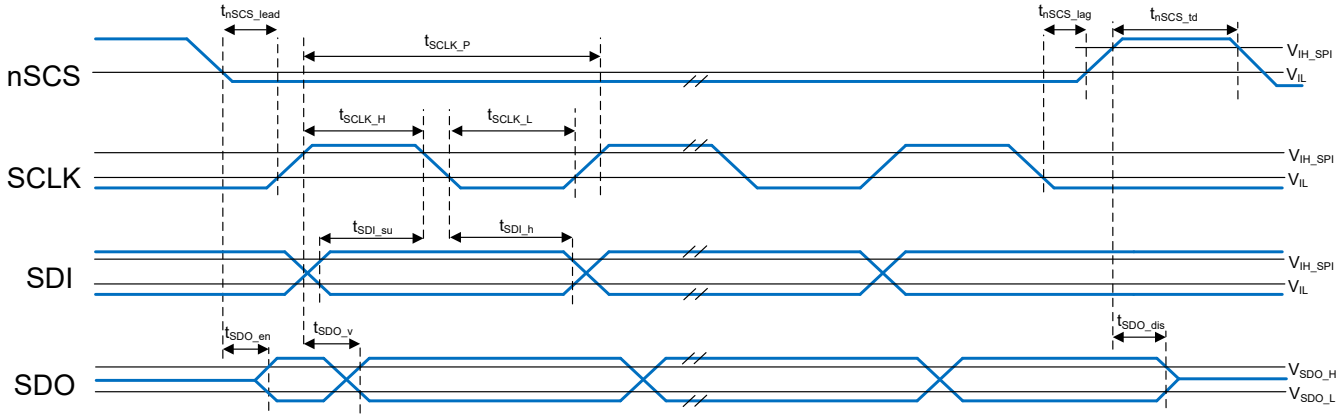

Figure 5-1. SPI Timing Diagram

5.6 Typical Characteristics

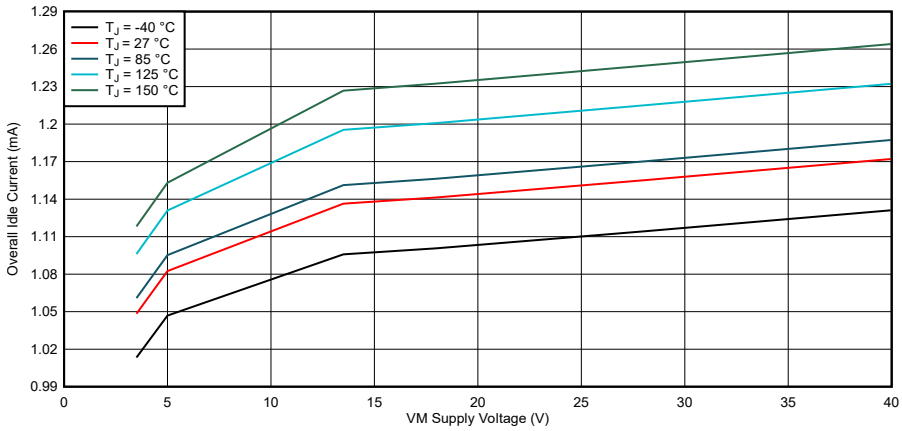

Figure 5-2. Idle mode supply current, VDD = 5.5V

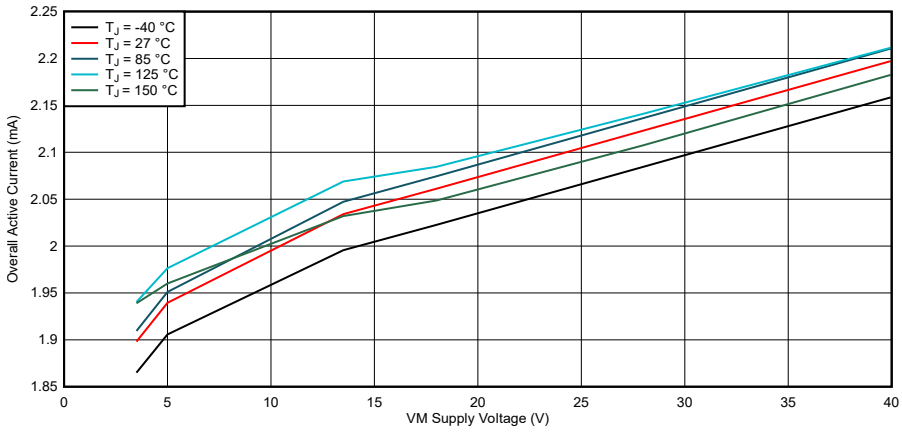

Figure 5-3. Active mode supply current, VDD = 5.5V

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5.6 Typical Characteristics (continued)

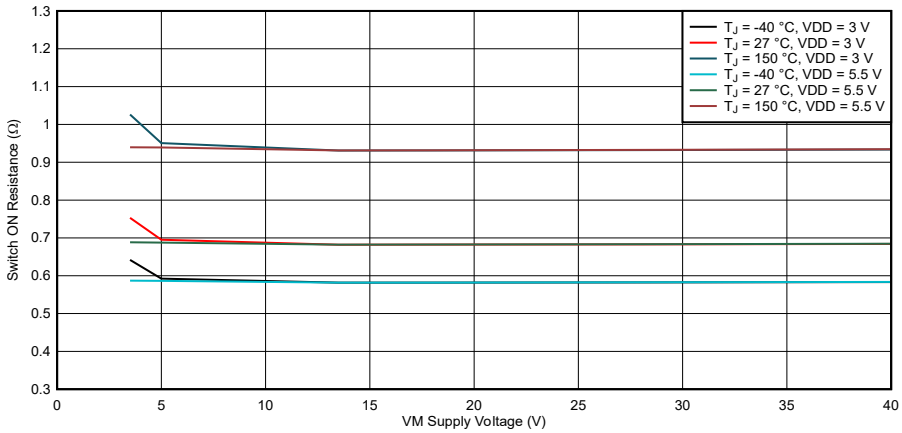

Figure 5-4. Switch ON Resistance

5.6 Typical Characteristics (continued)

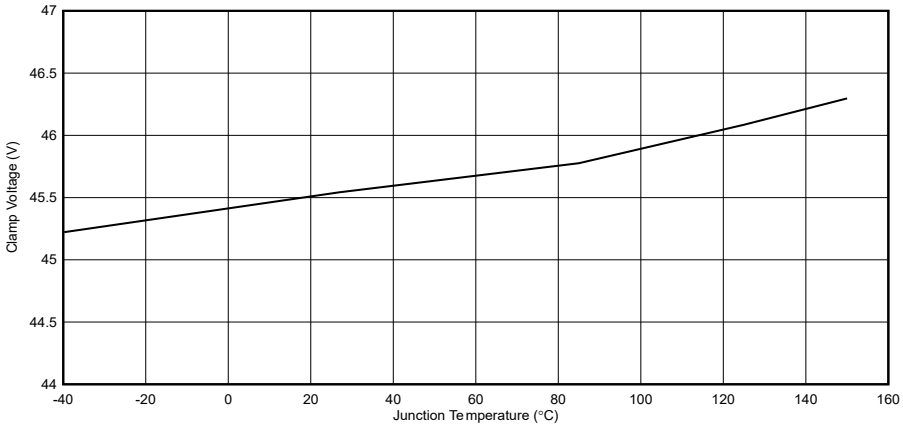

Figure 5-5. Drain-to-Source Clamp Voltage, VM = 13.5V, VDD = 5V

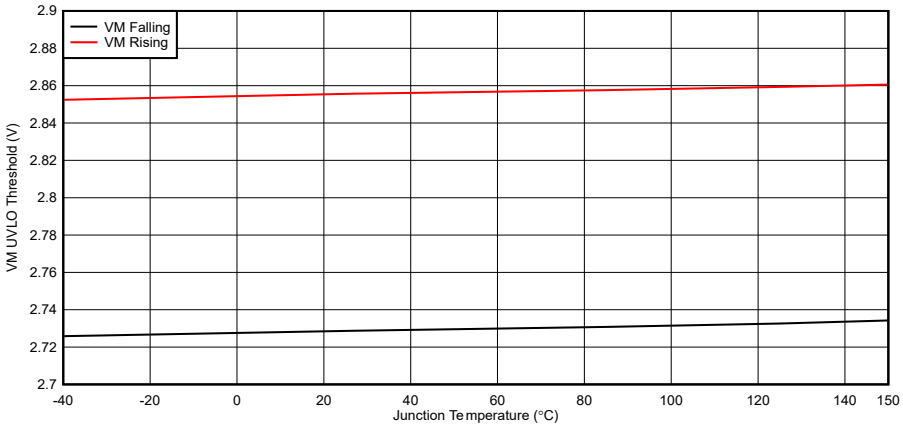

Figure 5-6. VM UVLO Threshold

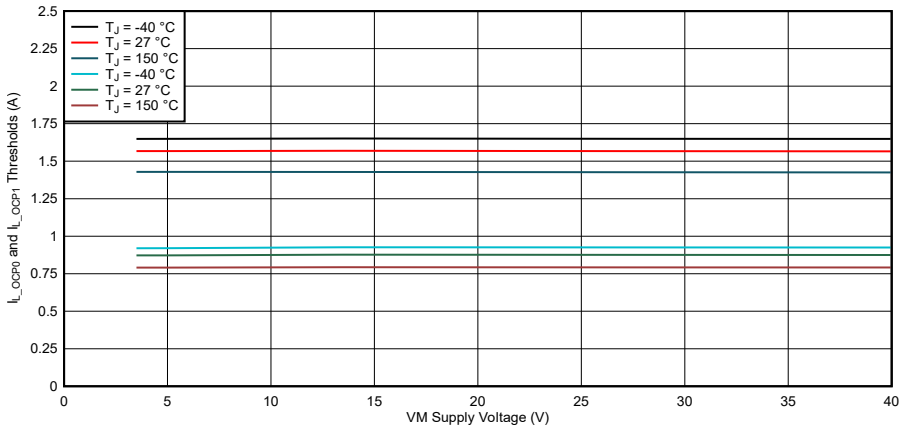

Figure 5-7. Overcurrent Protection Threshold, VDD = 5.5V, OCP = 0b

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5.6 Typical Characteristics (continued)

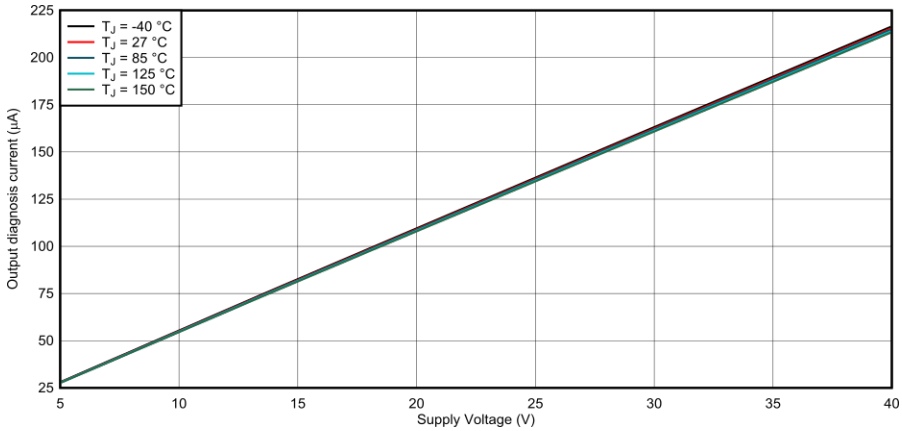

Figure 5-8. Output Diagnosis Current

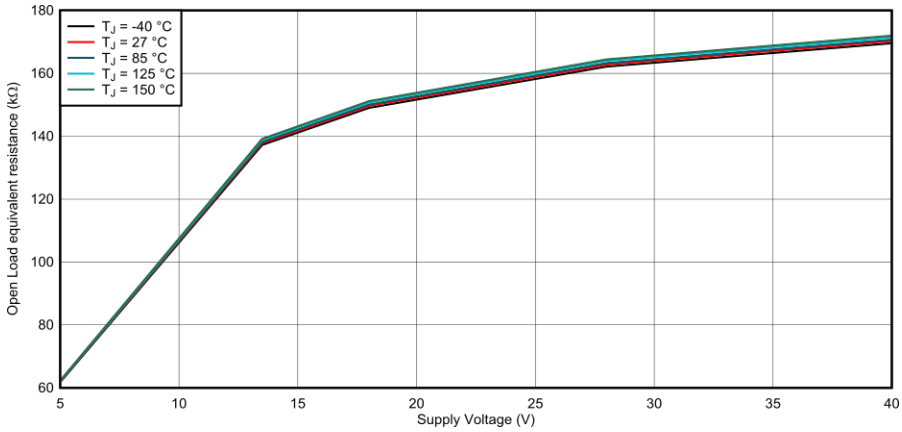

Figure 5-9. Open Load Equivalent Resistance

6 Detailed Description

6.1 Overview

The DRV81008-Q1 is an eight-channel low-side switch with integrated protection and diagnostic functions. The output stages include eight N-channel power MOSFET low-side switches (typical $R_{DS(ON)}$ at T_J = 25 °C is 700mΩ). The DRV81008-Q1 is designed for low-supply voltage operation. It can keep its state at a low battery voltage (V_M ≥ 3V).

The 16-bit SPI interface is used to control and diagnose the device and the loads. The SPI interface supports a daisy chain in order to connect multiple devices (also devices with 8-bit SPI) in one SPI chain by using the same microcontroller pins. The SPI feature is available only when the digital power supply is present.

The DRV81008-Q1 has two input pins that are connected to two outputs. When the nSLEEP pin is logic low, it is possible to activate channels 2 and 3 using the input pins independently from the availability of the digital supply voltage. With the Input Mapping feature, it is possible to connect the input pins to different outputs, or assign more outputs to the same input pin. In this case more channels can be controlled with one input signal.

The device provides diagnosis of the load via Open Load (in OFF state) and short circuit detection. For Open Load detection, an internal current source can be activated via SPI. Each output stage is protected against short circuit. In case of overcurrent, the affected channel switches OFF when the overcurrent detection threshold is reached and can be reactivated via SPI.

In Limp Home mode operation, the channels connected to an input pin set to logic high restart automatically after output restart time elapses. Temperature sensors are available for each channel to protect the device against over temperature.

Table 6-1. Product Summary

Parameter	Symbol	Values
Analog supply voltage	V_M	3.0V to 40V
Digital supply voltage	V_{DD}	3.0V to 5.5V
Minimum overvoltage protection	V_{M_AZ}	42V
Maximum on-state resistance at T_J = 150 °C	$R_{DS(ON)}$	1.4Ω
Nominal load current (T_A = 85 °C, all channels)	I_{L_NOM}	330mA
Maximum Energy dissipation - repetitive	E_{AR}	10mJ @ I_{L_EAR} = 220mA
Minimum Drain to Source clamping voltage	V_{DS_CL}	42V
Maximum overload switch OFF threshold	I_{L_OCP0}	2.2A or 3A
Maximum total quiescent current at T_J ≤ 85 °C	I_{SLEEP}	3µA
Maximum SPI clock frequency	f_{SCLK}	5MHz

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6.2 Functional Block Diagram

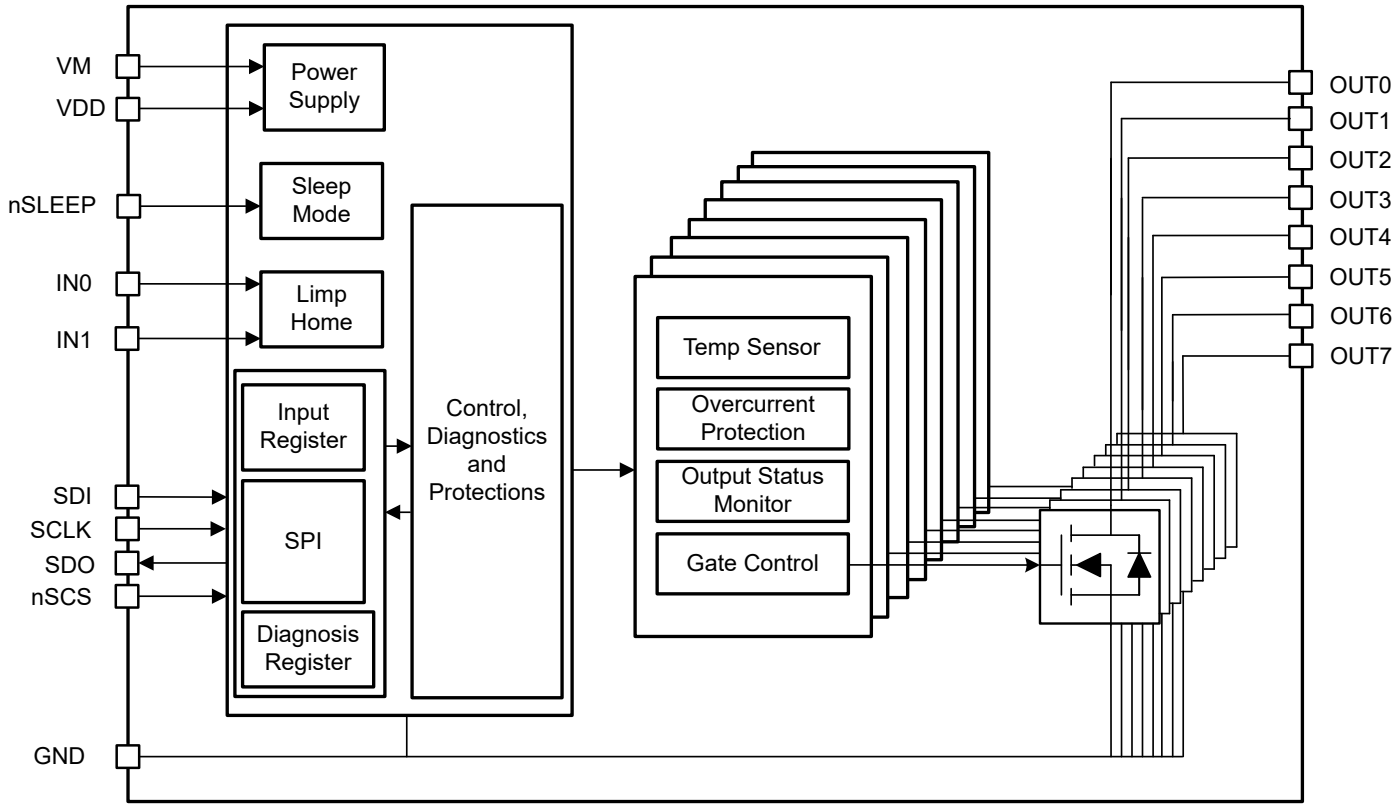

Figure 6-1. Functional Block Diagram

6.3 Feature Description

6.3.1 Control Pins

The device has three pins (IN0, IN1 and nSLEEP) to control the device directly without using SPI.

6.3.1.1 Input Pins

DRV81008-Q1 has two input pins. Each input pin is connected by default to one channel (IN0 to channel 2, IN1 to channel 3). Input Mapping Registers MAP0 and MAP1 can be programmed to connect additional or different channels to each input pin, as shown in Figure 6-2. The signals driving the channels are an OR combination between EN register status, IN0 and IN1 (according to Input Mapping registers status).

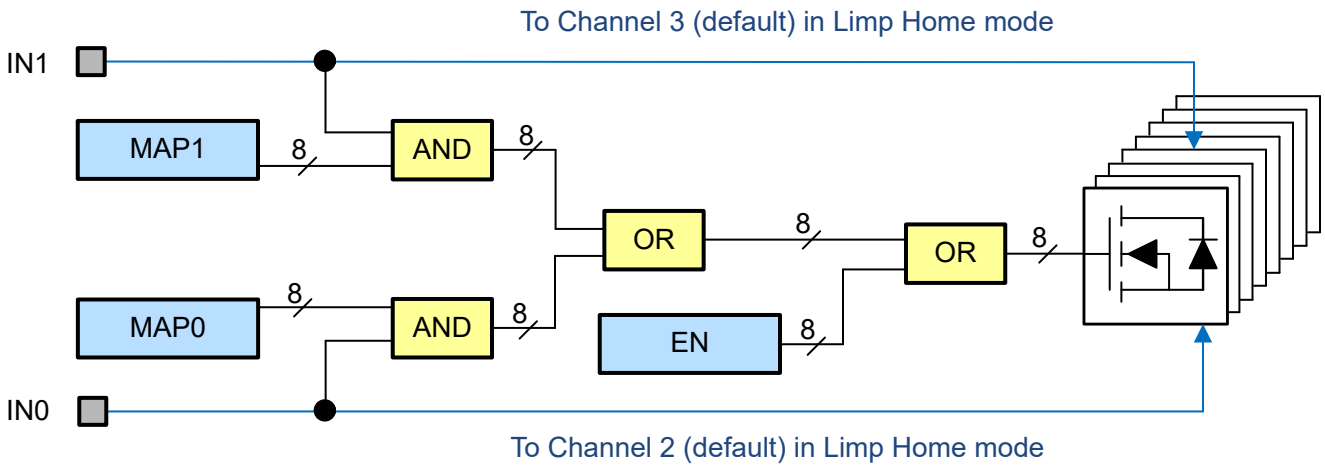

Figure 6-2. Input Mapping

The logic level of the input pins can be monitored using the Input Status Monitor Register (INST). The Input Status Monitor is operational also when the DRV81008-Q1 is in Limp Home mode. If one of the Input pins is set to logic high and the nSLEEP pin is set to logic low, the device switches into Limp Home mode and activates the channel mapped by default to the input pins.

6.3.1.2 nSLEEP Pin

The nSLEEP pin is used to bring the device into Sleep mode when it is set to logic low and all input pins are also set to logic low. When nSLEEP pin is set to logic low while one of the input pins is set to logic high, the device enters Limp Home mode.

To ensure a proper mode transition, nSLEEP pin must be set for at least t_{I2S} (transition from logic high to logic low) or t_{S2I} (transition from logic low to logic high).

Setting the nSLEEP pin to logic low results in:

- All registers in the SPI are reset to default values.
- V_{DD} and V_M undervoltage detection circuits are disabled to decrease current consumption (if both inputs are set to logic low).
- No SPI communication is allowed (SDO pin remains in high impedance also when nSCS pin is set to logic low) if both input pins are set to logic low.

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6.3.2 Power Supply

The DRV81008-Q1 is supplied by two supply voltages:

- V_M (analog supply voltage used also for the logic)
- V_{DD} (digital supply voltage)

The V_M supply is connected to a battery feed and used, in combination with V_{DD} supply, for the driving circuitry of the power stages. In situations where V_M voltage drops below V_{DD} voltage (for example during cranking events down to 3V), an increased current consumption may be observed at VDD pin. V_M and V_{DD} supply voltages have an undervoltage detection circuit.

- An undervoltage on both V_M and V_{DD} supply voltages prevents the activation of the power stages and any SPI communication (the SPI registers are reset)
- An undervoltage on V_{DD} supply prevents any SPI communication. SPI read/write registers are reset to default values.
- An undervoltage on V_M supply forces the DRV81008-Q1 to drain device current from V_{DD} supply.

Figure 6-3 shows a basic concept drawing of the interaction between supply pins V_M and V_{DD}, the output stage drivers and SDO supply line.

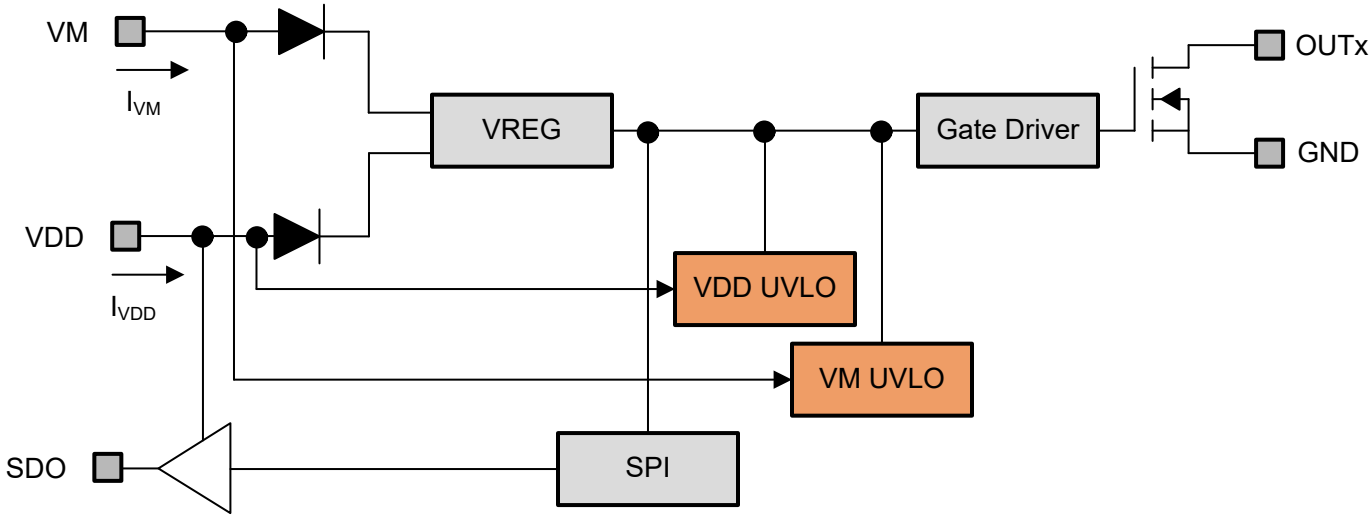

Figure 6-3. Internal Power Supply Architecture

When 3V ≤ V_M ≤ V_{DD} - V_{MDIFF}, DRV81008-Q1 operates in Cranking Operative Range (COR). In this condition, the current consumption from VDD pin increases while it decreases from VM pin. Total current consumption remains within the specified limits.

Figure 6-4 shows the voltage levels at VM pin where the device goes in and out of COR. During the transition to and from COR, I_{VM} and I_{VDD} change between values defined for normal operation and for COR operation. The sum of both current remains within limits specified in Section 5.5.

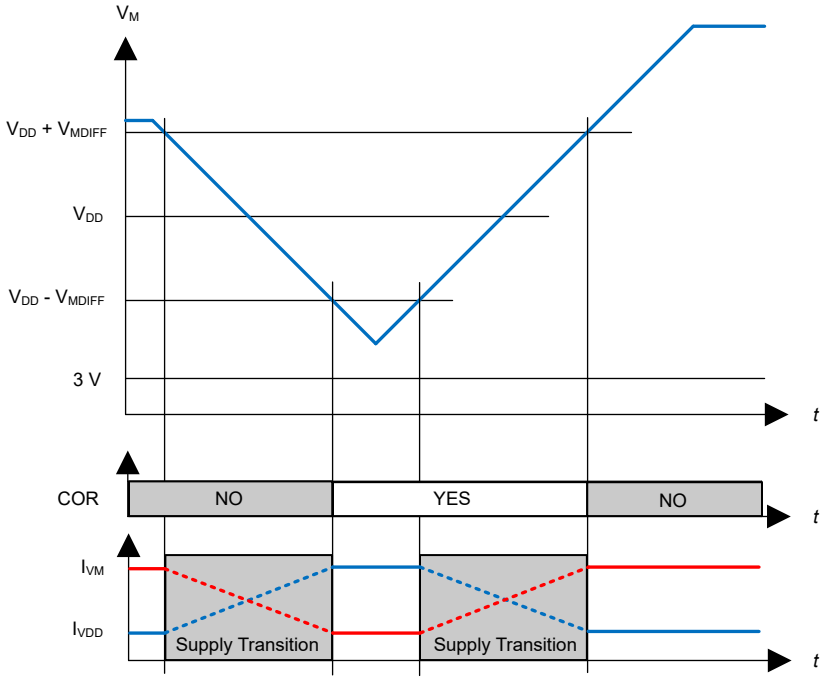

Figure 6-4. Cranking Operative Range

When $V_{M_UVLO} \leq V_M \leq V_{M_OP}$, it may be not possible to switch ON a channel that was previously OFF. All channels that are already ON keep their state unless they are switched OFF via SPI or via IN pins. An overview of channel behavior according to different V_M and V_{DD} supply voltages is shown in Table 6-2, Table 6-3 and Table 6-4 (the tables are valid after a successful power-up).

Table 6-2. Channel Control as function of V_M and V_{DD}

	$V_{DD} \leq V_{DD_UVLO}$	$V_{DD} > V_{DD_UVLO}$
$V_M \leq 3V$	Channels cannot be controlled	Channels can be switched ON and OFF (SPI control)($R_{DS(ON)}$ deviations possible)
$3V < V_M \leq V_{M_OP}$	Channels cannot be controlled by SPI	Channels can be switched ON and OFF (SPI control)($R_{DS(ON)}$ deviations possible)
$V_M > V_{M_OP}$	Channels cannot be controlled by SPI	Channels can be switched ON and OFF

Table 6-3. Limp Home mode as function of V_M and V_{DD}

	$V_{DD} \leq V_{DD_UVLO}$	$V_{DD} > V_{DD_UVLO}$
$V_M \leq 3V$	Not available	Available ($R_{DS(ON)}$ deviations possible)
$3V < V_M \leq V_{M_OP}$	Available ($R_{DS(ON)}$ deviations possible)	Available ($R_{DS(ON)}$ deviations possible)
$V_M > V_{M_OP}$	Available	Available

Table 6-4. SPI registers and SPI communication as function of V_M and V_{DD}

	$V_{DD} \leq V_{DD_UVLO}$	$V_{DD} > V_{DD_UVLO}$
SPI Registers	Reset	Available
SPI Communication	Not available (f_{SCLK} = 0MHz)	Possible (f_{SCLK} = 5MHz)

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6.3.2.1 Modes of Operation

DRV81008-Q1 has the following operation modes:

- Sleep mode
- Idle mode
- Active mode
- Limp Home mode

The transition between operation modes is determined according to following levels and states:

- Logic level at nSLEEP pin
- Logic level at INx pins
- ENx bits state
- ACT bit state

The state diagram including the possible transitions is shown in Figure 6-5. The behaviour of DRV81008-Q1 as well as some parameters may change according to the operation mode of the device. Also, due to the undervoltage detection circuitry, some changes within the same operation mode can be seen.

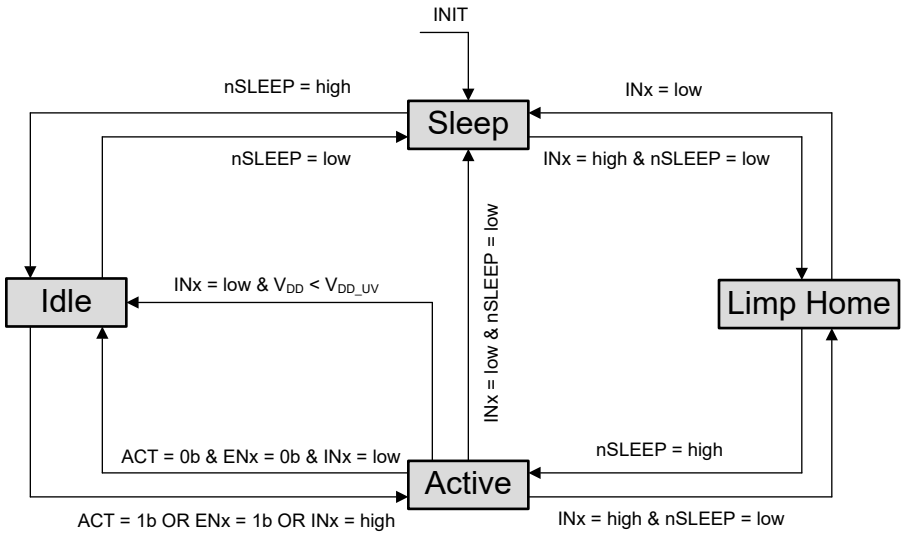

Figure 6-5. Mode of Operation State Diagram

The operation mode of the DRV81008-Q1 can be observed by:

- Status of output channels
- Status of SPI registers
- Current consumption at VDD pin (I_{VDD})
- Current consumption at VM pin (I_{VM})

The default operation mode to switch ON the loads is Active mode. If the device is not in Active mode and a request to switch ON one or more outputs comes (via SPI or via Input pins), it will switch into Active or Limp Home mode, according to nSLEEP pin status.

The channel turn-ON time is as defined by parameter t_{ON} when DRV81008-Q1 is in Active mode or in Limp Home mode. In all other cases, it is necessary to add the transition time required to reach one of the two aforementioned Power Supply modes (as shown in Figure 6-6).

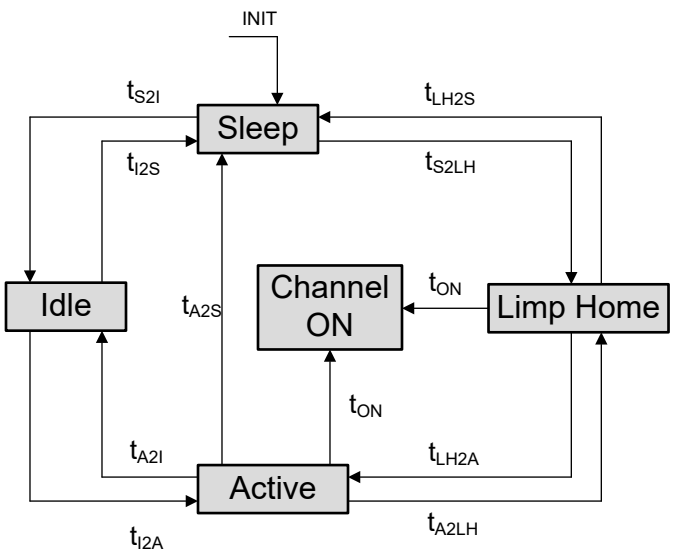

Figure 6-6. Mode Transition Timing

Table 6-5 shows the correlation between device operation modes, V_M and V_{DD} supply voltages, and state of the most important functions (channel control, SPI communication and SPI registers).

Table 6-5. Device function in relation to operation modes, V_M and V_{DD} voltages

Modes of Operation	Function	V_M UVLO, $V_{DD} \leq V_{DD_UVLO}$	V_M UVLO, $V_{DD} > V_{DD_UVLO}$	V_M not in UVLO, $V_{DD} \leq V_{DD_UVLO}$	V_M not in UVLO, $V_{DD} > V_{DD_UVLO}$
Sleep	Channels	Not available	Not available	Not available	Not available
	SPI comm.	Not available	Not available	Not available	Not available
	SPI registers	Reset	Reset	Reset	Reset
Idle	Channels	Not available	Not available	Not available	Not available
	SPI comm.	Not available	Yes	Not available	Yes
	SPI registers	Reset	Yes	Reset	Yes
Active	Channels	Not available	Yes	Yes, IN pins only	Yes
	SPI comm.	Not available	Yes	Not available	Yes
	SPI registers	Reset	Yes	Reset	Yes
Limp Home	Channels	Not available	Yes, IN pins only	Yes, IN pins only	Yes, IN pins only
	SPI comm.	Not available	Yes, read-only	Not available	Yes, read-only
	SPI registers	Reset	Yes, read-only	Reset	Yes, read-only

6.3.2.1.1 Power-up

The Power-up condition is satisfied when one of the supply voltages (V_M or V_{DD}) is applied to the device and the INx or nSLEEP pins are set to logic high. If V_M is above the threshold V_{M_OP} or if V_{DD} is above the UVLO threshold, the internal power-on signal is set.

6.3.2.1.2 Sleep mode

When DRV81008-Q1 is in Sleep mode, all outputs are OFF and the SPI registers are reset, independently from the supply voltages. The current consumption is minimum.

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6.3.2.1.3 Idle mode

In Idle mode, the current consumption of the device can reach the limits given by parameters I_{VDD_IDLE} and I_{VM_IDLE}, or by parameter I_{IDLE} for the whole device.

- The internal voltage regulator is working in this mode.
- Diagnosis functions are not available.
- The output channels are switched OFF, independently from the supply voltages.
- When V_{DD} is available, the SPI registers are working and SPI communication is possible.

6.3.2.1.4 Active mode

Active mode is the normal operation mode of the DRV81008-Q1 when no Limp Home condition is set and it is necessary to drive some or all loads. Voltage levels of V_{DD} and V_M influence the behavior as described in Section 6.3.2. Device current consumption is specified with I_{VDD_ACT} and I_{VM_ACT} (I_{ACT} for the whole device).

The device enters Active mode when nSLEEP pin is set to logic high and one of the input pins is set to logic high or one ENx bit is set to 1b.

- If ACT bit is set to 0b, the device returns to Idle mode as soon as all inputs pins are set to logic low and ENx bits are set to 0b.
- If ACT is set to 1b, the device remains in Active mode independently of the status of input pins and ENx bits.
- An undervoltage condition on V_{DD} supply brings the device into Idle mode, if all input pins are set to logic low.

Even if the registers MAP0 and MAP1 are both set to 00H but one of the input pins INx is set to logic high, the device goes into Active mode.

6.3.2.1.5 Limp Home mode

DRV81008-Q1 enters Limp Home mode when nSLEEP pin is logic low and one of the input pins is set to logic high, switching ON the channel connected to it. SPI communication is possible but only in read-only mode (SPI registers can be read but cannot be written).

- UVRVM is set to 1b
- MODE bits are set to 01b (Limp Home mode)
- TER bit is set to 1b on the first SPI command after entering Limp Home mode. Afterwards it works normally.
- OLOFF bit is set to 0b
- ERRx bits work normally
- OSMx bits can be read and work normally
- All other registers are set to their default value and cannot be programmed as long as the device is in Limp Home mode

See Table 6-3 for a detailed overview of supply voltage conditions required to switch ON channels 2 and 3 during Limp Home. All other channels are OFF.

A transmission of SPI commands during transition from Active to Limp Home mode or Limp Home to Active mode may result in undefined SPI responses.

6.3.2.2 Reset condition

One of the following three conditions resets the SPI registers to the default value:

- V_{DD} is not present or below the undervoltage threshold V_{DD_UVLO}
- nSLEEP pin is set to logic low
- A reset command (RST set to 1b) is executed
  - ERRx bits are not cleared by a reset command (for functional safety)

In particular, all channels are switched OFF (if there are no input pin set to logic high) and the Input Mapping configuration is reset.

6.3.3 Power Stage

The DRV81008-Q1 is an eight channels low-side relay switch. The power stages are built by N-channel MOSFETs. The ON-state resistance $R_{DS(ON)}$ depends on the supply voltage as well as the junction temperature T_J.

6.3.3.1 Switching Resistive Loads

When switching resistive loads the following switching times and slew rates should be considered.

The default slew rate is 1.2V/µs. The SR bit in configuration register 2 can be used to increase the slew rate to 3V/µs.

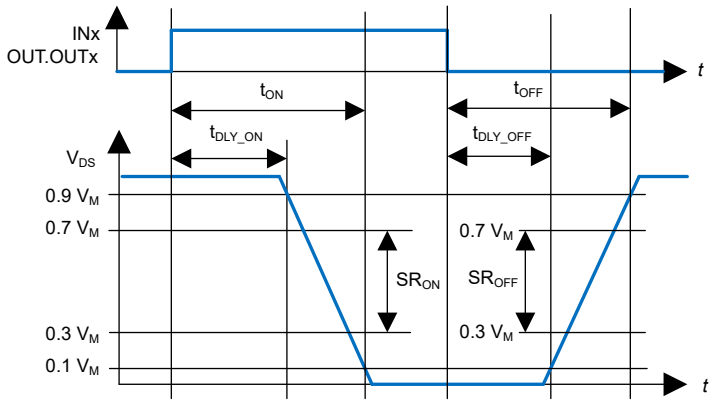

Figure 6-7. Switching a Resistive Load

6.3.3.2 Inductive Output Clamp

When switching off inductive loads, the voltage across the power switch rises to V_{DS_CL}, because the inductance intends to continue driving the current. The voltage clamping is necessary to prevent device damage.

Figure 6-8 shows a drawing of the output clamp. The maximum allowed load inductance is limited. The clamping structure protects the device in all modes (Sleep, Idle, Active, Limp Home).

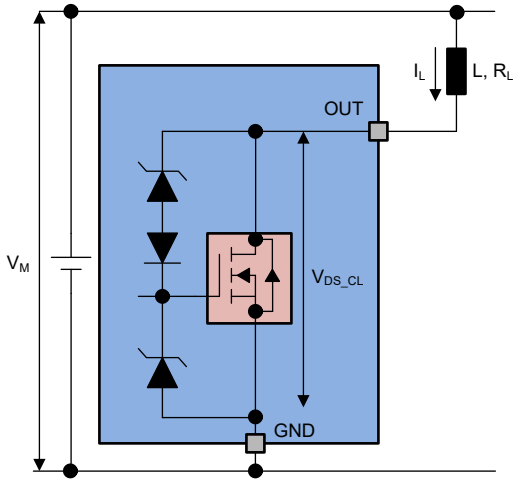

Figure 6-8. Output Clamp

6.3.3.3 Maximum Load Inductance

During demagnetization of inductive loads, magnetic energy is dissipated in the DRV81008-Q1. Equation 1 shows how to calculate the energy for low-side switches:

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$$E = V_{DS_CL} \times \left[\frac{V_M - V_{DS_CL}}{R_L} \times \ln\left(1 - \frac{R_L \times I_L}{V_M - V_{DS_CL}}\right) + I_L\right] \times \frac{L}{R_L} \quad (1)$$

The maximum energy, which is converted into heat, is limited by the thermal design of the component. The E_{AR} value provided in Section 5.1 assumes that all channels can dissipate the same energy when the inductances connected to the outputs are demagnetized at the same time.

6.3.3.4 Switching Channels in parallel

In case of a short circuit with channels in parallel, it may happen that the two channels switch OFF asynchronously, therefore bringing an additional thermal stress to the channel that switches OFF last. In order to avoid this condition, it is possible to configure in the SPI registers the parallel operation of two neighbour channels (using PAR bits). When operating in this mode, the fastest channel to react to an OverLoad or Over Temperature condition will deactivate also the other channel. The inductive energy that two parallel channels can handle is lower than twice the single channel energy. It is possible to synchronize the following couple of channels together:

- channel 0 and channel 2 → PAR0 set to 1b
- channel 1 and channel 3 → PAR1 set to 1b
- channel 4 and channel 6 → PAR2 set to 1b
- channel 5 and channel 7 → PAR3 set to 1b

The synchronization bits influence only how the channels react to Overcurrent or Over Temperature conditions. Synchronized channels have to be switched ON and OFF together by the microcontroller.

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6.3.4 Protection and Diagnostics

The DRV81008-Q1 supports multiple protection features, discussed in detail in the subsequent sections. The SPI interface provides diagnosis information about the device and the load status. Each channel diagnosis information is independent from other channels. An error condition on one channel has no influence on the diagnostic of other channels in the device (unless configured to work in parallel, see Section 6.3.3.4 for more details).

When either an Overcurrent or an Over Temperature occurs on one channel, the diagnosis bit ERRx is set accordingly. As described in Section 6.3.4.2 and Section 6.3.4.3, the channel latches OFF and must be reactivated setting corresponding CLRx bit to 1b.

6.3.4.1 Undervoltage on V_M

Between V_{M_UVLO} and V_{M_OP} the undervoltage mechanism is triggered. If the device is operating and the supply voltage drops below the undervoltage threshold V_{M_UVLO}, the logic sets the bit UVRVM to 1b. As soon as the supply voltage V_M is above the minimum voltage operating threshold V_{M_OP}, the bit UVRVM is set to 0b after the first Standard Diagnosis readout. Undervoltage condition on VM influences the status of the channels, as described in Section 6.3.2. Figure 6-9 shows the undervoltage behavior.

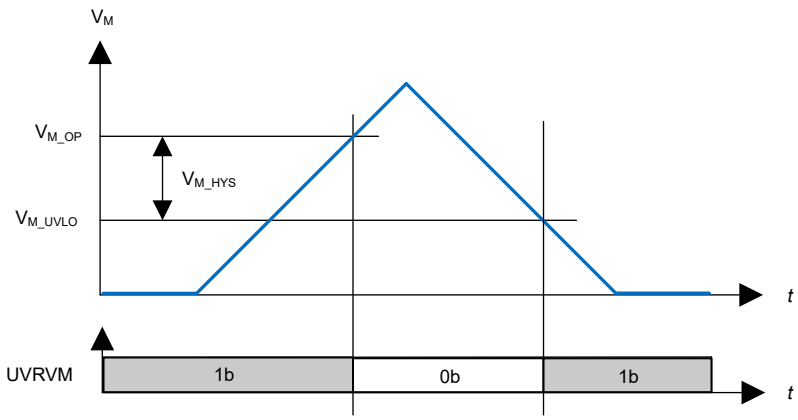

Figure 6-9. V_M Undervoltage

6.3.4.2 Overcurrent Protection

The DRV81008-Q1 is protected in case of overcurrent or short circuit of the load. There are two overcurrent thresholds (see Figure 6-10):

- I_{L_OCP0} between channel switch ON and t_{OCPIN}
- I_{L_OCP1} after t_{OCPIN}

The values of I_{L_OCP0} and I_{L_OCP1} depend on the OCP bit. Every time the channel is switched OFF for a time longer than 2 * t_{SYNC} the over load current threshold is set back to I_{L_OCP0}.

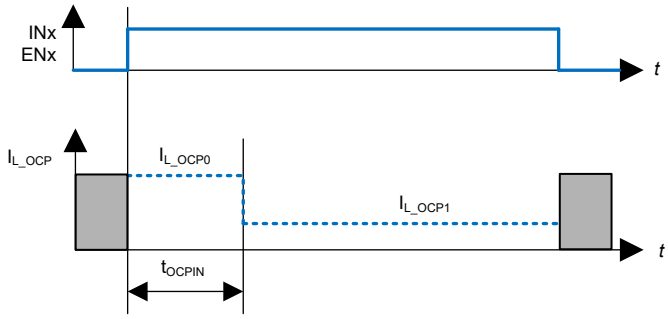

Figure 6-10. Overcurrent Threshold

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In case the load current is higher than I_{L_OCP0} or I_{L_OCP1}, after time t_{OFF_OCP} the over loaded channel is switched OFF and the diagnosis bit ERRx is set. The channel can be switched ON after clearing the protection latch by setting the corresponding CLRx bit to 1b. This bit is set back to 0b internally after de-latching the channel. Please refer to Figure 6-11 for details.

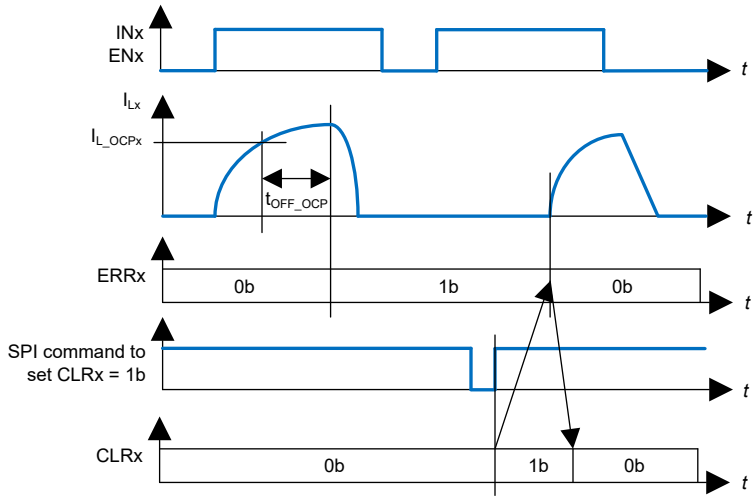

Figure 6-11. Latch OFF at Overcurrent

6.3.4.3 Over Temperature Protection

A temperature sensor is integrated for each channel, causing an overheated channel to switch OFF to prevent damage to the device. The corresponding diagnosis bit ERRx is set (combined with Over Load protection). The channel can be switched ON after clearing the protection latch by setting the corresponding CLRx bit to 1b. This bit is set back to 0b internally after de-latching the channel.

6.3.4.4 Over Temperature Warning

If the die temperature exceeds the trip point of the overtemperature warning (T_{OTW}), the OTW bit is set in the configuration register 2. The device performs no additional action and continues to function.

When the die temperature falls below the hysteresis point (T_{HYS_OTW}) of the overtemperature warning, the OTW bit clears automatically.

6.3.4.5 Over Temperature and Overcurrent Protection in Limp Home mode

When DRV81008-Q1 is in Limp Home mode, channels 2 and 3 can be switched ON using the input pins. In case of Overcurrent, Short Circuit or Over Temperature the channels switch OFF. If the input pins remain logic high, the channels restart with the following timings:

- 10ms (first 8 retries)
- 20ms (following 8 retries)
- 40ms (following 8 retries)
- 80ms (as long as the input pin remains logic high and the error is still present)

If at any time the input pin is set to logic low for longer than $2*t_{SYNC}$, the restart timer is reset. At the next channel activation while in Limp Home mode the timer starts from 10ms again. See Figure 6-12 for details. Overcurrent thresholds behave as described in Section 6.3.4.2.

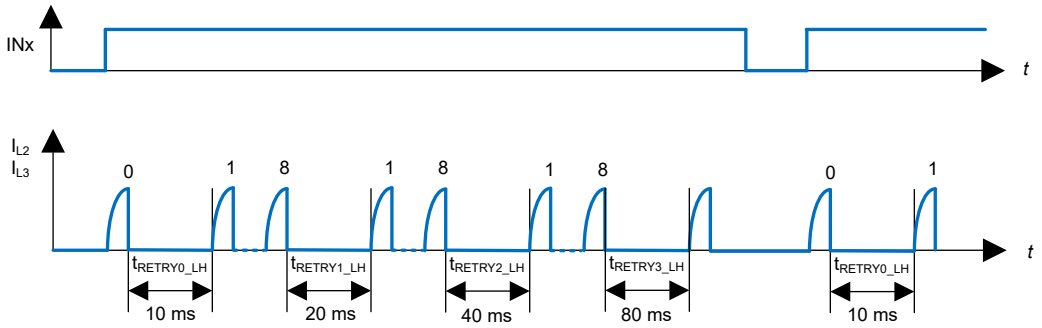

Figure 6-12. Restart Timer in Limp Home

6.3.4.6 Reverse Polarity Protection

In Reverse Polarity or Reverse Battery condition, power dissipation is caused by the body diode of each MOSFET. Each ESD diode of the logic and supply pins contributes to total power dissipation. The reverse current through the channels has to be limited by the connected loads. The current through digital power supply VDD and input pins has to be limited as well (please refer to Section 5.1).

Note

No protection mechanism like temperature protection or current limitation is active during reverse polarity.

6.3.4.7 Over Voltage Protection

In the case of supply voltages between V_{M_SC} and V_{M_LD} the output MOSFETs are still operational and follow the input pins or the EN bits.

In addition to the output clamp for inductive loads as described in Section 6.3.3.2, there is a clamp mechanism available for over voltage protection for the logic and all channels, monitoring the voltage between VM and GND pins (V_{M_AZ}).

6.3.4.8 Output Status Monitor

The device compares the V_{DS} of each channel with V_{DS_OL} and sets the corresponding OSMx bits. The bits are updated every time OSM register is read.

- $V_{DS} < V_{DS_OL} \rightarrow$ OSMx = 1b

A diagnosis current I_{OL} in parallel to the power switch can be enabled by programming the IOLx bit, which can be used for Open Load at OFF detection. Each channel has its dedicated diagnosis current source. If the diagnosis current I_{OL} is enabled or if the channel changes state (ON → OFF or OFF → ON) it is necessary to wait a time t_{OSM} for a reliable diagnosis. Enabling I_{OL} current sources increases the current consumption of the device. Even if an Open Load is detected, the channel is not latched OFF.

See Figure 6-13 for a timing overview (the values of IOLx refer to a channel in normal operation properly connected to the load).

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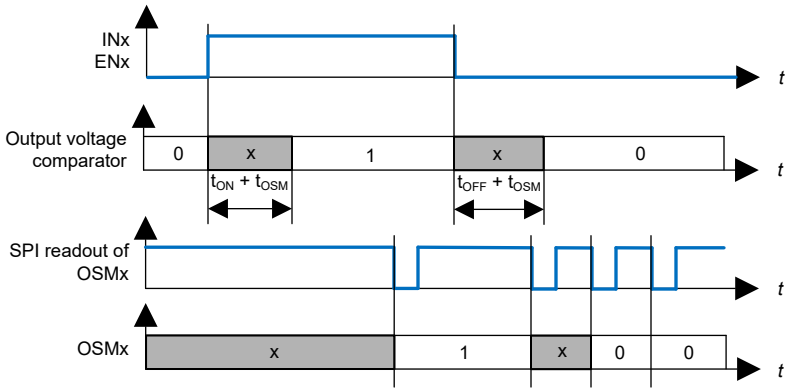

Figure 6-13. Output Status Monitor timing

Output Status Monitor diagnostic is available when $V_M = V_{M_NOR}$ and $V_{DD} \geq V_{DD_UVLO}$.

Due to the fact that Output Status Monitor checks the voltage level at the outputs in real time, for Open Load in OFF diagnostic it is necessary to synchronize the reading of OSM register with the OFF state of the channels.

Figure 6-14 shows how Output Status Monitor is implemented at concept level.

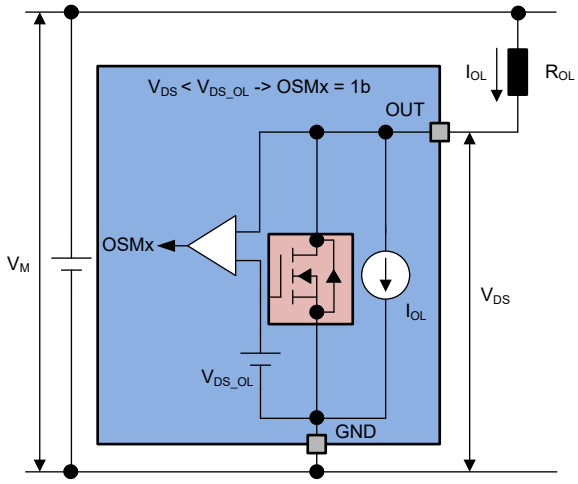

Figure 6-14. Output Status Monitor

In Standard Diagnosis the bit OLOFF represents the OR combination of all OSMx bits for all channels in OFF state which have the corresponding current source I_{OL} activated.

When the DISOL bit is 1b, open load detection is disabled by disabling all the I_{OL} current sources.

6.3.5 SPI Communication

The SPI interface is a full duplex synchronous serial follower interface, which uses four lines: SDO, SDI, SCLK and nSCS. Data is transferred by the lines SDI and SDO at the rate given by SCLK. The falling edge of nSCS indicates the beginning of an access. Data is sampled in on line SDI at the falling edge of SCLK and shifted out on line SDO at the rising edge of SCLK. Each access must be terminated by a rising edge of nSCS.

A modulo 8/16 counter ensures that data is taken only when a multiple of 8 bit has been transferred after the first 16 bits. Otherwise the TER bit is asserted. In this way the interface provides daisy chain capability with 16 bit as well as with 8 bit SPI devices.

6.3.5.1 SPI Signal Description

6.3.5.1.1 Chip Select (nSCS)

The microcontroller selects the DRV81008-Q1 by means of the nSCS pin. Whenever the pin is in logic low state, data transfer can take place. When nSCS is in logic high state, any signals at the SCLK and SDI pins are ignored and SDO is forced into a high impedance state.

6.3.5.1.1.1 Logic high to logic low Transition

- The requested information is transferred into the shift register.
- SDO changes from high impedance state to logic high or logic low state depending on the logic OR combination between the transmission error flag (TER) and the signal level at pin SDI. This allows to detect a faulty transmission even in daisy chain configuration.
- If the device is in Sleep mode, SDO pin remains in high impedance state and no SPI transmission occurs.

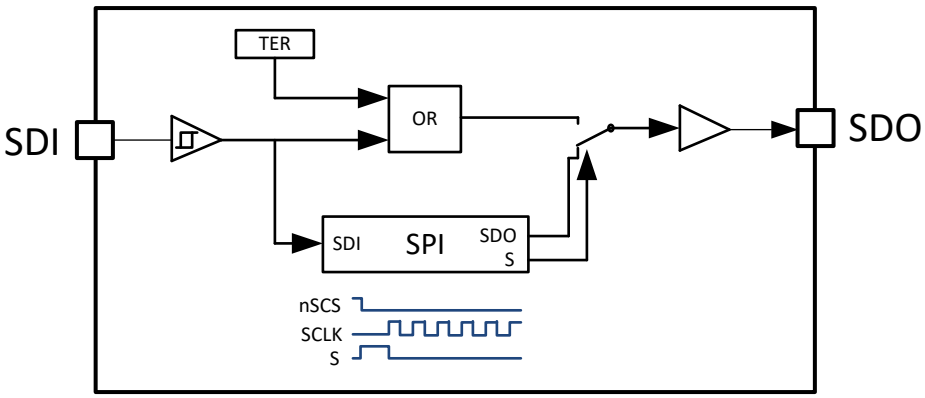

Figure 6-15. Combinational Logic for TER bit

6.3.5.1.1.2 Logic low to logic high Transition

- Command decoding is only done, when after the falling edge of nSCS exactly a multiple (1, 2, 3, ...) of eight SCLK signals have been detected after the first 16 SCLK pulses. In case of faulty transmission, the transmission error bit (TER) is set and the command is ignored.
- Data from shift register is transferred into the addressed register.

6.3.5.1.2 Serial Clock (SCLK)

This input pin clocks the internal shift register. The serial input (SDI) transfers data into the shift register on the falling edge of SCLK while the serial output (SDO) shifts diagnostic information out on the rising edge of the serial clock. It is essential that the SCLK pin is in logic low state whenever chip select nSCS makes any transition, otherwise the command may be not accepted.

6.3.5.1.3 Serial Input (SDI)

Serial input data bits are shift-in at this pin, the most significant bit first. SDI information is read on the falling edge of SCLK. The input data consists of two parts, control bits followed by data bits.

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6.3.5.1.4 Serial Output (SDO)

Data is shifted out serially at this pin, the most significant bit first. SDO is in high impedance state until the nSCS pin goes to logic low state. New data appears at the SDO pin following the rising edge of SCLK.

6.3.5.2 Daisy Chain Capability

The SPI of DRV81008-Q1 provides daisy chain capability. In this configuration several devices are activated by the same nSCS signal MCSN. The SDI line of one device is connected with the SDO line of another device, in order to build a chain. The end of the chain is connected to the output and input of the master device, M-SDO and M-SDI respectively. The commander device provides the clock M-SCLK which is connected to the SCLK line of each device in the chain.

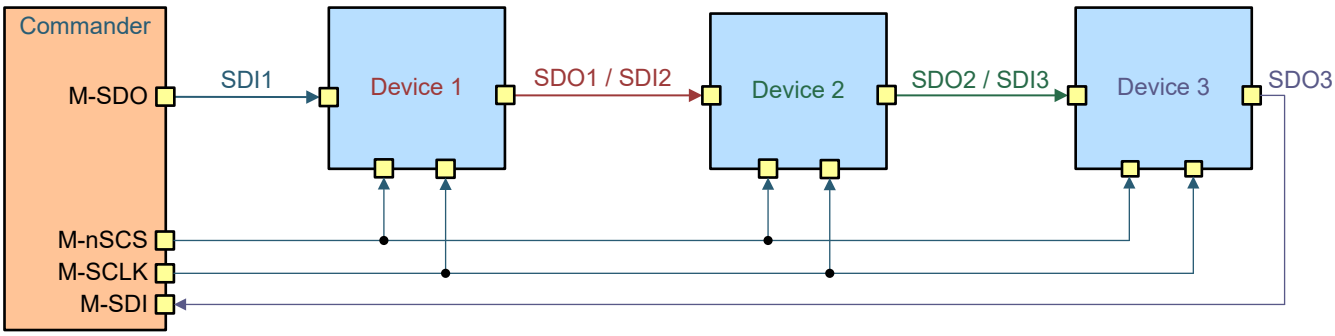

Figure 6-16. Daisy Chain Configuration

In the SPI block of each device, there is one shift register where each bit from SDI line is shifted in each SCLK. The bit shifted out occurs at the SDO pin. After sixteen SCLK cycles, the data transfer for one device is finished.

In single chip configuration, the nSCS line must turn logic high to make the device acknowledge the transferred data. In daisy chain configuration, the data shifted out at device 1 has been shifted in to device 2. When using three devices in daisy chain, several multiples of 8 bits have to be shifted through the devices (depending on how many devices with 8 bit SPI and how many with 16 bit SPI). After that, the M-nSCS line must turn logic high.

6.3.5.3 SPI Protocol

The relationship between SDI and SDO content during SPI communication is shown in Figure 6-17. SDI line represents the frame sent from the microcontroller and SDO line is the answer provided by DRV81008-Q1.

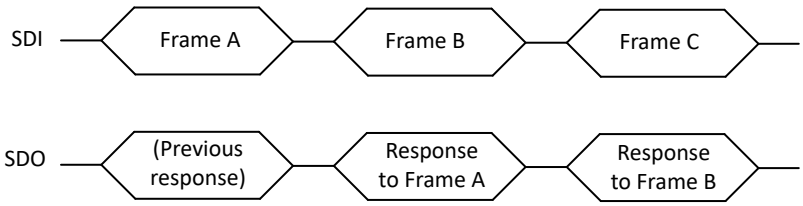

Figure 6-17. Relationship between SDI and SDO during SPI communication

The SPI protocol provides the answer to a command frame only with the next transmission triggered by the microcontroller. Although the biggest majority of commands and frames implemented in DRV81008-Q1 can be decoded without the knowledge of what happened before, it is advisable to consider what the microcontroller sent in the previous transmission to decode DRV81008-Q1 response frame completely. The sequence of commands to read and write the content of a register looks as follows:

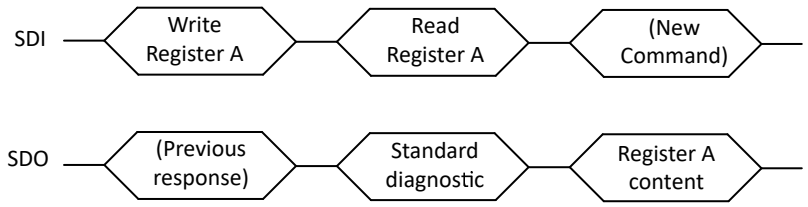

Figure 6-18. Register content sent back to microcontroller

There are 3 special situations where the frame sent back to the microcontroller is not related directly to the previous received frame:

- In case an error in transmission happened during the previous frame (for instance, the clock pulses were not multiple of 8 with a minimum of 16 bits), shown below.
- When DRV81008-Q1 logic supply comes out of Power-On reset condition or after a Software Reset, as shown below.
- In case of command syntax errors
  - write command starting with 11b instead of 10b
  - read command starting with 00b instead of 01b
  - read or write commands on registers which are reserved or not used

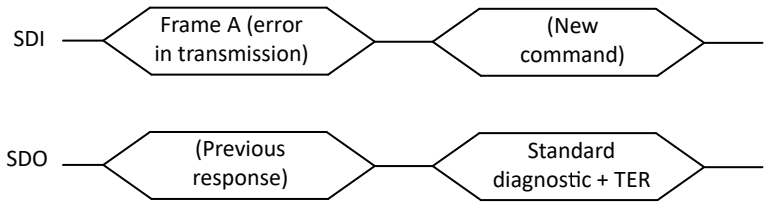

Figure 6-19. Response after a error in transmission

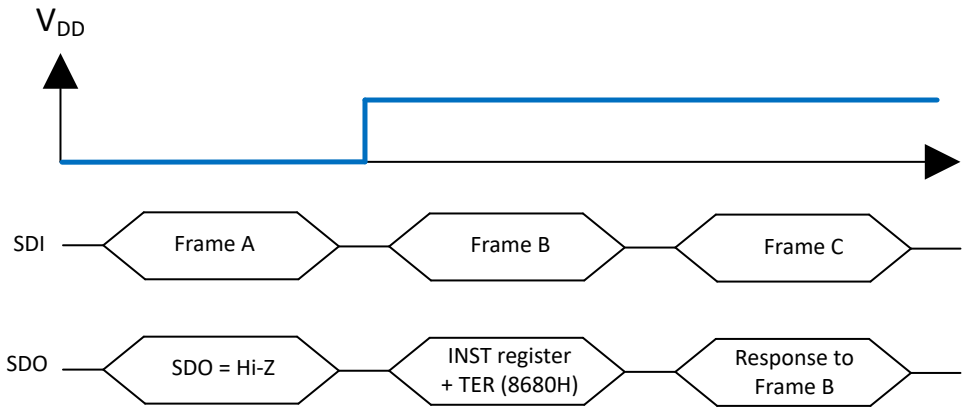

Figure 6-20. Response after coming out of Power-On reset at V_{DD}

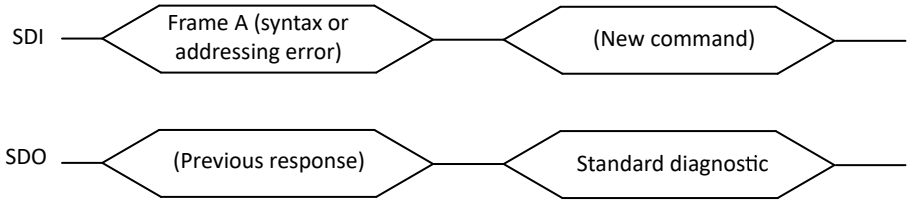

Figure 6-21. Response after a command syntax error

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A summary of all possible SPI commands is presented below, including the answer that DRV81008-Q1 sends back at the next transmission.

Table 6-6. SPI Command summary

Requested Operation	Frame sent to SDI pin	Frame received from SDO pin with the next command
Read Standard Diagnosis	0xxxxxxxxxxxxx01b (xxxxxxxxxxxxb = don't care)	0ddddddddddddddb (Standard Diagnosis)
Write 8 bit register	10ppppqqrrrrrrrrb where: ppppb = register address ADDR0, qqb = register address ADDR1, rrrrrrrrb = new register content	0ddddddddddddddb (Standard Diagnosis)
Read 8 bit registers	01ppppqqxxxxxx10b where: ppppb = register address ADDR0, qqb = register address ADDR1, xxxxxxb = don't care	10ppppqqrrrrrrrrb where: ppppb = register address ADDR0c, qqb = register address ADDR1, rrrrrrrrb = register content

“p” = address bits for ADDR0 field, “q” = address bit for ADDR1 field, “r” = register content, “d” = diagnostic bit

6.3.5.4 SPI Registers

The register banks have the following structure -

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
R = 0 W = 1	R = 1 W = 0	ADDR0				ADDR1		DATA								XXXXH

All registers with addresses not mentioned in subsequent sections have to be considered as reserved. Read operations performed on those registers return the Standard Diagnosis. The column Default indicates the content of the register (8 bits) after a reset.

The LOCK bits in configuration register 2 can be used to lock register settings from unintended SPI writes.

- Write 110b to lock the settings by ignoring further register writes except to LOCK bits and CLRx bits. Writing any sequence other than 110b has no effect when unlocked.
- Write 011b to unlock all registers. Writing any sequence other than 011b has no effect when locked.

6.3.5.4.1 Standard Diagnosis Register

Table 6-7. Standard Diagnosis Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0	UVRVM	0	MODE		TER	0	OLOFF	ERR7	ERR6	ERR5	ERR4	ERR3	ERR2	ERR1	ERR0	5800h

Table 6-8. Standard Diagnosis Register Description

Field	Bits	Type	Description
UVRVM	14	R	VM Undervoltage monitor • 0b: No undervoltage condition on VM detected • 1b (default): There was at least one VM Undervoltage condition since last Standard Diagnosis readout
MODE	12-11	R	Mode of operation monitor • 00b: Reserved • 01b: Limp Home Mode • 10b: Active Mode • 11b (default): Idle Mode
TER	10	R	Transmission error • 0b: Previous transmission was successful (modulo 16 + n*8 clocks received, where n = 0, 1, 2...) • 1b (default): Previous transmission failed. The first frame after a reset is TER set to 1b and the INST register. The second frame is the Standard Diagnosis with TER set to 0b (if there was no fail in the previous transmission).
OLOFF	8	R	Open load in OFF diagnosis • 0b (default): All channels in OFF state (which have IOLx bit set to 1b) have $V_{DS} > V_{DS_OL}$ • 1b: At least one channel in OFF state (with IOLx bit set to 1b) has $V_{DS} < V_{DS_OL}$. Channels in ON state are not considered.
ERRx	7-0	R	Overload / Over temperature Diagnosis of Channel x • 0b (default): No failure detected • 1b: Over temperature or overload

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6.3.5.4.2 Output control register

Table 6-9. Output Control Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
R = 0 W = 1	R = 1 W = 0	0000				00		EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0	00h

Table 6-10. Output Control Register Description

Field	Bits	Type	Description
ENx	7-0	RW	Output x control register • 0b (default): Output x is OFF • 1b: Output is ON

6.3.5.4.3 Input 0 Mapping Register

Table 6-11. Input 0 Mapping Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
R = 0 W = 1	R = 1 W = 0	0001				00		MAP07	MAP06	MAP05	MAP04	MAP03	MAP02	MAP01	MAP00	04h

Table 6-12. Input 0 Mapping Register Description

Field	Bits	Type	Description
MAP0x	7-0	RW	Input pin 0 Mapping register • 0b (default): Output x is not connected to the input pin 0 • 1b: The output is connected to the input pin Note: Channel 2 has the corresponding bit set to 1b by default

6.3.5.4.4 Input 1 Mapping Register

Table 6-13. Input 1 Mapping Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
R = 0 W = 1	R = 1 W = 0	0001				01		MAP17	MAP16	MAP15	MAP14	MAP13	MAP12	MAP11	MAP10	08h

Table 6-14. Input 1 Mapping Register Description

Field	Bits	Type	Description
MAP1x	7-0	RW	Input pin 1 Mapping register • 0b (default): Output x is not connected to the input pin 1 • 1b: The output is connected to the input pin Note: Channel 3 has the corresponding bit set to 1b by default

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6.3.5.4.5 Input Status Monitor Register

This is the first register transmitted after a reset of the logic

.

Table 6-15. Input Status Monitor Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0	1	0001				10		TER	RSVD					INST1	INST0	00h

Table 6-16. Input 1 Mapping Register Description

Field	Bits	Type	Description
TER	7	R	• 0b: Previous transmission was successful (modulo 16 + n*8 clocks received, where n = 0, 1, 2...) • 1b (default): Previous transmission failed
RSVD	6-2	R	Reserved
INST1	1	R	• 0b (default): The input pin is set to logic low • 1b: The input pin is set to logic high
INST0	0	R	• 0b (default): The input pin is set to logic low • 1b: The input pin is set to logic high

6.3.5.4.6 Open Load Current Control Register

Table 6-17. Open Load Current Control Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
R = 0 W = 1	R = 1 W = 0	0010				00		IOL7	IOL6	IOL5	IOL4	IOL3	IOL2	IOL1	IOL0	00h

Table 6-18. Open Load Current Control Register Description

Field	Bits	Type	Description
IOLx	7-0	RW	• 0b (default): IOL current source not enabled • 1b: IOL current source enabled

6.3.5.4.7 Output Status Monitor Register

Table 6-19. Output Status Monitor Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
0	1	0010				01		OSM7	OSM6	OSM5	OSM4	OSM3	OSM2	OSM1	OSM0	00h

Table 6-20. Output Status Monitor Register Description

Field	Bits	Type	Description
OSMx	7-0	R	• 0b (default): $V_{DS} > V_{DS_OL}$ • 1b: $V_{DS} < V_{DS_OL}$

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6.3.5.4.8 Configuration Register

Table 6-21. Configuration Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
R = 0 W = 1	R = 1 W = 0	0011				00		ACT	RST	DISOL	OCP	PAR3	PAR2	PAR1	PAR0	00h

Table 6-22. Configuration Register Description

Field	Bits	Type	Description
ACT	7	RW	• 0b (default): Normal operation or device leaves Active Mode • 1b: Device enters Active Mode
RST	6	RW	• 0b (default): Normal operation • 1b: Execute Reset command (self clearing)
DISOL	5	RW	• 0b (default): Open load detection is enabled • 1b: Open load detection is disabled
OCP	4	RW	• 0b (default): Overcurrent protection current profile 1 • 1b: Overcurrent protection current profile 2
PAR3	3	RW	• 0b (default): Normal operation • 1b: Channel 5 and 7 have Over Load and Over Temperature synchronized
PAR2	2	RW	• 0b (default): Normal operation • 1b: Channel 4 and 6 have Over Load and Over Temperature synchronized
PAR1	1	RW	• 0b (default): Normal operation • 1b: Channel 1 and 3 have Over Load and Over Temperature synchronized
PAR0	0	RW	• 0b (default): Normal operation • 1b: Channel 0 and 2 have Over Load and Over Temperature synchronized

6.3.5.4.9 Output Clear Latch Register

Table 6-23. Output Clear Latch Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
R = 0 W = 1	R = 1 W = 0	0011				01		CLR7	CLR6	CLR5	CLR4	CLR3	CLR2	CLR1	CLR0	00h

Table 6-24. Output Clear Latch Register Description

Field	Bits	Type	Description
CLRx	7-0	RW	• 0b (default): Normal operation • 1b: Clear the error latch for the selected output

6.3.5.4.10 Configuration Register 2

Table 6-25. Configuration Register 2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
R = 0 W = 1	R = 1 W = 0	1010				00		LOCK[2:0]			RSVD		OTW	RSVD	SR	60h

Table 6-26. Configuration Register 2 Description

Field	Bits	Type	Description
LOCK[2:0]	7-5	RW	Write 110b to lock the settings by ignoring further register writes except to LOCK bits and CLRx bits. Writing any sequence other than 110b has no effect when unlocked. Write 011b to this register to unlock all registers. Writing any sequence other than 011b has no effect when locked.
RSVD	4-3, 1	R	Reserved
OTW	2	R	Overtemperature Warning Flag • 0b (default): No Overtemperature event • 1b: Overtemperature event
SR	0	RW	Sets output slew rate • 0b (default): 1.2 V/µs slew rate • 1b: 3 V/µs slew rate

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The DRV81008-Q1 is primarily used to drive relays in Automotive and Industrial applications.

7.1.1 Typical Application

Figure 7-1 shows the application schematic for the DRV81008-Q1.

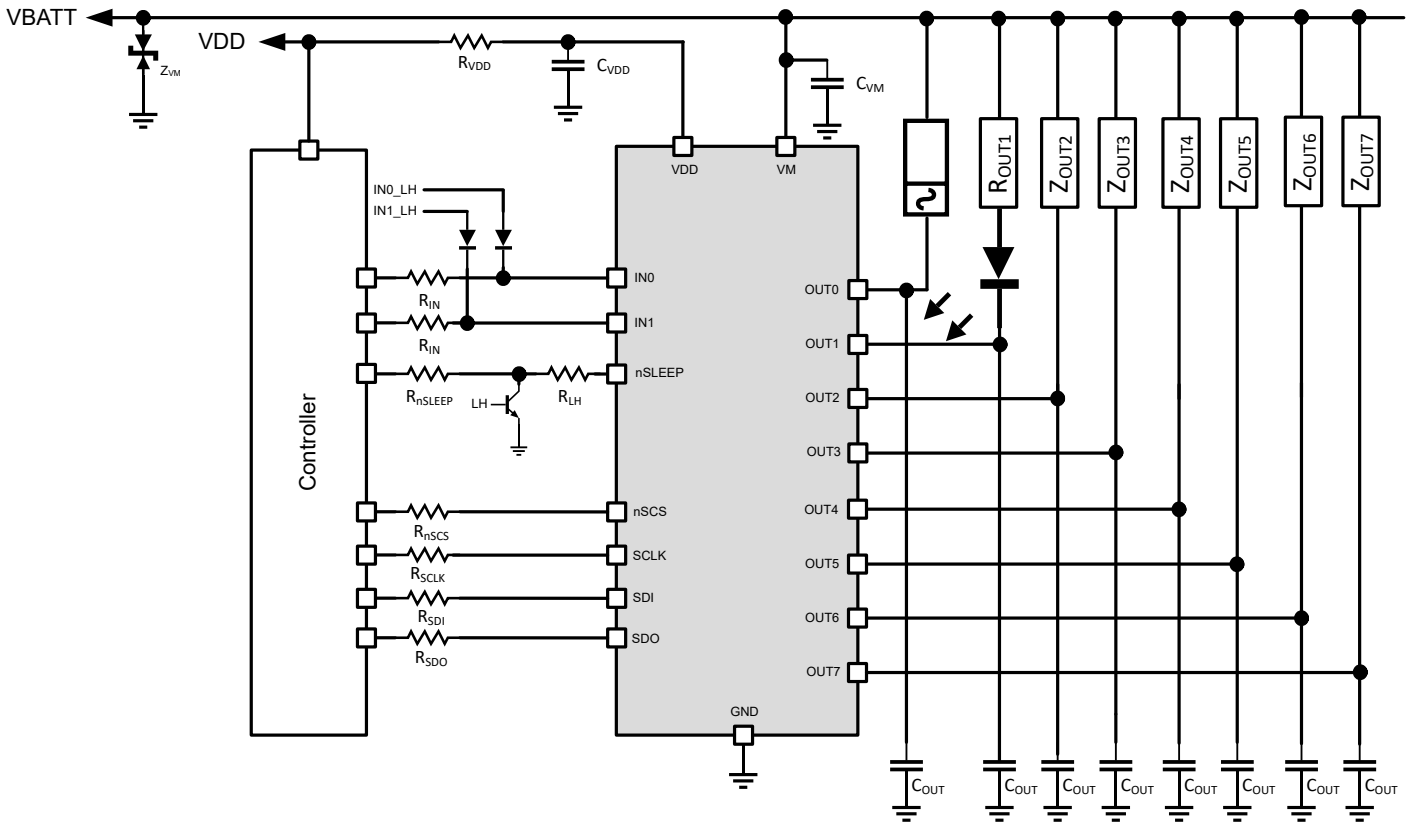

Figure 7-1. Application Schematic

7.1.2 Suggested External Components

Table 7-1 lists the recommended external components for the DRV81008-Q1.

Table 7-1. Suggested External Components

Description	Value	Purpose
Resistors in series with IN0, IN1 and nSLEEP pins	4.7kΩ	Protection of the microcontroller during over voltage and reverse polarity. Also to guarantee output channels OFF during loss of ground.
Resistors in series with nSCS, SCLK, SDI and SDO pins	470Ω	Protection of the microcontroller during over voltage and reverse polarity
Resistor in series with VDD pin	100Ω	Logic supply voltage filtering
Bypass capacitor on VDD pin	100nF	Logic supply voltage filtering
Bypass capacitor on VM pin	68nF	Battery voltage filtering
TVS diode on VM pin	TVS3300	Protection of device during overvoltage
Capacitor on each OUT pin (optional)	10nF	Protection of the device against ESD and BCI

7.1.3 Application Plots

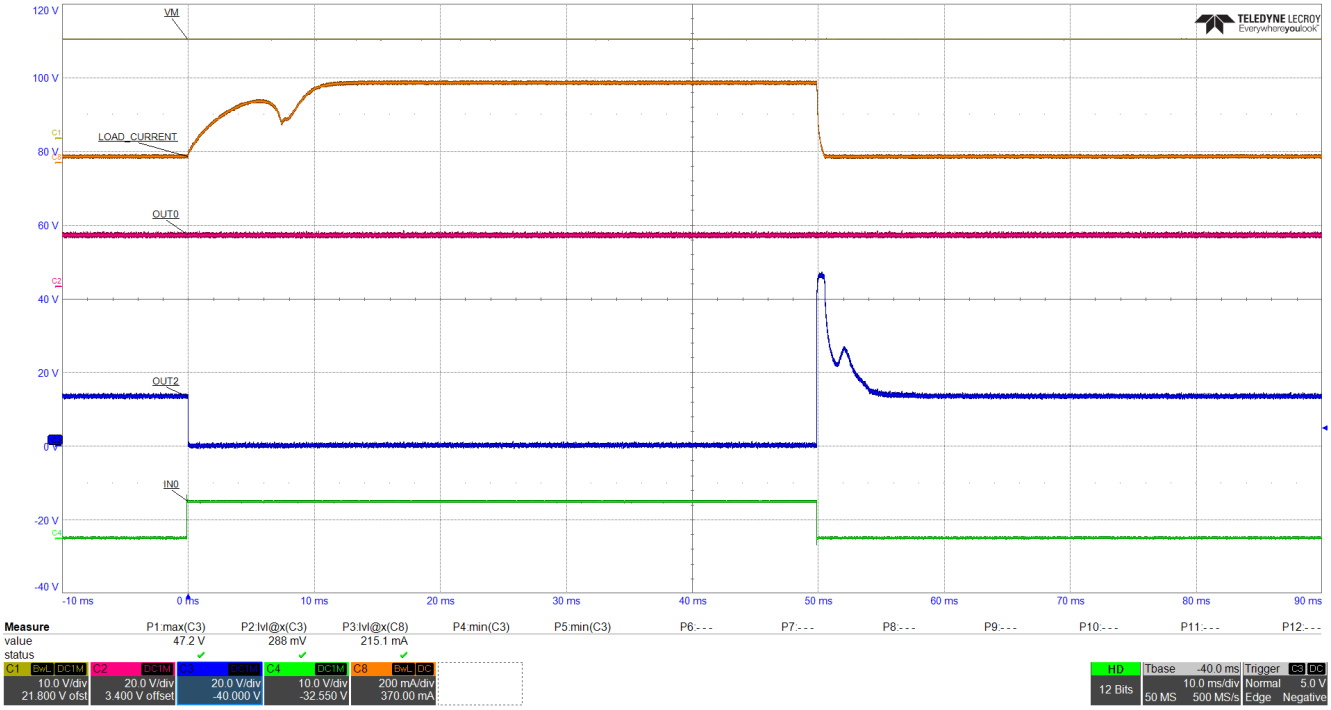

Figure 7-2. Output Turn-ON/OFF from IN0 pin

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7.2 Layout

7.2.1 Layout Guidelines

- The VM pin should be bypassed to GND using low-ESR ceramic bypass capacitor with a recommended value of 68nF rated for VM. The capacitor should be placed as close to the VM pin as possible with a thick trace or ground plane connection to the device GND pin.
- Bypass the VDD pin to ground with a low-ESR ceramic capacitor. A value of 100nF rated for 6.3V is recommended. Place this bypassing capacitor as close to the pin as possible.
- In general, inductance between the power supply pins and decoupling capacitors must be avoided.
- Connect series resistors between IN0, IN1, nSLEEP, nSCS, SCLK, SDI, SDO and VDD pins of the DRV81008-Q1 and corresponding pins of the microcontroller. The recommended values of the resistors are shown in Section 6.3.
- The thermal PAD of the package must be connected to system ground.
  - It is recommended to use a big unbroken single ground plane for the whole system / board. The ground plane can be made at bottom PCB layer.
  - In order to minimize the impedance and inductance, the traces from ground pins should be as short and wide as possible, before connecting to bottom layer ground plane through vias.
  - Multiple vias are suggested to reduce the impedance.
  - Try to clear the space around the device as much as possible especially at bottom PCB layer to improve the heat spreading.
  - Single or multiple internal ground planes connected to the thermal PAD will also help spreading the heat and reduce the thermal resistance.

7.2.2 Package Footprint Compatibility

The PWP0024T package of the DRV81008-Q1 is footprint compatible with other SO-24 packages used in the industry, as shown in Figure 7-3 and Figure 7-4.

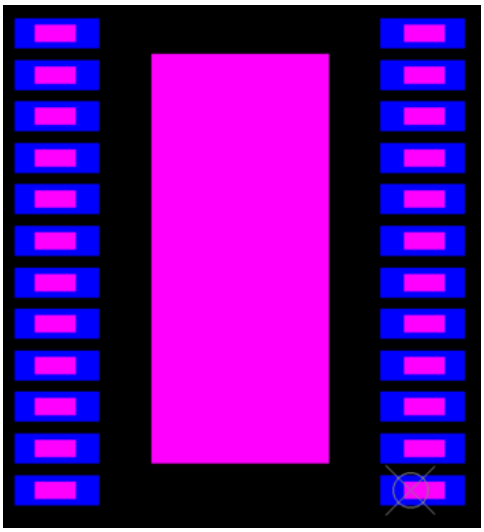

Figure 7-3. PWP0024T on another SO-24 PCB Pad, Pink: TI PWP0024T leads, Blue: other SO-24 PCB Pad

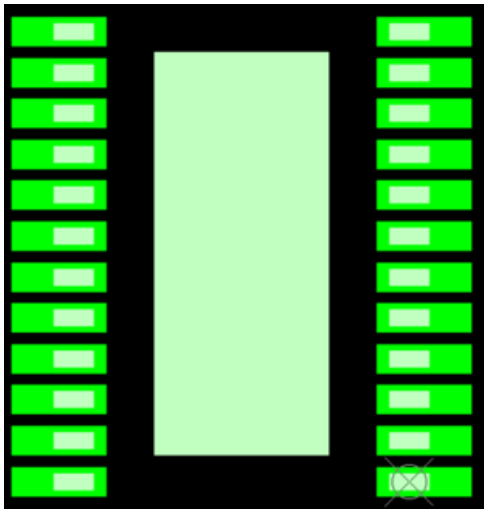

Figure 7-4. SO-24 on PWP0024T PCB Pad, White: other SO-24 leads, Green: TI PWP0024T PCB Pad

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8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

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8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (December 2024) to Revision B (February 2025)	Page
• Added notes for AECQ100 compliance and Functional Safety compliance	1
• VDS_OL minimum and maximum limits in the EC table have been updated to 3V and 3.6V from 2.9V/3.7V	6
• Added typical operating plots of ROL vs. VM and IOL vs. VM	10

Changes from Revision * (November 2024) to Revision A (December 2024)	Page
• Updated device status to production data	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV81008QPWPRQ1	Active	Production	HTSSOP (PWP) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	81008Q1
DRV81008QPWPRQ1.A	Active	Production	HTSSOP (PWP) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	81008Q1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

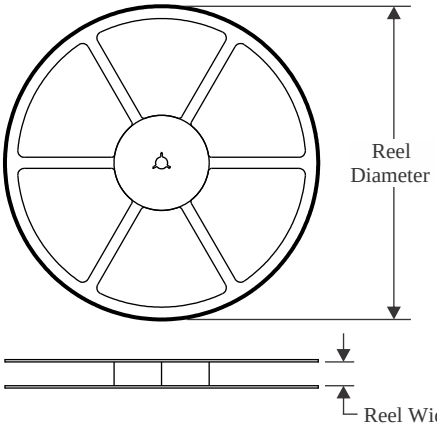
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

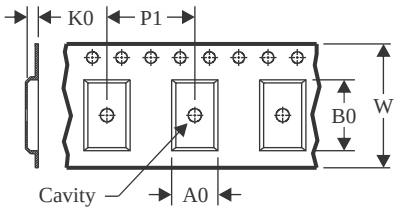
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

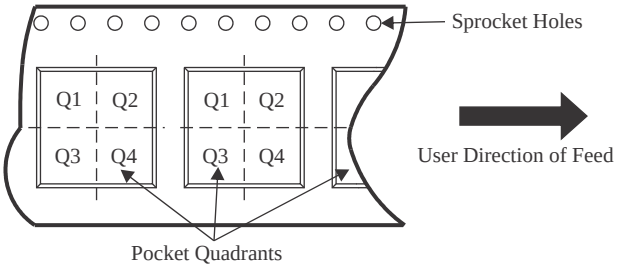


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

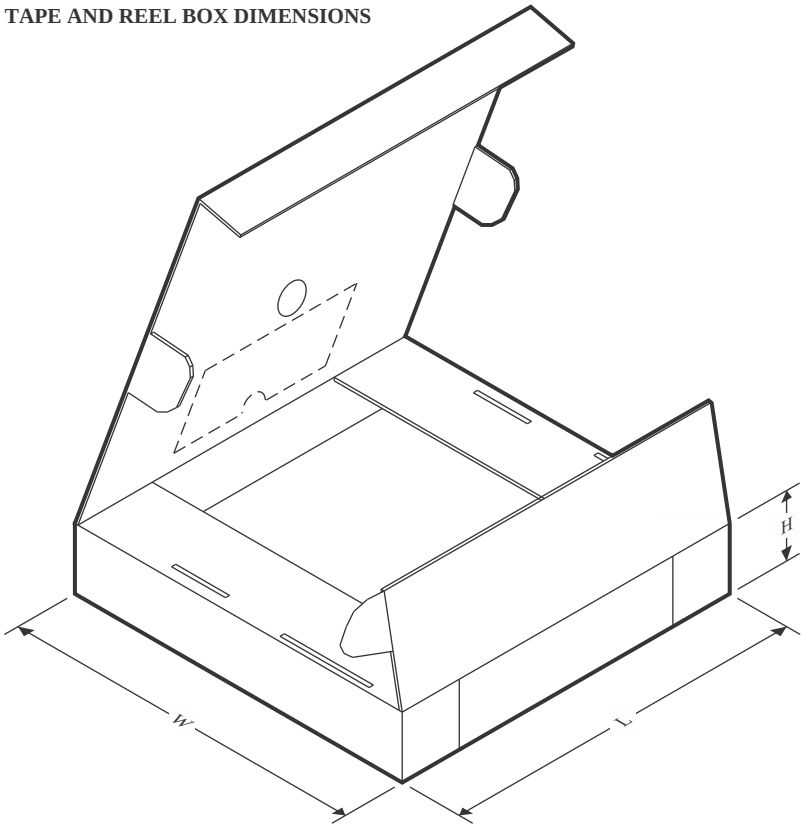
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV81008QPWPRQ1	HTSSOP	PWP	24	3000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV81008QPWPRQ1	HTSSOP	PWP	24	3000	353.0	353.0	32.0

GENERIC PACKAGE VIEW

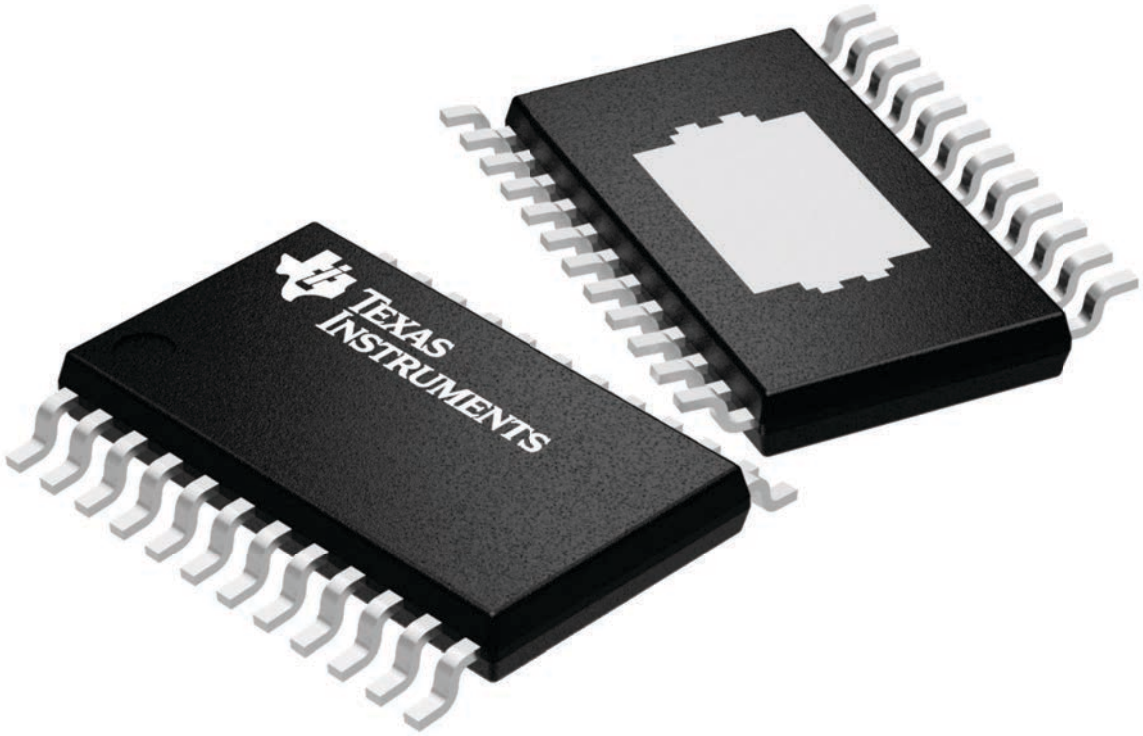
PWP 24

PowerPAD™ TSSOP - 1.2 mm max height

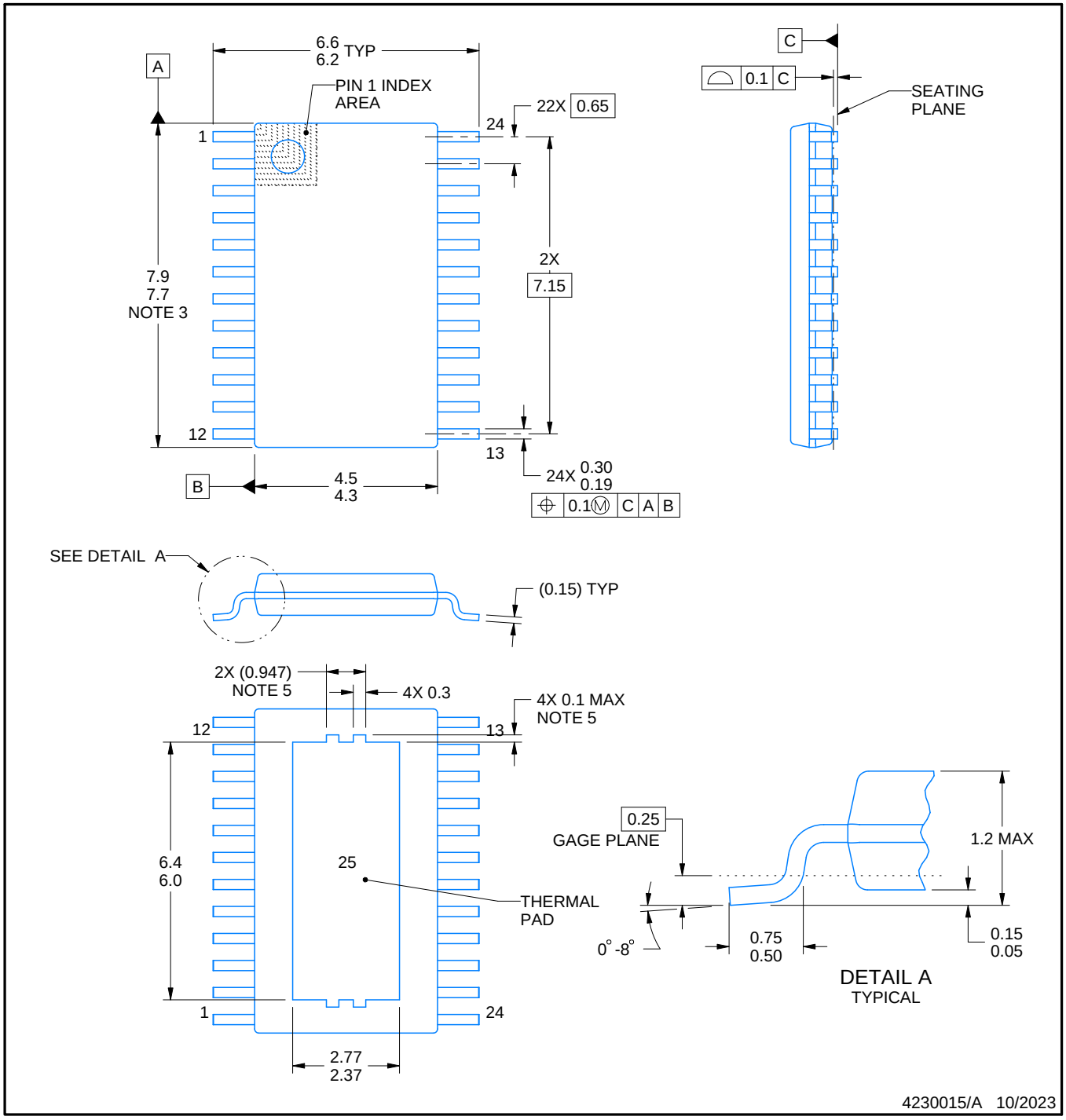
4.4 x 7.6, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



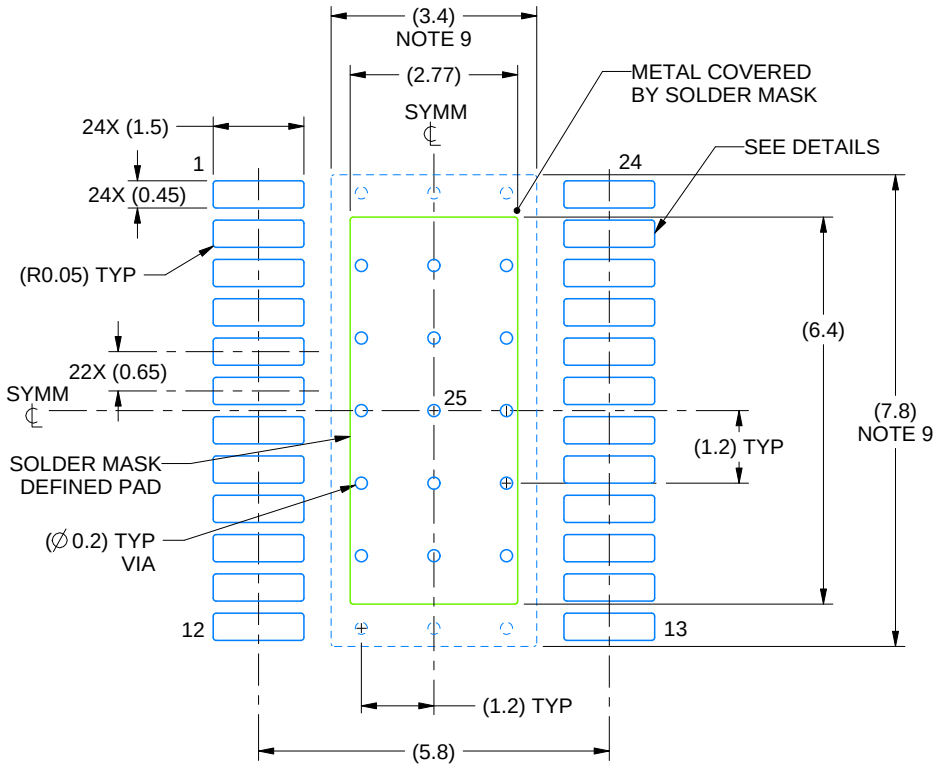
4224742/B



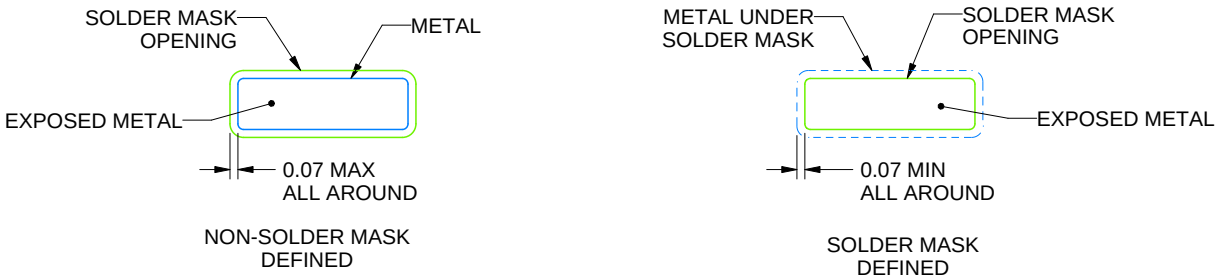
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

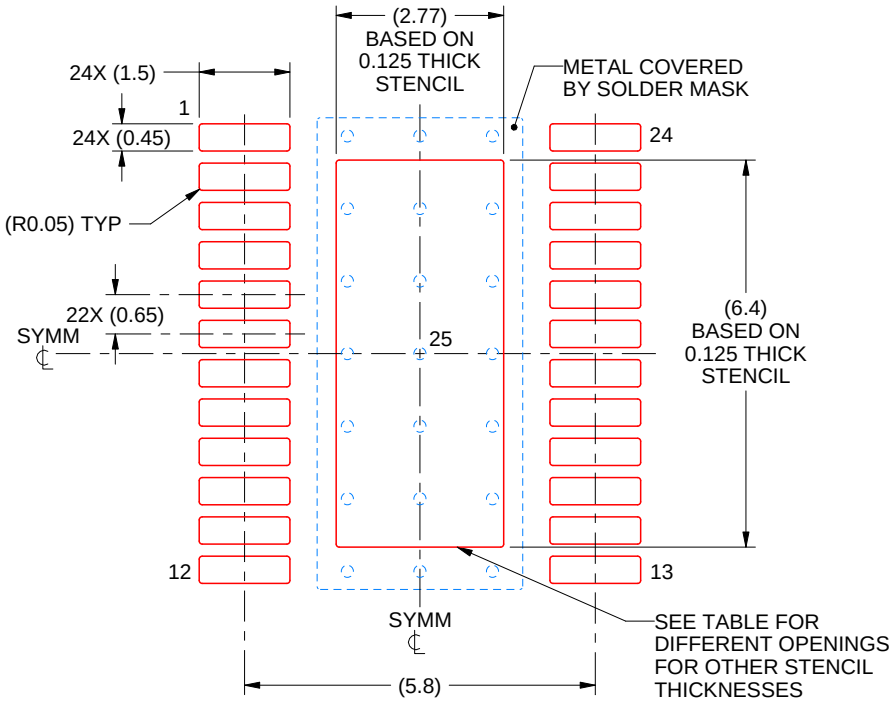


SOLDER MASK DETAILS

4230015/A 10/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.10 X 7.16
0.125	2.77 X 6.40 (SHOWN)
0.15	2.53 X 5.84
0.175	2.34 X 5.41

4230015/A 10/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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