

TAS6684-Q1 - 45V, 13A Digital Input 4-Channel Automotive Class-D Audio Amplifier with Current Sense and Real-time Load Diagnostics

1 Features

- AEC-Q100 qualified for automotive applications
 - Temperature grade 1: -40°C to $+125^{\circ}\text{C}$, T_A
- General operation
 - 4.5V to 45V supply voltage, 50V load dump
 - Support for 1.8V and 3.3V I/O's
 - I²C control with 8 address options
 - <2-W idle power loss at 14.4V, <8uA max VBAT+PVDD shutdown loss
- Integrated DSP processing
 - Class-H supply voltage control
 - Thermal monitoring and foldback
 - Clip detection, PVDD monitoring and foldback
- Output current sensing by channel via I²S/TDM
 - No need for external circuitry
- Real-time load diagnostics
 - Monitor output conditions while playing audio
 - Real-time temperature monitor for each channel
 - Open load, Shorted load, Short-to-power, Short-to-ground detection
- DC and AC Standby load diagnostics
- Audio inputs
 - 2-4 channel I²S or 4-16 channel TDM input
 - Input sample rates: 44.1, 48, 96, 192kHz
 - Low latency < 100us at 96k sample rate
- Audio outputs
 - 4-channel bridge-tied load (BTL), configurable 2-channel parallel BTL (PBTL)
 - 384kHz to 2MHz configurable output switching frequency
 - Up to 13A channel output current
 - 400VA peak BTL output power
 - 118W (45V, 8 Ω , 1% THD, BTL)
 - 218W (45V, 4 Ω , 1% THD, BTL)
- Audio Performance
 - THD+N 0.03% (8 Ω , 1W, 1kHz)
 - 111dB SNR
 - 37 μV (14.4V), 80 μV (45V) output noise
- Protection
 - Output short protection
 - DC offset, undervoltage and overvoltage
 - Configurable overtemperature warning and individual channel shutdown
 - I²C temperature and supply voltage readout
- Easily meet CISPR25-L5 EMC specification
 - Advanced spread-spectrum

2 Applications

- [Automotive external amplifier](#)
- [Automotive head unit](#)

3 Description

The TAS6684-Q1 is a four-channel, digital-input, high-voltage, Class-D audio amplifier that supports up to 45V supply voltage. Combined with up to 13A output current, this device delivers maximum output power and high fidelity audio in high and low impedance loads. The device provides four channels at 118W (45V, 8 Ω , 1% THD, BTL) and 218W (45V, 4 Ω , 1% THD, BTL).

The TAS6684-Q1 integrates DC and AC load diagnostics to determine the status of the connected loads before enabling the output stage. During audio playback, the status can be monitored through the output current sense and temperature of each channel which is available for each channel, and reports the measurement to a host processor through TDM with minimal delay. The device monitors the output load condition while playing audio using real-time load diagnostics which operate independently from the host and audio input.

To optimize system efficiency, the integrated DSP of the TAS6684-Q1 enables Class-H envelope tracking control, eliminating the need for the development of complex tracking software and making local boost voltage control possible without the need for an external microcontroller.

The TAS6684-Q1 device features an additional low-latency signal path for each channel, providing up to 70% faster signal processing at 48kHz and support an audio signal path latency of < 100us at 96kHz sample rate, which enables time-sensitive Active Noise Cancellation (ANC), Road Noise Cancellation (RNC) applications.

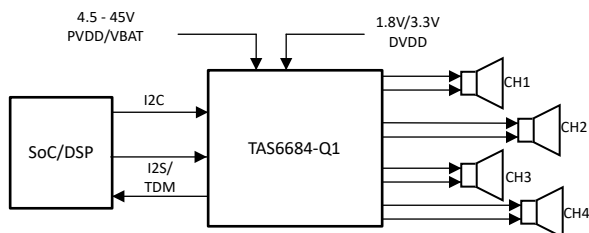
The TAS6684-Q1 is offered in a 64-pin QFP package with the exposed thermal pad up, TAS6684-Q1 is pin-to-pin compatible with TAS6584-Q1.



Device Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE (NOM) ⁽²⁾
TAS6684-Q1	HTQFP (64)	14.00mm x 14.00mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
 (2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Diagram

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4 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

4.1 Device Support

4.2 Documentation Support

4.2.1 Related Documentation

4.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

4.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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4.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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4.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

4.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (July 2024) to Revision A (October 2024)	Page
• Changed device status from <i>Advanced Information</i> to <i>Production Data</i>	1

6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

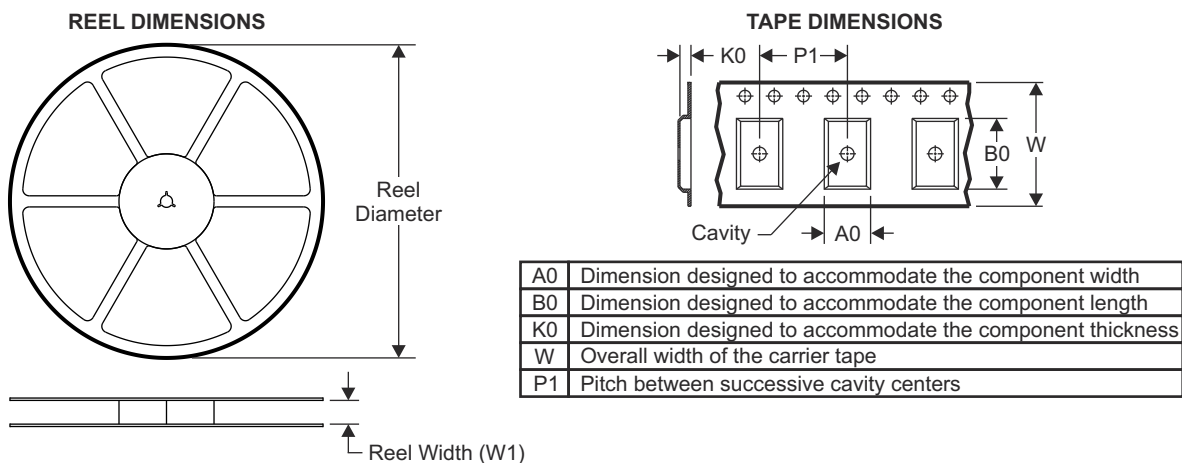
6.1 Package Option Addendum

Packaging Information

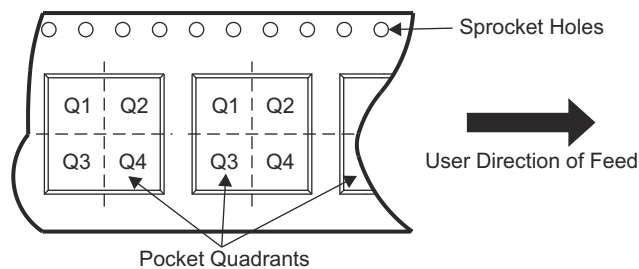
Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish ⁽⁶⁾	MSL Peak Temp ⁽³⁾	Op Temp (°C)	Device Marking ⁽⁴⁾ ⁽⁵⁾
TAS6684QPHDRQ1	ACTIVE	HTQFP	PHD	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TAS6684

- (1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.
- (2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).
- (3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

6.2 Tape and Reel Information

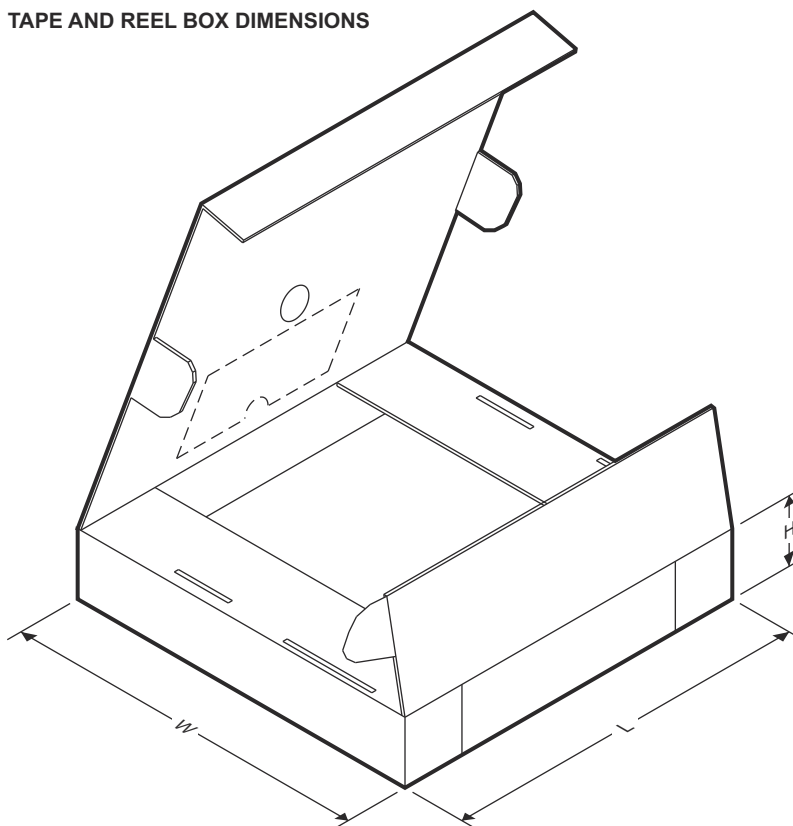


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



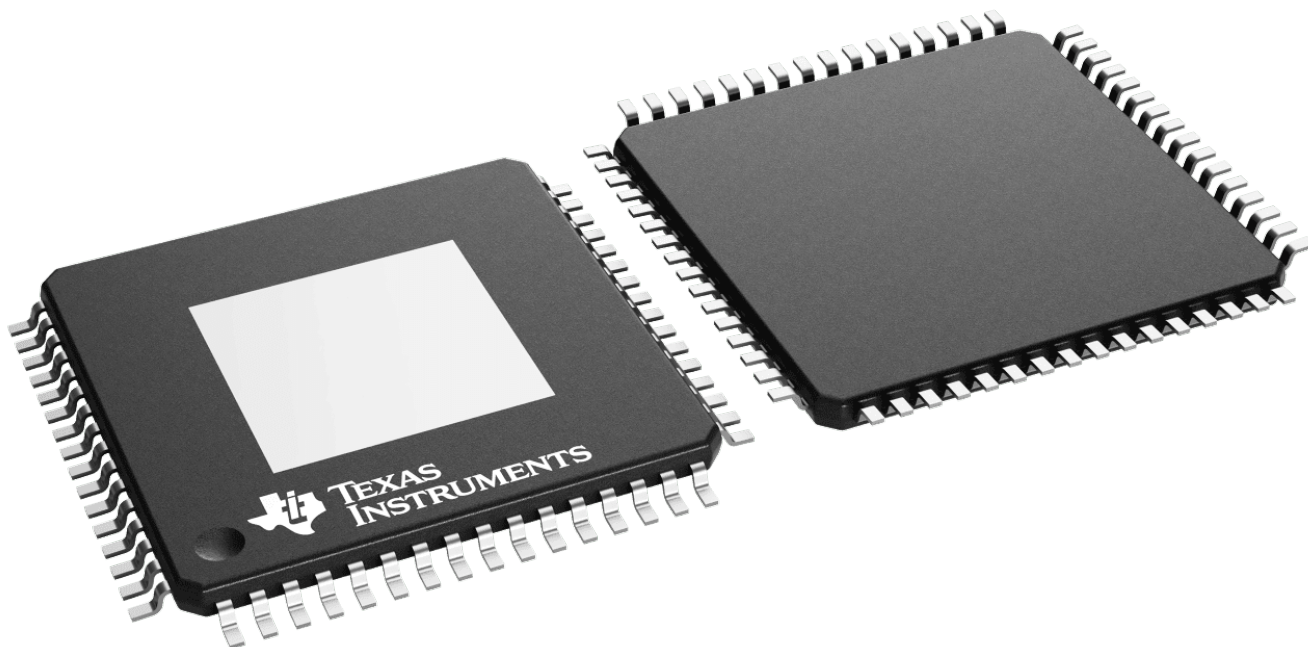
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS6684QPHDRQ1	HTQFP	PHD	64	1000	330.0	24.4	17.0	17.0	1.5	20.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS6684QPHDRQ1	HTQFP	PHD	64	1000	350.0	350.0	43.0

6.3 Mechanical Data

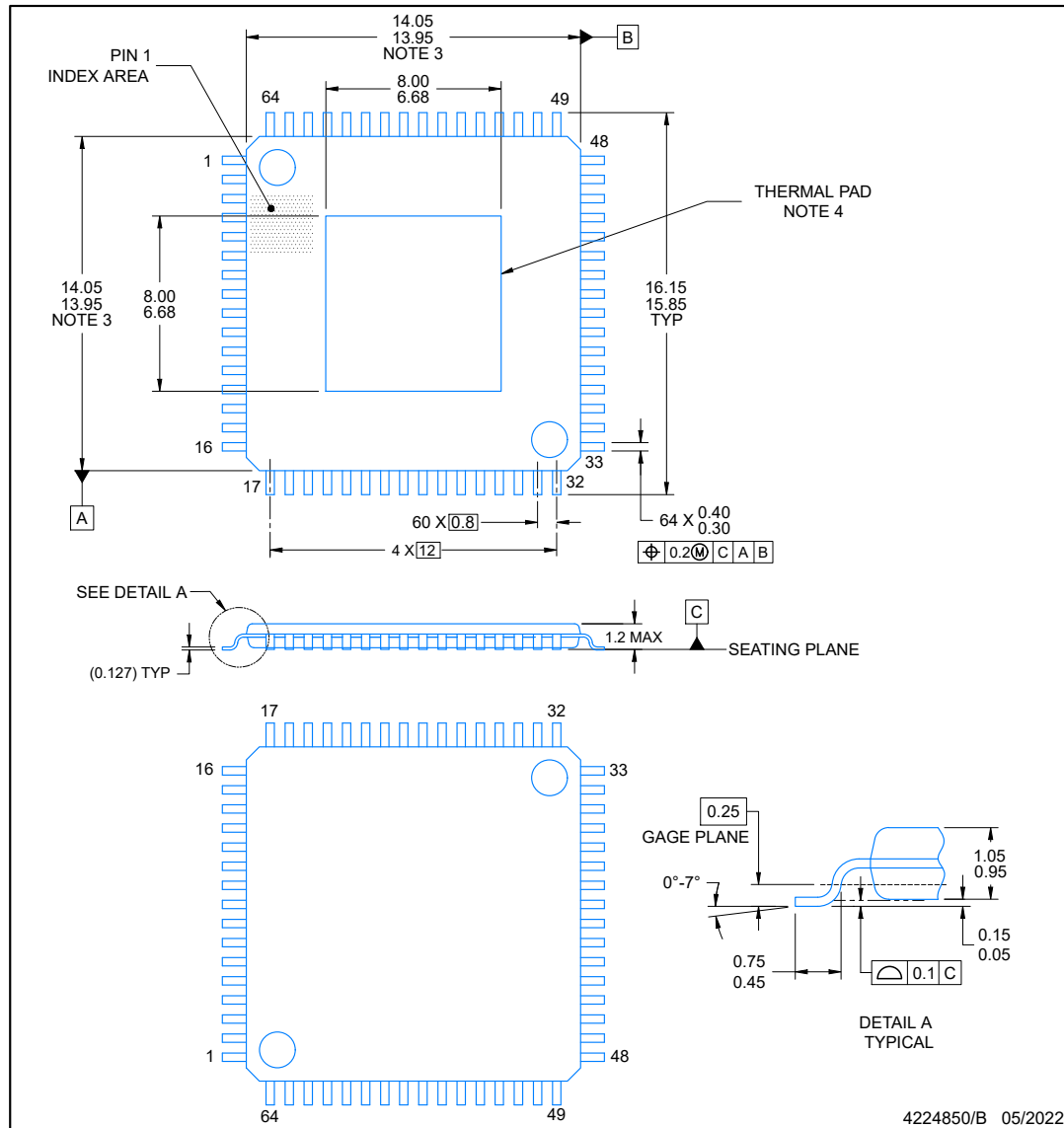


PHD0064B

PACKAGE OUTLINE

HTQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



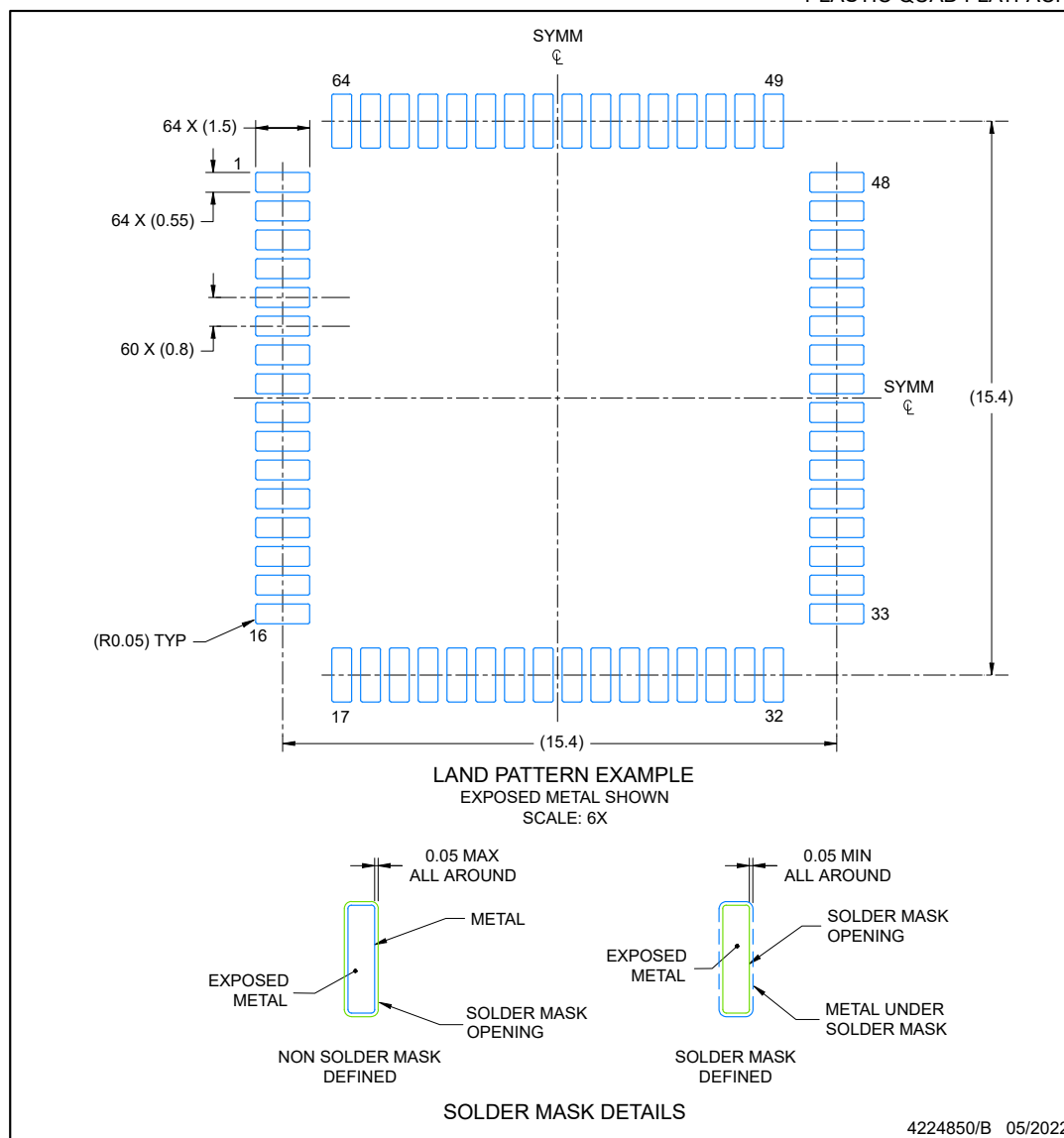
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. See technical brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004) for information regarding recommended board layout.

PHD0064B

EXAMPLE BOARD LAYOUT
HTQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK

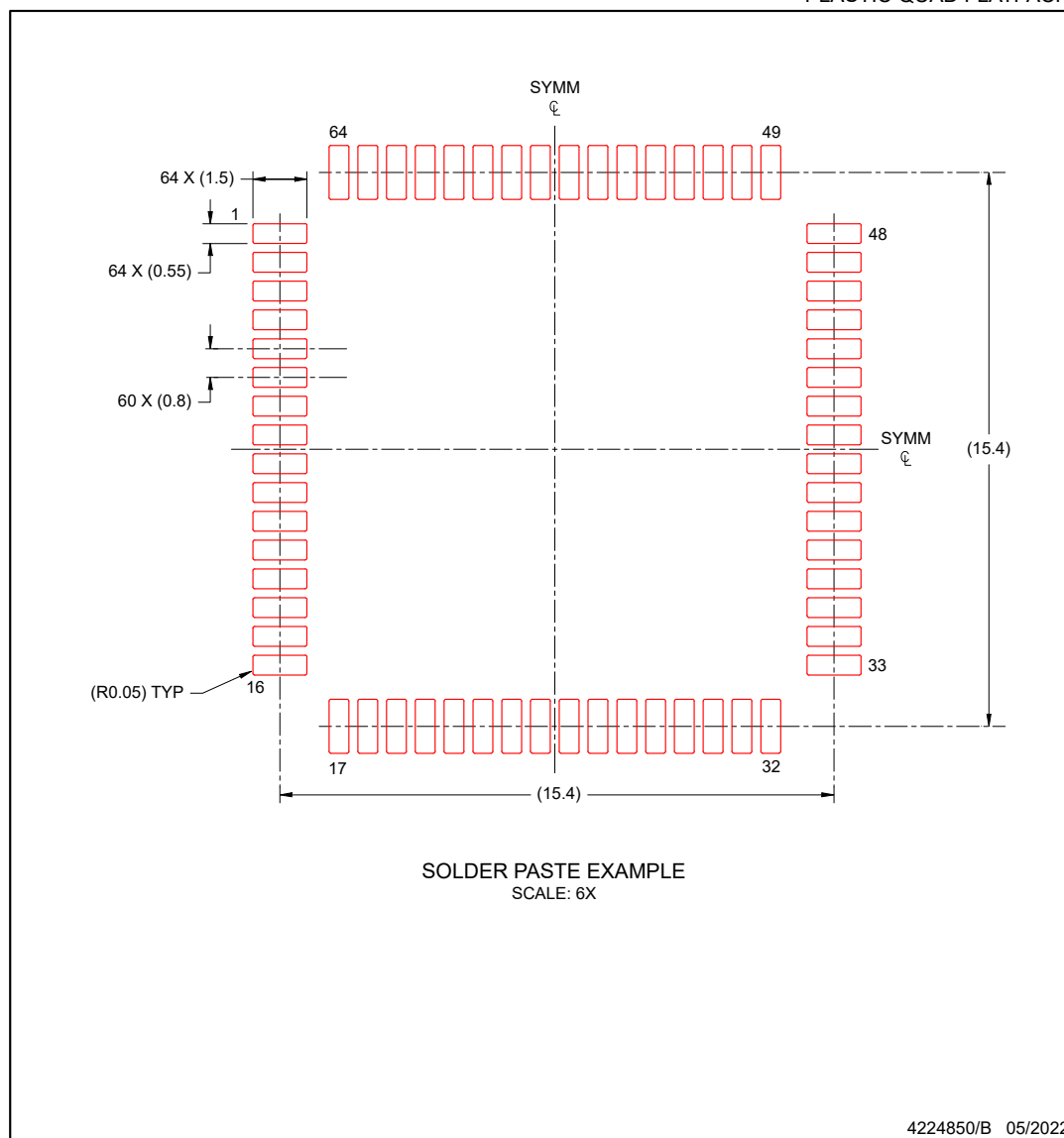


NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN**PHD0064B****HTQFP - 1.2 mm max height**

PLASTIC QUAD FLATPACK



NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

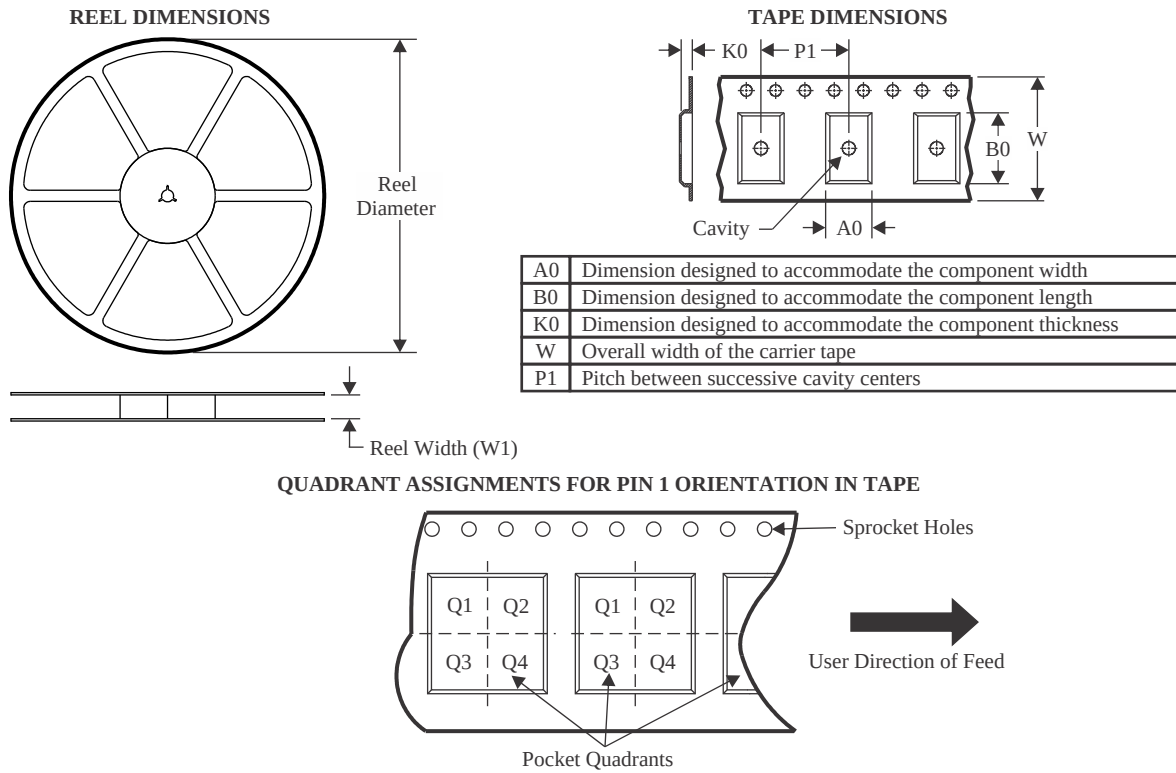
Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TAS6684QPHDRQ1	Active	Production	HTQFP (PHD) 64	1000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TAS6684
TAS6684QPHDRQ1.A	Active	Production	HTQFP (PHD) 64	1000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TAS6684

- ⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).
- ⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- ⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- ⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- ⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- ⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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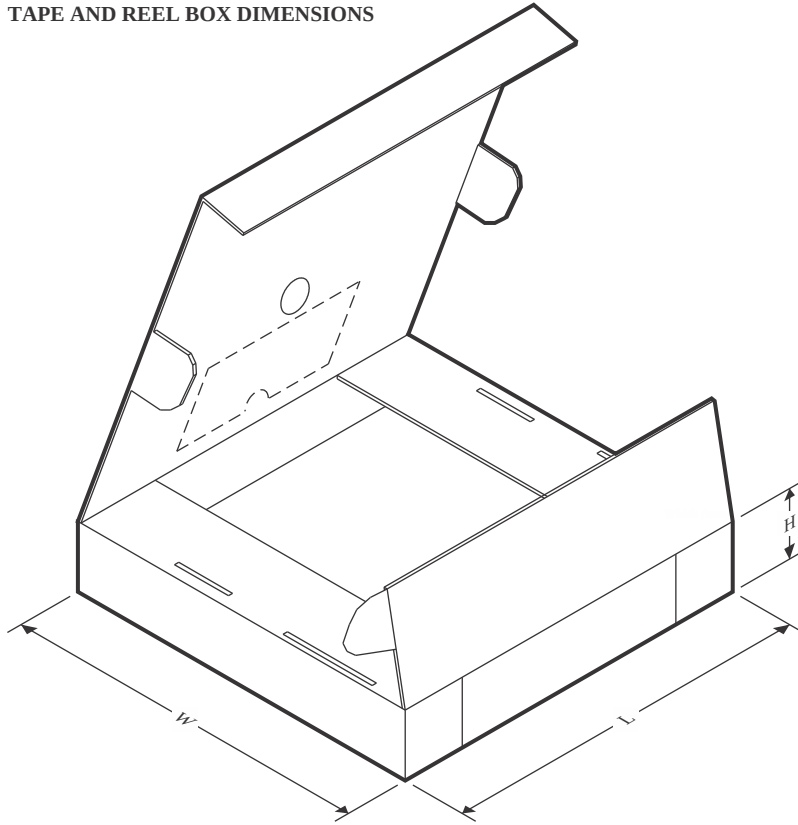
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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS6684QPHDRQ1	HTQFP	PHD	64	1000	330.0	24.4	17.0	17.0	1.5	20.0	24.0	Q2
TAS6684QPHDRQ1	HTQFP	PHD	64	1000	330.0	24.4	17.0	17.0	1.5	20.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS6684QPHDRQ1	HTQFP	PHD	64	1000	367.0	367.0	55.0
TAS6684QPHDRQ1	HTQFP	PHD	64	1000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

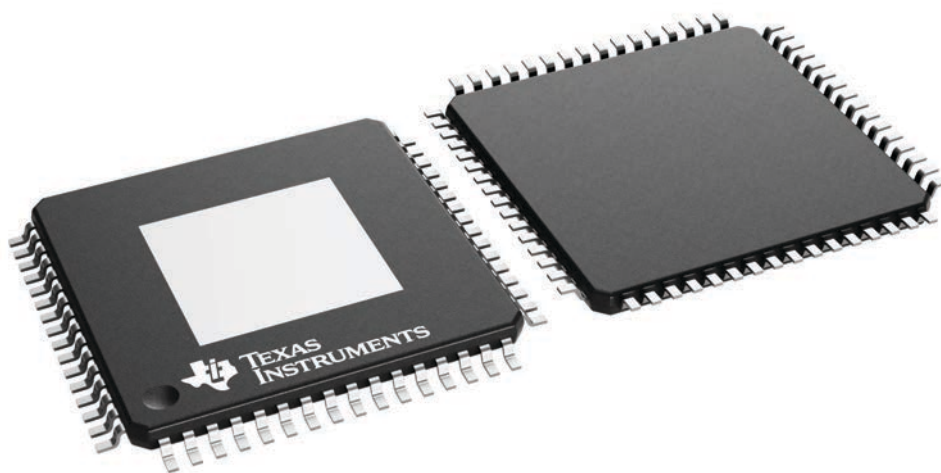
PHD 64

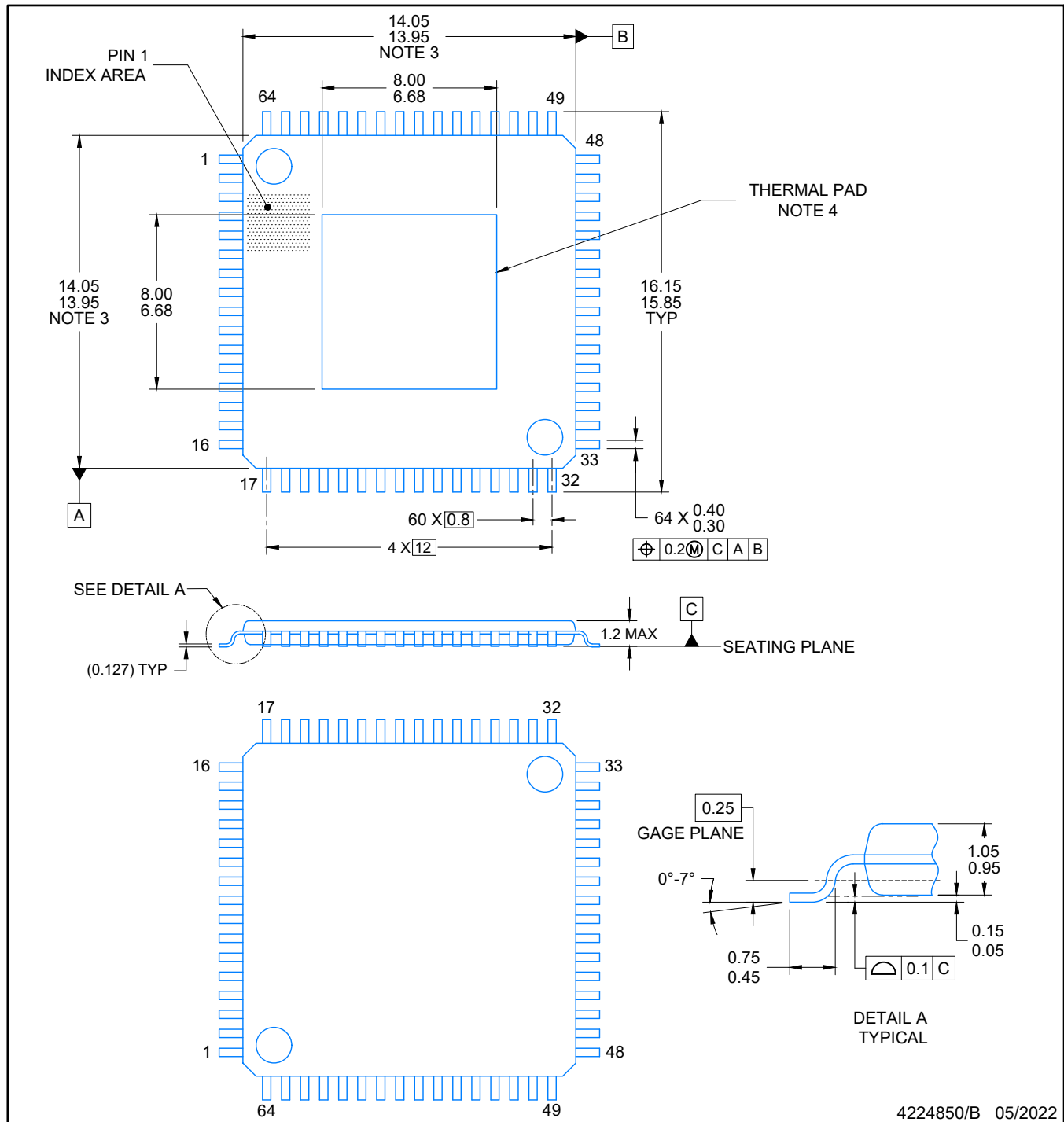
HTQFP - 1.2 mm max height

14 x 14, 0.8 mm pitch

PLASTIC QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.





4224850/B 05/2022

NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
- See technical brief. PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004) for information regarding recommended board layout.

HTQFP - 1.2 mm max height

SYMM
CL

64 49

64 X (1.5)

1

64 X (0.55)

60 X (0.8)

16

(R0.05) TYP

17 32

(15.4)

SYMM
CL

(15.4)

48 33

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 6X

0.05 MAX
ALL AROUND

METAL

EXPOSED METAL

SOLDER MASK OPENING

NON SOLDER MASK
DEFINED

0.05 MIN
ALL AROUND

EXPOSED METAL

SOLDER MASK OPENING

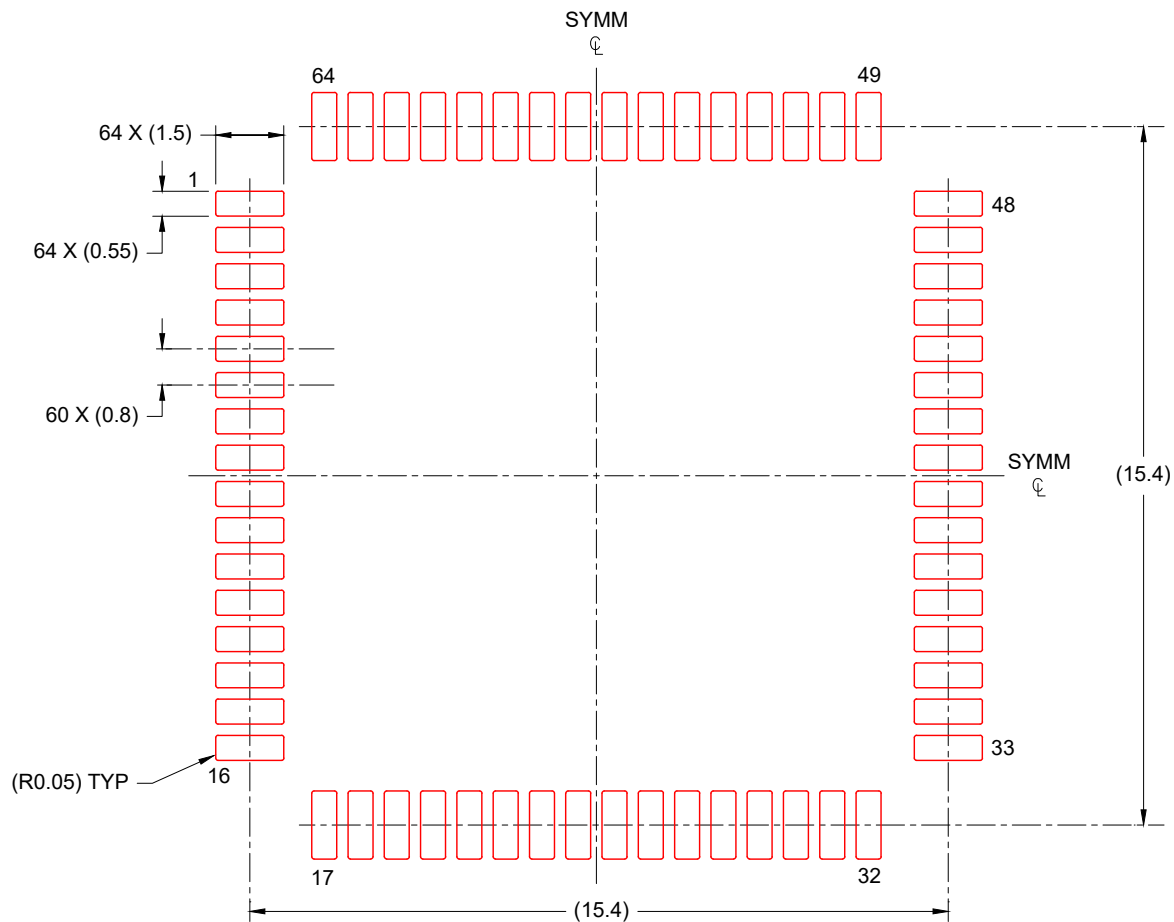
METAL UNDER
SOLDER MASK

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4224850/B 05/2022

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
SCALE: 6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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