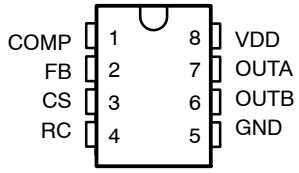
UCC2808A-1EP, UCC2808A-2EP
LOW POWER CURRENT MODE PUSH-PULL PWM

SGLS187B– SEPTEMBER 2003 – REVISED MARCH 2013

- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Extended Temperature Performance of –40°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree†**
- **Dual Output Drive Stages in Push-Pull Configuration**
- **Current Sense Discharge Transistor to Improve Dynamic Response**
- **130-μA Typical Starting Current**
- **1-mA Typical Run Current**
- **Operation to 1 MHz**
- **Internal Soft Start**
- **On-Chip Error Amplifier With 2-MHz Gain Bandwidth Product**
- **On Chip VDD Clamping**
- **Output Drive Stages Capable of 500-mA Peak-Source Current, 1-A Peak-Sink Current**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

D PACKAGE
(TOP VIEW)



description/ordering information

The UCC2808A is a family of BiCMOS push-pull, high-speed, low-power, pulse-width modulators. The UCC2808A contains all of the control and drive circuitry required for off-line or dc-to-dc fixed frequency current-mode switching power supplies with minimal external parts count.

The UCC2808A dual output drive stages are arranged in a push-pull configuration. Both outputs switch at half the oscillator frequency using a toggle flip-flop. The dead time between the two outputs is typically 60 ns to 200 ns depending on the values of the timing capacitor and resistors, thus limiting each output stage duty cycle to less than 50%.

The UCC2808A family offers a variety of package options and choice of undervoltage lockout levels. The family has UVLO thresholds and hysteresis options for off-line and battery powered systems. Thresholds are shown in the ordering information table.

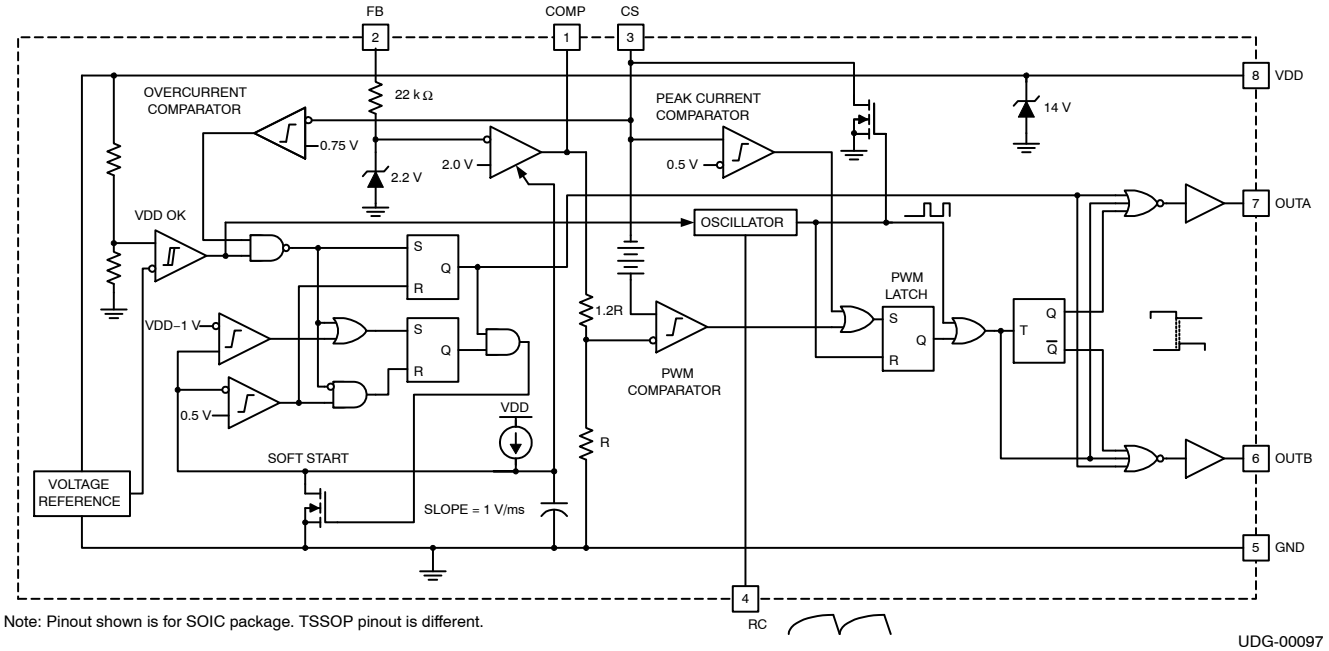
The UCC2808A is an enhanced version of the UCC2808 family. The significant difference is that the A versions feature an internal discharge transistor from the CS pin to ground, which is activated each clock cycle during the oscillator dead time. The feature discharges any filter capacitance on the CS pin during each cycle and helps minimize filter capacitor values and current sense delay.

ORDERING INFORMATION†

T_A	UVLO Option	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	12.5 V/8.3 V	SOIC (D)	Tape and reel	UCC2808AQDR–1EP	UCC2808
–40°C to 125°C	4.3 V/4.1 V	SOIC (D)	Tape and reel	UCC2808AQDR–2EP	UCC2808

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

block diagram



Note: Pinout shown is for SOIC package. TSSOP pinout is different.

UDG-00097

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†‡

Supply voltage (IDD ≤ 10 mA) . . . . . 15 V
Supply current . . . . . 20 mA
OUTA/OUTB source current (peak) . . . . . –0.5 A
OUTA/OUTB sink current (peak) . . . . . 1.0 A
Analog inputs (FB, CS) . . . . . –0.3 V to VDD 0.3 V, not to exceed 6 V
Power dissipation at T_A = 25°C (D package) . . . . . 650 mW
Storage temperature, T_{stg}§ . . . . . –65°C to150°C
Junction temperature, T_J . . . . . –55°C to 150°C
Lead temperature (soldering, 10 sec.) . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the *Power Supply Control Data Book (TI Literature Number SLUD003)* for thermal limitations and considerations of packages.

§ Long term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See http://www.ti.com/ep_quality for additional information on enhanced plastic packaging.

electrical characteristics, T_A = –40°C to 125°C for the UCC2808AQ-x, VDD = 10 V (see Note 6), 1-μF capacitor from VDD to GND, R = 22 kΩ, C = 330 pF $T_A = T_J$, (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Section					
Oscillator frequency		175	194	213	kHz
Oscillator amplitude/VDD	See Note 1	0.44	0.5	0.56	V/V

NOTES: 1. Measured at RC. Signal amplitude tracks VDD.
6. For UCCx808A–1, set VDD above the start threshold before setting at 10 V.

electrical characteristics, T_A = –40°C to 125°C for the UCC2808AQ-x, VDD = 10 V (see Note 6), 1-μF capacitor from VDD to GND, R = 22 kΩ, C = 330 pF $T_A = T_J$, (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNITS
Error Amplifier Section							
Input voltage	COMP = 2 V			1.95	2	2.05	V
Input bias current				–1		1	μA
Open loop voltage gain				60	80		dB
COMP sink current	FB = 2.2 V,	COMP = 1 V		0.3	2.5		mA
COMP source current	FB = 1.3 V,	COMP = 3.5 V		–0.2	–0.5		mA
PWM Section							
Maximum duty cycle	Measured at OUTA or OUTB			48	49	50	%
Minimum duty cycle	COMP = 0 V					0	%
Current Sense Section							
Gain	See Note 2			1.9	2.2	2.5	V/V
Maximum input signal	COMP = 5 V	See Note 3		0.45	0.5	0.55	V
CS to output delay	COMP = 3.5 V,	CS from 0 mV to 600 mV			100	200	ns
CS source current				–200			nA
CS sink current	CS = 0.5 V,	RC = 5.5 V	See Note 7	4	10		mA
Over current threshold				0.65	0.75	0.85	V
COMP to CS offset	CS = 0 V			0.35	0.8	1.2	V
Output Section							
OUT low level	I = 100 mA				0.5	1.1	V
OUT high level	I = –50 mA,	VDD – OUT			0.5	1	V
Rise time	C_L = 1 nF				25	60	ns
Fall time	C_L = 1 nF				25	60	ns
Undervoltage Lockout Section							
Start threshold	UCCx808A–1	See Note 6		11.5	12.5	13.5	V
	UCCx808A–2			4.1	4.3	4.5	V
Minimum operating voltage after start	UCCx808A–1			7.6	8.3	9	V
	UCCx808A–2			3.9	4.1	4.3	V
Hysteresis	UCCx808A–1			3.5	4.2	5.1	V
	UCCx808A–2			0.1	0.2	0.3	V
Soft Start Section							
COMP rise time	FB = 1.8 V,	Rise from 0.5 V to 4 V			3.5	20	ms
Overall Section							
Startup current	VDD < start threshold				130	260	μA
Operating supply current	FB = 0 V,	CS = 0 V	See Note 5 and 6		1	2	mA
VDD zener shunt voltage	IDD = 10 mA	See Note 4		13	14	15	V

NOTES: 2. Gain is defined by: $A = \frac{\Delta V_{COMP}}{\Delta V_{CS}}$, $0 \le V_{CS} \le 0.4$ V.

3. Parameter measured at trip point of latch with FB at 0 V.
4. Start threshold and zener shunt threshold track one another.
5. Does not include current in the external oscillator network.
6. For UCC2808A–1, set VDD above the start threshold before setting at 10 V.
7. The internal current sink on the CS pin is designed to discharge an external filter capacitor. It is not intended to be a dc sink path.

pin assignments

COMP: COMP is the output of the error amplifier and the input of the PWM comparator. The error amplifier in the UCC2808A is a true low-output impedance, 2-MHz operational amplifier. As such, the COMP pin can both source and sink current. However, the error amplifier is internally current limited, so that zero duty cycle can be externally forced by pulling COMP to GND.

The UCC2808A family features built-in full-cycle soft start. Soft start is implemented as a clamp on the maximum COMP voltage.

CS: The input to the PWM, peak current, and overcurrent comparators. The overcurrent comparator is only intended for fault sensing. Exceeding the overcurrent threshold will cause a soft start cycle. An internal MOSFET discharges the current sense filter capacitor to improve dynamic performance of the power converter.

FB: The inverting input to the error amplifier. For best stability, keep FB lead length as short as possible and FB stray capacitance as small as possible.

GND: Reference ground and power ground for all functions. Due to high currents, and high frequency operation of the UCC2808A, a low impedance circuit board ground plane is highly recommended.

OUTA and OUTB: Alternating high current output stages. Both stages are capable of driving the gate of a power MOSFET. Each stage is capable of 500-mA peak-source current, and 1-A peak-sink current.

The output stages switch at half the oscillator frequency, in a push-pull configuration. When the voltage on the RC pin is rising, one of the two outputs is high, but during fall time, both outputs are off. This *dead time* between the two outputs, along with a slower output rise time than fall time, insures that the two outputs can not be on at the same time. This dead time is typically 60 ns to 200 ns and depends upon the values of the timing capacitor and resistor.

The high-current-output drivers consist of MOSFET output devices, which switch from VDD to GND. Each output stage also provides a very low impedance to overshoot and undershoot. This means that in many cases, external-schottky-clamp diodes are not required.

RC: The oscillator programming pin. The UCC2808A's oscillator tracks VDD and GND internally, so that variations in power supply rails minimally affect frequency stability. Figure 1 shows the oscillator block diagram.

Only two components are required to program the oscillator: a resistor (tied to the VDD and RC), and a capacitor (tied to the RC and GND). The approximate oscillator frequency is determined by the simple formula:

$$f_{OSCILLATOR} = \frac{1.41}{RC}$$

where frequency is in Hz, resistance in Ohms, and capacitance in Farads. The recommended range of timing resistors is between 10 kΩ and 200 kΩ and range of timing capacitors is between 100 pF and 1000 pF. Timing resistors less than 10 kΩ should be avoided.

For best performance, keep the timing capacitor lead to GND as short as possible, the timing resistor lead from VDD as short as possible, and the leads between timing components and RC as short as possible. Separate ground and VDD traces to the external timing network are encouraged.

pin assignments (continued)

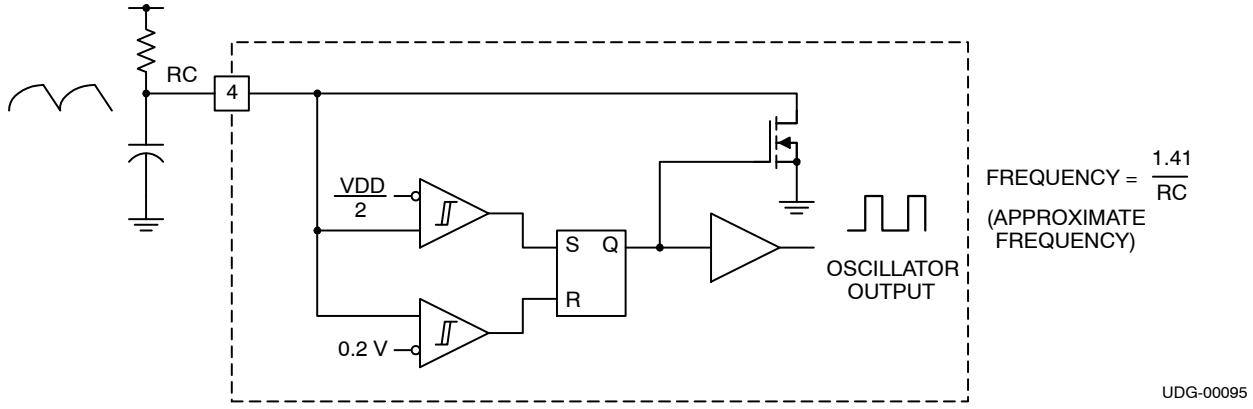


Figure 1. Block Diagram for Oscillator

NOTE A: The oscillator generates a sawtooth waveform on RC. During the RC rise time, the output stages alternate on time, but both stages are off during the RC fall time. The output stages switch a 1/2 the oscillator frequency, with ensured duty cycle of < 50% for both outputs.

VDD: The power input connection for this device. Although quiescent VDD current is very low, total supply current will be higher, depending on OUTA and OUTB current, and the programmed oscillator frequency. Total VDD current is the sum of quiescent VDD current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Qg), average OUT current can be calculated from:

$$I_{OUT} = Q_g \times F, \text{ where F is frequency}$$

To prevent noise problems, bypass VDD to GND with a ceramic capacitor as close to the chip as possible along with an electrolytic capacitor. A 1-μF decoupling capacitor is recommended.

APPLICATION INFORMATION

A 200-kHz push-pull application circuit with a full-wave rectifier is shown in Figure 2. The output, V_O, provides 5 V at 50 W maximum and is electrically isolated from the input. Since the UCC2808A is a peak-current-mode controller the 2N2907 emitter following amplifier (buffers the CT waveform) provides slope compensation which is necessary for duty ratios greater than 50%. Capacitor decoupling is very important with a single ground IC controller, and a 1 μF is suggested as close to the IC as possible. The controller supply is a series RC for start-up, paralleled with a bias winding on the output inductor used in steady state operation.

Isolation is provided by an optocoupler with regulation done on the secondary side using the TL431 adjustable precision shunt regulator. Small signal compensation with tight voltage regulation is achieved using this part on the secondary side. Many choices exist for the output inductor depending on cost, volume, and mechanicall strength. Several design options are iron powder, molypermalloy (MPP), or a ferrite core with an air gap as shown here. The main power transformer has a Magnetics Inc. ER28 size core made of P material for efficient operation at this frequency and temperature. The input voltage may range from 36 V dc to 72 V dc.

APPLICATION INFORMATION

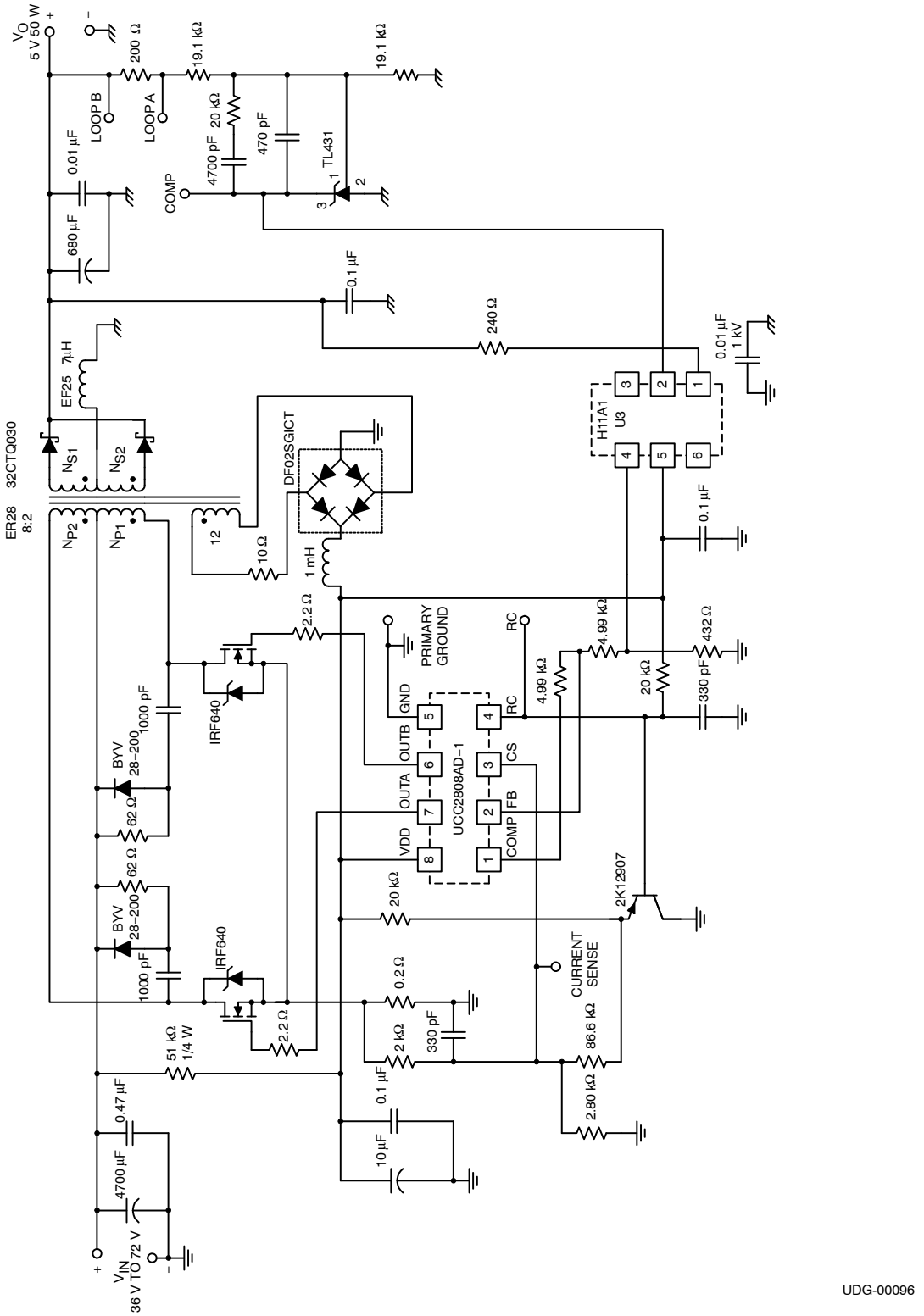


Figure 2. Typical Application Diagram: 48-V In, 5-V, 50-W Output

TYPICAL CHARACTERISTICS

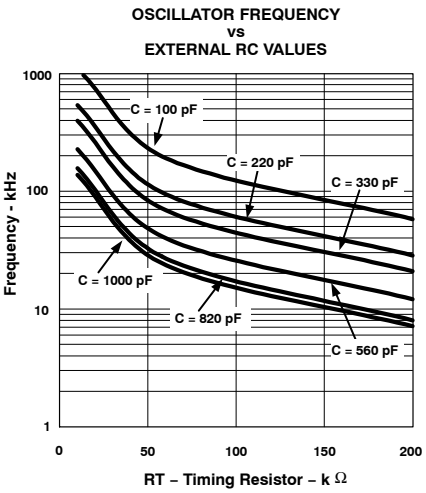


Figure 3

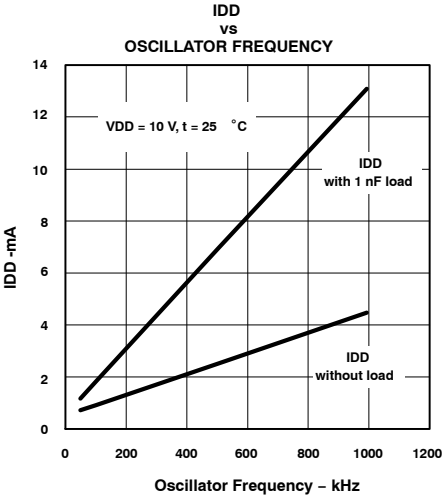


Figure 4

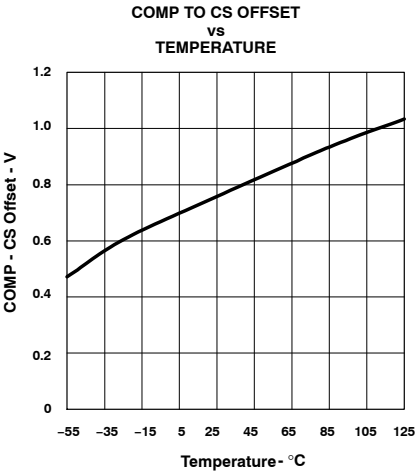


Figure 5

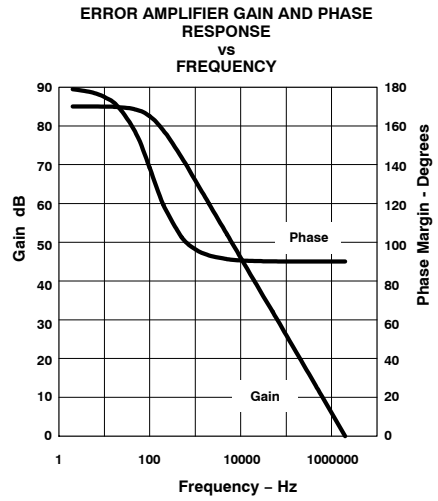


Figure 6

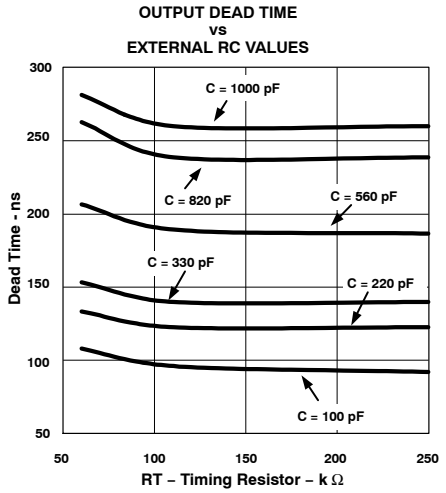


Figure 7

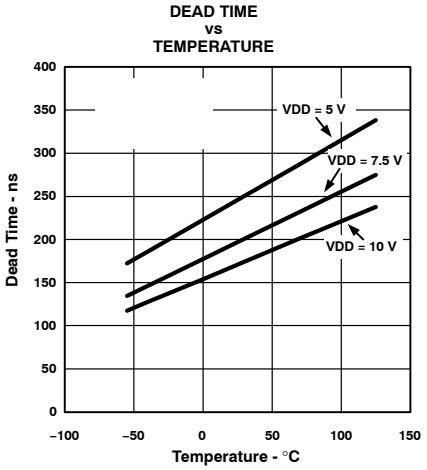


Figure 8

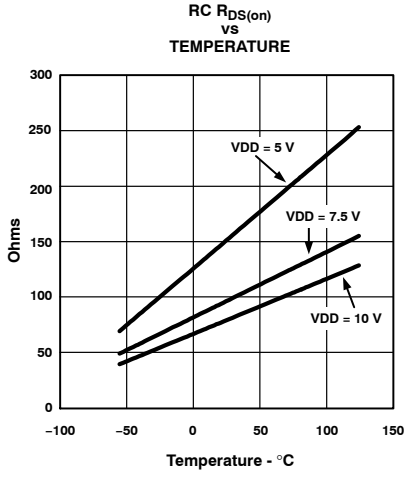


Figure 9

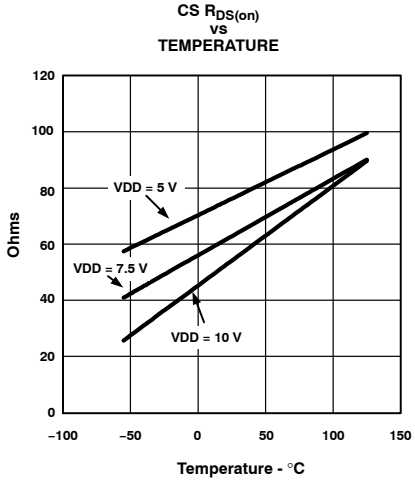


Figure 10

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC2808AQDR-1EP	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI | Nipdau	Level-1-260C-UNLIM	-40 to 125	UCC2808 A-1EP
UCC2808AQDR-1EP.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC2808 A-1EP
UCC2808AQDR-2EP	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI | Nipdau	Level-1-260C-UNLIM	-40 to 125	UCC2808 A-2EP
UCC2808AQDR-2EP.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC2808 A-2EP
V62/04642-01XE	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC2808 A-1EP
V62/04642-02XE	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC2808 A-2EP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

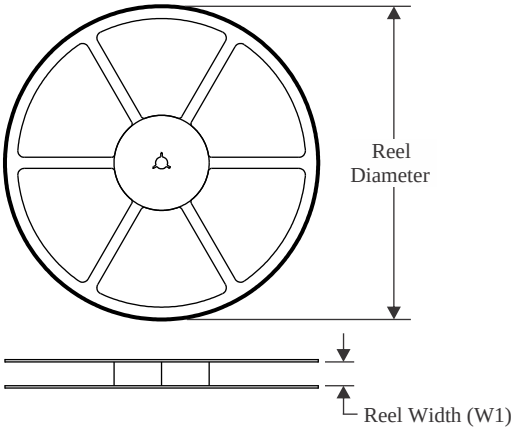
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

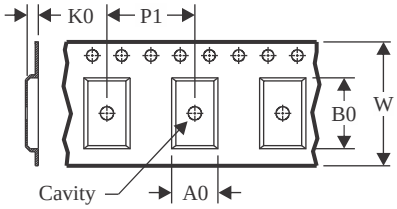
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

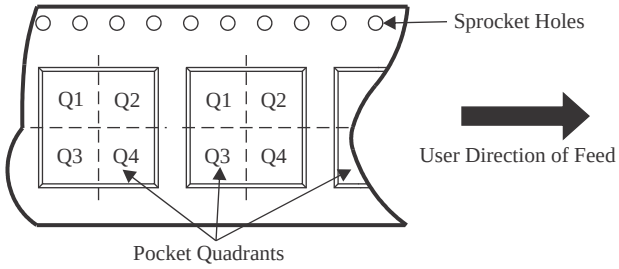


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

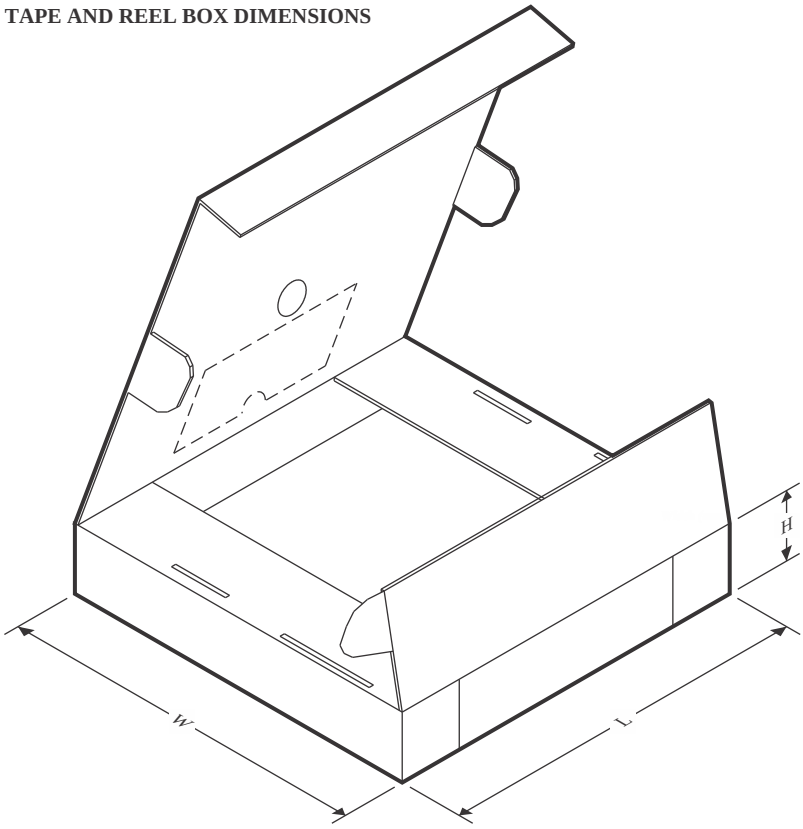
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC2808AQDR-1EP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2808AQDR-2EP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC2808AQDR-1EP	SOIC	D	8	2500	356.0	356.0	35.0
UCC2808AQDR-2EP	SOIC	D	8	2500	356.0	356.0	35.0

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