TLC592x 16-Channel Constant-Current LED Sink Drivers

1 Features

- 16 Constant-Current Output Channels
- Output Current Adjusted By External Resistor
- Constant Output Current Range: 5 mA to 120 mA
- Constant Output Current Invariant to Load Voltage Change
- Open-Load and Shorted-Load Detection
- 256-Step Programmable Global Current Gain
- Excellent Output Current Accuracy:
  - Between Channels: < ±6% (Max), 10 mA to 50 mA
  - Between ICs: < ±6% (Max), 10 mA to 50 mA
- 30-MHz Maximum Clock Frequency
- Schmitt-Trigger Input
- 3.3-V or 5-V Supply Voltage
- Thermal Shutdown for Overtemperature Protection

2 Applications

- General LED Lighting Applications
- LED Display Systems
- LED Signage
- Automotive LED Lighting
- White Goods

3 Description

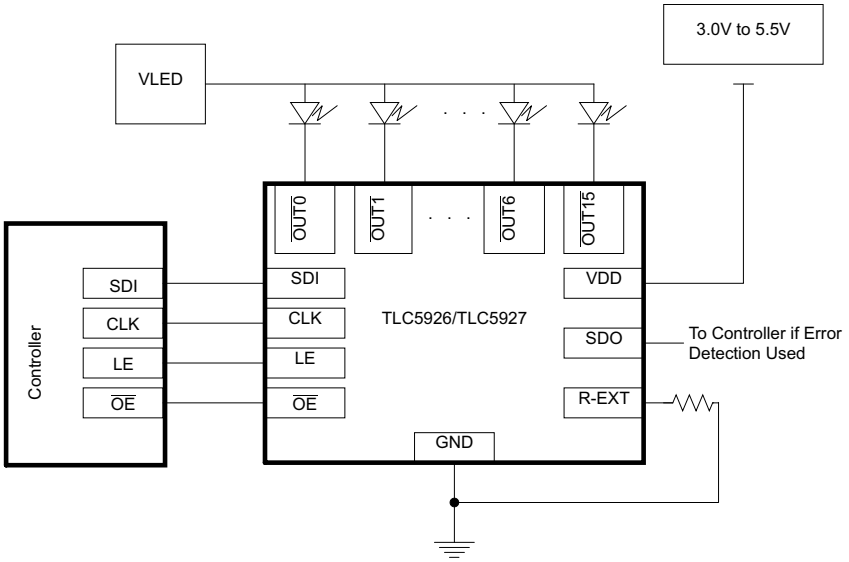
The TLC592x is designed for LED displays and LED lighting applications with open-load, shorted-load, and over temperature detection, and constant-current control. The TLC592x contains a 16-bit shift register and data latches, which convert serial input data into parallel output format. At the TLC592x output stage, 16 regulated-current ports provide uniform and constant current for driving LEDs within a wide range of V_F (forward voltage) variations. Used in systems designed for LED display applications (for example, LED panels), TLC592x provides great flexibility and device performance. Users can adjust the output current from 5 mA to 120 mA through an external resistor, R_{ext}, which gives flexibility in controlling the light intensity of LEDs. The TLC592x is designed for up to 17 V at the output port. The high clock frequency, 30 MHz, also satisfies the system requirements of high-volume data transmission.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLC5926	SSOP (24)	8.65 mm × 3.90 mm
	SOIC (24)	15.40 mm × 7.50 mm
	HTSSOP (24)	7.80 mm × 4.40 mm
TLC5927	SSOP (24)	8.65 mm × 3.90 mm
	SOIC (24)	15.40 mm × 7.50 mm
	HTSSOP (24)	7.80 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Single Implementation of TLC592x Device



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (October 2014) to Revision C	Page
• Updated Default Relationship Curve graphic.	19

Changes from Revision A (June 2009) to Revision B	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

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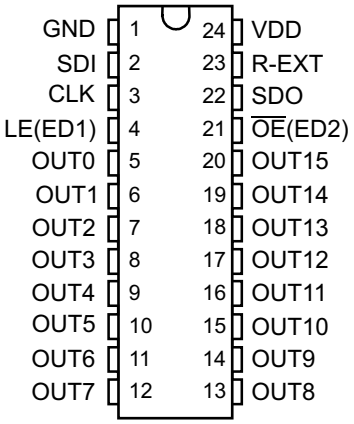
5 Device Comparison Table

DEVICE (1)	OPEN-LOAD DETECTION	SHORT TO GND DETECTION	SHORT TO V_{LED} DETECTION
TLC5926	x	x	
TLC5927	x	x	x

(1) The device has one single error register for all these conditions (one error bit per channe.l)

6 Pin Configuration and Functions

DBQ, DW, or PWP Package
24-PIN SSOP, SOIC, HTSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CLK	3	I	Clock input pin for data shift on rising edge
GND	1	—	Ground pin for control logic and current sink
LE(ED1)	4	I	Data strobe input pn Serial data is transferred to the respective latch when LE(ED1) is high. The data is latched when LE(ED1) goes low. Also, a control signal input for an Error Detection mode and Current Adjust mode. LE(ED1) has an internal pulldown.
$\overline{OE}$(ED2)	21	I	Output enable pin. When $\overline{OE}$ (ED2)(active) is low, the output drivers are enabled; when $\overline{OE}$(ED2) is high, all output drivers are turned OFF (blanked). Also, a control signal input for an Error Detection mode and Current Adjust mode). $\overline{OE}$(ED2) has an internal pullup.
OUT0–OUT15	5-20	O	Constant-current output pins
R-EXT	23	I	Input pin used to connect an external resistor for setting up all output currents
SDI	2	I	Serial-data input to the Shift register
SDO	22	O	Serial-data output to the following SDI of next driver IC or to the microcontroller
VDD	24	I	Supply voltage pin
Thermal Pad	-	-	Thermal pad (exposed center pad) to alleviate thermal stress. Tie to GND. See Layout Guidelines for more information. (PWP package only)

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{DD}	Supply voltage	0	7	V
V_I	Input voltage	–0.4	V_{DD} + 0.4	V
V_O	Output voltage	–0.5	20	V
I_{OUT}	Output current		120	mA
I_{GND}	GND terminal current		1920	mA
T_A	Free-air operating temperature range	–40	125	°C
T_J	Operating junction temperature range	–40	150	°C
T_{stg}	Storage temperature range	–55	150	°C

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		TEST CONDITIONS		MIN	MAX	UNIT
V_{DD}	Supply voltage			3	5.5	V
V_O	Supply voltage to the output pins	OUT0–OUT15			17	V
I_O	Output current	DC test circuit	$V_O \geq 0.6$ V	5		mA
			$V_O \geq 1$ V		120	
I_{OH}	High-level output current	SDO			–1	mA
I_{OL}	Low-level output current	SDO			1	mA
V_{IH}	High-level input voltage	CLK, $\overline{OE}$(ED2), LE(ED1), and SDI		0.7 × V_{DD}	V_{DD}	V
V_{IL}	Low-level input voltage	CLK, $\overline{OE}$(ED2), LE(ED1), and SDI		0	0.3 × V_{DD}	V

7.4 Thermal Information

THERMAL METRIC (1)		TLC5926, TLC5927			UNIT
		DBQ (SSOP)	DW (SOIC)	PWP (HTSSOP)	
		24 PINS	24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance (Mounted on JEDEC 1-layer board (JESD 51-3), No airflow)	99.8	80.5	63.9	°C/W
	Junction-to-ambient thermal resistance (Mounted on JEDEC 4-layer board (JESD 51-7), No airflow)	61	45.5	42.7	°C/W
	Junction-to-ambient thermal resistance (Mounted on JEDEC 4-layer board (JESD 51-5), No airflow)	-	-	34.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	49.6	40.8	23.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	38	40.5	21.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.5	18	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.7	40.2	21.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	-	5.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics: V_{DD} = 3 V

V_{DD} = 3 V, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Supply voltage to the output pins					17	V
I_O	Output current	V_O ≥ 0.6 V		5			mA
		V_O ≥ 1 V				120	
V_{IH}	High-level input voltage			0.7 × V_{DD}		V_{DD}	V
V_{IL}	Low-level input voltage			GND		0.3 × V_{DD}	
I_{leak}	Output leakage current	V_{OH} = 17 V	T_J = 25°C			0.5	µA
			T_J = 125°C			1	
V_{OH}	High-level output voltage	SDO, I_{OL} = –1 mA		V_{DD} – 0.4			V
V_{OL}	Low-level output voltage	SDO, I_{OH} = 1 mA				0.4	V
$I_{O(1)}$	Output current 1	V_{OUT} = 0.6 V, R_{ext} = 720 Ω, CG = 0.992			26		mA
	Output current error, die-die	I_{OL} = 26 mA, V_O = 0.6 V, R_{ext} = 720 Ω, T_J = 25°C				±6%	
	Output current error, channel-to-channel	I_{OL} = 26 mA, V_O = 0.6 V, R_{ext} = 720 Ω, T_J = 25°C				±6%	
$I_{O(2)}$	Output current 2	V_O = 0.8 V, R_{ext} = 360 Ω, CG = 0.992			52		mA
	Output current error, die-die	I_{OL} = 52 mA, V_O = 0.8 V, R_{ext} = 360 Ω, T_J = 25°C				±6%	
	Output current error, channel-to-channel	I_{OL} = 52 mA, V_O = 0.8 V, R_{ext} = 360 Ω, T_J = 25°C				±6%	
I_{OUT} vs V_{OUT}	Output current vs output voltage regulation	V_O = 1 V to 3 V, I_O = 26 mA			±0.1		%/V
I_{OUT} vs V_{DD}	Output current vs supply voltage	V_{DD} = 3.0 V to 5.5 V, I_O = 26 mA/120 mA			±1		
	Pullup resistance	$\overline{OE}$(ED2)		250	500	800	kΩ
	Pulldown resistance	LE(ED1)		250	500	800	kΩ
T_{sd}	Overtemperature shutdown(1)			150	175	200	°C
T_{hys}	Restart temperature hysteresis				15		°C
$I_{OUT,Th}$	Threshold current for open error detection	$I_{OUT,target}$ = 5 mA to 120 mA			0.5% × I_{target}		
$V_{OUT,TTh}$	Trigger threshold voltage for short-error detection (TLC5927 only)	$I_{OUT,target}$ = 5 mA to 120 mA		2.4	2.6	3.1	V
$V_{OUT,\ RTh}$	Return threshold voltage for short-error detection (TLC5927 only)	$I_{OUT,target}$ = 5 mA to 120 mA		2.2			V
I_{DD}	Supply current	OUT0–OUT15 = off, R_{ext} = Open, $\overline{OE}$ = V_{IH}				10	mA
		OUT0–OUT15 = off, R_{ext} = 720 Ω, $\overline{OE}$ = V_{IH}				14	
		OUT0–OUT15 = off, R_{ext} = 360 Ω, $\overline{OE}$ = V_{IH}				18	
		OUT0–OUT15 = off, R_{ext} = 180 Ω, $\overline{OE}$ = V_{IH}				20	
		OUT0–OUT15 = on, R_{ext} = 720 Ω, $\overline{OE}$ = V_{IL}				14	
		OUT0–OUT15 = on, R_{ext} = 360 Ω, $\overline{OE}$ = V_{IL}				18	
		OUT0–OUT15 = on, R_{ext} = 180 Ω, $\overline{OE}$ = V_{IL}				20	

(1) Specified by design

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7.6 Electrical Characteristics: V_{DD} = 5.5 V

V_{DD} = 5.5 V, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Supply voltage to the output pins					17	V
I_O	Output current	V_O ≥ 0.6 V		5			mA
		V_O ≥ 1 V				120	
V_{IH}	High-level input voltage			0.7 × V_{DD}		V_{DD}	V
V_{IL}	Low-level input voltage			GND		03 × V_{DD}	
I_{leak}	Output leakage current	V_{OH} = 17 V	T_J = 25°C			0.5	µA
			T_J = 125°C			1	
V_{OH}	High-level output voltage	SDO, I_{OL} = –1 mA		V_{DD} – 0.4			V
V_{OL}	Low-level output voltage	SDO, I_{OH} = 1 mA				0.4	V
$I_{O(1)}$	Output current 1	V_{OUT} = 0.6 V, R_{ext} = 720 Ω, CG = 0.992			26		mA
	Output current error, die-die	I_{OL} = 26 mA, V_O = 0.6 V, R_{ext} = 720 Ω, T_J = 25°C				±6%	
	Output current error, channel-to-channel	I_{OL} = 26 mA, V_O = 0.6 V, R_{ext} = 720 Ω, T_J = 25°C				±6%	
$I_{O(2)}$	Output current 2	V_O = 0.8 V, R_{ext} = 360 Ω, CG = 0.992			52		mA
	Output current error, die-die	I_{OL} = 52 mA, V_O = 0.8 V, R_{ext} = 360 Ω, T_J = 25°C				±6%	
	Output current error, channel-to-channel	I_{OL} = 52 mA, V_O = 0.8 V, R_{ext} = 360 Ω, T_J = 25°C				±6%	
I_{OUT} vs V_{OUT}	Output current vs output voltage regulation	V_O = 1 V to 3 V , I_O = 26 mA			±0.1		%/V
I_{OUT} vs V_{DD}	Output current vs supply voltage	V_{DD} = 3.0 V to 5.5 V, I_O = 26 mA/120 mA			±1		
	Pullup resistance	$\overline{OE}$(ED2),		250	500	800	kΩ
	Pulldown resistance	LE(ED1),		250	500	800	kΩ
T_{sd}	Over temperature shutdown(1)			150	175	200	°C
T_{hys}	Restart temperature hysteresis				15		°C
$I_{OUT,Th}$	Threshold current for open error detection	$I_{OUT,target}$ = 5 mA to 120 mA			0.5% × I_{target}		
$V_{OUT,TTh}$	Trigger threshold voltage for short-error detection (TLC5927 only)	$I_{OUT,target}$ = 5 mA to 120 mA		2.4	2.6	3.1	V
$V_{OUT,\ RTh}$	Return threshold voltage for short-error detection (TLC5927 only)	$I_{OUT,target}$ = 5 mA to 120 mA		2.2			V
I_{DD}	Supply current	OUT0–OUT15 = off, R_{ext} = Open, $\overline{OE}$ = V_{IH}				11	mA
		OUT0–OUT15 = off, R_{ext} = 720 Ω, $\overline{OE}$ = V_{IH}				17	
		OUT0–OUT15 = off, R_{ext} = 360 Ω, $\overline{OE}$ = V_{IH}				18	
		OUT0–OUT15 = off, R_{ext} = 180 Ω, $\overline{OE}$ = V_{IH}				25	
		OUT0–OUT15 = on, R_{ext} = 720 Ω, $\overline{OE}$ = V_{IL}				17	
		OUT0–OUT15 = on, R_{ext} = 360 Ω, $\overline{OE}$ = V_{IL}				18	
		OUT0–OUT15 = on, R_{ext} = 180 Ω, $\overline{OE}$ = V_{IL}				25	

(1) Specified by design

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7.7 Timing Recommendations

V_{DD} = 3 V to 5.5 V (unless otherwise noted)

			MIN	MAX	UNIT
$t_{w(L)}$	LE(ED1) pulse duration	Normal mode	20		ns
$t_{w(CLK)}$	CLK pulse duration	Normal mode	20		ns
$t_{w(OE)}$	$\overline{OE}$(ED2) pulse duration	Normal mode	1000		ns
$t_{su(D)}$	Setup time for SDI	Normal mode	7		ns
$t_{h(D)}$	Hold time for SDI	Normal mode	3		ns
$t_{su(L)}$	Setup time for LE(ED1)	Normal mode	18		ns
$t_{h(L)}$	Hold time for LE(ED1)	Normal mode	18		ns
$t_{w(CLK)}$	CLK pulse duration	Error Detection mode	20		ns
$t_{w(ED2)}$	$\overline{OE}$(ED2) pulse duration	Error Detection mode	2000		ns
$t_{su(ED1)}$	Setup time for LE(ED1)	Error Detection mode	7		ns
$t_{h(ED1)}$	Hold time for LE(ED1)	Error Detection mode	10		ns
$t_{su(ED2)}$	Setup time for $\overline{OE}$(ED2)	Error Detection mode	7		ns
$t_{h(ED2)}$	Hold time for $\overline{OE}$(ED2)	Error Detection mode	10		ns
f_{CLK}	Clock frequency	Cascade operation, V_{DD} = 3 V to 5.5 V		30	MHz

7.8 Switching Characteristics: V_{DD} = 3 V

V_{DD} = 3 V, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH1}	Low-to-high propagation delay time, CLK to OUTn	$V_{IH} = V_{DD}$, V_{IL} = GND, R_{ext} = 360 Ω, V_L = 4 V, R_L = 44 Ω, C_L = 70 pF, CG = 0.992	35	65	105	ns
t_{PLH2}	Low-to-high propagation delay time, LE(ED1) to OUTn		35	65	105	ns
t_{PLH3}	Low-to-high propagation delay time, $\overline{OE}$(ED2) to OUTn		35	65	105	ns
t_{PLH4}	Low-to-high propagation delay time, CLK to SDO			20	45	ns
t_{PHL1}	High-to-low propagation delay time, CLK to OUTn		200	300	470	ns
t_{PHL2}	High-to-low propagation delay time, LE(ED1) to OUTn		200	300	470	ns
t_{PHL3}	High-to-low propagation delay time, $\overline{OE}$(ED2) to OUTn		200	300	470	ns
t_{PHL4}	High-to-low propagation delay time, CLK to SDO			20	40	ns
$t_{w(CLK)}$	Pulse duration, CLK		20			ns
$t_{w(L)}$	Pulse duration LE(ED1)		20			ns
$t_{w(OE)}$	Pulse duration, $\overline{OE}$(ED2)		1000			ns
$t_{w(ED2)}$	Pulse duration, $\overline{OE}$(ED2) in Error Detection mode		2			µs
$t_{h(ED1,ED2)}$	Hold time, LE(ED1), and $\overline{OE}$(ED2)		10			ns
$t_{h(D)}$	Hold time, SDI		5			ns
$t_{su(D,ED1,ED2)}$	Setup time, SDI, LE(ED1), and $\overline{OE}$(ED2)		7			ns
$t_{h(L)}$	Hold time, LE(ED1), Normal mode		18			ns
$t_{su(L)}$	Setup time, LE(ED1), Normal mode		18			ns
t_r	Rise time, CLK (1)				500	ns
t_f	Fall time, CLK (1)				500	ns
t_{or}	Rise time, outputs (off)				245	ns
t_{of}	Rise time, outputs (on)				600	ns
f_{CLK}	Clock frequency	Cascade operation			30	MHz

(1) If the devices are connected in cascade and t_r or t_f is large, it may be critical to achieve the timing required for data transfer between two cascaded devices.

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7.9 Switching Characteristics: V_{DD} = 5.5 V

V_{DD} = 5.5 V, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH1}	Low-to-high propagation delay time, CLK to OUTn	$V_{IH} = V_{DD}$, V_{IL} = GND, R_{ext} = 360 Ω, V_L = 4 V, R_L = 44 Ω, C_L = 70 pF, CG = 0.992	27	65	95	ns
t_{PLH2}	Low-to-high propagation delay time, LE(ED1) to OUTn		27	65	95	ns
t_{PLH3}	Low-to-high propagation delay time, $\overline{OE}$(ED2) to OUTn		27	65	95	ns
t_{PLH4}	Low-to-high propagation delay time, CLK to SDO			20	30	ns
t_{PHL1}	High-to-low propagation delay time, CLK to OUTn		180	300	445	ns
t_{PHL2}	High-to-low propagation delay time, LE(ED1) to OUTn		180	300	445	ns
t_{PHL3}	High-to-low propagation delay time, $\overline{OE}$(ED2) to OUTn		180	300	445	ns
t_{PHL4}	High-to-low propagation delay time, CLK to SDO			20	30	ns
$t_{w(CLK)}$	Pulse duration, CLK		20			ns
$t_{w(L)}$	Pulse duration LE(ED1)		20			ns
$t_{w(OE)}$	Pulse duration, $\overline{OE}$(ED2)		1000			ns
$t_{w(ED2)}$	Pulse duration, $\overline{OE}$(ED2) in Error Detection mode		2			µs
$t_{h(ED1,ED2)}$	Hold time, LE(ED1), and $\overline{OE}$(ED2)		10			ns
$t_{h(D)}$	Hold time, SDI		3			ns
$t_{su(D,ED1,ED2)}$	Setup time, SDI, LE(ED1), and $\overline{OE}$(ED2)		4			ns
$t_{h(L)}$	Hold time, LE(ED1), Normal mode		15			ns
$t_{su(L)}$	Setup time, LE(ED1), Normal mode		15			ns
t_r	Rise time, CLK (1)				500	ns
t_f	Fall time, CLK (1)				500	ns
t_{or}	Rise time, outputs (off)				245	ns
t_{of}	Rise time, outputs (on)				570	ns
f_{CLK}	Clock frequency	Cascade operation			30	MHz

(1) If the devices are connected in cascade and t_r or t_f is large, it may be critical to achieve the timing required for data transfer between two cascaded devices.

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7.10 Typical Characteristics

Figure 1: At low voltage levels (V_O), the output current (I_O) may be limited. Figure 1 shows the dependency of the output current on the output voltage.

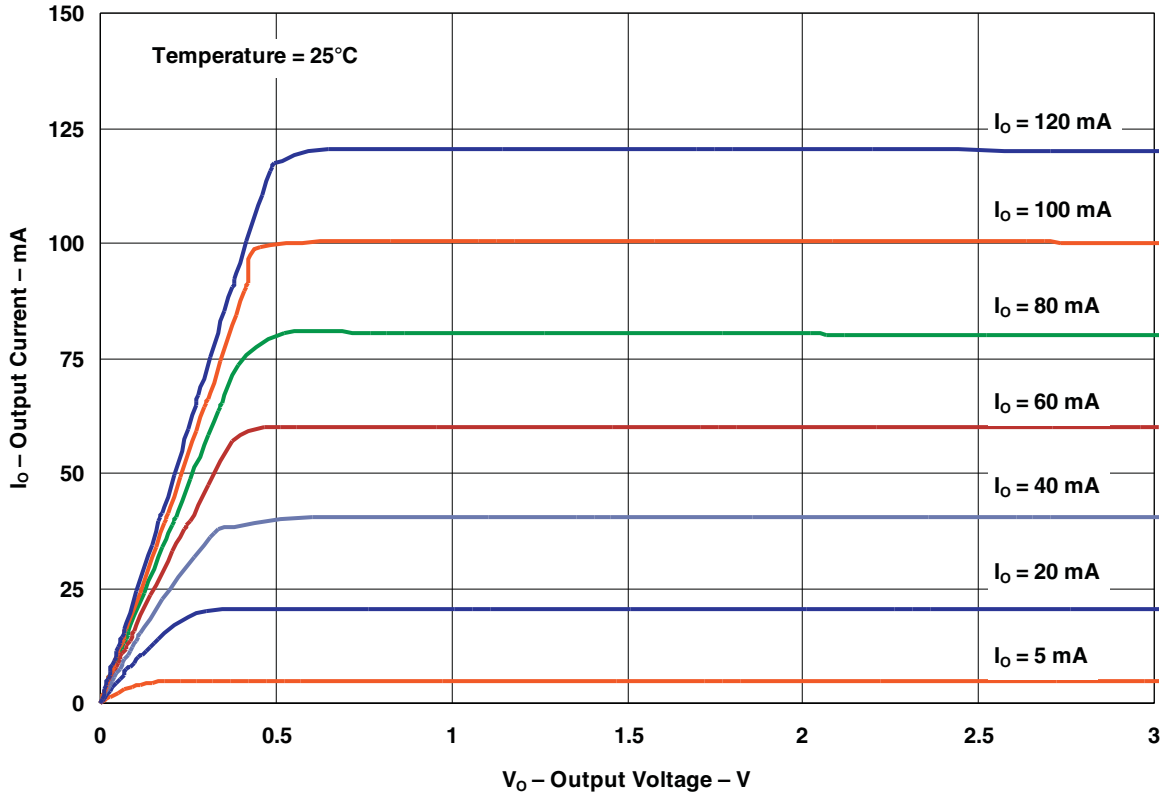

Figure 1. Output Current vs Output Voltage

8 Parameter Measurement Information

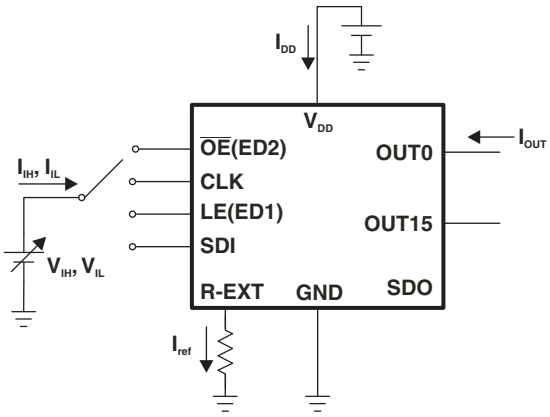

Figure 2. Test Circuit for Electrical Characteristics

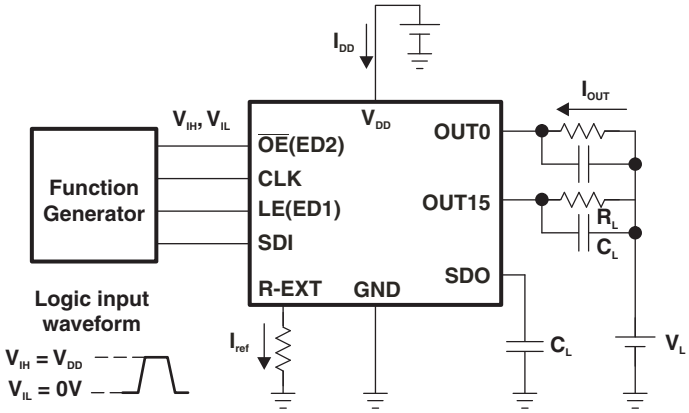

Figure 3. Test Circuit for Switching Characteristics

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Parameter Measurement Information (continued)

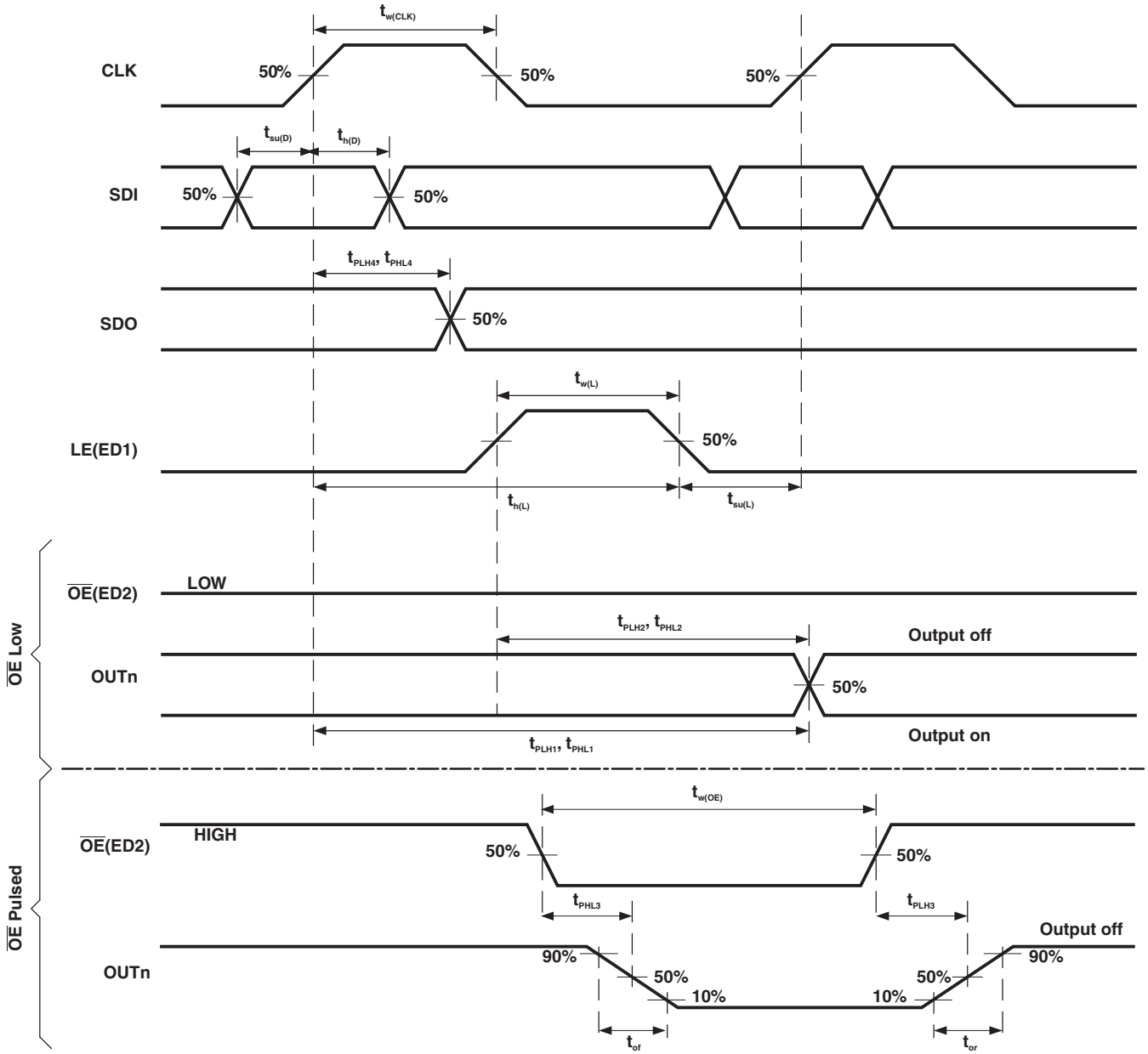

Figure 4. Normal Mode Timing Waveforms

Parameter Measurement Information (continued)

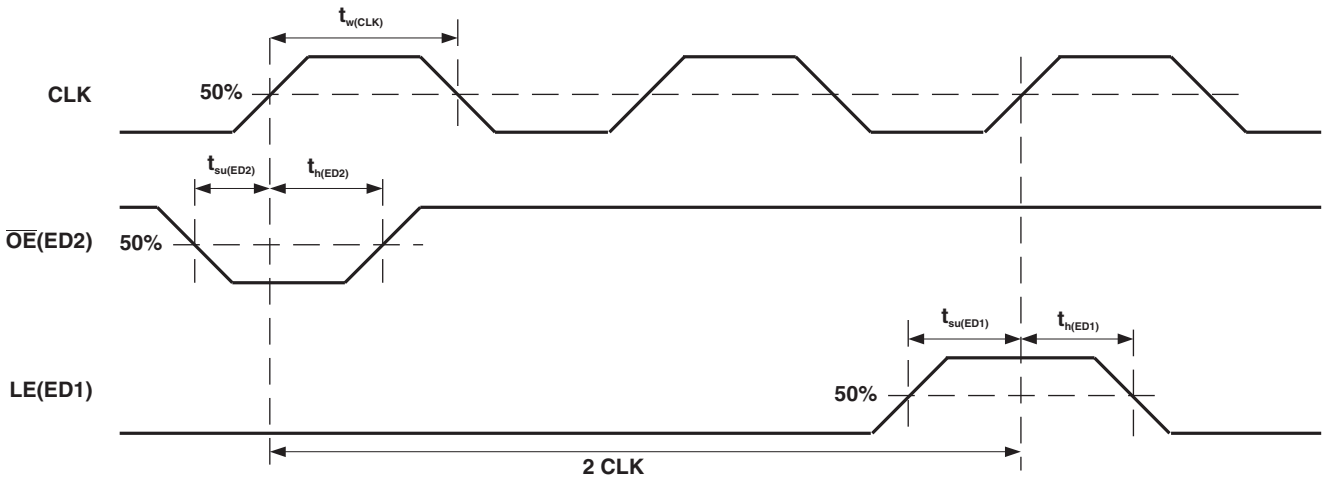

Figure 5. Switching to Special Mode Timing Waveforms

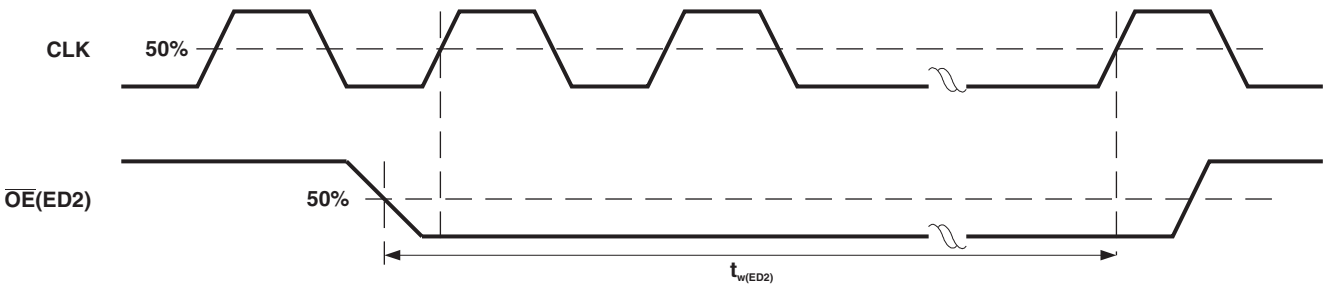

Figure 6. Reading Error Status Code Timing Waveforms

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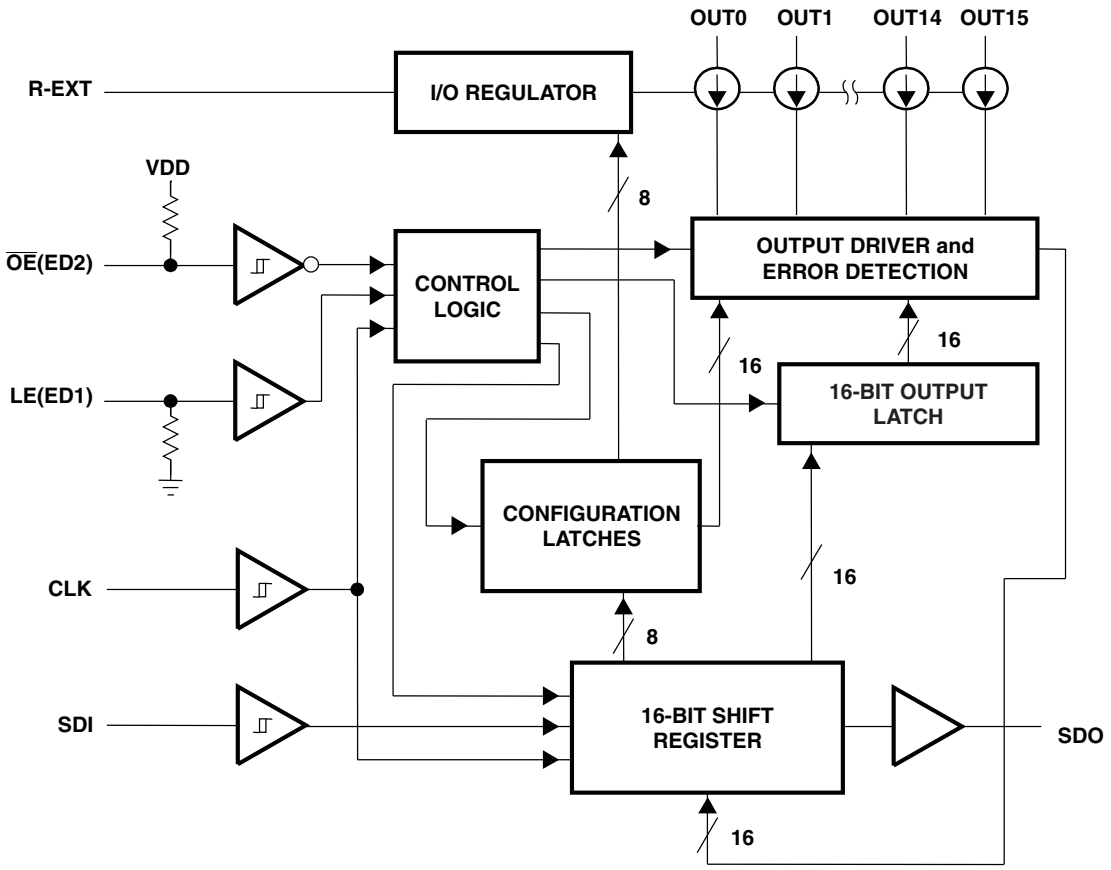
9 Detailed Description

9.1 Overview

The TLC592x is designed for LED displays and LED lighting applications with open-load, shorted-load, and overtemperature detection, and constant-current control. The TLC592x contains a 16-bit shift register and data latches, which convert serial input data into parallel output format. At the TLC592x output stage, 16 regulated-current ports provide uniform and constant current for driving LEDs within a wide range of VF (Forward Voltage) variations. Used in systems designed for LED display applications (e.g., LED panels), TLC592x provides great flexibility and device performance. Users can adjust the output current from 5 mA to 120 mA through an external resistor, R_{ext}, which gives flexibility in controlling the light intensity of LEDs. TLC592x is designed for up to 17 V at the output port. The high clock frequency, 30 MHz, also satisfies the system requirements of high-volume data transmission.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Open-Circuit Detection Principle

The LED Open-Circuit Detection compares the effective current level I_{OUT} with the open load detection threshold current $I_{OUT,Th}$. If I_{OUT} is below the $I_{OUT,Th}$ threshold, the TLC592x detects an open-load condition. This error status can be read as an error status code in the Special mode. For open-circuit error detection, a channel must be on.

Feature Description (continued)

Table 1. Open-Circuit Detection

STATE OF OUTPUT PORT	CONDITION OF OUTPUT CURRENT	ERROR STATUS CODE	MEANING
Off	I_{OUT} = 0 mA	0	Detection not possible
On	$I_{OUT} < I_{OUT,Th}$ (1)	0	Open circuit
	$I_{OUT} \geq I_{OUT,Th}$ (1)	1	Normal

(1) $I_{OUT,Th} = 0.5 \times I_{OUT,target}$ (typical)

9.3.2 Short-Circuit Detection Principle (TLC5927 Only)

The LED short-circuit detection compares the effective voltage level V_{OUT} with the shorted-load detection threshold voltages $V_{OUT,TTh}$ and $V_{OUT,RTh}$. If V_{OUT} is above the $V_{OUT,TTh}$ threshold, the TLC5927 detects a shorted-load condition. If the V_{OUT} is below $V_{OUT,RTh}$ threshold, no error is detected and the error bit is reset. This error status can be read as an error status code in the Special mode. For short-circuit error detection, a channel must be on.

Table 2. Short-Circuit Detection

STATE OF OUTPUT PORT	CONDITION OF OUTPUT VOLTAGE	ERROR STATUS CODE	MEANING
Off	I_{OUT} = 0 mA	0	Detection not possible
On	$V_{OUT} \geq V_{OUT,TTh}$	0	Short circuit
	$V_{OUT} < V_{OUT,RTh}$	1	Normal

9.3.3 Overtemperature Detection and Shutdown

The TLC592x is equipped with a global overtemperature sensor and 16 individual, channel-specific overtemperature sensors.

- When the global sensor reaches the trip temperature, all output channels are shutdown, and the error status is stored in the internal Error Status register of every channel. After shutdown, the channels automatically restart after cooling down, if the control signal (output latch) remains on. The stored error status is not reset after cooling down and can be read out as the error status code in the Special mode.
- When one of the channel-specific sensors reaches trip temperature, only the affected output channel is shut down, and the error status is stored only in the internal Error Status register of the affected channel. After shutdown, the channel automatically restarts after cooling down, if the control signal (output latch) remains on. The stored error status is not reset after cooling down and can be read out as error status code in the Special mode.

For channel-specific overtemperature error detection, a channel must be on.

The error status code is reset when the TLC592x returns to Normal mode.

Table 3. Overtemperature Detection (1)

STATE OF OUTPUT PORT	CONDITION	ERROR STATUS CODE	MEANING
Off	I_{OUT} = 0 mA	0	
On On → all channels Off	$T_j < T_{j,trip}$ global	1	Normal
	$T_j > T_{j,trip}$ global	All error status bits = 0	Global overtemperature
On On → Off	$T_j < T_{j,trip}$ channel n	1	Normal
	$T_j > T_{j,trip}$ channel n	Channel n error status bit = 0	Channel n overtemperature

(1) The global shutdown threshold temperature is approximately 170°C.

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9.4 Device Functional Modes

The TLC592x provides a Special Mode in which two functions are included, Error Detection and Current Gain Control. In the TLC592x there are two operation modes and three phases: Normal Mode phase, Mode Switching transition phase, and Special mode phase. The signal on the multiple-function pin $\overline{OE}$(ED2) is monitored, and when a one-clock-wide short pulse appears on $\overline{OE}$(ED2), TLC592x enters the Mode Switching phase. At this time, the voltage level on LE(ED1) determines the next mode into which the TLC592x switches.

In the Normal Mode phase, the serial data is transferred into TLC592x via SDI, shifted in the shift register, and transferred out via SDO. LE(ED1) can latch the serial data in the shift register to the output latch. $\overline{OE}$(ED2) enables the output drivers to sink current.

In the Special Mode phase, the low-voltage-level signal $\overline{OE}$(ED2) can enable output channels and detect the status of the output current, to tell if the driving current level is enough or not. The detected error status is loaded into the 16-bit shift register and shifted out via SDO, along with the CLK signal. The system controller can read the error status to determine whether or not the LEDs are properly lit. In the Special Mode phase, TLC592x also allows users to adjust the output current level by setting a runtime-programmable Configuration Code. The code is sent into TLC592x via SDI. The positive pulse of LE(ED1) latches the code in the shift register into a built-in 8-bit configuration latch, instead of the output latch. The code affects the voltage at R-EXT and controls the output-current regulator. The output current can be adjusted finely by a gain ranging from 1/12 to 127/128 in 256 steps. Therefore, the current skew between ICs can be compensated within less than 1%, and this feature is suitable for white balancing in LED color-display panels.

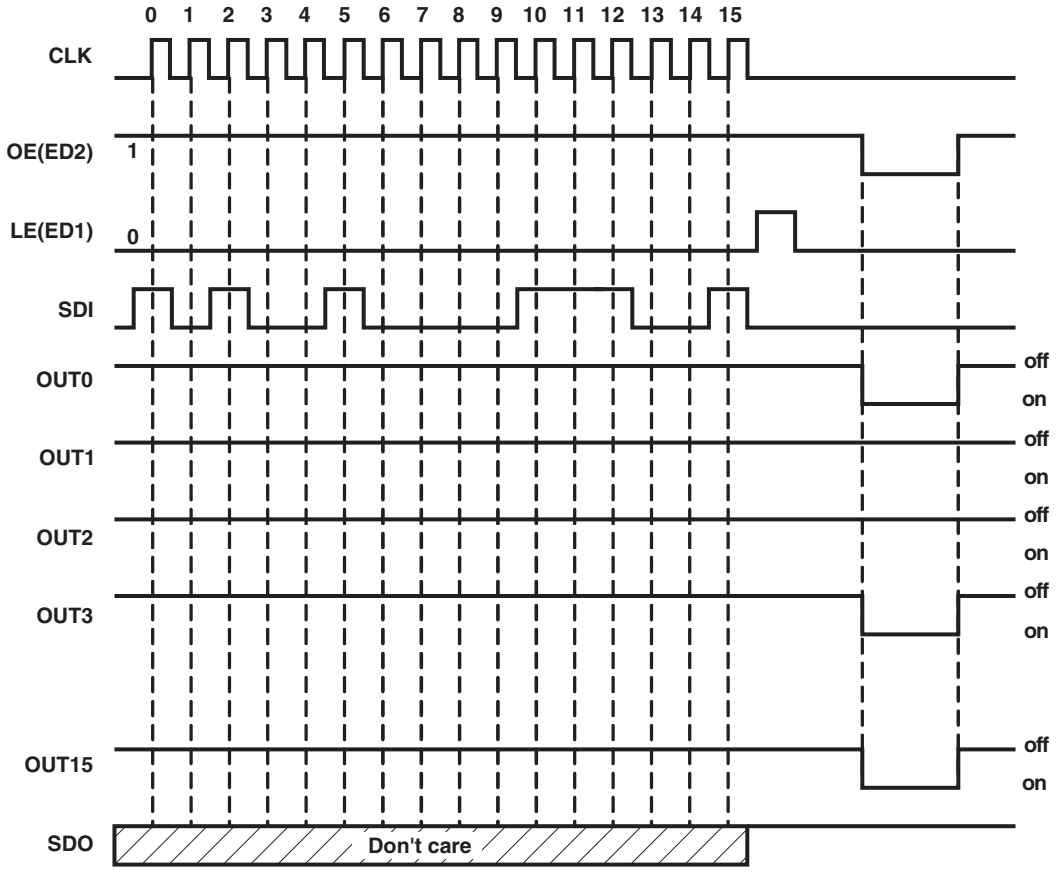

Figure 7. Normal Mode

Table 4. Truth Table in Normal Mode

CLK	LE(ED1)	$\overline{OE}$(ED2)	SDI	OUT0...OUT15	SDO
↑	H	L	Dn	Dn...Dn – 7...Dn – 15	Dn – 15
↑	L	L	Dn + 1	No change	Dn – 14

Device Functional Modes (continued)

Table 4. Truth Table in Normal Mode (continued)

CLK	LE(ED1)	$\overline{OE}$(ED2)	SDI	OUT0...OUT15	SDO
↑	H	L	Dn + 2	Dn + 2...Dn – 5...Dn – 13	Dn – 13
↓	X	L	Dn + 3	Dn + 2...Dn – 5...Dn – 13	Dn – 13
↓	X	H	Dn + 3	off	Dn – 13

The signal sequence shown in Figure 8 makes the TLC592x enter Current Adjust and Error Detection mode.

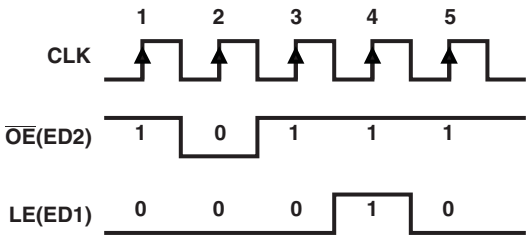

Figure 8. Switching to Special Mode

In the Current Adjust mode, sending the positive pulse of LE(ED1), the content of the shift register (a current adjust code) is written to the 16-bit configuration latch (see Figure 9).

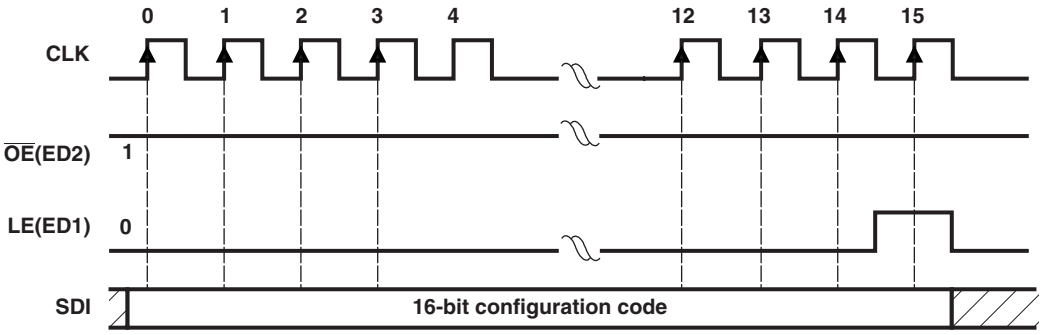

Figure 9. Writing Configuration Code

When the TLC592x is in the error detection mode, the signal sequence shown in Figure 10 enables a system controller to read error status codes through SDO.

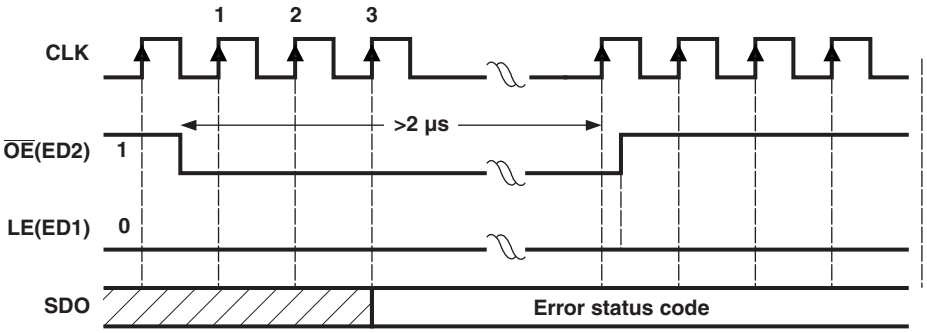

Figure 10. Reading Error Status Code

The signal sequence shown in Figure 11 makes TLC592x resume the Normal mode. Switching to Normal mode resets all internal Error Status registers. $\overline{OE}$ (ED2) always enables the output port, whether the TLC592x enters current adjust mode or not.

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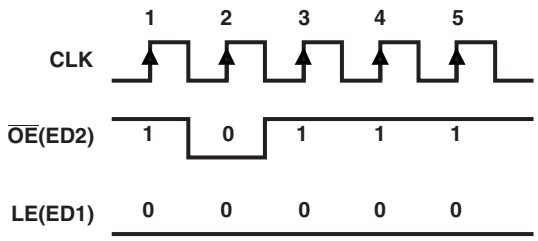

Figure 11. Switching to Normal Mode

9.4.1 Operation Mode Switching

In order to switch between its two modes, TLC592x monitors the signal $\overline{OE}$(ED2). When a one-clock-wide pulse of $\overline{OE}$(ED2) appears, TLC592x enters the two-clock-period transition phase, the Mode Switching phase. After power on, the default operation mode is the Normal Mode (see Figure 12).

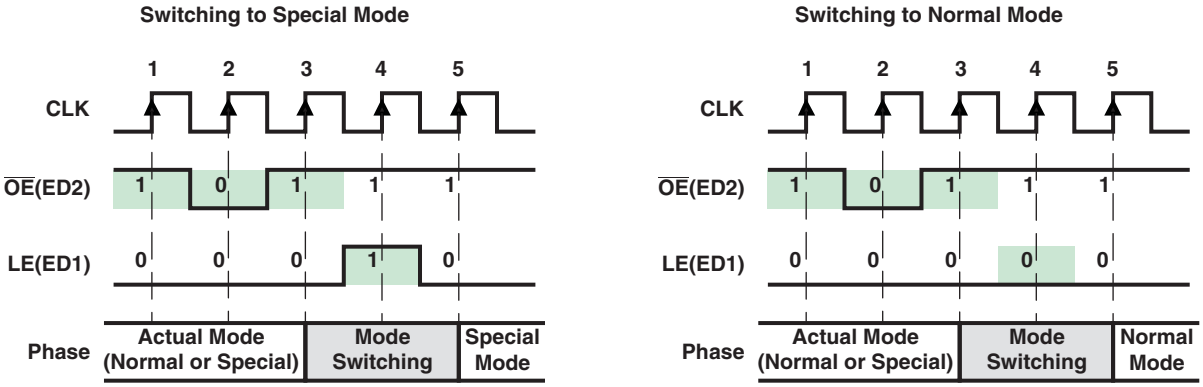

Figure 12. Mode Switching

As shown in Figure 12, once a one-clock-wide short pulse (101) of $\overline{OE}$(ED2) appears, TLC592x enters the Mode Switching phase. At the fourth rising edge of CLK, if LE(ED1) is sampled as voltage high, TLC592x switches to Special mode; otherwise, it switches to Normal mode. The signal LE(ED1) between the third and the fifth rising edges of CLK cannot latch any data. Its level is used only to determine into which mode to switch. However, the short pulse of $\overline{OE}$(ED2) can still enable the output ports. During mode switching, the serial data can still be transferred through SDI and shifted out from SDO.

NOTES:

1. The signal sequence for the mode switching may be used frequently to ensure that the TLC592x is in the proper mode.
2. The 1 and 0 on the LE(ED1) signal are sampled at the rising edge of CLK. The X means its level does not affect the result of mode switching mechanism.
3. After power on, the default operation mode is Normal mode.

9.4.2 Normal Mode Phase

Serial data is transferred into TLC592x through SDI, shifted in the Shift Register, and output through SDO. LE(ED1) can latch the serial data in the Shift Register to the Output Latch. $\overline{OE}$(ED2) enables the output drivers to sink current. These functions differ only as described in Operation Mode Switching, in which case, a short pulse triggers TLC592x to switch the operation mode. However, as long as LE(ED1) is high in the Mode Switching phase, TLC592x remains in the Normal mode, as if no mode switching occurred.

9.4.3 Special Mode Phase

In the Special mode, as long as $\overline{OE}$(ED2) is not low, the serial data is shifted to the Shift Register through SDI and shifted out through SDO, as in the Normal mode. However, there are two differences between the Special Mode and the Normal Mode, as shown in the following sections.

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9.4.3.1 Reading Error Status Code in Special Mode

When $\overline{OE}$(ED2) is pulled low while in Special mode, error detection and load error status codes are loaded into the Shift Register, in addition to enabling output ports to sink current. Figure 13 shows the timing sequence for error detection. The 0 and 1 signal levels are sampled at the rising edge of each CLK. At least three zeros must be sampled at the voltage low signal $\overline{OE}$(ED2). Immediately after the second 0 is sampled, the data input source of the Shift Register changes to the 16-bit parallel Error Status Code register, instead of from the serial data on SDI. Normally, the error status codes are generated at least 2 µs after the falling edge of $\overline{OE}$(ED2). The occurrence of the third or later 0 saves the detected error status codes into the Shift Register. Therefore, when $\overline{OE}$(ED2) is low, the serial data cannot be shifted into TLC592x through SDI. When $\overline{OE}$(ED2) is pulled high, the data input source of the Shift Register is changed back to SDI. At the same time, the output ports are disabled and the error detection is completed. Then, the error status codes saved in the Shift Register can be shifted out through SDO bit-by-bit along with CLK. Additionally, the new serial data can be shifted into TLC592x through SDI.

While in Special mode, the TLC592x cannot simultaneously transfer serial data and detect LED load error status.

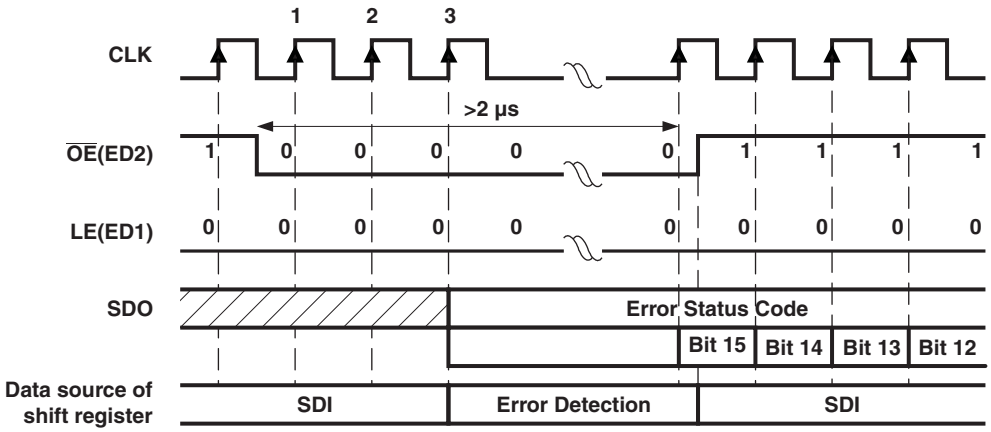

Figure 13. Reading Error Status Code

9.4.4 Writing Configuration Code in Special Mode

When in Special mode, the active high signal LE(ED1) latches the serial data in the Shift Register to the Configuration Latch, instead of the Output Latch. The latched serial data is used as the Configuration Code.

The code is stored until power off or the Configuration Latch is rewritten. As shown in Figure 14, the timing for writing the Configuration Code is the same as the timing in the Normal Mode to latching output channel data. Both the Configuration Code and Error Status Code are transferred in the common 16-bit Shift Register. Users must pay attention to the sequence of error detection and current adjustment to avoid the the Error Status Code overwriting the Configuration Code.

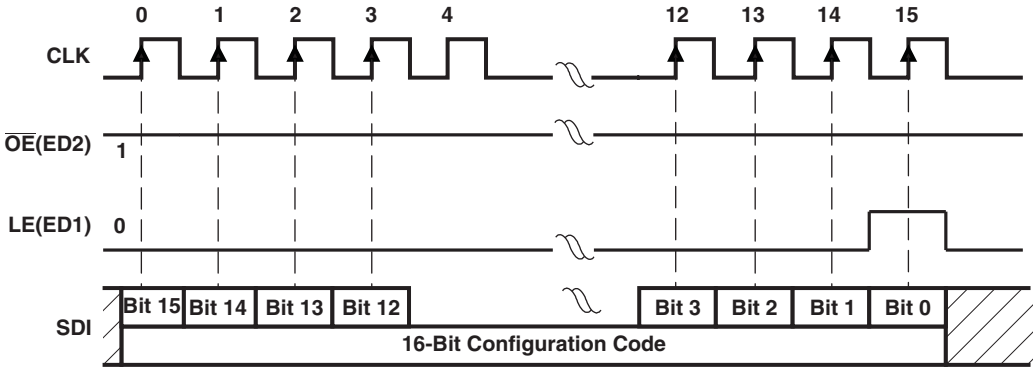

Figure 14. Writing Configuration Code

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10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Constant Current

In LED display applications, TLC592x provides nearly no current variations from channel to channel and from IC to IC. While $I_{OUT} \leq 50$ mA, the maximum current skew between channels is less than ±6% and between ICs is less than ±6%.

10.1.2 Adjusting Output Current

TLC592x scales up the reference current, I_{ref}, set by the external resistor R_{ext} to sink a current, I_{out}, at each output port. Users can follow Equation 1, Equation 2, and Equation 3 to calculate the target output current $I_{OUT,target}$ in the saturation region:

$$V_{R\text{-}EXT} = 1.26\ V \times VG \quad (1)$$

$$I_{ref} = V_{R\text{-}EXT}/R_{ext}, \text{ if another end of the external resistor } R_{ext} \text{ is connected to ground.} \quad (2)$$

$$I_{OUT,target} = I_{ref} \times 15 \times 3^{CM-1} \quad (3)$$

Where R_{ext} is the resistance of the external resistor connected to the R-EXT terminal, and $V_{R\text{-}EXT}$ is the voltage of R-EXT, which is controlled by the programmable voltage gain (VG), which is defined by the Configuration Code. The Current Multiplier (CM) determines that the ratio $I_{OUT,target}/I_{ref}$ is 15 or 5. After power on, the default value of VG is 127/128 = 0.992, and the default value of CM is 1, so that the ratio $I_{OUT,target}/I_{ref} = 15$. Based on the default VG and CM.

$$V_{R\text{-}EXT} = 1.26\ V \times 127/128 = 1.25\ V \quad (4)$$

$$I_{OUT,target} = (1.25\ V/R_{ext}) \times 15 \quad (5)$$

Therefore, the default current is approximately 52 mA at 360 Ω and 26 mA at 720 Ω. The default relationship after power on between $I_{OUT,target}$ and R_{ext} is shown in Figure 15.

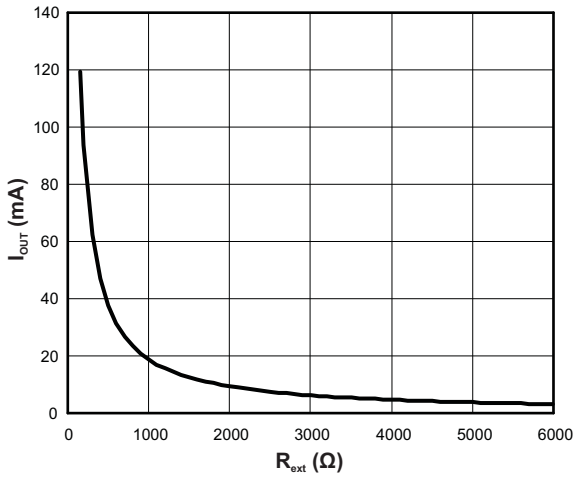

Figure 15. Default Relationship Curve Between $I_{OUT,target}$ and R_{ext}

10.1.3 16-Bit Configuration Code and Current Gain

Table 5 lists bit definition of the Configuration Code in the Configuration Latch.

Application Information (continued)

Table 5. Bit Definition of 8-Bit Configuration Code

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8–15
Meaning	CM	HC	CC0	CC1	CC2	CC3	CC4	CC5	Don't care
Default	1	1	1	1	1	1	1	1	X

Bit 7 is first sent into TLC592x through SDI. Bits 1 to 7 {HC, CC[0:5]} determine the voltage gain (VG) that affects the voltage at R-EXT and indirectly affects the reference current, I_{ref}, flowing through the external resistor at R-EXT. Bit 0 is the Current Multiplier (CM) that determines the ratio $I_{OUT,target}/I_{ref}$. Each combination of VG and CM gives a specific Current Gain (CG).

- VG: the relationship between {HC,CC[0:5]} and the voltage gain is calculated as shown in Equation 6 and Equation 7:

  $$VG = (1 + HC) \times (1 + D/64) / 4 \quad (6)$$

  $$D = CC0 \times 2^5 + CC1 \times 2^4 + CC2 \times 2^3 + CC3 \times 2^2 + CC4 \times 2^1 + CC5 \times 2^0 \quad (7)$$

  Where HC is 1 or 0, and D is the binary value of CC[0:5]. So, the VG could be regarded as a floating-point number with 1-bit exponent HC and 6-bit mantissa CC[0:5]. {HC,CC[0:5]} divides the programmable voltage gain VG into 128 steps and two subbands:

  Low voltage subband (HC = 0): VG = 1/4 ~ 127/256, linearly divided into 64 steps

  High voltage subband (HC = 1): VG = 1/2 ~ 127/128, linearly divided into 64 steps
- CM: In addition to determining the ratio $I_{OUT,target}/I_{ref}$, CM limits the output current range.

  High Current Multiplier (CM = 1): $I_{OUT,target}/I_{ref}$ = 15, suitable for output current range I_{OUT} = 10 mA to 120 mA.

  Low Current Multiplier (CM = 0): $I_{OUT,target}/I_{ref}$ = 5, suitable for output current range I_{OUT} = 5 mA to 40 mA
- CG: The total Current Gain is defined as Equation 8, Equation 9, Equation 10, and Equation 11.

  $$V_{R\text{-}EXT} = 1.26\ V \times VG \quad (8)$$

  $I_{ref} = V_{R\text{-}EXT}/R_{ext}$, if the external resistor, R_{ext}, is connected to ground. (9)

  $$I_{OUT,target} = I_{ref} \times 15 \times 3^{CM-1} = 1.26\ V/R_{ext} \times VG \times 15 \times 3^{CM-1} = (1.26\ V/R_{ext} \times 15) \times CG \quad (10)$$

  $$CG = VG \times 3^{CM-1} \quad (11)$$

  Therefore, CG = (1/12) to (127/128) divided into 256 steps.

Examples

- Configuration Code {CM, HC, CC[0:5]} = {1,1,111111}

  VG = 127/128 = 0.992 and CG = VG × 3^0 = VG = 0.992
- Configuration Code = {1,1,000000}

  VG = (1 + 1) × (1 + 0/64)/4 = 1/2 = 0.5, and CG = 0.5
- Configuration Code = {0,0,000000}

  VG = (1 + 0) × (1 + 0/64)/4 = 1/4, and CG = (1/4) × 3^{-1} = 1/12

After power on, the default value of the Configuration Code {CM, HC, CC[0:5]} is {1,1,111111}. Therefore, VG = CG = 0.992. The relationship between the Configuration Code and the Current Gain is shown in Figure 16.

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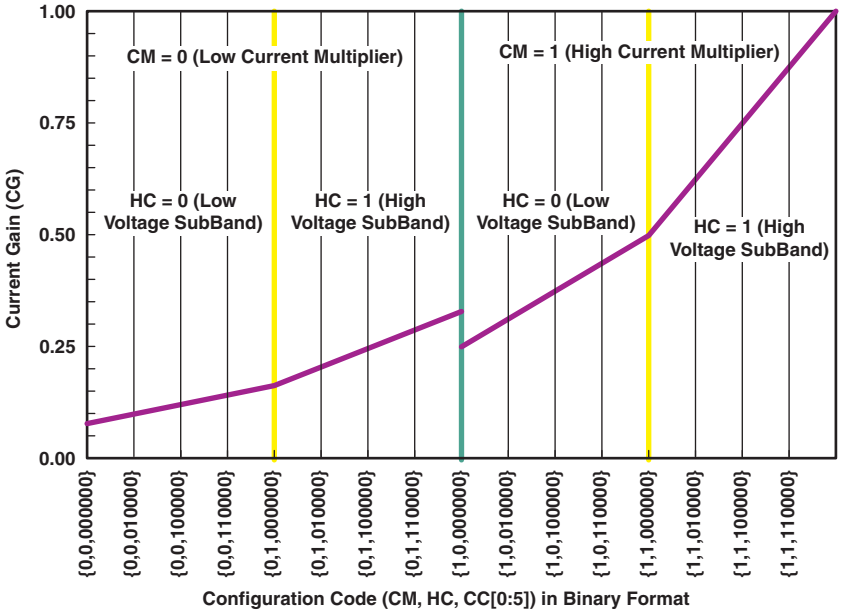

Figure 16. Current Gain vs Configuration Code

10.2 Typical Application

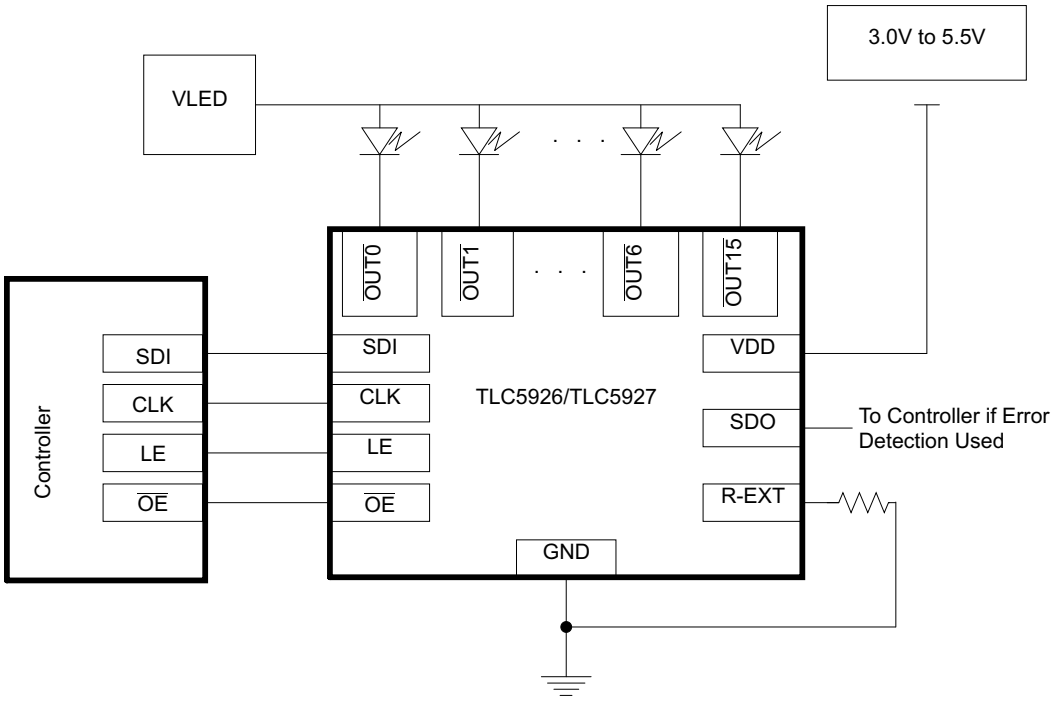

Figure 17. Single Implementation of TLC592x Device

10.2.1 Design Requirements

For this design example, use the parameters listed in Table 6. The purpose of this design procedure is to calculate the power dissipation in the device and the operating junction temperature.

Typical Application (continued)

Table 6. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
No. of LED strings	16
No. of LEDs per string	3
LED current (mA)	20
Forward voltage of each LED (V)	3.5
Junction-to-ambient thermal resistance (°C/W)	40
Ambient temperature of application (°C)	115
V_{DD} (V)	5
I_{DD} (mA)	17
Max operating junction temperature (°C)	150

10.2.2 Detailed Design Procedure

$$T_J = T_A + \theta_{JA} \times P_{D_TOT}$$

where

- T_J is the junction temperature
- T_A is the ambient temperature
- θ_{JA} is the junction-to-ambient thermal resistance
- P_{D_TOT} is the total power dissipation in the IC (12)

$$P_{D_TOT} = P_{D_CS} + I_{DD} \times V_{DD}$$

where

- P_{D_CS} is the power dissipation in the LED current sinks
- I_{DD} is the IC supply current
- V_{DD} is the IC supply voltage (13)

$$P_{D_CS} = I_O \times V_O \times n_{CH}$$

where

- I_O is the LED current
- V_O is the voltage at the output pin
- n_{CH} is the number of LED strings (14)

$$V_O = V_{LED} – (n_{LED} \times V_F)$$

where

- V_{LED} is the voltage applied to the LED string
- n_{LED} is the number of LEDs in the string
- V_F is the forward voltage of each LED (15)

V_O should not be too high as this will cause excess power dissipation inside the current sink. However, V_O should also not be loo low as this will not allow the full LED current (refer to the output voltage vs. output current graph). With V_{LED} = 12 V:

$$V_O = 12\ V – (3 \times 3.5\ V) = 1.5\ V \quad (16)$$

$$P_{D_CS} = 20\ mA \times 1.5\ V \times 16 = 0.48\ W \quad (17)$$

Using P_{D_CS}, calculate:

$$P_{D_TOT} = P_{D_CS} + I_{DD} \times V_{DD} = 0.48\ W + 0.017\ A \times 5\ V = 0.565\ W \quad (18)$$

Using P_{D_TOT}, calculate:

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$$T_J = T_A + \theta_{JA} \times P_{D_TOT} = 115°C + 40°C/W \times 0.565\ W = 137.6°C \quad (19)$$

This design example has demonstrated how to calculate power dissipation in the IC and ensure that the junction temperature is kept below 150°C.

NOTE

This design example assumes that all channels have the same electrical parameters (n_{LED}, I_O, V_F, V_{LED}). If the parameters are unique for each channel, then the power dissipation must be calculated for each current sink separately. Then, each result must be added together to calculate the total power dissipation in the current sinks.

10.2.3 Application Curve

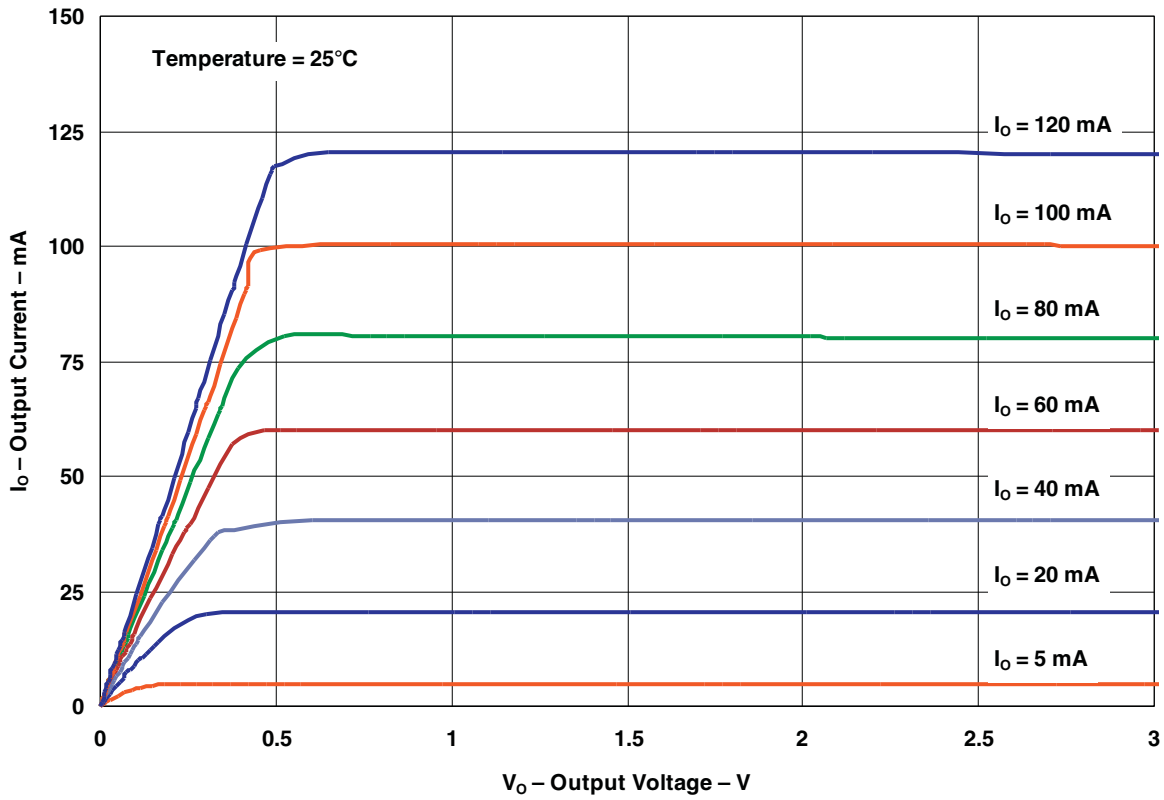

Figure 18. Output Current vs Output Voltage

11 Power Supply Recommendations

The device is designed to operate from a VDD supply between 3 V and 5.5 V. The LED supply voltage should be determined by the number of LEDs in each string and the forward voltage of the LEDs. The maximum recommended supply voltage on the output pins (OUT0-OUT15) is 17V.

12 Layout

12.1 Layout Guidelines

The traces that carry current from the LED cathodes to the OUTx pins must be wide enough to support the default current (up to 120 mA).

The SDI, CLK, LE(ED1), OE(ED2), and SDO pins should be connected to the microcontroller. There are several ways to achieve this, including the following methods:

- Traces may be routed underneath the package on the top layer.
- The signal may travel through a via to another layer.

The thermal pad in the PWP package should be connected to the ground plane through thermal relief vias. This layout technique will improve the thermal performance of the package.

12.2 Layout Example

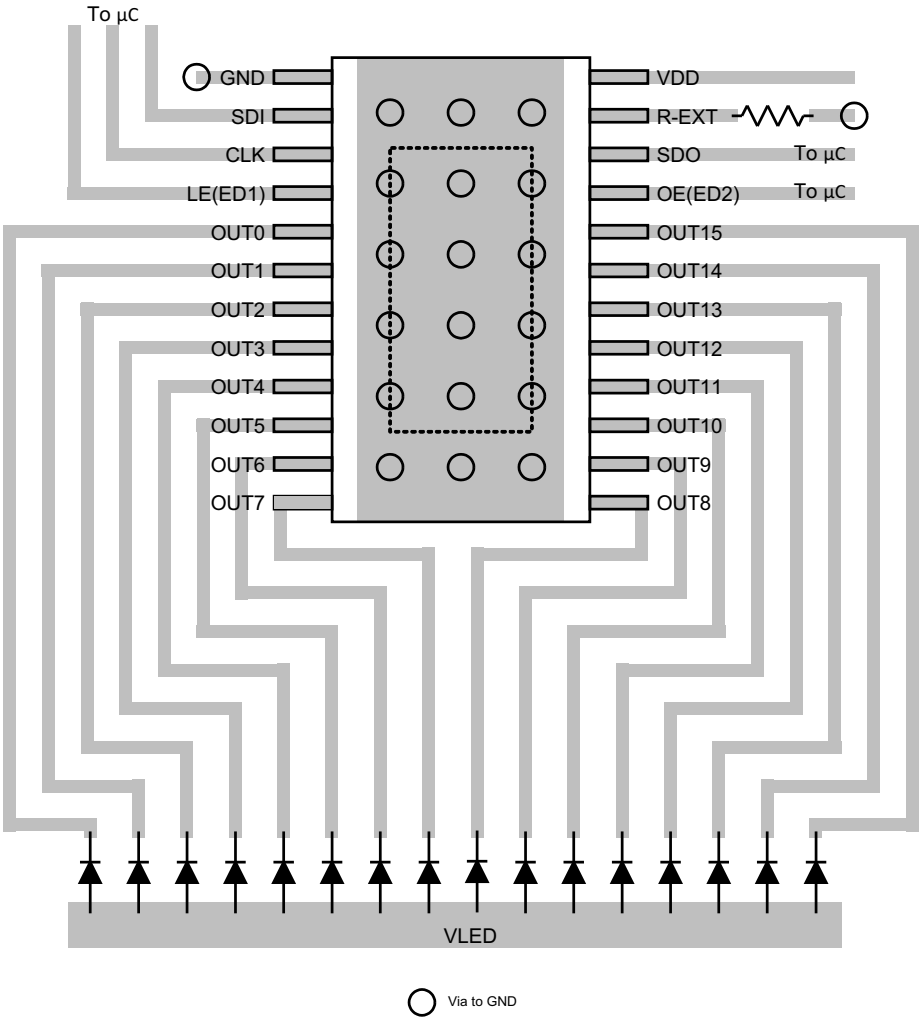

Figure 19. PWP Layout Example

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Layout Example (continued)

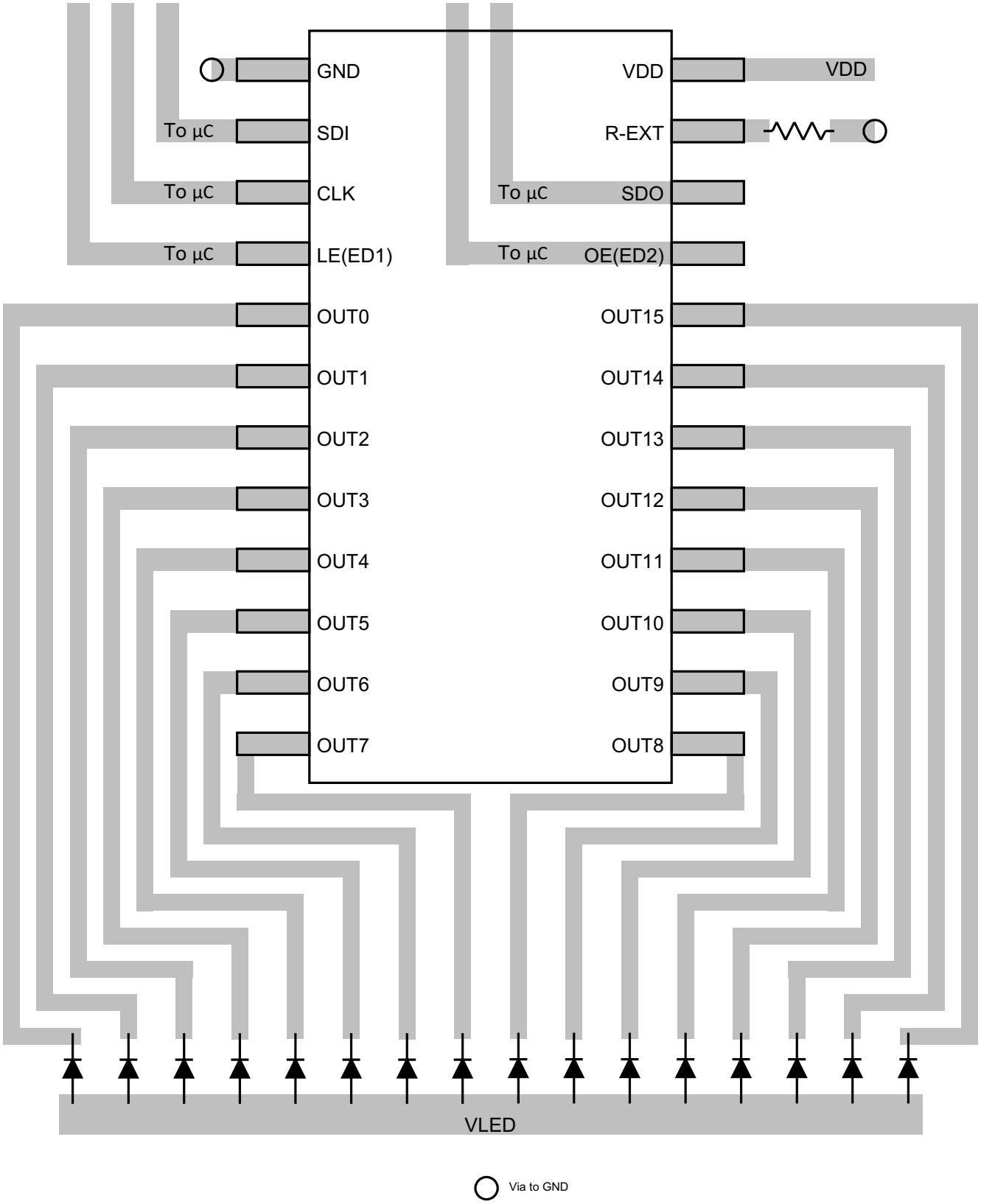

Figure 20. DW Layout Example

Layout Example (continued)

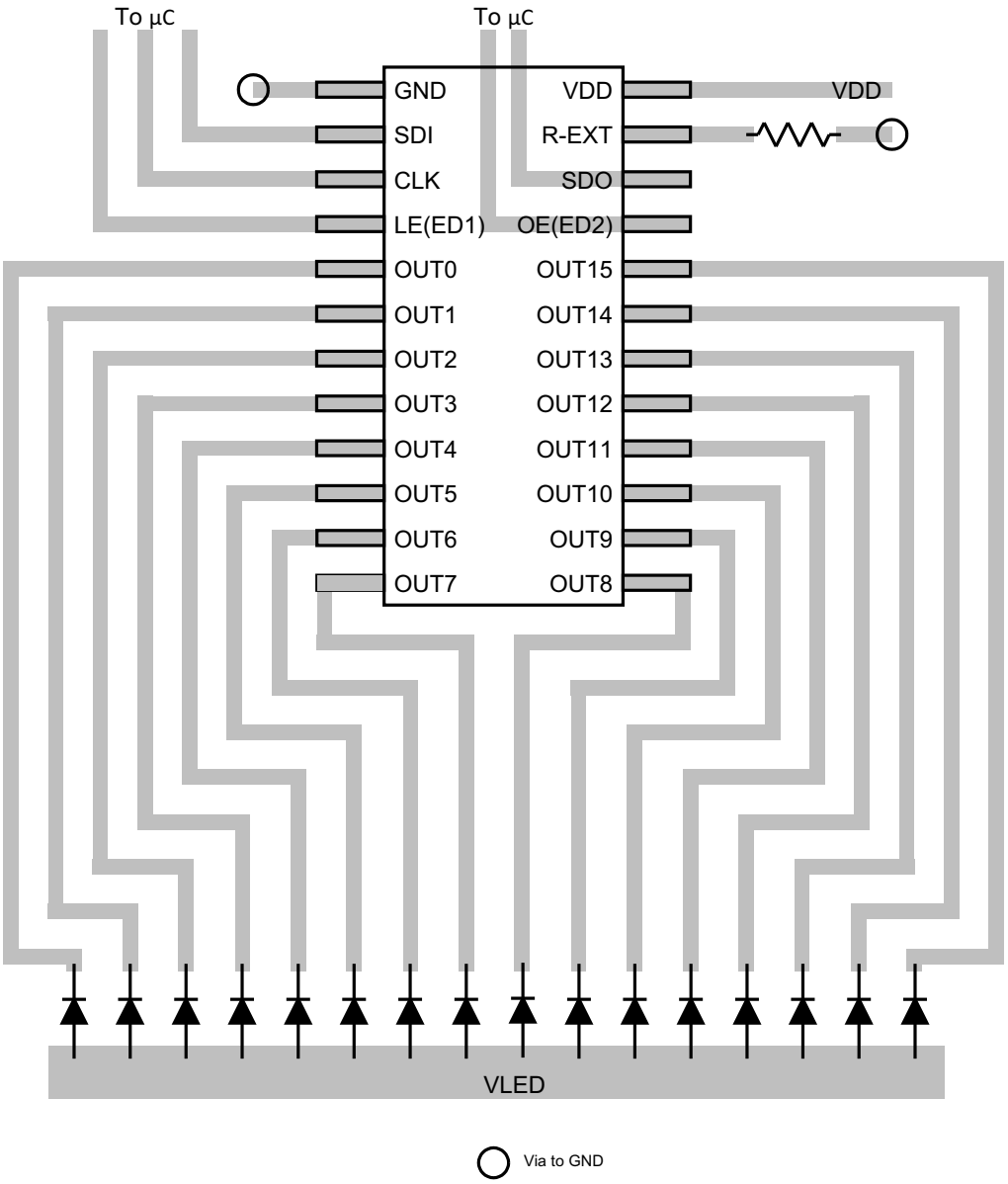

Figure 21. DBQ Layout Example

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13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 7. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLC5926	Click here	Click here	Click here	Click here	Click here
TLC5927	Click here	Click here	Click here	Click here	Click here

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC5926IDBQR	Active	Production	SSOP (DBQ) | 24	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLC5926I
TLC5926IDBQR.A	Active	Production	SSOP (DBQ) | 24	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLC5926I
TLC5926IDWR	Active	Production	SOIC (DW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC5926I
TLC5926IDWR.A	Active	Production	SOIC (DW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC5926I
TLC5926IDWRG4.A	Active	Production	SOIC (DW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC5926I
TLC5926IPWPR	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	Y5926
TLC5926IPWPR.A	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	Y5926
TLC5926IPWPRG4	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	Y5926
TLC5927IDBQR	Active	Production	SSOP (DBQ) | 24	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLC5927I
TLC5927IDBQR.A	Active	Production	SSOP (DBQ) | 24	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLC5927I
TLC5927IDBQRG4	Active	Production	SSOP (DBQ) | 24	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLC5927I
TLC5927IDBQRG4.A	Active	Production	SSOP (DBQ) | 24	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLC5927I
TLC5927IDWR	Active	Production	SOIC (DW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC5927I
TLC5927IDWR.A	Active	Production	SOIC (DW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC5927I
TLC5927IDWRG4.A	Active	Production	SOIC (DW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC5927I
TLC5927IPWPR	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	Y5927
TLC5927IPWPR.A	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	Y5927
TLC5927IPWPRG4	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	Y5927
TLC5927IPWPRG4.A	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	Y5927

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLC5926, TLC5927 :

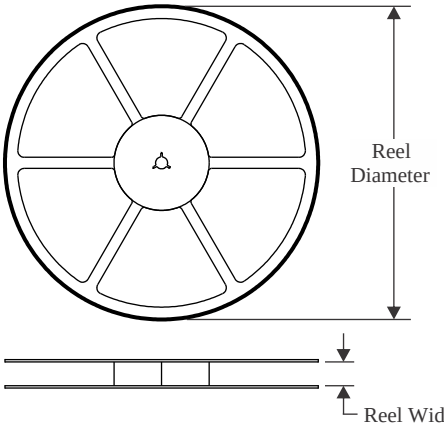
- Automotive : TLC5926-Q1, TLC5927-Q1

NOTE: Qualified Version Definitions:

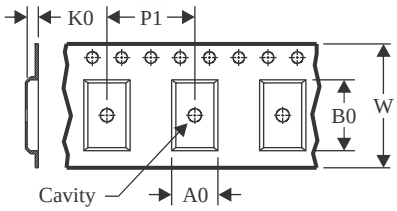
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

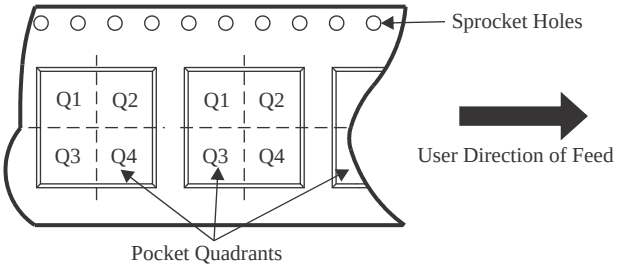


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

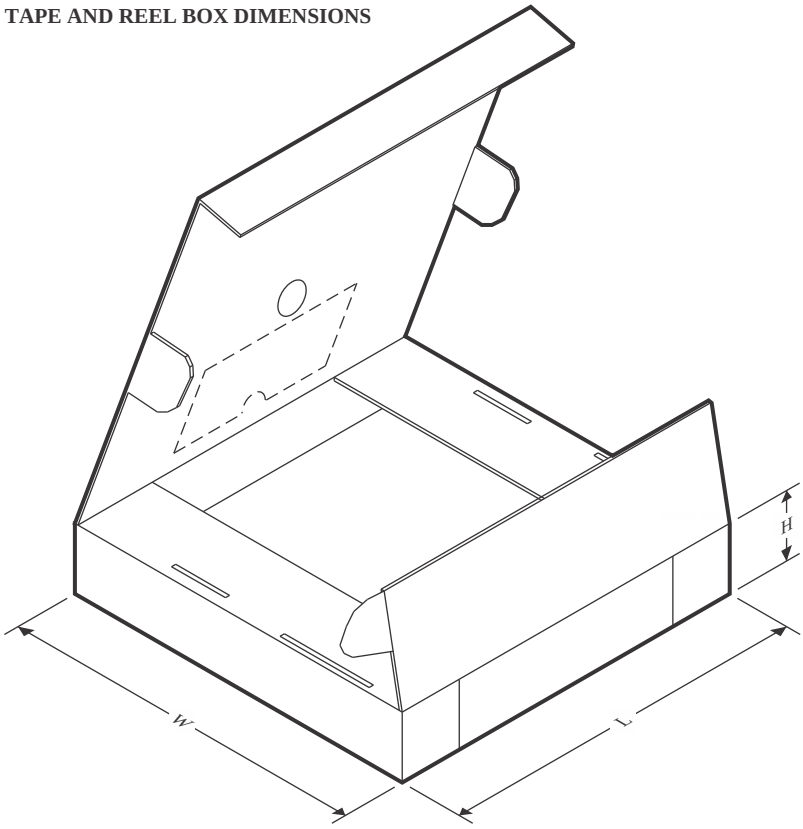
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5926IDBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC5926IDWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
TLC5927IDBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC5927IDBQRG4	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC5927IDWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
TLC5927IPWPRG4	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

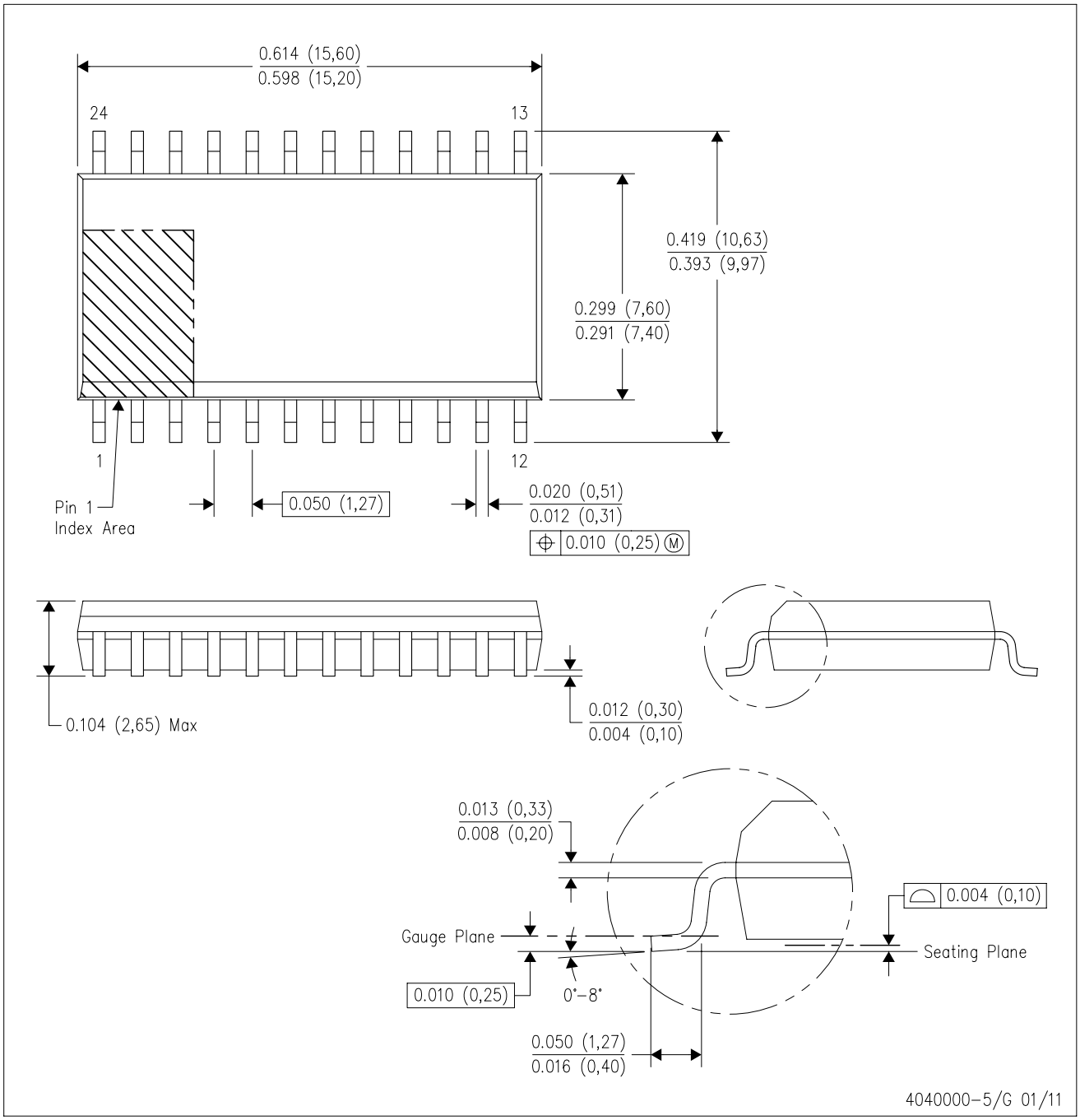
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

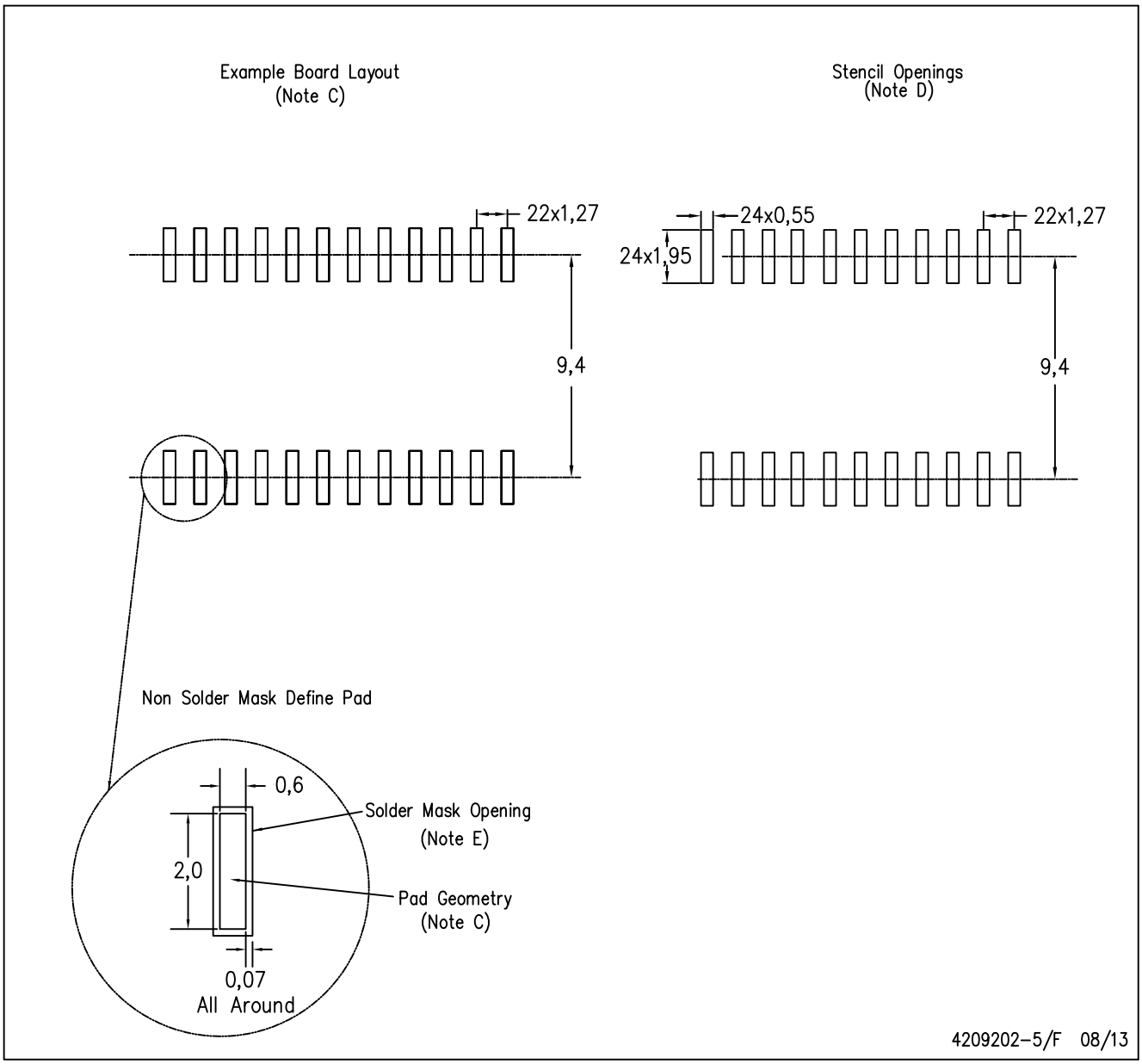
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5926IDBQR	SSOP	DBQ	24	2500	356.0	356.0	35.0
TLC5926IDWR	SOIC	DW	24	2000	350.0	350.0	43.0
TLC5927IDBQR	SSOP	DBQ	24	2500	356.0	356.0	35.0
TLC5927IDBQRG4	SSOP	DBQ	24	2500	356.0	356.0	35.0
TLC5927IDWR	SOIC	DW	24	2000	350.0	350.0	43.0
TLC5927IPWPRG4	HTSSOP	PWP	24	2000	356.0	356.0	35.0

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

GENERIC PACKAGE VIEW

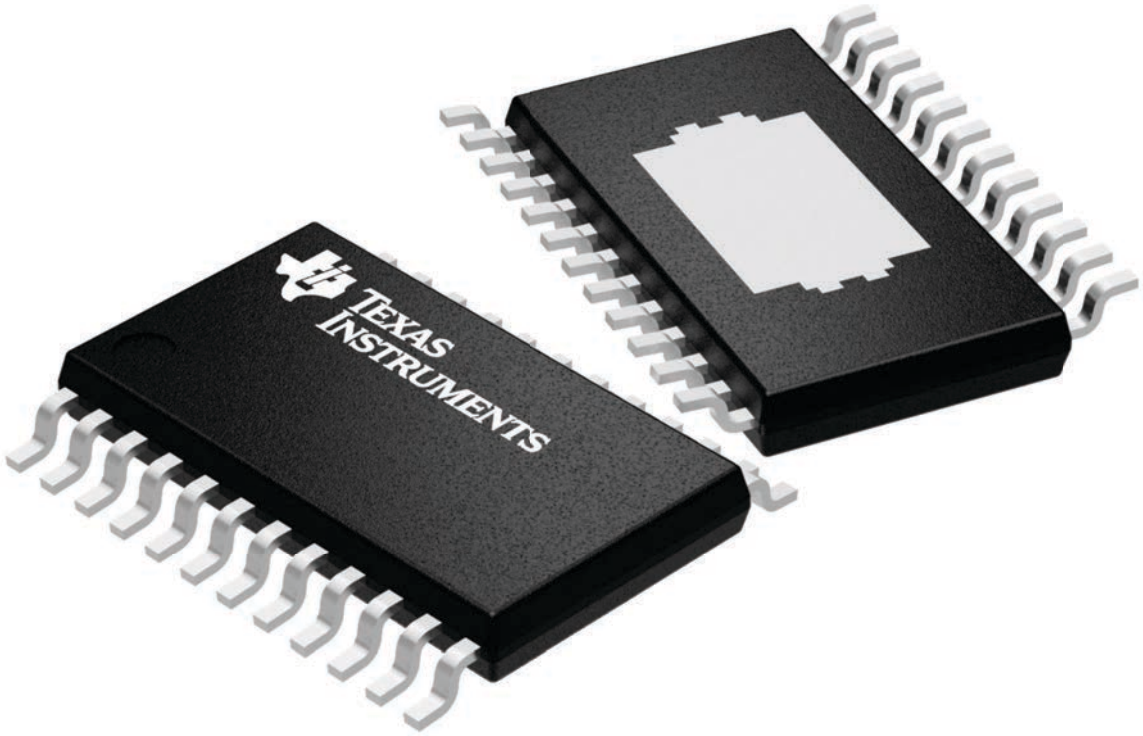
PWP 24

PowerPAD™ TSSOP - 1.2 mm max height

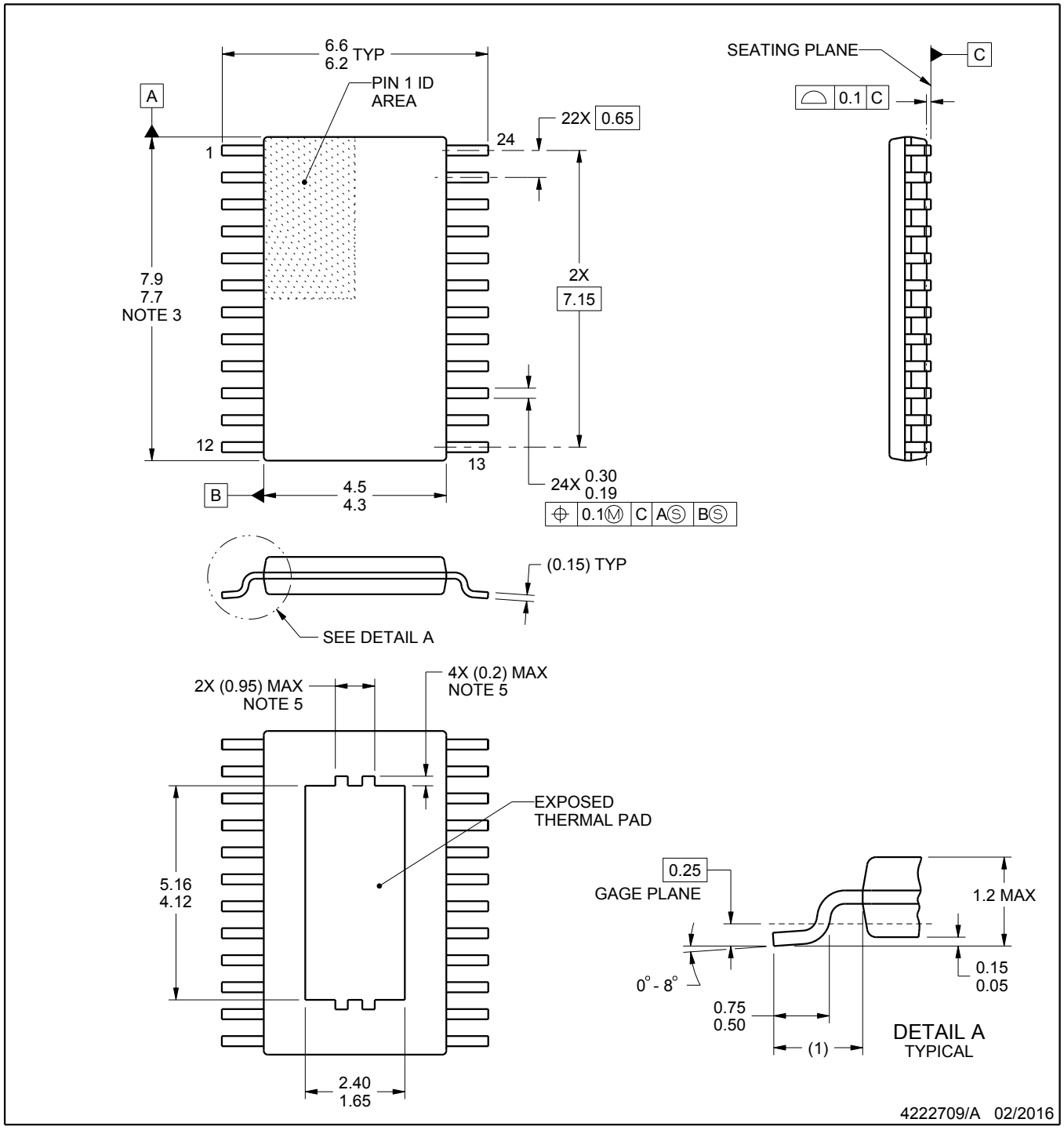
4.4 x 7.6, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



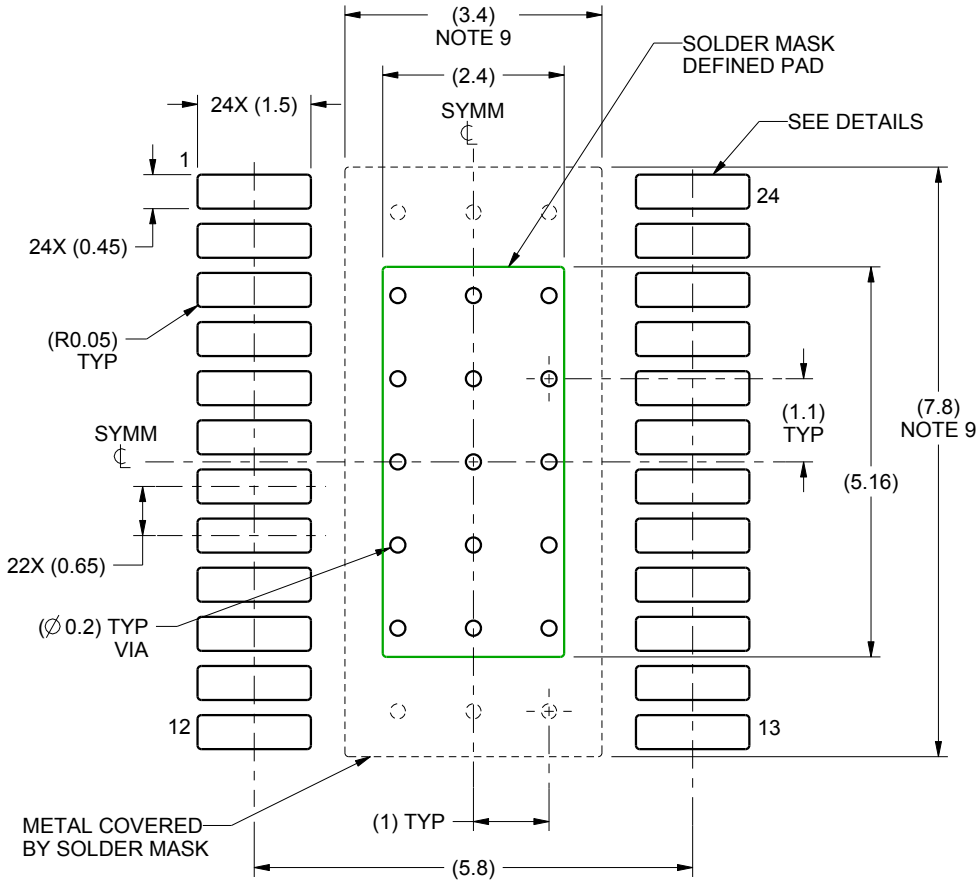
4224742/B



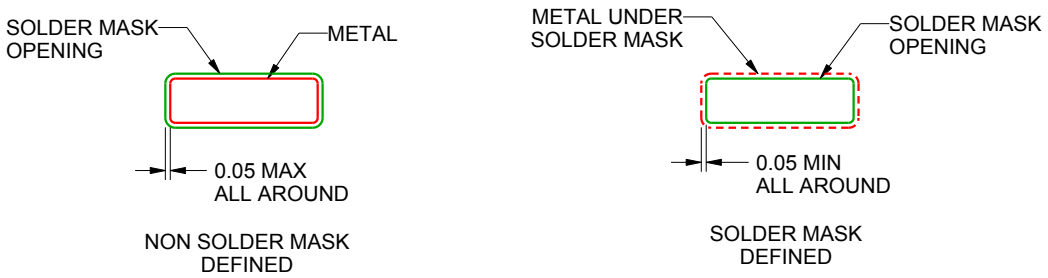
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present and may vary.



LAND PATTERN EXAMPLE
SCALE:10X

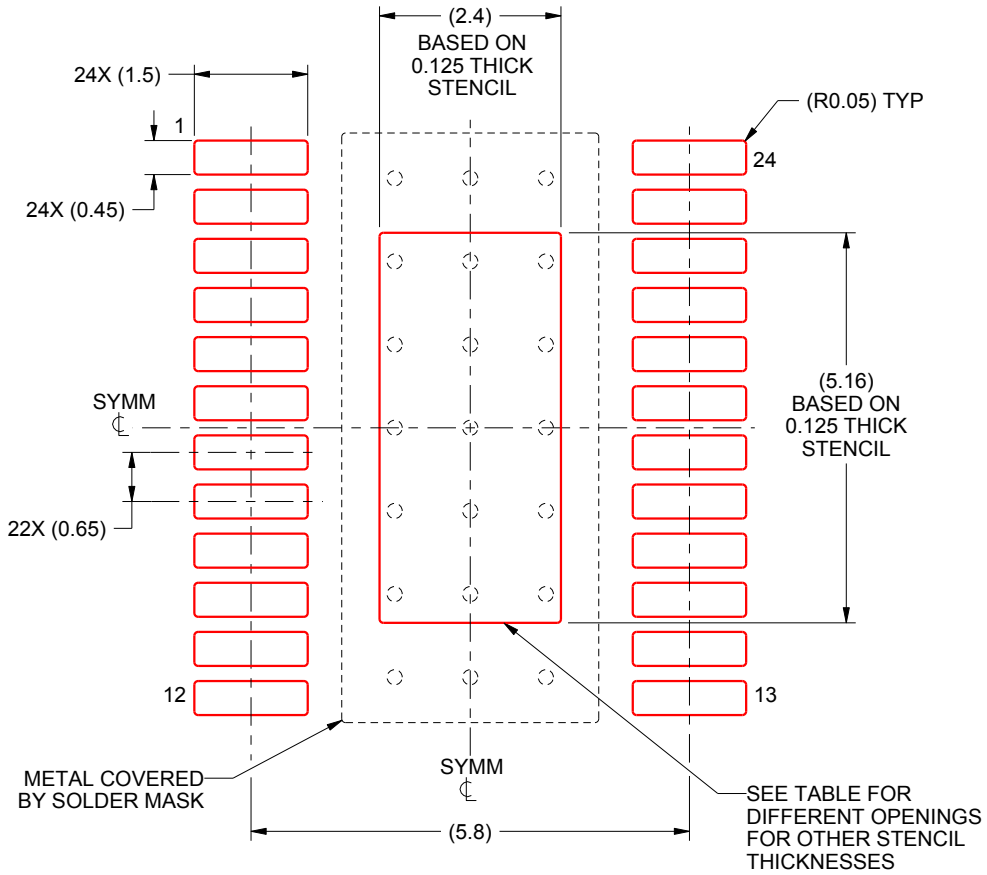


SOLDER MASK DETAILS
PADS 1-24

4222709/A 02/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

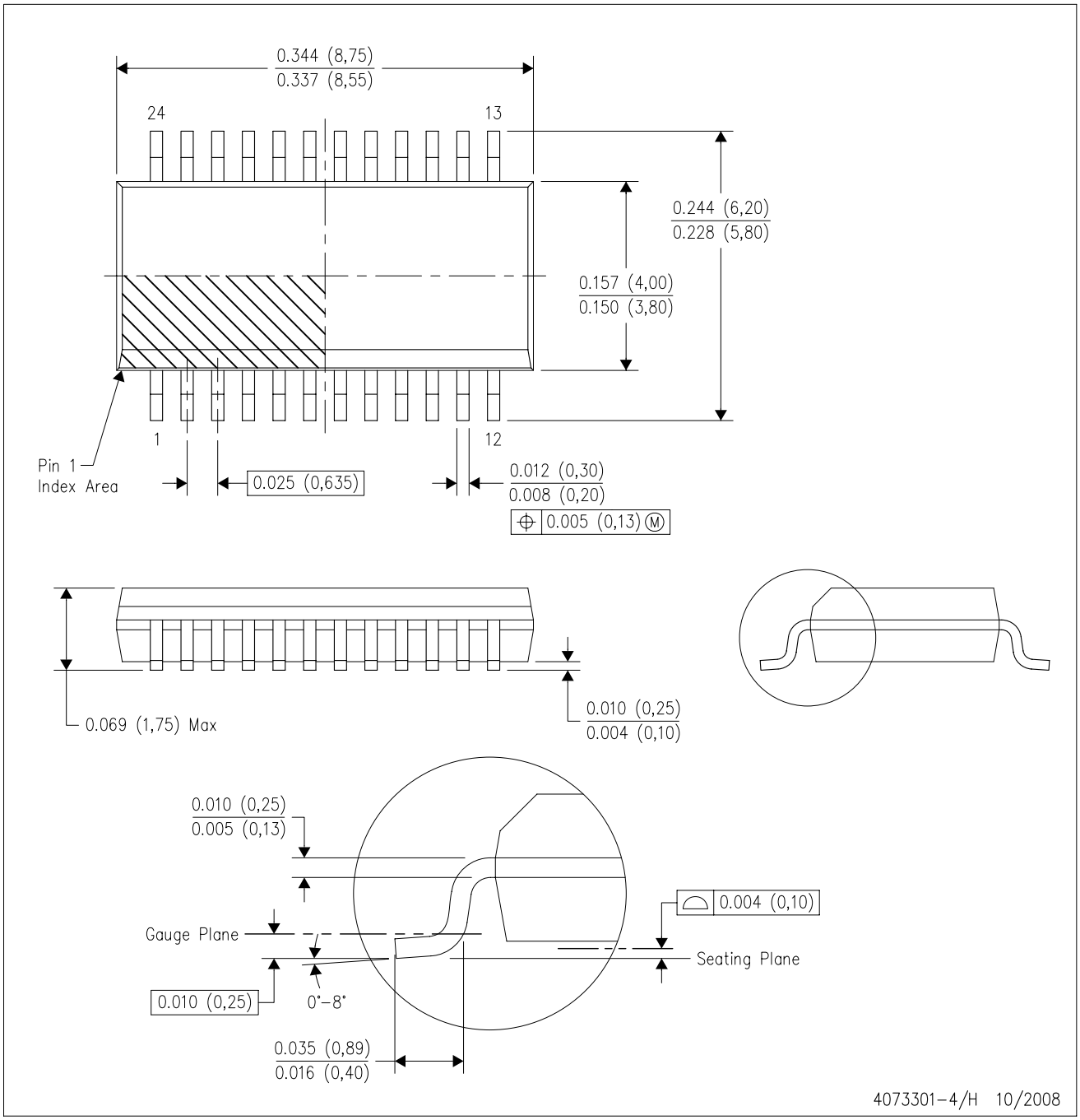
STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.68 X 5.77
0.125	2.4 X 5.16 (SHOWN)
0.15	2.19 X 4.71
0.175	2.03 X 4.36

4222709/A 02/2016

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

DBQ (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AE.

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