# SN74LV163A 4-Bit Synchronous Binary Counters

## 1 Features

- 2V to 5.5V $V_{CC}$ operation
- Max $t_{pd}$ of 9.5ns at 5V
- Typical $V_{OLP}$ (output ground bounce) <0.8V at $V_{CC}$ = 3.3V, $T_A$ = 25°C
- Typical $V_{OHV}$ (output $V_{OH}$ undershoot) >2.3V at $V_{CC}$ = 3.3V, $T_A$ = 25°C
- Support mixed-mode voltage operation on all ports
- Internal look ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Synchronously programmable
- $I_{off}$ supports partial-power-down mode operation
- Latch-up performance exceeds 100mA per JESD 78, class II

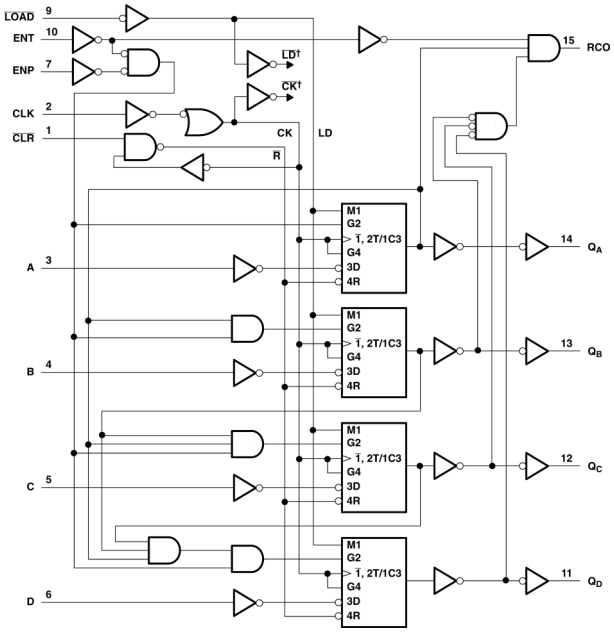
## 2 Description

The ’LV163A devices are 4-bit synchronous binary counters designed for 2V to 5.5V $V_{CC}$ operation.

**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) | BODY SIZE(3) |
|---|---|---|---|
| SN74LV163A | D (SOIC, 16) | 9.9mm × 6mm | 9.90mm × 3.91mm |
| | DB (SSOP, 16) | 6.2mm × 7.8mm | 6.20mm × 5.30mm |
| | DGV (TVSOP, 16) | 3.6mm × 6.4mm | 5.00mm × 4.40mm |
| | NS (SOP, 16) | 10.2mm × 7.8mm | 10.20mm x 5.30mm |
| | PW (TSSOP, 16) | 5.00mm × 6.4mm | 5.00mm × 4.40mm |
| | RGY (VQFN, 16) | 4mm × 3.5mm | 4.00mm × 3.50mm |

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.




**Logic Diagram (Positive Logic)**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 3 Pin Configuration and Functions

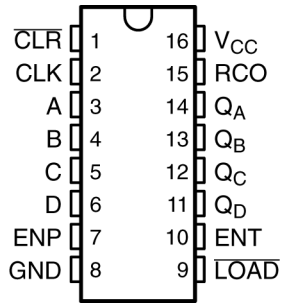


**Figure 3-1. SN74LV163A D, DB, DGV, NS, or PW Package; 16-Pin SOIC, SSOP, TVSOP, SOP, or TSSOP (Top View)**

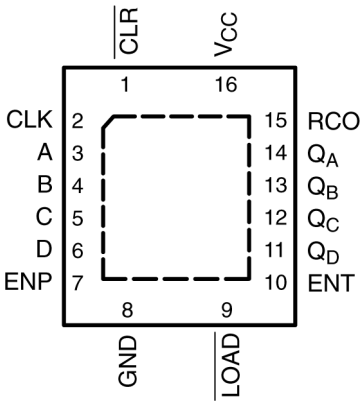


**Figure 3-2. SN74LV163A RGY Package, 16-Pin VQFN (Top View)**

Pin Functions

| NAME | PIN | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| $\overline{CLR}$ | 1 | I | Clear, active low |
| CLK | 2 | I | Clock, rising edge triggered |
| A | 3 | I | Load data A |
| B | 4 | I | Load data B |
| C | 5 | I | Load data C |
| D | 6 | I | Load data D |
| ENP | 7 | I | Count enable, does not affect RCO |
| GND | 8 | — | Ground |
| $\overline{LOAD}$ | 9 | I | Parallel load, active low |
| ENT | 10 | I | Count enable, affects RCO |
| $Q_D$ | 11 | O | $Q_D$ output |
| $Q_C$ | 12 | O | $Q_C$ output |
| $Q_B$ | 13 | O | $Q_B$ output |
| $Q_A$ | 14 | O | $Q_A$ output |
| RCO | 15 | O | Ripple-carry output |
| $V_{CC}$ | 16 | __ | Supply |

1. I = input, O = output, P = power, FB = feedback, GND = ground, N/A = not applicable

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# 4 Specifications

## 4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | −0.5 | 7 | V |
| $V_I$ [2] | Input voltage range | | −0.5 | 7 | V |
| $V_O$ [2] | Output voltage range applied in high or low state | | −0.5 | $V_{CC}$ + 0.5 | V |
| $V_O$ [2] | Voltage range applied to any output in the power-off state | | −0.5 | 7 | V |
| $I_{IK}$ | Input clamp current | ($V_I$ < 0) | | −20 | mA |
| $I_{OK}$ | Output clamp current | ($V_O$ < 0) | | −50 | mA |
| $I_O$ | Continuous output current | ($V_O$ = 0 to $V_{CC}$) | | ±25 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±50 | mA |
| $T_{stg}$ | Storage temperature range | | −65 | 150 | °C |

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

## 4.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±2000 | V |
| | | JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.[1] | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

## 4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

| | | | SN74LV163A | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | $V_{CC}$ × 0.7 | | |
| | | $V_{CC}$ = 3 V to 3.6 V | $V_{CC}$ × 0.7 | | |
| | | $V_{CC}$ = 4.5 V to 1.5 V | $V_{CC}$ × 0.7 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | $V_{CC}$ × 0.3 | |
| | | $V_{CC}$ = 3 V to 3.6 V | | $V_{CC}$ × 0.3 | |
| | | $V_{CC}$ = 4.5 V to 1.5 V | | $V_{CC}$ × 0.3 | |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | -50 | µA |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | -2 | mA |
| | | $V_{CC}$ = 3 V to 3.6 V | | -6 | |
| | | $V_{CC}$ = 4.5 V to 1.5 V | | -12 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | µA |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 2 | mA |
| | | $V_{CC}$ = 3 V to 3.6 V | | 6 | |
| | | $V_{CC}$ = 4.5 V to 1.5 V | | 12 | |


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over operating free-air temperature range (unless otherwise noted)[1]

| | | | SN74LV163A | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| Δt/Δv | Input transition rise or fall rate | $V_{CC}$ = 2.3 V to 2.7 V | | 200 | ns/V |
| | | $V_{CC}$ = 3 V to 3.6 V | | 100 | |
| | | $V_{CC}$ = 4.5 V to 1.5 V | | 20 | |
| $T_A$ | Operating free-air temperature | | -40 | 85 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## 4.4 Thermal Information

| THERMAL METRIC[1] | | SN74LV163A | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | D | DB | DGV | NS | PW | RGY | |
| | | 16 PINS | 16 PINS | 16 PINS | 16 PINS | 16 PINS | 16 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 73 | 82 | 120 | 64 | 108 | 39 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 4.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | SN74LV163A | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| $V_{OH}$ | $I_{OH}$ = −50 μA | 2 V to 5.5 V | $V_{CC}$−0.1 | | | V |
| | $I_{OH}$ = −2 mA | 2.3 V | 2 | | | |
| | $I_{OH}$ = −6 mA | 3 V | 2.48 | | | |
| | $I_{OH}$ = −12 mA | 4.5 V | 3.8 | | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 2 V to 5.5 V | | | 0.1 | V |
| | $I_{OL}$ = 2 mA | 2.3 V | | | 0.4 | |
| | $I_{OL}$ = 6 mA | 3 V | | | 0.44 | |
| | $I_{OL}$ = 12 mA | 4.5 V | | | 0.55 | |
| $I_I$ | $V_I$ = 5.5 V or GND | 0 to 5.5 V | | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 20 | μA |
| $I_{off}$ | $V_I$ or $V_O$ = 0 to 5.5 V | 0 | | | 5 | μA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 3.3 V | | 1.8 | | pF |

## 4.6 Timing Requirements, $V_{CC}$ = 2.5V ± 0.2V

over recommended operating free-air temperature range, $V_{CC}$ = 2.5V ± 0.2V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| | | | $T_A$ = 25°C | | SN74LV163A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, CLK high or low | | 7 | | 7 | | ns |
| $t_{su}$ | Setup time before CLK↑ | $\overline{CLR}$ | 6 | | 6 | | ns |
| | | Data (A, B, C, and D) | 7.5 | | 8.5 | | |
| | | ENP, ENT | 9.5 | | 11 | | |
| | | $\overline{LOAD}$ low | 10 | | 11.5 | | |
| $t_h$ | Hold time, all synchronous inputs after CLK↑ | | 1.5 | | 1.5 | | ns |

## 4.7 Timing Requirements, $V_{CC}$ = 3.3V ± 0.3V

over recommended operating free-air temperature range, $V_{CC}$ = 3.3V ± 0.3V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| | | | $T_A$ = 25°C | | SN74LV163A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, CLK high or low | | 5 | | 5 | | ns |
| $t_{su}$ | Setup time before CLK↑ | $\overline{CLR}$ | 4 | | 4 | | ns |
| | | Data (A, B, C, and D) | 5.5 | | 6.5 | | |
| | | ENP, ENT | 7.5 | | 9 | | |
| | | $\overline{LOAD}$ low | 8 | | 9.5 | | |
| $t_h$ | Hold time, all synchronous inputs after CLK↑ | | 1 | | 1 | | ns |

## 4.8 Timing Requirements, $V_{CC}$ = 5V ± 0.5V

over recommended operating free-air temperature range, $V_{CC}$ = 5V ± 0.5V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| | | | $T_A$ = 25°C | | SN74LV163A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, CLK high or low | | 5 | | 5 | | ns |
| $t_{su}$ | Setup time before CLK↑ | $\overline{CLR}$ | 3.5 | | 3.5 | | ns |
| | | Data (A, B, C, and D) | 4.5 | | 4.5 | | |
| | | ENP, ENT | 5 | | 6 | | |
| | | $\overline{LOAD}$ low | 5 | | 6 | | |
| $t_h$ | Hold time, all synchronous inputs after CLK↑ | | 1 | | 1 | | ns |

## 4.9 Switching Characteristics, $V_{CC}$ = 2.5V ± 0.2V

over recommended operating free-air temperature range, $V_{CC}$ = 2.5V ± 0.2V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | TA = 25°C | | | SN74LV163A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | |
| $f_{max}$ | | | $C_L$ = 15 pF | 50(1) | 115(1) | | 40 | | MHz |
| | | | $C_L$ = 50 pF | 30 | 90 | | 25 | | |
| $t_{pd}$ | CLK | Q | $C_L$ = 15 pF | | 8.5(1) | 16.2(1) | 1 | 19.5 | ns |
| | | RCO (count mode) | | | 9.1(1) | 17(1) | 1 | 20.5 | |
| | | RCO (preset mode) | | | 12.1(1) | 20.6(1) | 1 | 24.5 | |
| | ENT | RCO | | | 8.7(1) | 15.7(1) | 1 | 19 | |
| $t_{pd}$ | CLK | Q | $C_L$ = 50 pF | | 11 | 19.2 | 1 | 22.5 | ns |
| | | RCO (count mode) | | | 11.9 | 20 | 1 | 23.5 | |
| | | RCO (preset mode) | | | 14.6 | 23.6 | 1 | 27.5 | |
| | ENT | RCO | | | 11.7 | 18.7 | 1 | 22 | |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.


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## 4.10 Switching Characteristics, $V_{CC}$ = 3.3V ± 0.3V

over recommended operating free-air temperature range, $V_{CC}$ = 3.3V ± 0.3V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | TA = 25°C | | | SN74LV163A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | |
| $f_{max}$ | | | $C_L$ = 15 pF | 80[1] | 160[1] | | 70 | | MHz |
| | | | $C_L$ = 50 pF | 55 | 125 | | 50 | | |
| $t_{pd}$ | CLK | Q | $C_L$ = 15 pF | | 6.2[1] | 12.8[1] | 1 | 15 | ns |
| | | RCO (count mode) | | | 6.8[1] | 13.6[1] | 1 | 16 | |
| | | RCO (preset mode) | | | 8.8[1] | 17.2[1] | 1 | 20 | |
| | ENT | RCO | | | 6.5[1] | 12.3[1] | 1 | 14.5 | |
| $t_{pd}$ | CLK | Q | $C_L$ = 50 pF | | 8 | 16.3 | 1 | 18.5 | ns |
| | | RCO (count mode) | | | 8.8 | 17.1 | 1 | 19.5 | |
| | | RCO (preset mode) | | | 10.7 | 20.7 | 1 | 23.5 | |
| | ENT | RCO | | | 8.2 | 15.8 | 1 | 18 | |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 4.11 Switching Characteristics, $V_{CC}$ = 5V ± 0.5V

over recommended operating free-air temperature range, $V_{CC}$ = 5V ± 0.5V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | TA = 25°C | | | SN74LV163A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | |
| $f_{max}$ | | | $C_L$ = 15 pF | 135[1] | 210[1] | | 115 | | MHz |
| | | | $C_L$ = 50 pF | 95 | 160 | | 85 | | |
| $t_{pd}$ | CLK | Q | $C_L$ = 15 pF | | 4.7[1] | 8.1[1] | 1 | 9.5 | ns |
| | | RCO (count mode) | | | 5.2[1] | 8.1[1] | 1 | 9.5 | |
| | | RCO (preset mode) | | | 6.4[1] | 10.3[1] | 1 | 12 | |
| | ENT | RCO | | | 4.9[1] | 8.1[1] | 1 | 9.5 | |
| $t_{pd}$ | CLK | Q | $C_L$ = 50 pF | | 6.1 | 10.1 | 1 | 11.5 | ns |
| | | RCO (count mode) | | | 6.6 | 10.1 | 1 | 11.5 | |
| | | RCO (preset mode) | | | 7.8 | 12.3 | 1 | 14 | |
| | ENT | RCO | | | 6.3 | 10.1 | 1 | 11.5 | |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 4.12 Noise Characteristics

$V_{CC}$ = 3.3 V, $C_L$ = 50 pF, $T_A$ = 25°C[1]

| PARAMETER | | SN74LV163A | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.3 | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | −0.2 | −0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 3 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2.31 | | | V |

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$V_{CC}$ = 3.3 V, $C_L$ = 50 pF, $T_A$ = 25°C[(1)]

| PARAMETER | | SN74LV163A | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.99 | V |

(1) Characteristics are for surface-mount packages only.

## 4.13 Operating Characteristics

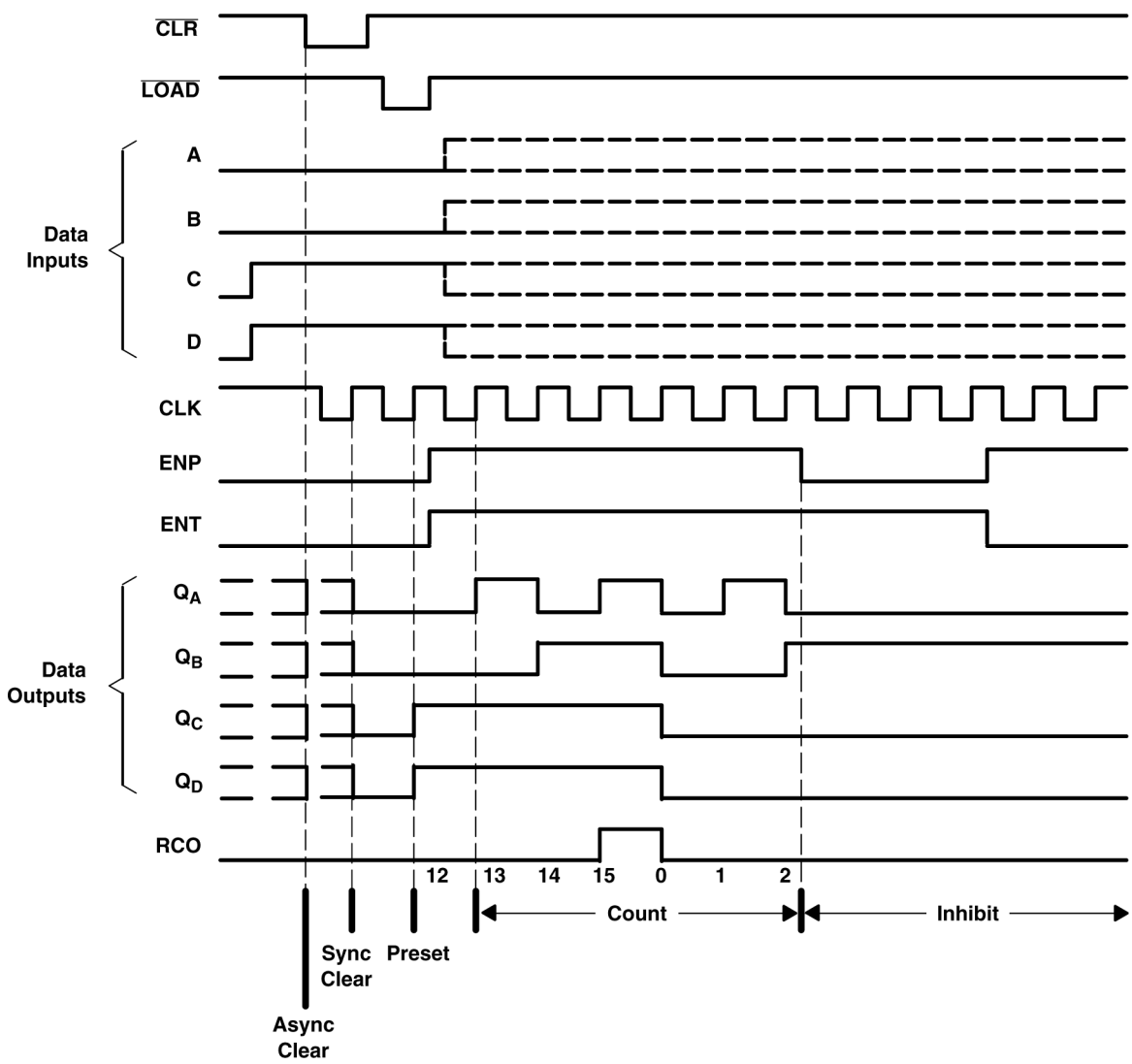
$T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | TYP | UNIT |
|---|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | $C_L$ = 50 pF, | f = 10 MHz | 3.3 V | 23.8 | pF |
| | | | | 5 V | 26 | |

## 4.14 Typical Clear, Preset, Count, and Inhibit Sequence

The following sequence is illustrated below:

1. Clear outputs to zero (synchronous)
2. Preset to binary 12
3. Count to 13, 14, 15, 0, 1, and 2
4. Inhibit





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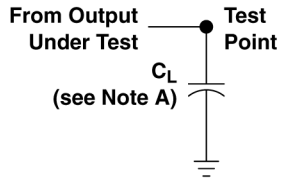
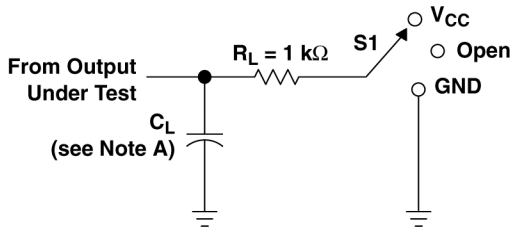
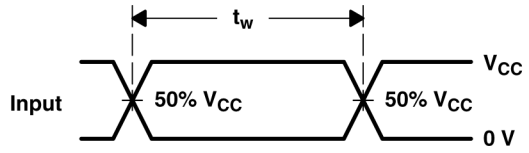
## 5 Parameter Measurement Information



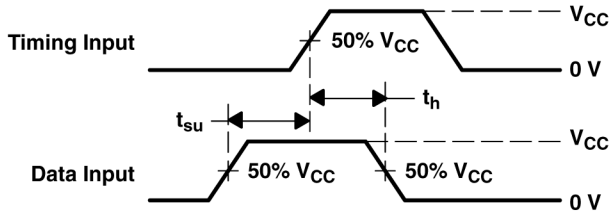

LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS



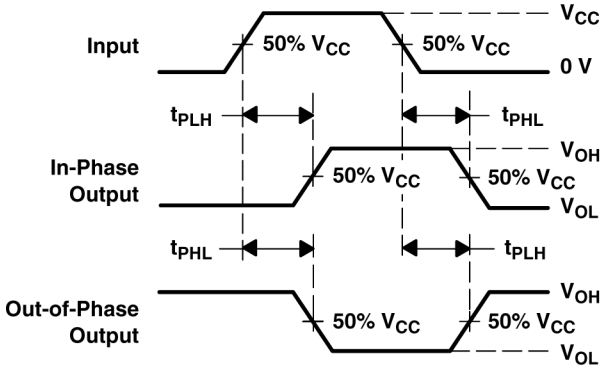

LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS



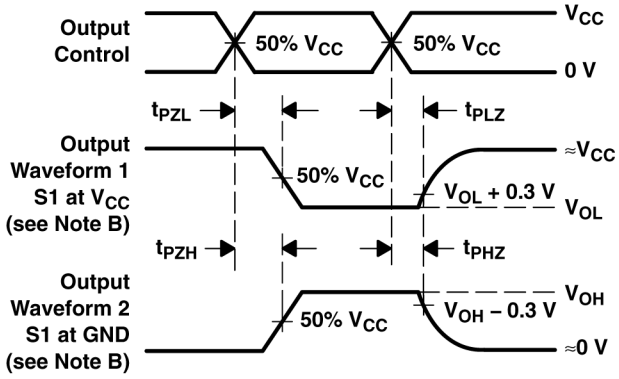

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.

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G. $t_{PHL}$ and $t_{PLH}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**Figure 5-1. Load Circuit and Voltage Waveforms**

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |
| Open Drain | $V_{CC}$ |


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# 6 Detailed Description

## 6.1 Overview

The ’LV163A devices are 4-bit synchronous binary counters designed for 2-V to 5.5-V $V_{CC}$ operation.

These synchronous, presettable counters feature an internal carry look ahead for application in high-speed counting designs. The ’LV163A devices are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes normally associated with synchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, they can be preset to any number between 0 and 9 or 15. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs.

The clear function for the ’LV163A devices is synchronous. A low level at the clear ($\overline{CLR}$) input sets all four of the flip-flop outputs low after the next low-to-high transition of CLK, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily by decoding the Q outputs for the maximum count desired. The active-low output of the gate used for decoding is connected to $\overline{CLR}$ to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. ENP, ENT, and a ripple-carry output (RCO) are instrumental in accomplishing this function. Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. Enabling RCO produces a high-level pulse while the count is maximum (9 or 15 with $Q_A$ high). This high-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{LOAD}$) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

These devices are fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

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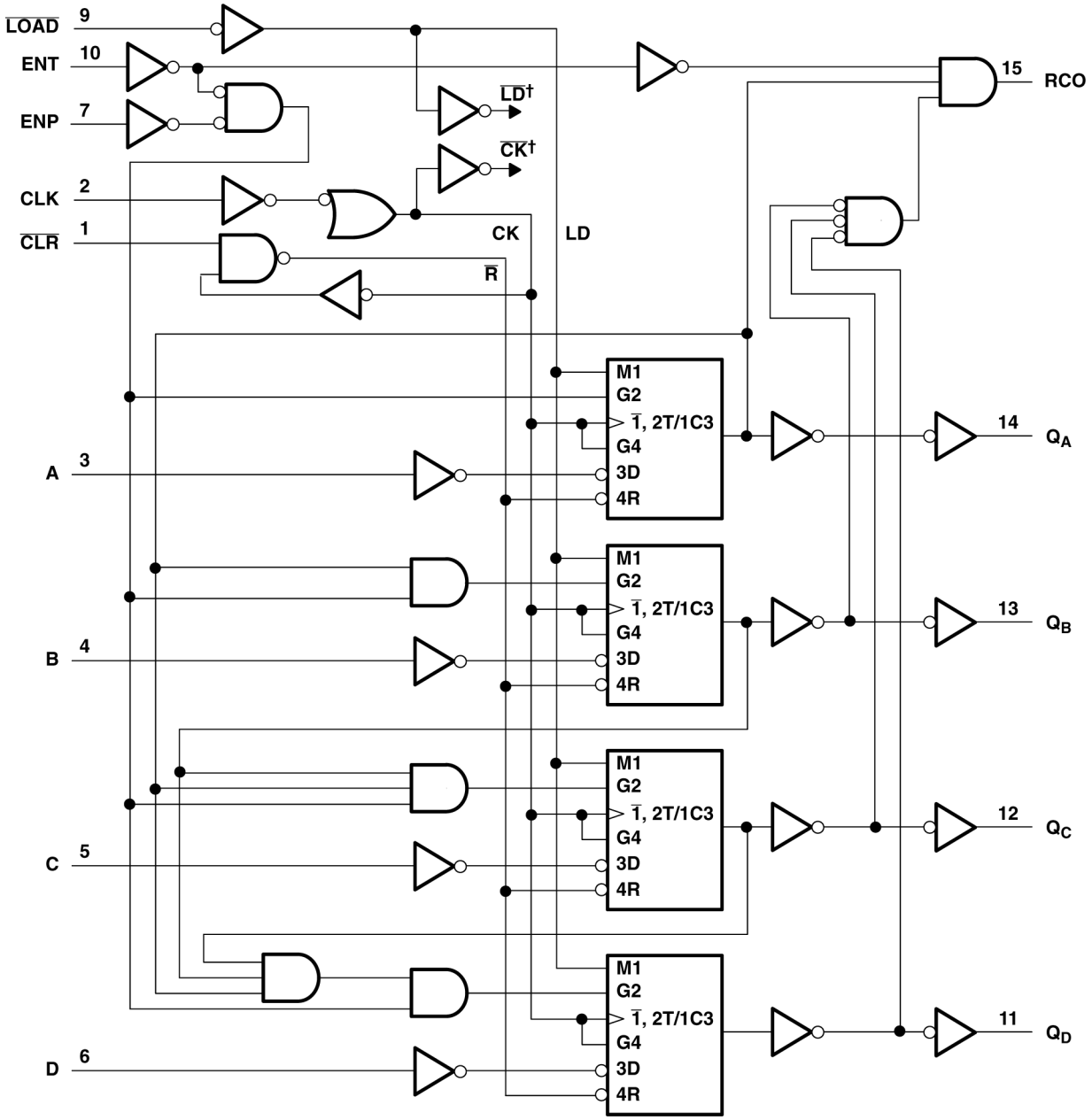
## 6.2 Functional Block Diagram




A. For simplicity, routing of complementary signals $\overline{LD}$ and $\overline{CK}$ is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.

**Figure 6-1. Logic Diagram (Positive Logic)**

Pin numbers shown are for the D, DB, DGV, J, NS, PW, RGY, and W packages.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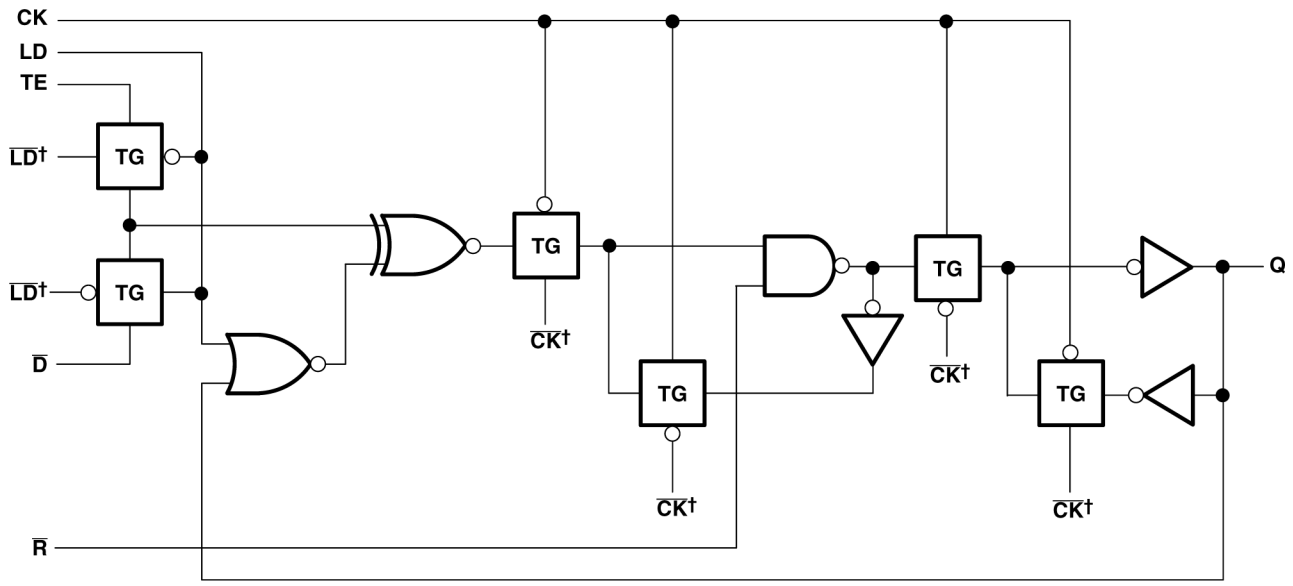


A. The origins of $\overline{LD}$ and $\overline{CK}$ are shown in the overall logic diagram of the device.

**Figure 6-2. Logic Diagram, Each D/T Flip-flop (Positive Logic)**

## 6.3 Device Functional Modes

**Table 6-1. Function Table**

| INPUTS | | | | | OUTPUTS | | | | FUNCTION |
|---|---|---|---|---|---|---|---|---|---|
| $\overline{CLR}$ | $\overline{LOAD}$ | ENP | ENT | CLK | $\overline{QA}$ | QB | QC | QD | |
| L | X | X | X | X | L | L | L | L | Reset to “0” |
| H | L | X | X | | A | B | C | D | Preset data |
| H | H | X | L | | | No change | | | No count |
| H | H | L | X | | | No change | | | No count |
| H | H | H | H | | | Count up | | | Count |
| H | X | X | X | | | No change | | | No count |

# 7 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 7.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each $V_{CC}$ terminal should have a good bypass capacitor to prevent power disturbance. A 0.1µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 7.2 Layout

### *7.2.1 Layout Guidelines*

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces with ground
  - For traces longer than 12cm
    - Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - Avoid branches; buffer signals that must branch separately

### *7.2.2 Layout Example*

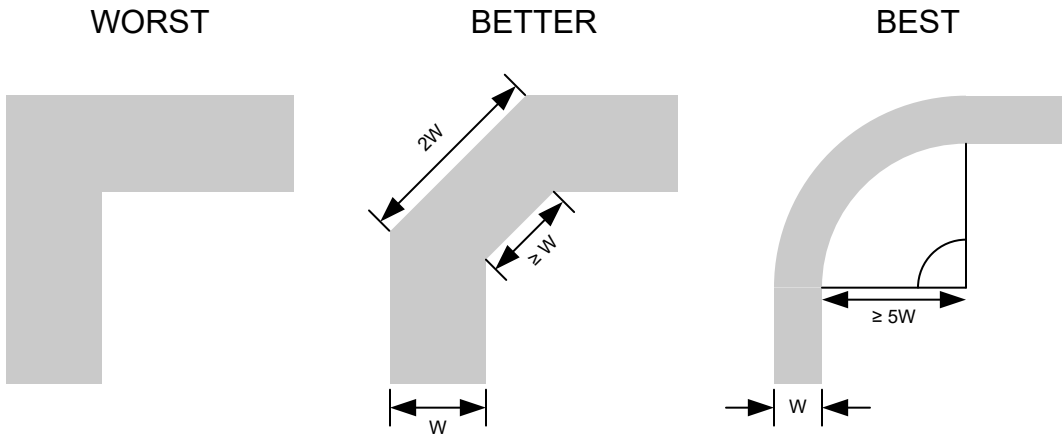


**Figure 7-1. Example Trace Corners for Improved Signal Integrity**


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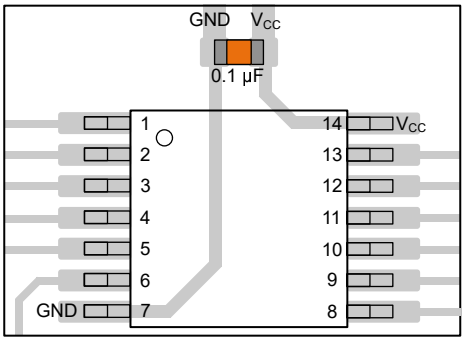


**Figure 7-2. Example Bypass Capacitor Placement for TSSOP and Similar Packages**

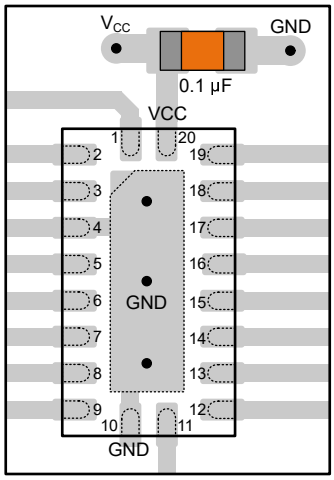


**Figure 7-3. Example Bypass Capacitor Placement for WQFN and Similar Packages**

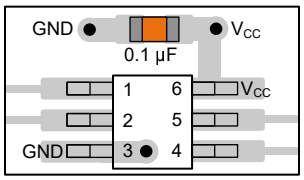


**Figure 7-4. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages**

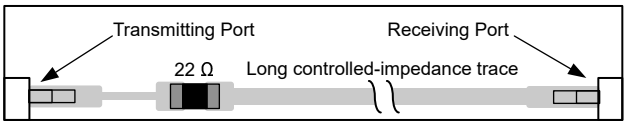


**Figure 7-5. Example Damping Resistor Placement for Improved Signal Integrity**

# 8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 8.1 Documentation Support

### *8.1.1 Related Documentation*

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and $C_{pd}$ Calculation* application report
- Texas Instruments, *Designing With Logic* application report
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application report

## 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 8.4 Trademarks

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## 8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision F (April 2005) to Revision G (January 2025) | Page |
|---|---|
| • Added *Package Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Device Functional Modes,* Application and Implementation section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section | 1 |
| • Deleted references to SN54LV163A product preview | 1 |

# 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN74LV163AD | Obsolete | Production | SOIC (D) \| 16 | - | - | Call TI | Call TI | -40 to 85 | LV163A |
| SN74LV163ADBR | Active | Production | SSOP (DB) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV163A |
| SN74LV163ADBR.A | Active | Production | SSOP (DB) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV163A |
| SN74LV163ADGVR | Active | Production | TVSOP (DGV) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV163A |
| SN74LV163ADGVR.A | Active | Production | TVSOP (DGV) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV163A |
| SN74LV163ADR | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV163A |
| SN74LV163ADR.A | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV163A |
| SN74LV163ANSR | Active | Production | SOP (NS) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 74LV163A |
| SN74LV163ANSR.A | Active | Production | SOP (NS) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 74LV163A |
| SN74LV163APW | Obsolete | Production | TSSOP (PW) \| 16 | - | - | Call TI | Call TI | -40 to 85 | LV163A |
| SN74LV163APWR | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 85 | LV163A |
| SN74LV163APWR.A | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV163A |
| SN74LV163APWRG4 | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | No | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV163A |
| SN74LV163APWRG4 | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV163A |
| SN74LV163APWRG4.A | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | No | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV163A |
| SN74LV163APWRG4.A | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV163A |
| SN74LV163ARGYR | Active | Production | VQFN (RGY) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV163A |
| SN74LV163ARGYR.A | Active | Production | VQFN (RGY) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV163A |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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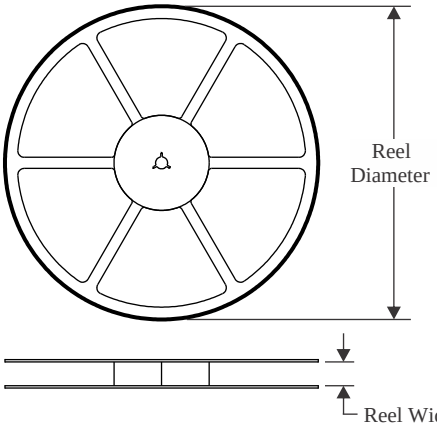
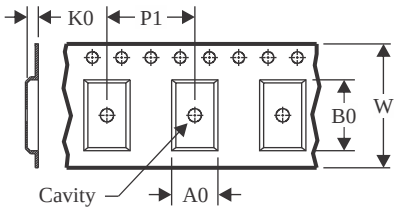
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

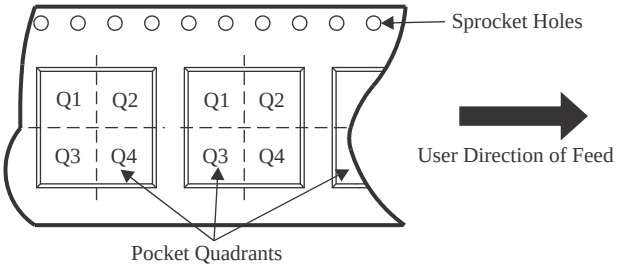



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

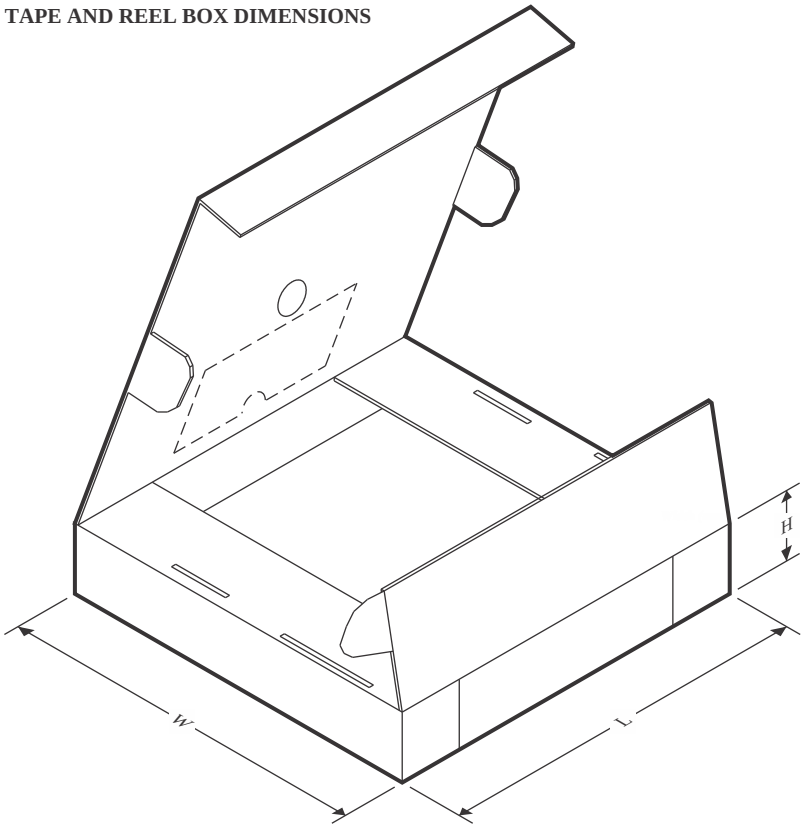
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LV163ADBR | SSOP | DB | 16 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |
| SN74LV163ADGVR | TVSOP | DGV | 16 | 2000 | 330.0 | 12.4 | 6.8 | 4.0 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV163ADR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LV163ANSR | SOP | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LV163APWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV163APWRG4 | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV163ARGYR | VQFN | RGY | 16 | 3000 | 330.0 | 12.4 | 3.8 | 4.3 | 1.5 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

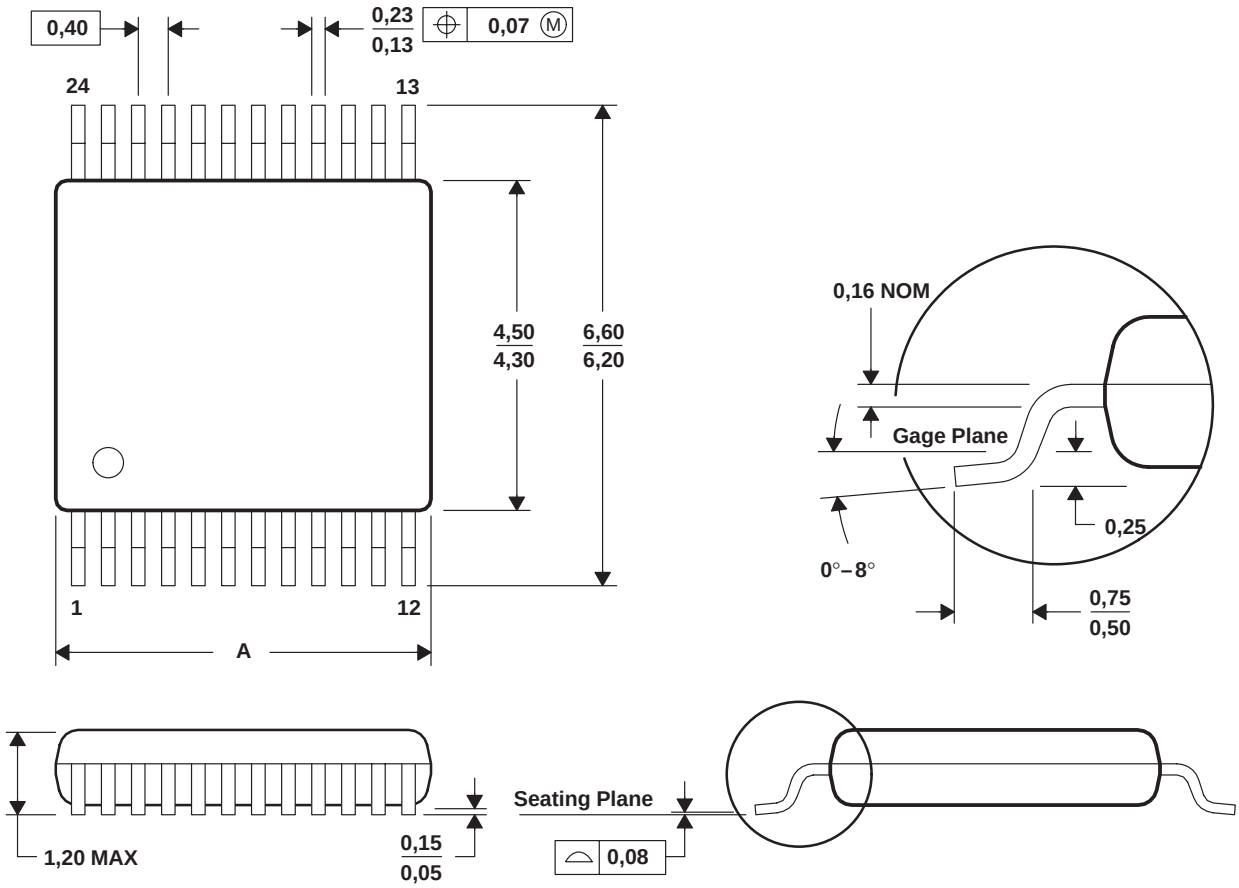



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LV163ADBR | SSOP | DB | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LV163ADGVR | TVSOP | DGV | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LV163ADR | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |
| SN74LV163ANSR | SOP | NS | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LV163APWR | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LV163APWRG4 | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LV163ARGYR | VQFN | RGY | 16 | 3000 | 360.0 | 360.0 | 36.0 |

**DGV (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**24 PINS SHOWN**

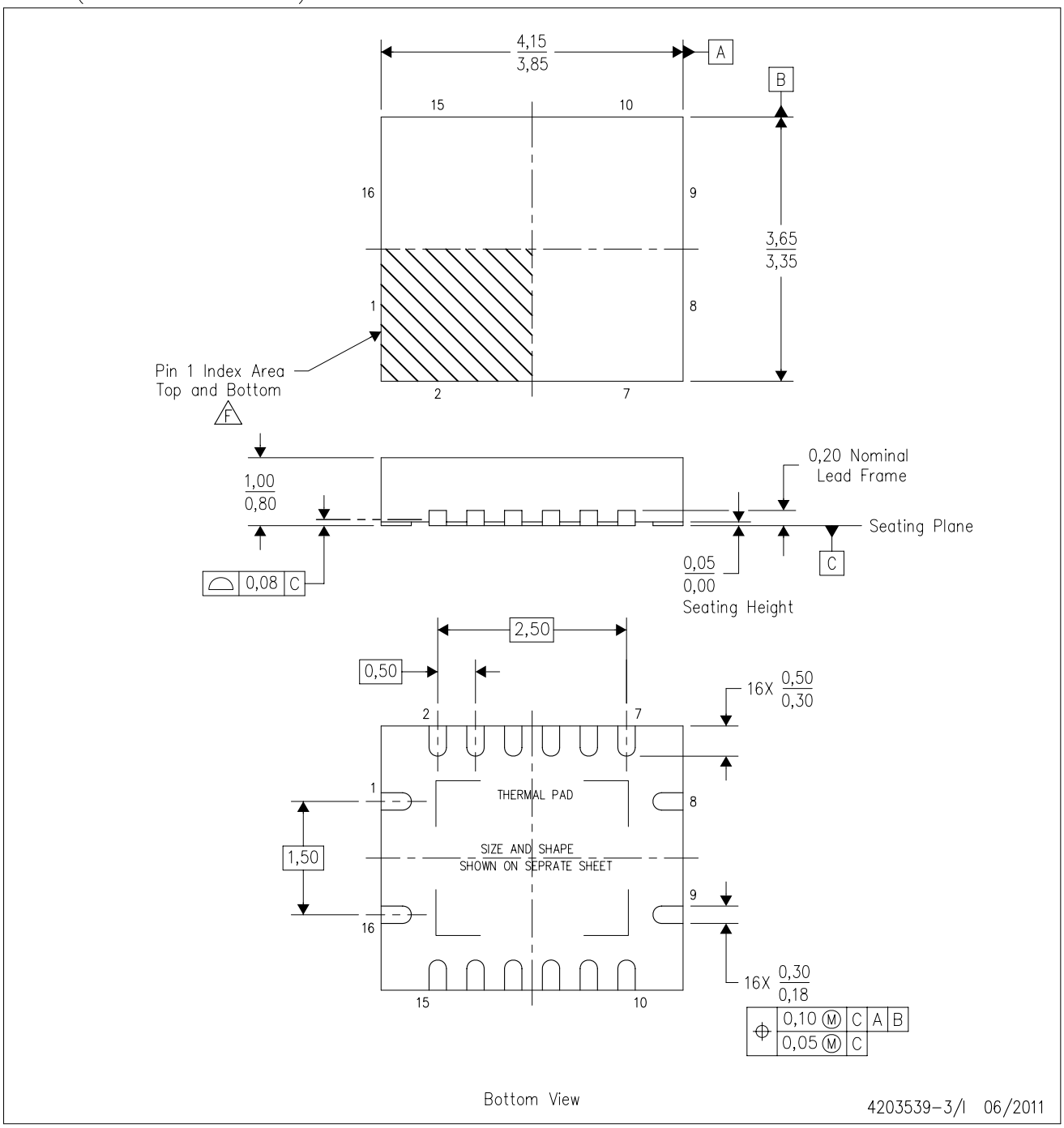



| DIM \ PINS ** | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| A MAX | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| A MIN | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

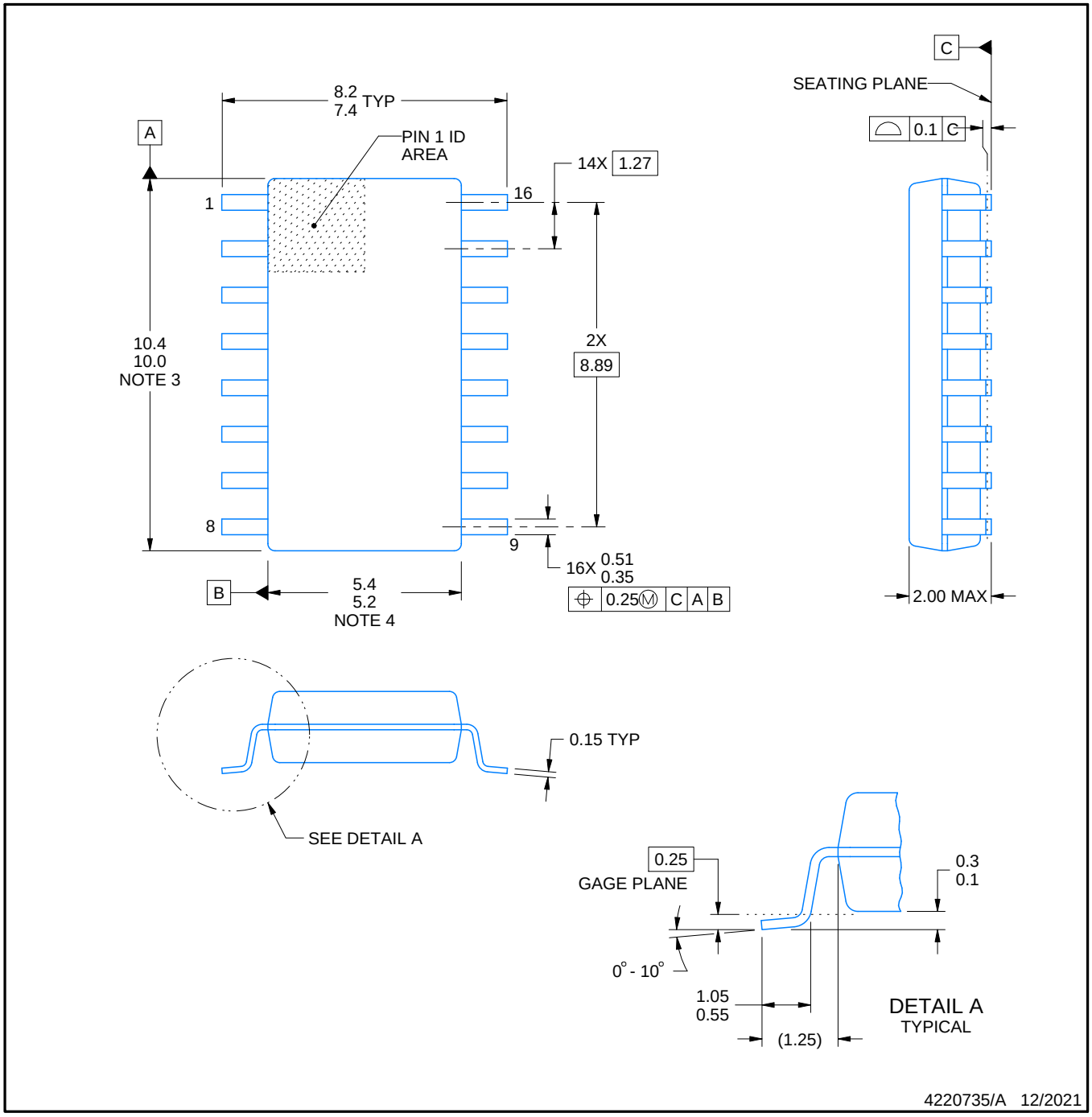
**4073251/E 08/00**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

RGY (R-PVQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD

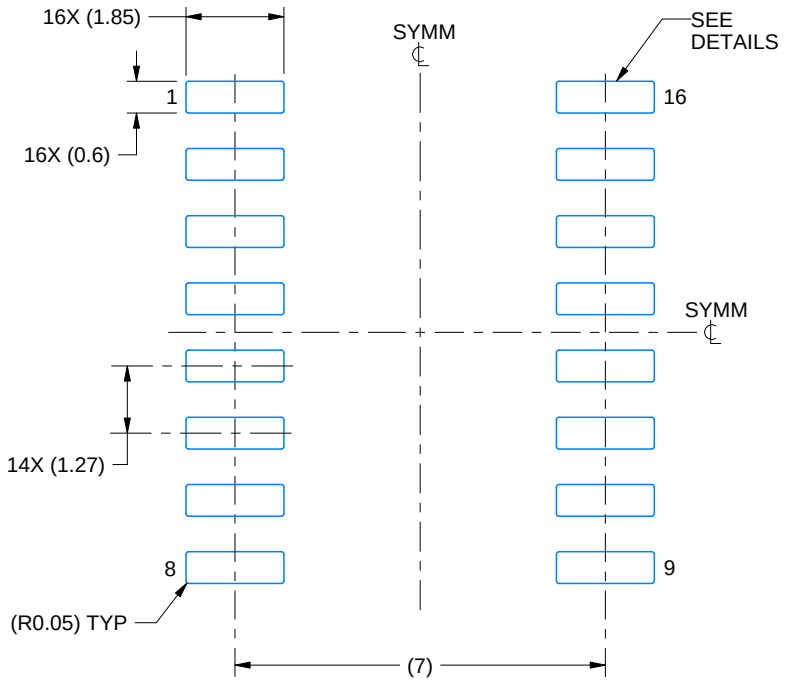



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- G. Package complies to JEDEC MO-241 variation BA.

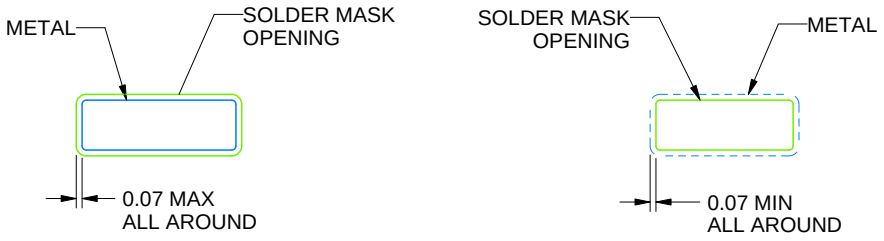



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.




LAND PATTERN EXAMPLE
SCALE:7X




NON SOLDER MASK DEFINED

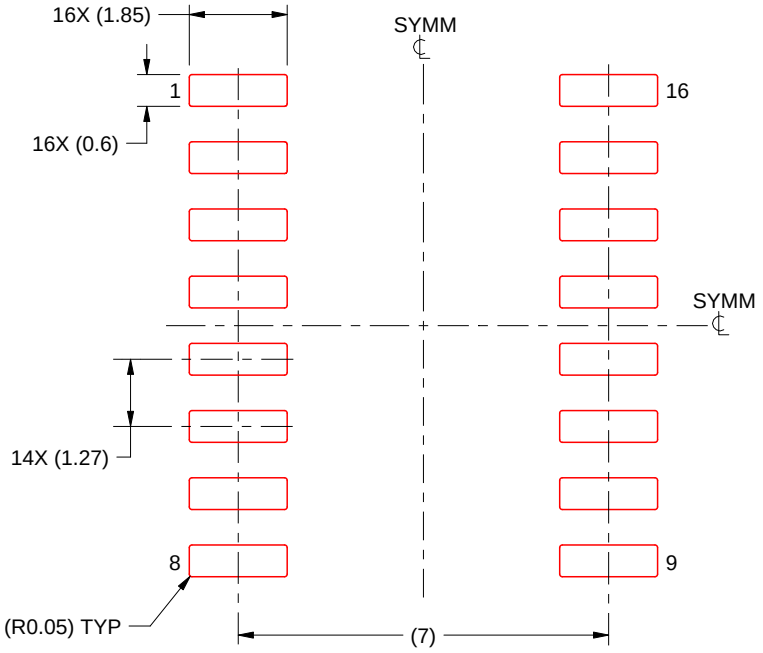
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



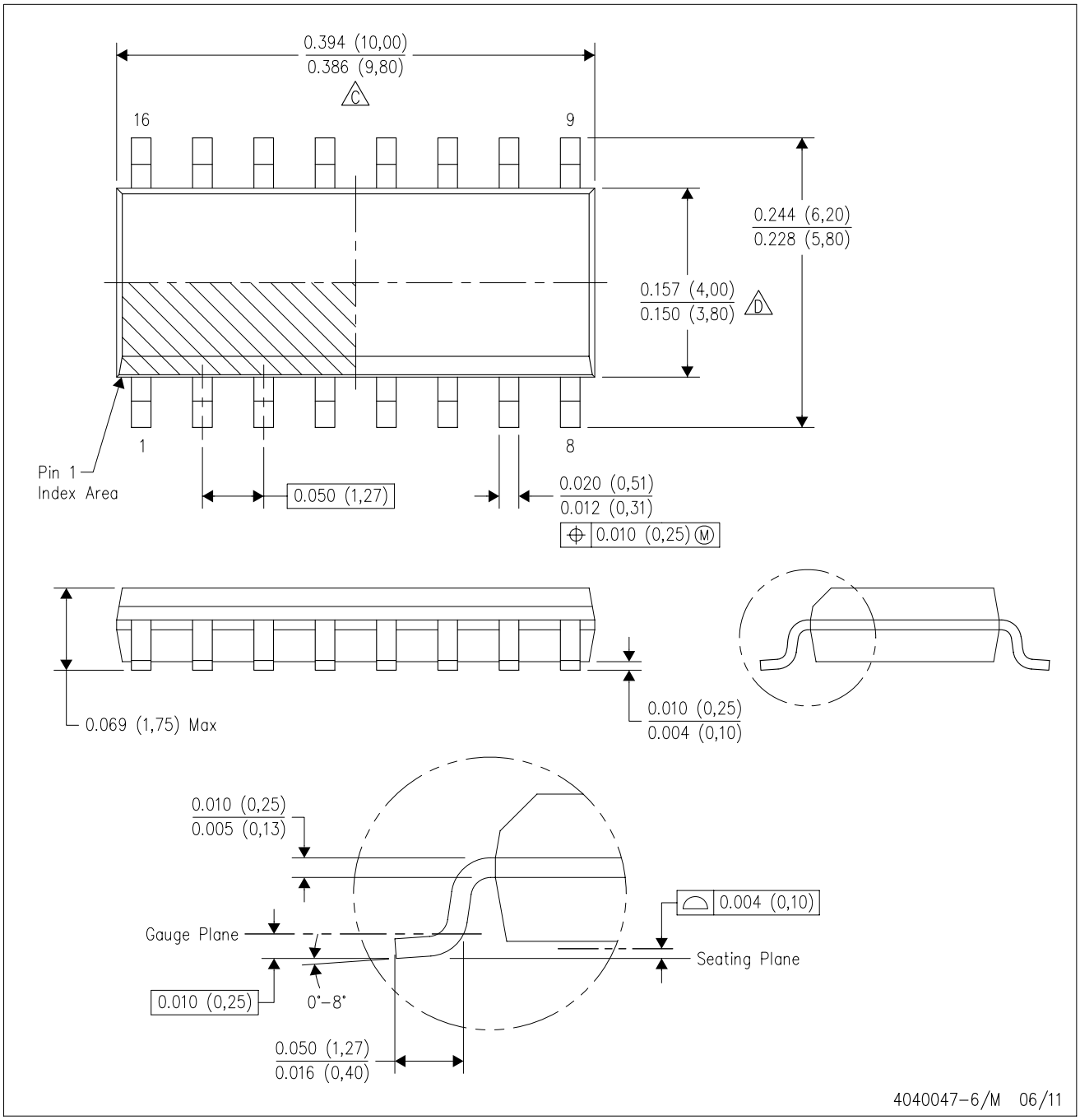

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

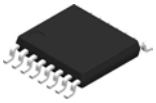
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

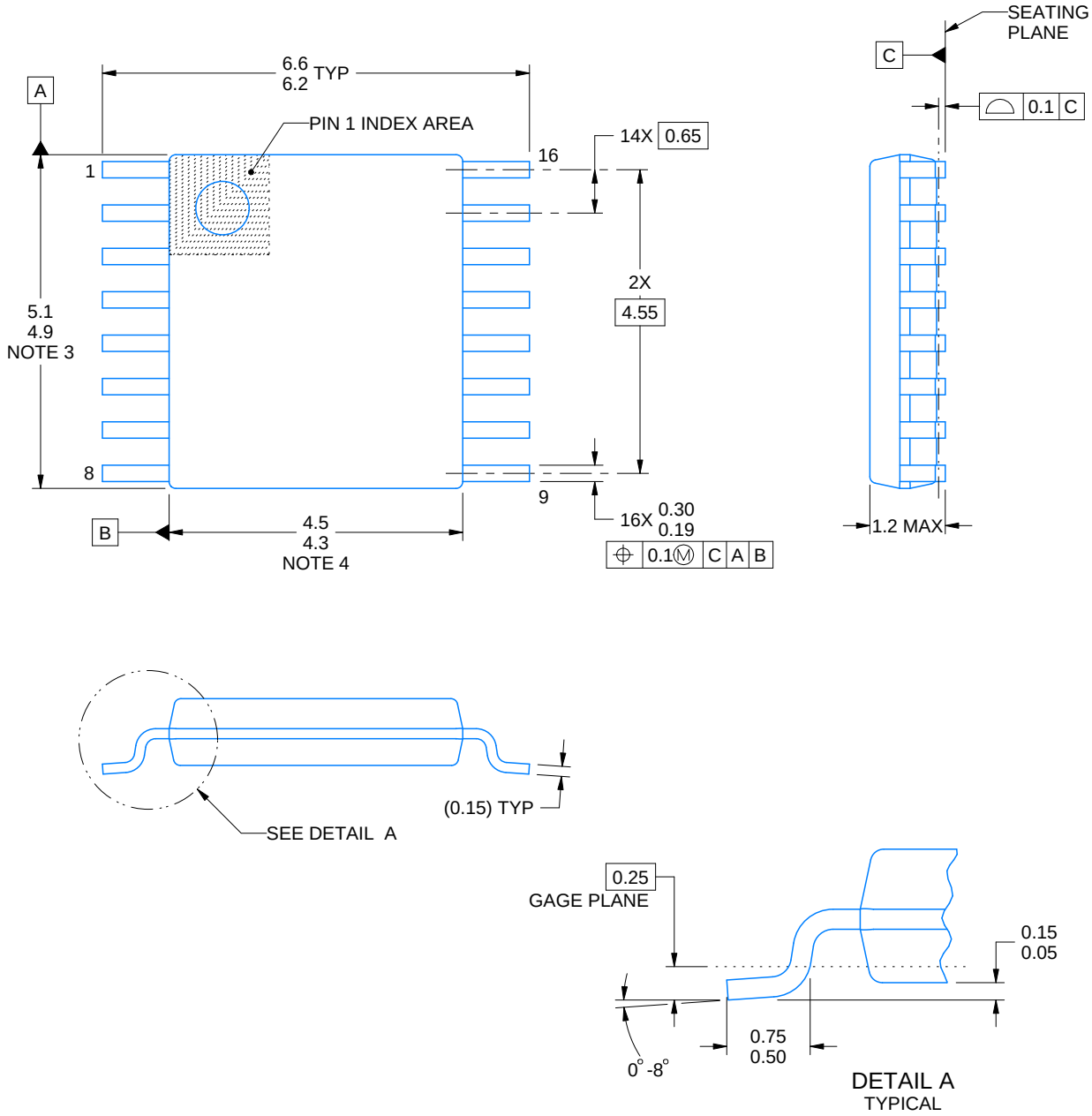
# PW0016A



# PACKAGE OUTLINE

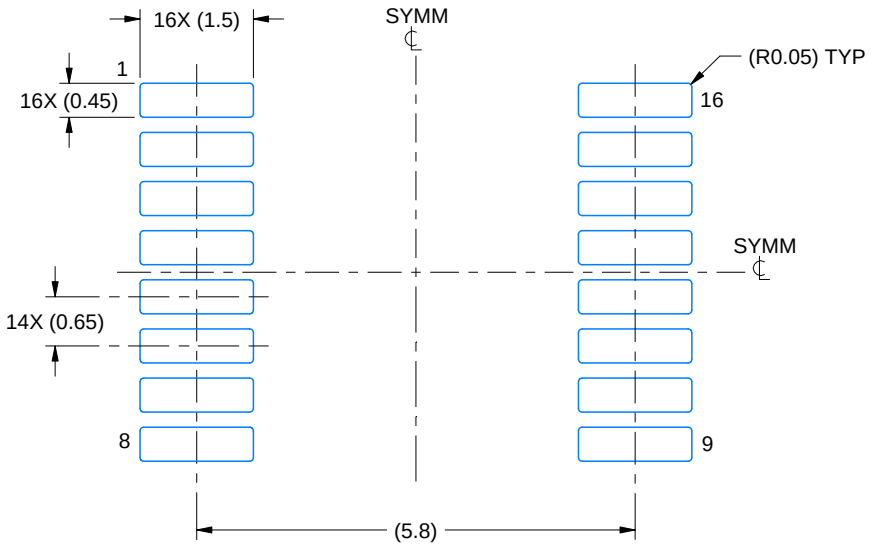
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK DEFINED (PREFERRED)

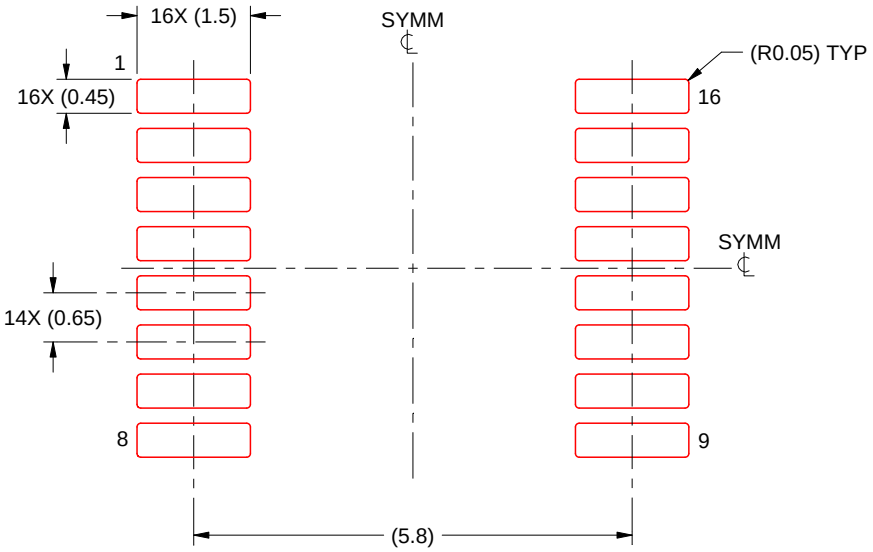
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

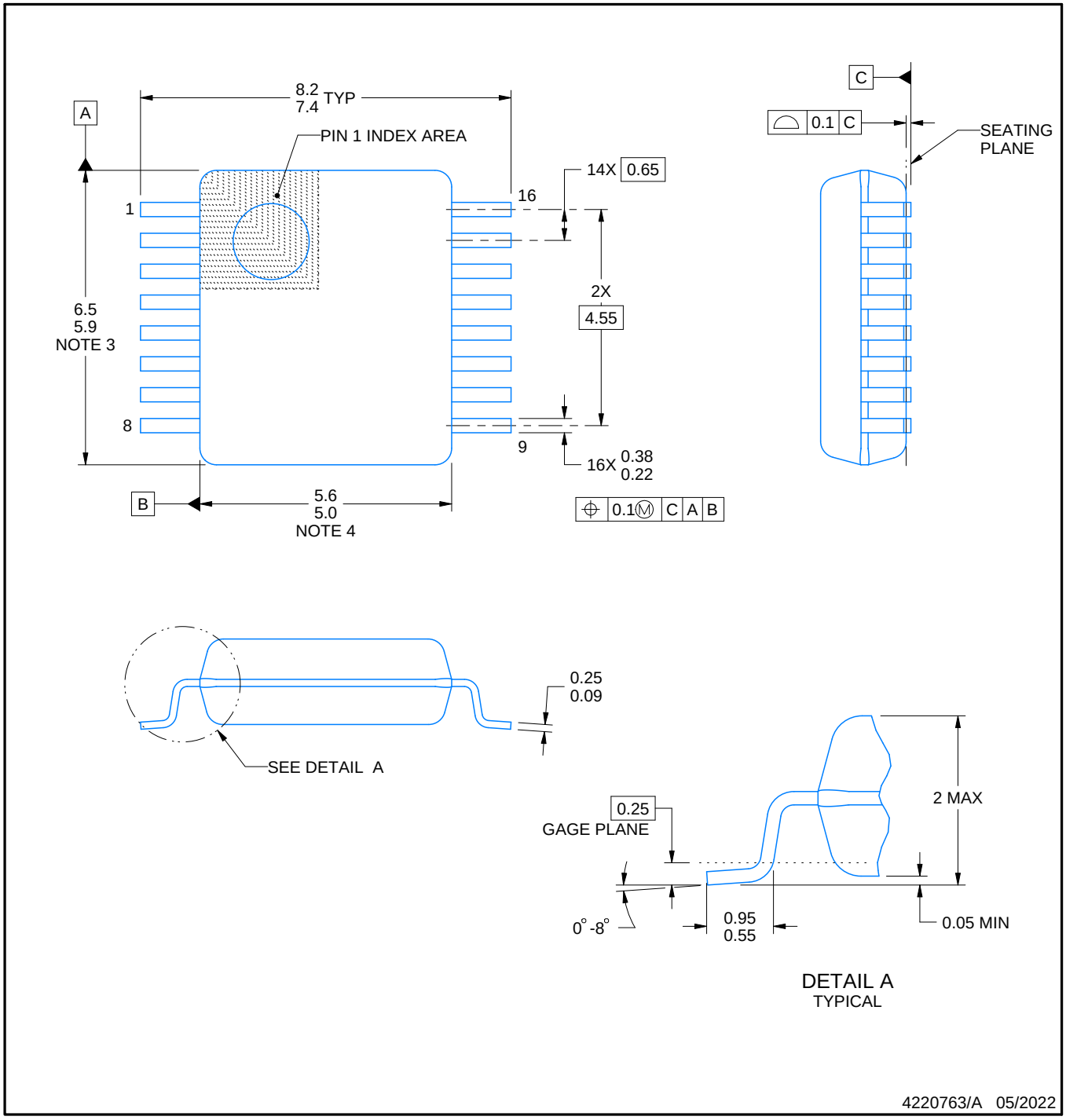



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

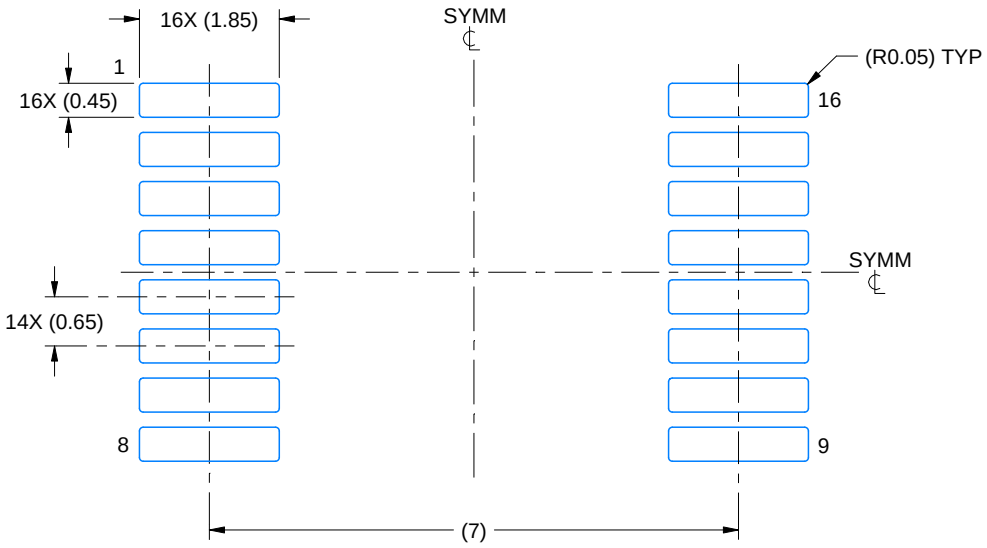
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

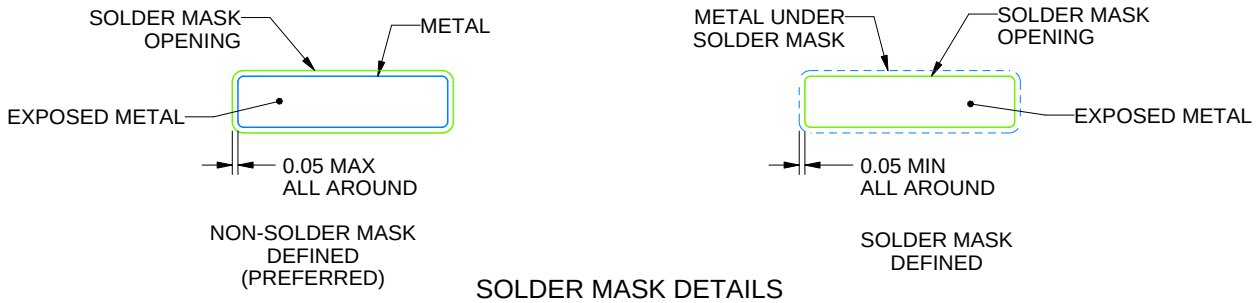



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

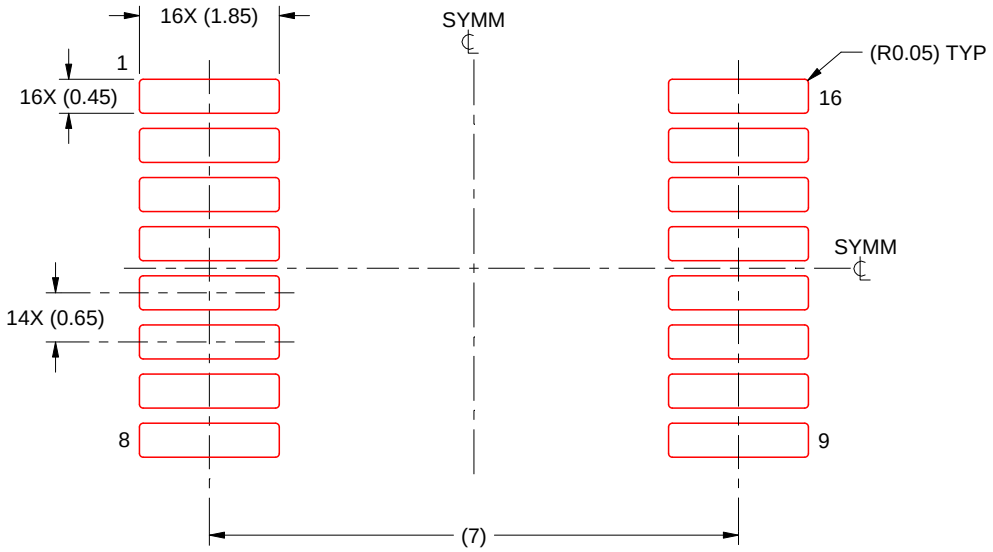



SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

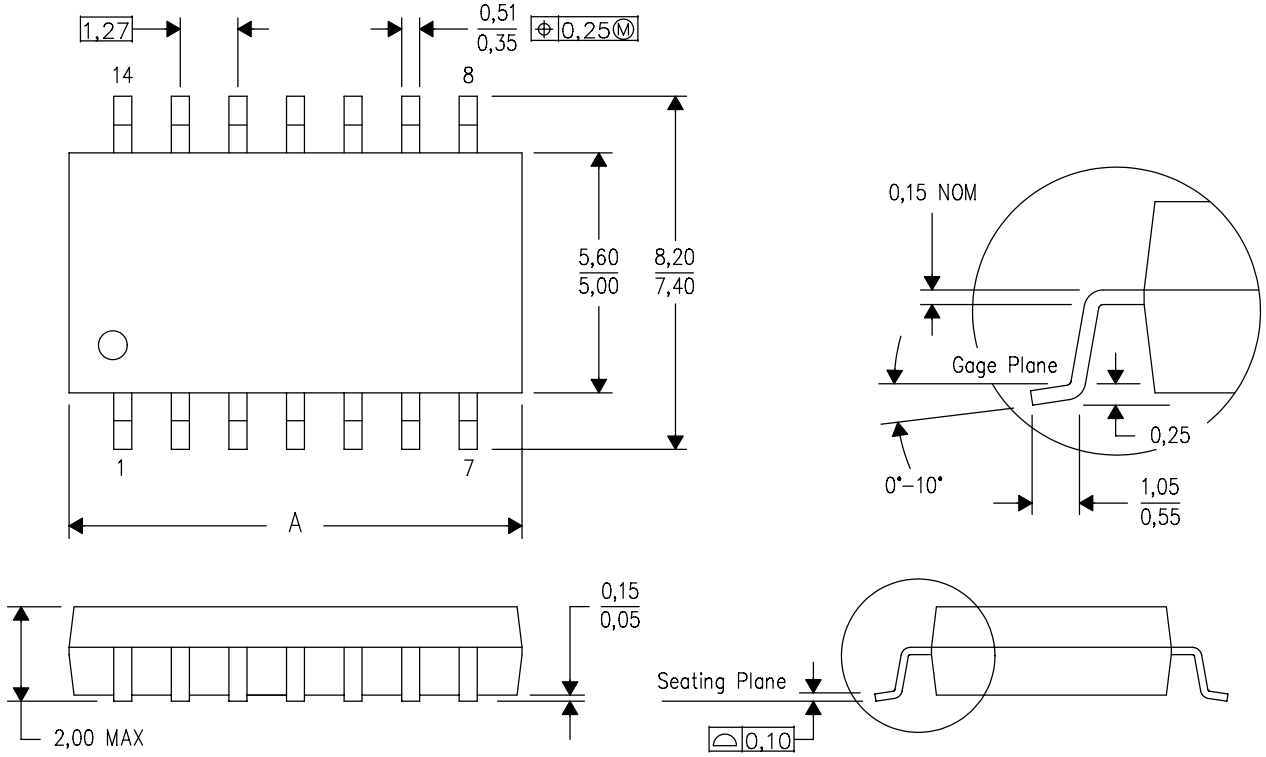
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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