- **Qualified for Automotive Applications**
- **High Slew Rate . . . 10.5 V/µs Typ**
- **High-Gain Bandwidth . . . 5.1 MHz Typ**
- **Supply Voltage Range 2.5 V to 5.5 V**
- **Rail-to-Rail Output**
- **360-µV Input Offset Voltage**
- **Low Distortion Driving 600-Ω . . . 0.005% THD+N**
- **1-mA Supply Current (Per Channel)**
- **17-nV/√Hz Input Noise Voltage**
- **2-pA Input Bias Current**
- **Characterized From T_A = –40°C to 125°C**
- **Available in MSOP and SOT-23 Packages**
- **Micropower Shutdown Mode . . . I_{DD} < 1 µA**

description

The TLV277x CMOS operational amplifier family combines high slew rate and bandwidth, rail-to-rail output swing, high output drive, and excellent dc-precision. The device provides 10.5 V/µs of slew rate and 5.1 MHz of bandwidth while only consuming 1 mA of supply current per channel. This ac-performance is much higher than current competitive CMOS amplifiers. The rail-to-rail output swing and high output drive make these devices a good choice for driving the analog input or reference of analog-to-digital converters. These devices also have low distortion while driving a 600-Ω load for use in telecom systems.

These amplifiers have a 360-µV input offset voltage, a 17 nV/√Hz input noise voltage, and a 2-pA input bias current for measurement, medical, and industrial applications. The TLV277x family is also specified across an extended temperature range (–40°C to 125°C), making it useful for automotive systems.

These devices operate from a 2.5-V to 5.5-V single supply voltage and are characterized at 2.7 V and 5 V. The single-supply operation and low power consumption make these devices a good solution for portable applications. The following table lists the packages available.

FAMILY PACKAGE TABLE

DEVICE	NUMBER OF CHANNELS	PACKAGE TYPES			SHUTDOWN	UNIVERSAL EVM BOARD
		SOIC	TSSOP	SOT-23		
TLV2770	1	8	—	—	Yes	See the EVM Selection Guide (SLOU060)
TLV2771	1	8	—	5	—	
TLV2772	2	8	8	—	—	
TLV2773	2	14	—	—	Yes	
TLV2774	4	14	14	—	—	
TLV2775	4	16	16	—	Yes	

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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A SELECTION OF SINGLE-SUPPLY OPERATIONAL AMPLIFIER PRODUCTS†

DEVICE	V_{DD} (V)	BW (MHz)	SLEW RATE (V/μs)	I_{DD} (per channel) (μA)	RAIL-TO-RAIL
TLV277x	2.5 – 6	5.1	10.5	1000	O
TLV247x	2.7 – 6	2.8	1.5	600	I/O
TLV245x	2.7 – 6	0.22	0.11	23	I/O
TLV246x	2.7 – 6	6.4	1.6	550	I/O

† All specifications measured at 5 V.

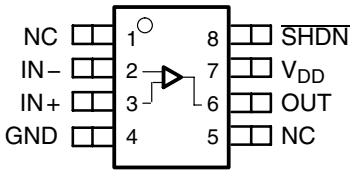
ORDERING INFORMATION†

T_A	V_{IO}max AT 25°C (mV)	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	2.5	SOIC (D)	Tape and reel	TLV2770QDRQ1§	
	1.6	SOIC (D)	Tape and reel	TLV2770AQDRQ1§	
	2.5	SOT-23 (DBV)	Tape and reel	TLV2771QDBVRQ1	VBPQ
	2.5	SOIC (D)	Tape and reel	TLV2771QDRQ1§	
	1.6	SOIC (D)	Tape and reel	TLV2771AQDRQ1§	
	2.5	SOIC (D)	Tape and reel	TLV2772QDRQ1	TLV2772QI
		TSSOP (PW)	Tape and reel	TLV2772QPWRQ1	TLV2772QI
	1.6	SOIC (D)	Tape and reel	TLV2772AQDRQ1	TLV2772AQ
		TSSOP (PW)	Tape and reel	TLV2772AQPWRQ1	TLV2772AQ
	2.5	SOIC (D)	Tape and reel	TLV2773QDRQ1§	
	1.6	SOIC (D)	Tape and reel	TLV2773AQDRQ1§	
	2.7	SOIC (D)	Tape and reel	TLV2774QDRQ1§	
		TSSOP (PW)	Tape and reel	TLV2774QPWRQ1§	
	2.1	SOIC (D)	Tape and reel	TLV2774AQDRQ1§	
		TSSOP (PW)	Tape and reel	TLV2774AQPWRQ1§	
	2.7	SOIC (D)	Tape and reel	TLV2775QDRQ1§	
		TSSOP (PW)	Tape and reel	TLV2775QPWRQ1§	
	2.1	SOIC (D)	Tape and reel	TLV2775AQDRQ1§	
		TSSOP (PW)	Tape and reel	TLV2775AQPWRQ1§	

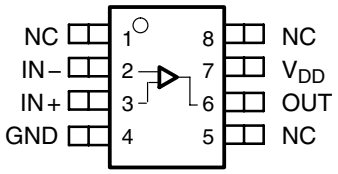
† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.
‡ Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.
§ Product Preview

TLV277x PACKAGE PINOUTS

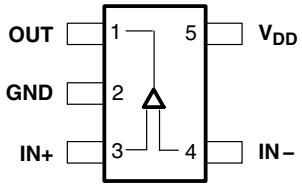
TLV2770†
D PACKAGE
(TOP VIEW)



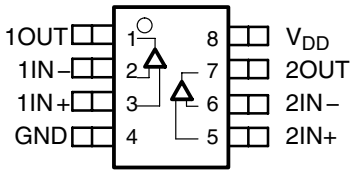
TLV2771†
D PACKAGE
(TOP VIEW)



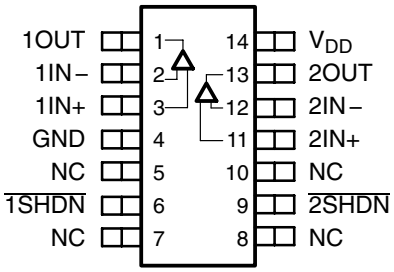
TLV2771
DBV PACKAGE
(TOP VIEW)



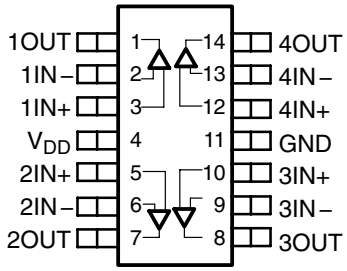
TLV2772
D OR PW PACKAGE
(TOP VIEW)



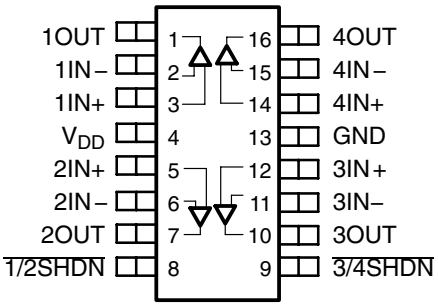
TLV2773†
D PACKAGE
(TOP VIEW)



TLV2774†
D OR PW PACKAGE
(TOP VIEW)



TLV2775†
D OR PW PACKAGE
(TOP VIEW)



NC – No internal connection

† This device is in the Product Preview stage of development. Contact your local Texas Instruments sales office for availability.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 7 V
Differential input voltage, V_{ID} (see Note 2) . . . . . $\pm V_{DD}$
Input voltage range, V_I (any input, see Note 1) . . . . . –0.3 V to V_{DD}
Input current, I_I (any input) . . . . . ±4 mA
Output current, I_O . . . . . ±50 mA
Total current into V_{DD+} . . . . . ±50 mA
Total current out of GND . . . . . ±50 mA
Duration of short-circuit current (at or below) 25°C (see Note 3) . . . . . Unlimited
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: Q suffix . . . . . –40°C to 125°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to GND.
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows when input is brought below GND – 0.3 V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

ESD RATING TABLE

ESD rating	Human Body Model (4)	2 (H1C)	kV
	Charged-Device Model (4)	1 (C5)	
	Machine Model (4)	150 (M2)	V
	Machine Model (5)	100 (M1)	V

NOTE 4: ESD protection level per AEC Q100 Classification TLV2771QDBVRQ1
NOTE 5: ESD protection level per AEC Q100 Classification TLV2772QPWRG4Q1

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
DBV	437 mW	3.5 mW/°C	280 mW	227 mW	87 mW
PW	700 mW	5.6 mW/°C	448 mW	364 mW	140 mW

recommended operating conditions

	Q SUFFIX		UNIT
	MIN	MAX	
Supply voltage, V_{DD}	2.5	6	V
Input voltage range, V_I	GND	$V_{DD+} - 1.3$	V
Common-mode input voltage, V_{IC}	GND	$V_{DD+} - 1.3$	V
Operating free-air temperature, T_A	–40	125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 2.7 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLV2771-Q1			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω V_{DD} = ±1.35 V, No load	25°C		0.48	2.5	mV
			Full range		0.53	2.7	
α_{VIO}	Temperature coefficient of input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω	25°C to 125°C		2		µV/°C
I_{IO}	Input offset current		25°C		1	60	pA
			Full range		2	125	
I_{IB}	Input bias current		25°C		2	60	pA
			Full range		6	350	
V_{OH}	High-level output voltage	I_{OH} = –0.675 mA	25°C		2.6		V
			Full range		2.5		
		I_{OH} = –2.2 mA	25°C		2.4		
			Full range		2.1		
V_{OL}	Low-level output voltage	V_{IC} = 1.35 V, I_{OL} = 0.675 mA	25°C		0.1		V
			Full range		0.2		
		V_{IC} = 1.35 V, I_{OL} = 2.2 mA	25°C		0.21		
			Full range		0.6		
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1.35 V, R_L = 10 kΩ‡, V_O = 0.6 V to 2.1 V	25°C	20	380		V/mV
			Full range	13			
$r_{i(d)}$	Differential input resistance		25°C		10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz	25°C		8		pF
z_o	Closed-loop output impedance	f = 100 kHz, A_V = 10	25°C		25		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.5 V, V_O = V_{DD}/2, R_S = 50 Ω	25°C	60	84		dB
			Full range	60	82		
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} /ΔV_{IO})	V_{DD} = 2.7 V to 5 V, V_{IC} = V_{DD}/2, No load	25°C	70	89		dB
			Full range	70	84		
I_{DD}	Supply current (per channel)	V_O = V_{DD}/2, No load	25°C		1	2	mA
			Full range			2	

† Full range is –40°C to 125°C for Q level part.
‡ Referenced to 1.35 V

operating characteristics at specified free-air temperature, V_{DD} = 2.7 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2771-Q1			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_{O(PP)}$ = 0.8 V, C_L = 100 pF, R_L = 10 kΩ		25°C	5	9		V/µs
				Full range	4.7	6		
V_n	Equivalent input noise voltage	f = 1 kHz		25°C		21		nV/√Hz
		f = 10 kHz		25°C		17		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.33		µV
		f = 0.1 Hz to 10 Hz		25°C		0.86		µV
I_n	Equivalent input noise current	f = 100 Hz		25°C		0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	R_L = 600 Ω, f = 1 kHz	A_V = 1	25°C		0.0085%		
			A_V = 10			0.025%		
			A_V = 100			0.12%		
	Gain-bandwidth product	f = 10 kHz, R_L = 600 Ω, C_L = 100 pF		25°C		4.8		MHz
t_s	Settling time	A_V = –1, Step = 0.85 V to 1.85 V, R_L = 600 Ω, C_L = 100 pF	0.1%	25°C		0.186		µs
			0.01%	25°C		3.92		
ϕ_m	Phase margin at unity gain	R_L = 600 Ω, C_L = 100 pF		25°C		46°		
	Gain margin			25°C		12		dB

† Full range is –40°C to 125°C.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLV2771-Q1			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, No load V_O = 0, R_S = 50 Ω, V_{DD} = ±2.5 V	25°C		0.5	2.5	mV
			Full range		0.6	2.7	
α_{VIO}	Temperature coefficient of input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω, V_{DD} = ±2.5 V	25°C to 125°C		2		μV/°C
I_{IO}	Input offset current		25°C		1	60	pA
			Full range		2	125	
I_{IB}	Input bias current		25°C		2	60	pA
			Full range		6	350	
V_{OH}	High-level output voltage	I_{OH} = –1.3 mA	25°C		4.9		V
			Full range		4.8		
		I_{OH} = –4.2 mA	25°C		4.7		
			Full range		4.4		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 1.3 mA	25°C		0.1		V
			Full range		0.2		
		V_{IC} = 2.5 V, I_{OL} = 4.2 mA	25°C		0.21		
			Full range		0.6		
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, R_L = 10 kΩ‡, V_O = 1 V to 4 V	25°C	20	450		V/mV
			Full range	13			
$r_{i(d)}$	Differential input resistance		25°C		10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz	25°C		8		pF
z_o	Closed-loop output impedance	f = 100 kHz, A_V = 10	25°C		20		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 3.7 V, V_O = V_{DD}/2, R_S = 50 Ω	25°C	60	96		dB
			Full range	60	93		
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} /ΔV_{IO})	V_{DD} = 2.7 V to 5 V, V_{IC} = V_{DD}/2, No load	25°C	70	89		dB
			Full range	70	84		
I_{DD}	Supply current (per channel)	V_O = V_{DD}/2, No load	25°C		1	2	mA
			Full range			2	

† Full range is – 40°C to 125°C for Q level part.
‡ Referenced to 2.5 V

operating characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2771-Q1			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_{O(PP)}$ = 1.5 V, C_L = 100 pF, R_L = 10 kΩ		25°C	5	10.5		V/µs
				Full range	4.7	6		
V_n	Equivalent input noise voltage	f = 1 kHz		25°C		17		nV/√Hz
		f = 10 kHz		25°C		12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.33		µV
		f = 0.1 Hz to 10 Hz		25°C		0.86		µV
I_n	Equivalent input noise current	f = 100 Hz		25°C		0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	R_L = 600 Ω, f = 1 kHz	A_V = 1	25°C		0.005%		
			A_V = 10			0.016%		
			A_V = 100			0.095%		
	Gain-bandwidth product	f = 10 kHz, R_L = 600 Ω, C_L = 100 pF		25°C		5.1		MHz
t_s	Settling time	A_V = –1, Step = 1.5 V to 3.5 V, R_L = 600 Ω, C_L = 100 pF	0.1%	25°C		0.134		µs
			0.01%	25°C		1.97		
ϕ_m	Phase margin at unity gain	R_L = 600 Ω, C_L = 100 pF		25°C		46°		
	Gain margin			25°C		12		dB

† Full range is –40°C to 125°C.

electrical characteristics at specified free-air temperature, V_{DD} = 2.7 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2772-Q1			TLV2772A-Q1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{DD} = ±1.35 V, V_{IC} = 0, R_S = 50 Ω	V_O = 0,	25°C		0.44	2.5		0.44	1.6	mV
				Full range		0.47	2.7		0.47	1.9	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 125°C		2			2		µV/°C
I_{IO}	Input offset current			25°C		1	60		1	60	pA
				Full range		2	125		2	125	
I_{IB}	Input bias current			25°C		2	60		2	60	pA
				Full range		6	350		6	350	
V_{ICR}	Common-mode input voltage range	CMRR > 60 dB,	R_S = 50 Ω	25°C	0 to 1.4	−0.3 to 1.7		0 to 1.4	−0.3 to 1.7		V
				Full range	0 to 1.4	−0.3 to 1.7		0 to 1.4	−0.3 to 1.7		
V_{OH}	High-level output voltage	I_{OH} = −0.675 mA		25°C		2.6			2.6		V
				Full range	2.45			2.45			
		I_{OH} = −2.2 mA		25°C		2.4			2.4		
				Full range	2.1			2.1			
V_{OL}	Low-level output voltage	V_{IC} = 1.35 V,	I_{OL} = 0.675 mA	25°C		0.1			0.1		V
				Full range			0.2			0.2	
		V_{IC} = 1.35 V,	I_{OL} = 2.2 mA	25°C		0.21			0.21		
				Full range			0.6			0.6	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1.35 V, V_O = 0.6 V to 2.1 V	R_L = 10 kΩ,‡	25°C	20	380		20	380		V/mV
				Full range	13			13			
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,		25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		25			25		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} (min), R_S = 50 Ω	V_O = 1.5 V,	25°C	60	84		60	84		dB
				Full range	60	82		60	82		
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} /ΔV_{IO})	V_{DD} = 2.7 V to 5 V, No load	V_{IC} = V_{DD}/2,	25°C	70	89		70	89		dB
				Full range	70	84		70	84		
I_{DD}	Supply current (per channel)	V_O = 1.5 V,	No load	25°C		1	2		1	2	mA
				Full range			2			2	

† Full range is −40°C to 125°C for Q level part.
‡ Referenced to 1.35 V

operating characteristics at specified free-air temperature, V_{DD} = 2.7 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2772-Q1			TLV2772A-Q1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_{O(PP)}$ = 0.8 V, R_L = 10 kΩ, C_L = 100 pF		25°C	5	9		5	9		V/µs
				Full range	4.7	6		4.7	6		
V_n	Equivalent input noise voltage	f = 1 kHz		25°C		21			21		nV/√Hz
		f = 10 kHz		25°C		17			17		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.33			0.33		µV
		f = 0.1 Hz to 10 Hz		25°C		0.86			0.86		µV
I_n	Equivalent input noise current	f = 100 Hz		25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	R_L = 600 Ω, f = 1 kHz	A_V = 1	25°C		0.0085%			0.0085%		
			A_V = 10			0.025%			0.025%		
			A_V = 100			0.12%			0.12%		
	Gain-bandwidth product	f = 10 kHz, R_L = 600 Ω, C_L = 100 pF		25°C		4.8			4.8		MHz
t_s	Settling time	A_V = –1, Step = 0.85 V to 1.85 V, R_L = 600 Ω, C_L = 100 pF	0.1%	25°C		0.186			0.186		µs
			0.01%	25°C		3.92			3.92		
ϕ_m	Phase margin at unity gain	R_L = 600 Ω, C_L = 100 pF		25°C		46°			46°		
	Gain margin			25°C		12			12		dB

† Full range is –40°C to 125°C for Q level part.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2772-Q1			TLV2772A-Q1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{DD} = ±2.5 V, V_{IC} = 0,	V_O = 0, R_S = 50 Ω	25°C		0.36	2.5		0.36	1.6	mV
				Full range		0.4	2.7		0.4	1.9	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 125°C		2			2		µV/°C
I_{IO}	Input offset current			25°C		1	60		1	60	pA
				Full range		2	125		2	125	
I_{IB}	Input bias current			25°C		2	60		2	60	pA
				Full range		6	350		6	350	
V_{ICR}	Common-mode input voltage range	CMRR > 60 dB,	R_S = 50 Ω	25°C	0 to 3.7	−0.3 to 3.8		0 to 3.7	−0.3 to 3.8		V
				Full range	0 to 3.7	−0.3 to 3.8		0 to 3.7	−0.3 to 3.8		
V_{OH}	High-level output voltage	I_{OH} = −1.3 mA		25°C		4.9			4.9		V
				Full range	4.8			4.8			
		I_{OH} = −4.2 mA		25°C		4.7			4.7		
				Full range	4.4			4.4			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 1.3 mA	25°C		0.1			0.1		V
				Full range			0.2			0.2	
		V_{IC} = 2.5 V,	I_{OL} = 4.2 mA	25°C		0.21			0.21		
				Full range			0.6			0.6	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 10 kΩ,‡	25°C	20	450		20	450		V/mV
				Full range	13			13			
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,		25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		20			20		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} (min), R_S = 50 Ω	V_O = 3.7 V,	25°C	60	96		60	96		dB
				Full range	60	93		60	93		
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} /ΔV_{IO})	V_{DD} = 2.7 V to 5 V, No load	V_{IC} = V_{DD}/2,	25°C	70	89		70	89		dB
				Full range	70	84		70	84		
I_{DD}	Supply current (per channel)	V_O = 1.5 V,	No load	25°C		1	2		1	2	mA
				Full range			2			2	

† Full range is −40°C to 125°C for Q level part.
‡ Referenced to 2.5 V

operating characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2772-Q1			TLV2772A-Q1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_{O(PP)}$ = 1.5 V, R_L = 10 kΩ	C_L = 100 pF,	25°C	5	10.5		5	10.5		V/µs
				Full range	4.7	6		4.7	6		
V_n	Equivalent input noise voltage	f = 1 kHz		25°C		17			17		nV/√Hz
		f = 10 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.33			0.33		µV
		f = 0.1 Hz to 10 Hz		25°C		0.86			0.86		µV
I_n	Equivalent input noise current	f = 100 Hz		25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	R_L = 600 Ω, f = 1 kHz	A_V = 1	25°C		0.005%			0.005%		
			A_V = 10			0.016%			0.016%		
			A_V = 100			0.095%			0.095%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF	R_L = 600 Ω,	25°C		5.1			5.1		MHz
t_s	Settling time	A_V = –1, Step = 1.5 V to 3.5 V, R_L = 600 Ω, C_L = 100 pF	0.1%	25°C		0.134			0.134		µs
			0.01%	25°C		1.97			1.97		
ϕ_m	Phase margin at unity gain	R_L = 600 Ω,	C_L = 100 pF	25°C		46°			46°		
	Gain margin			25°C		12			12		dB

† Full range is –40°C to 125°C for Q level part.

TYPICAL CHARACTERISTICS

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TYPICAL CHARACTERISTICS

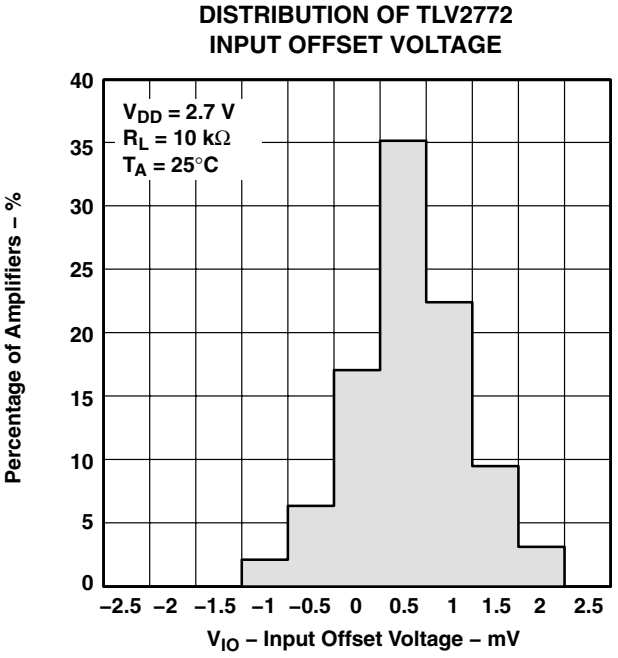


Figure 1

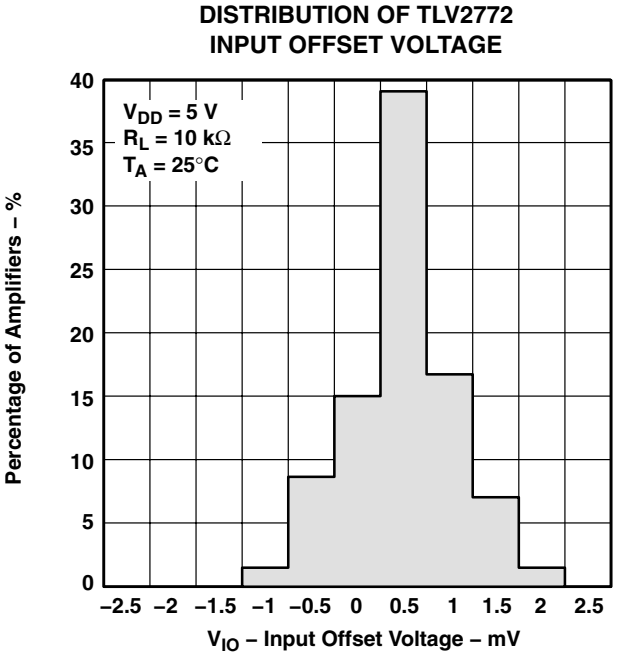


Figure 2

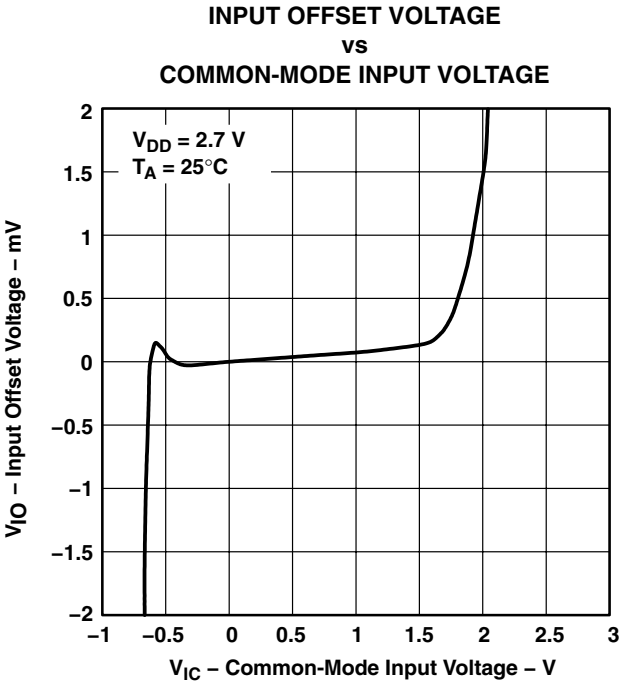


Figure 3

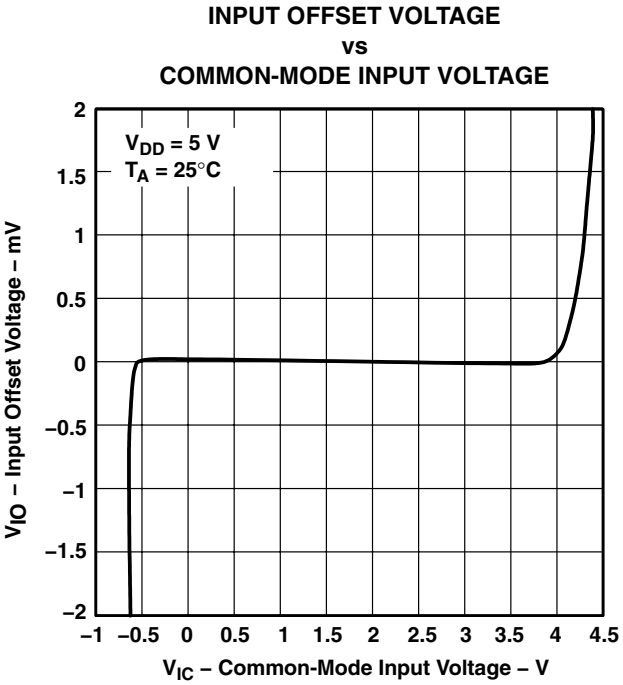


Figure 4

TYPICAL CHARACTERISTICS

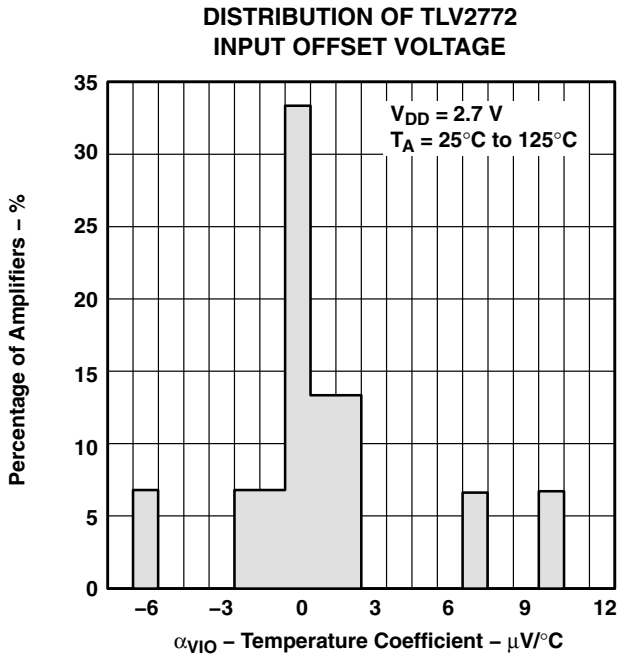


Figure 5

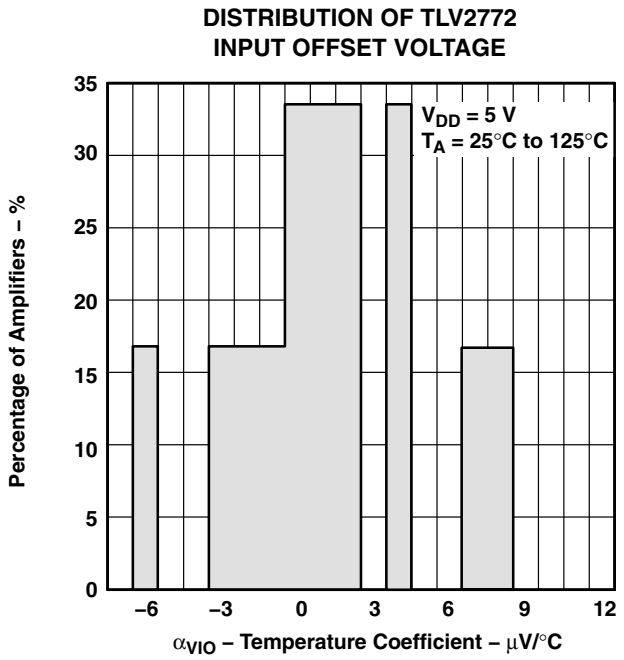


Figure 6

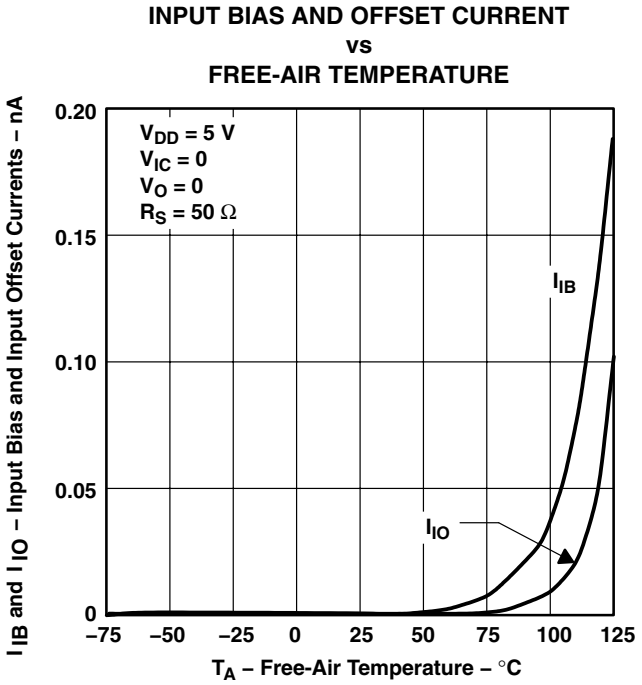


Figure 7

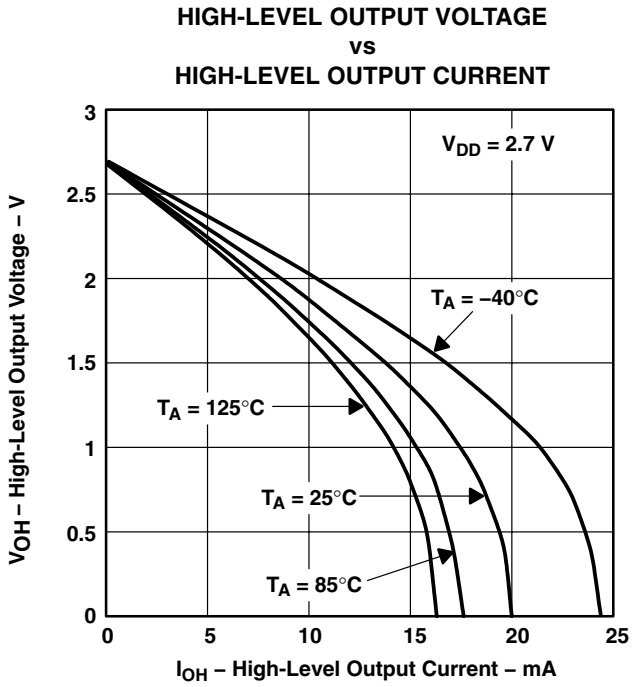


Figure 8

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

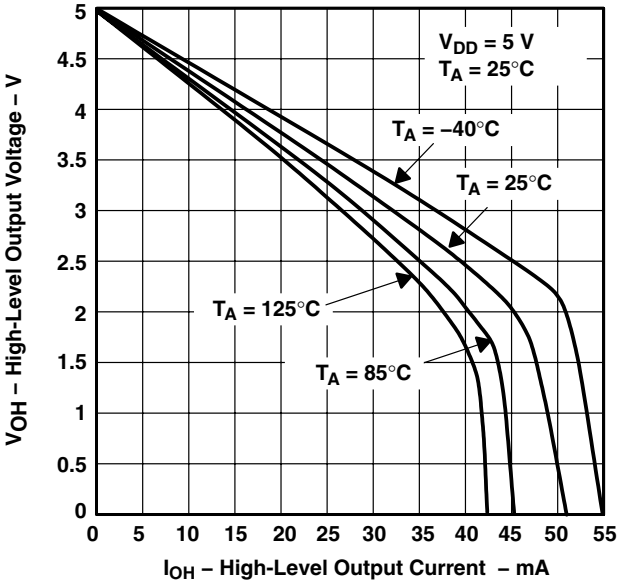


Figure 9

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

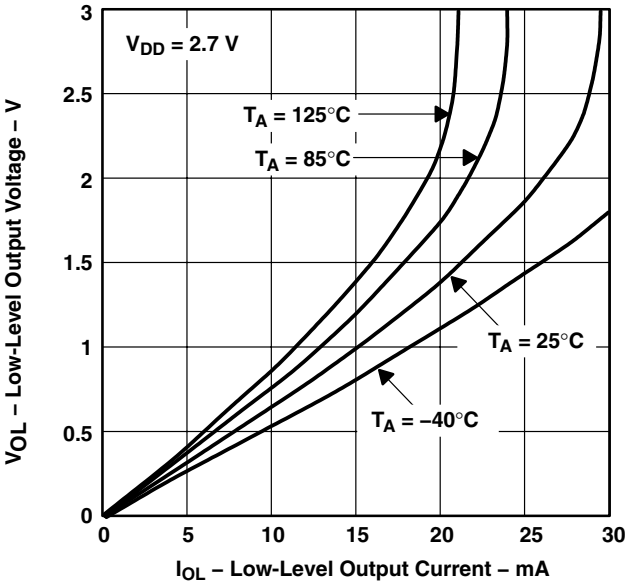


Figure 10

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

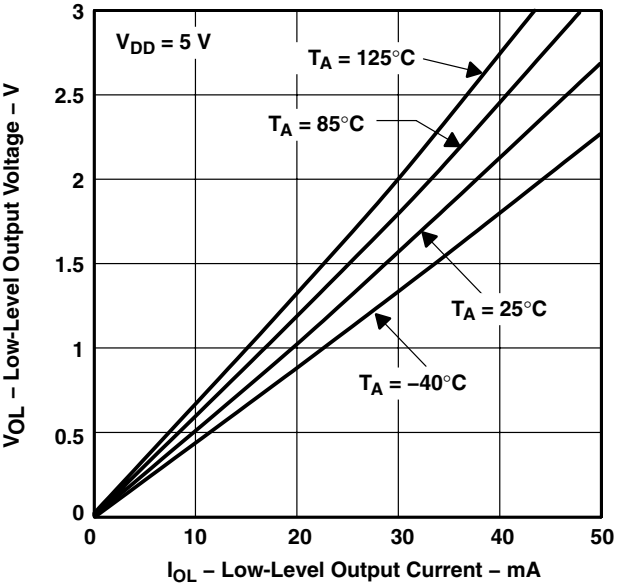


Figure 11

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

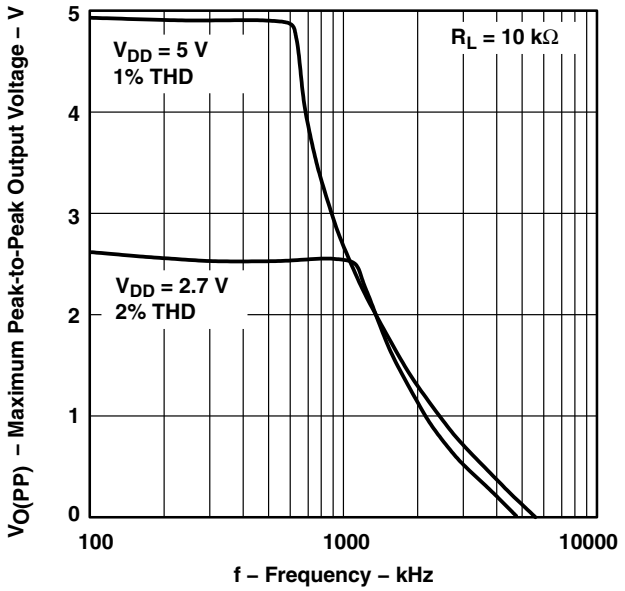


Figure 12

TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

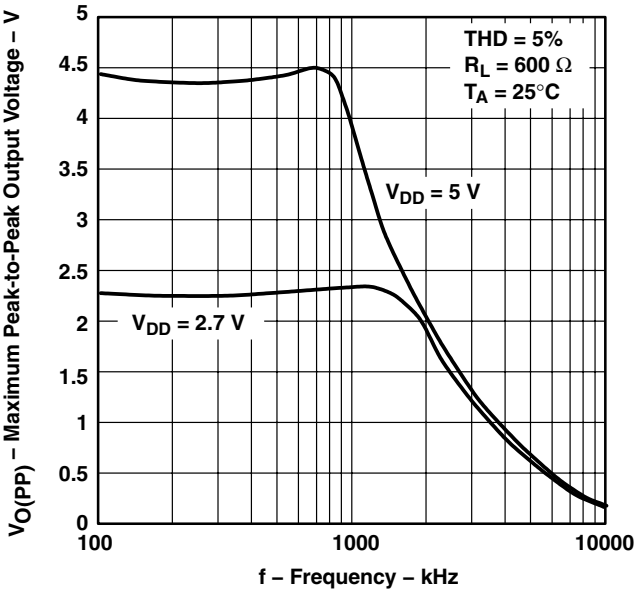


Figure 13

SHORT-CIRCUIT OUTPUT CURRENT vs SUPPLY VOLTAGE

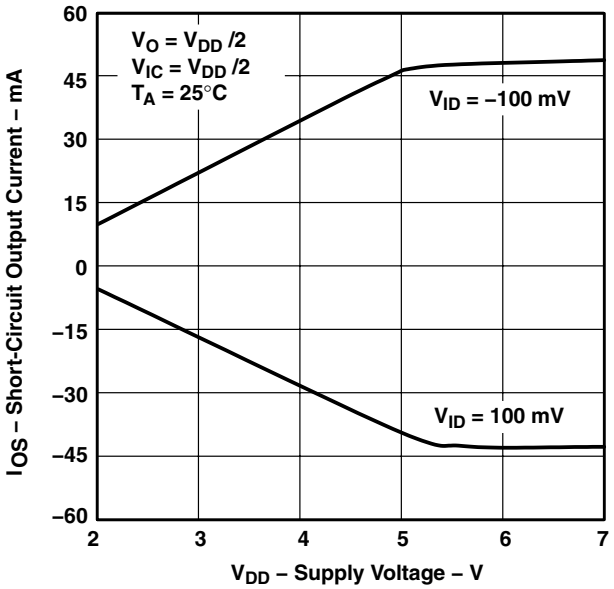


Figure 14

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

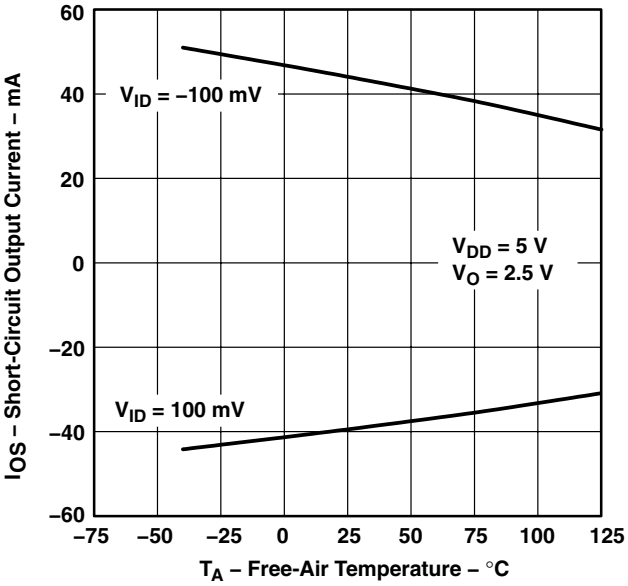


Figure 15

OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

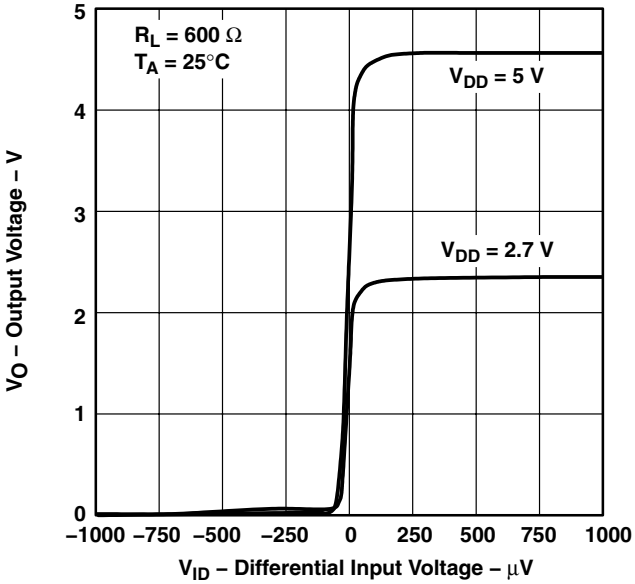


Figure 16

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

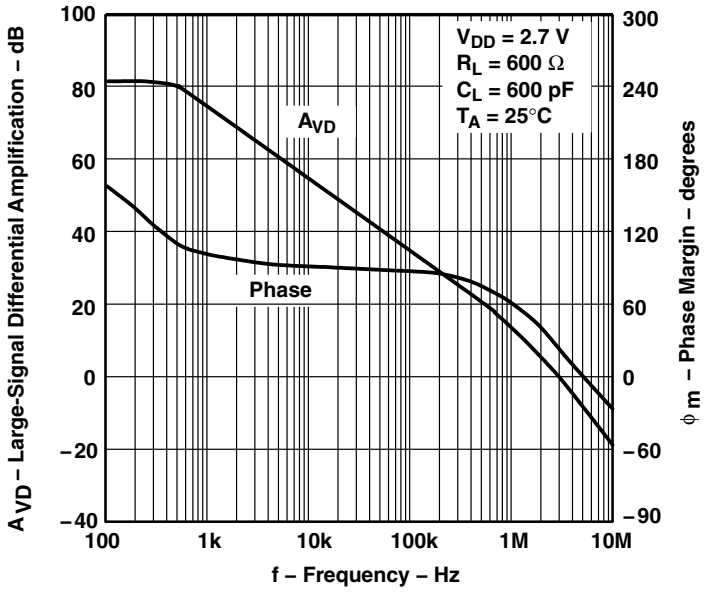


Figure 17

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

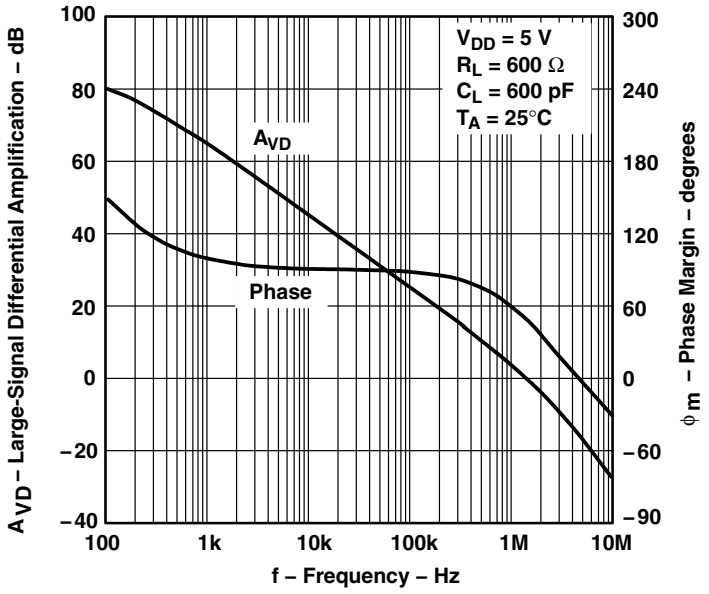


Figure 18

TYPICAL CHARACTERISTICS

DIFFERENTIAL VOLTAGE AMPLIFICATION vs LOAD RESISTANCE

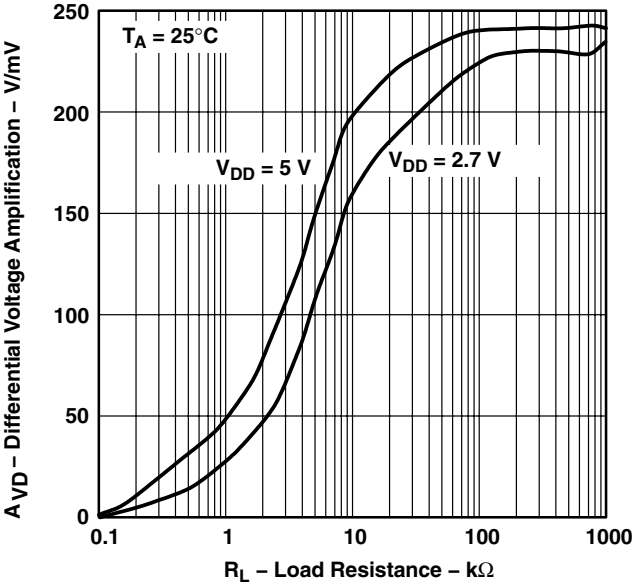


Figure 19

DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

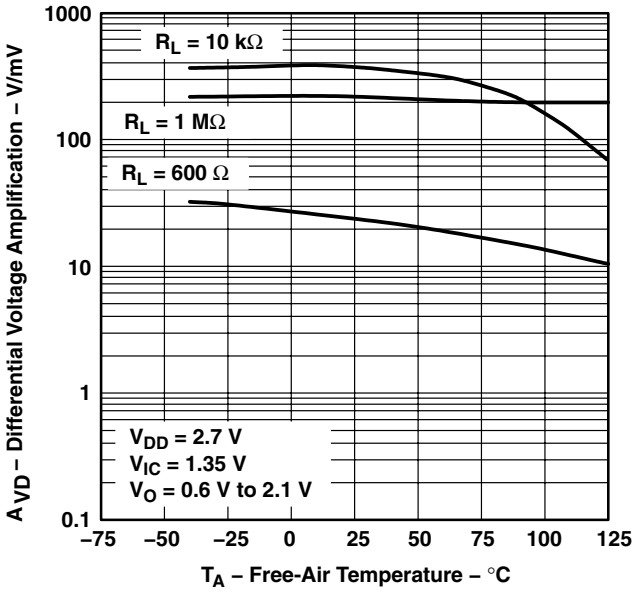


Figure 20

DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

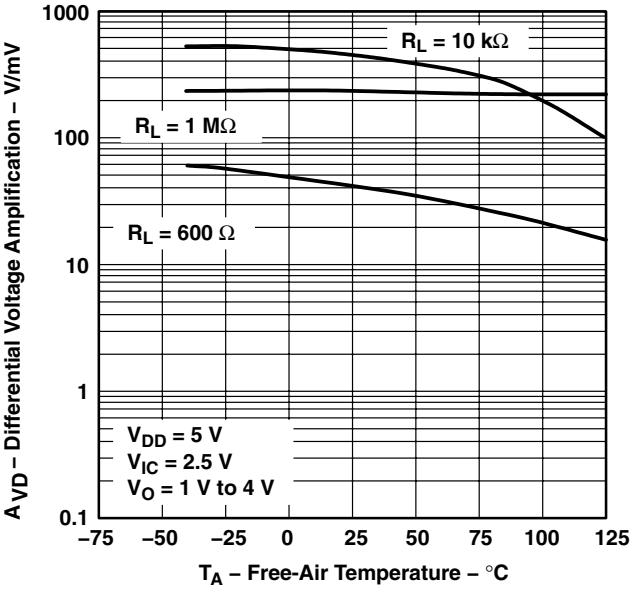


Figure 21

OUTPUT IMPEDANCE vs FREQUENCY

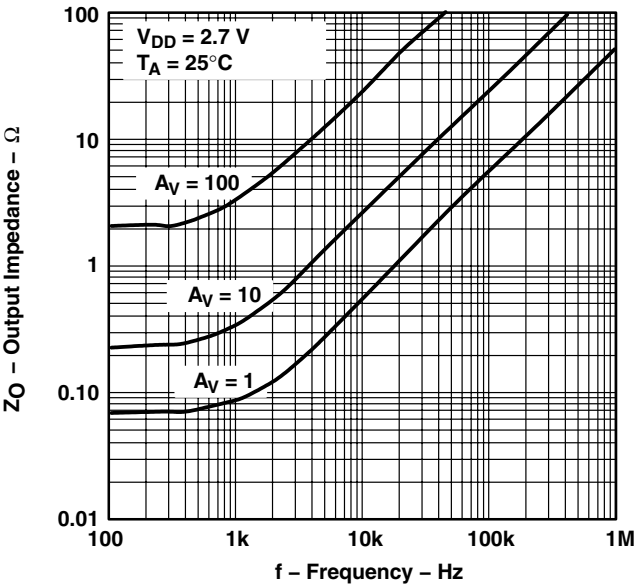


Figure 22

TYPICAL CHARACTERISTICS

OUTPUT IMPEDANCE vs FREQUENCY

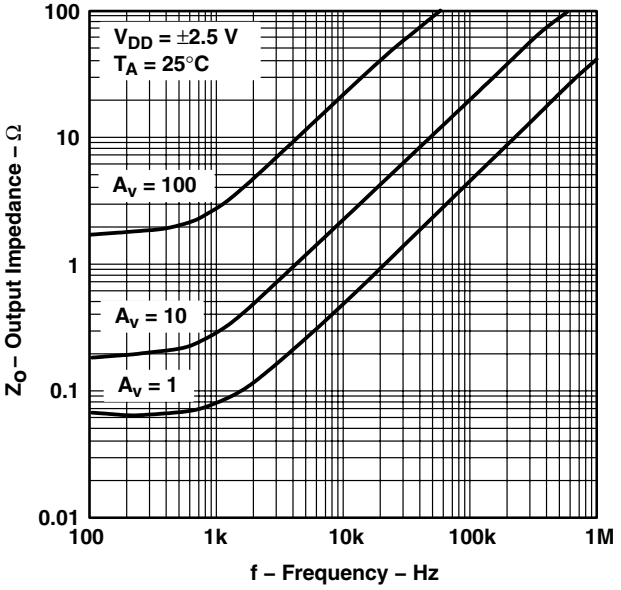


Figure 23

COMMON-MODE REJECTION RATIO vs FREQUENCY

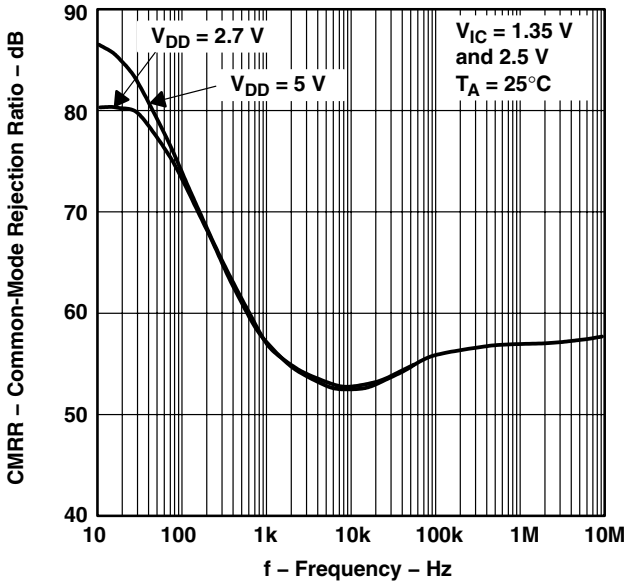


Figure 24

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

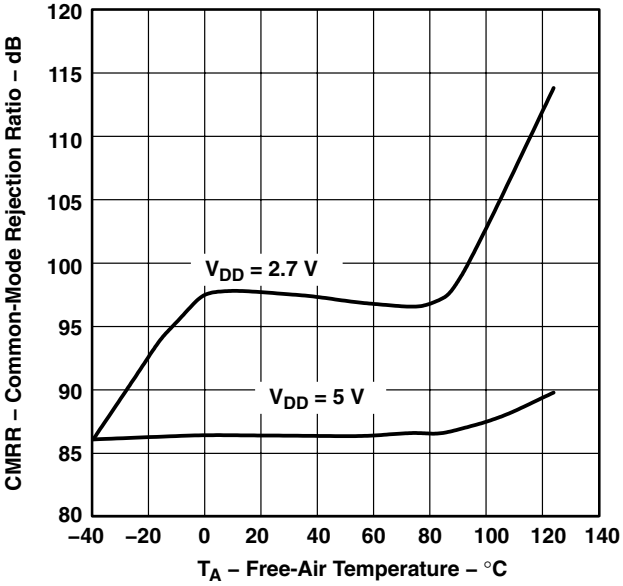


Figure 25

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

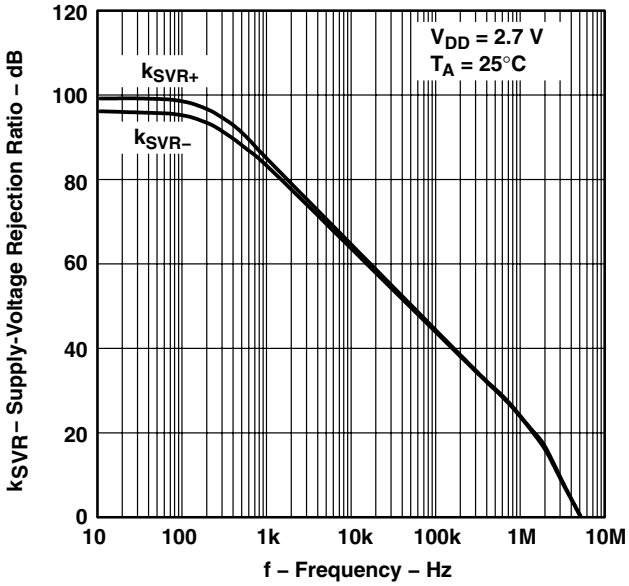


Figure 26

TYPICAL CHARACTERISTICS

SUPPLY VOLTAGE REJECTION RATIO vs FREQUENCY

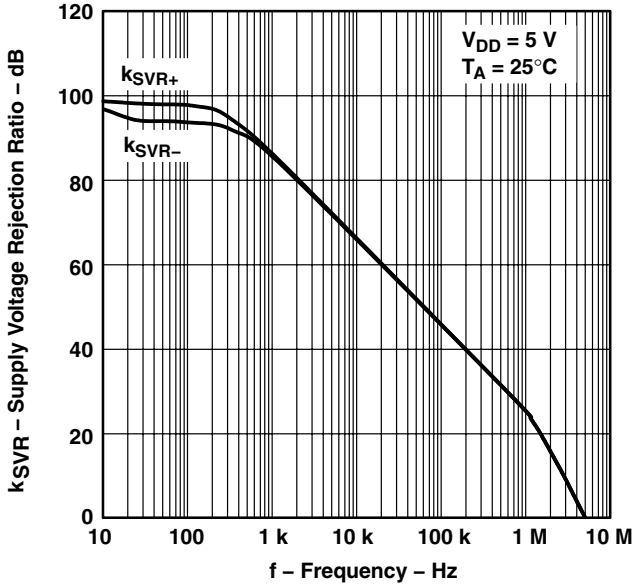


Figure 27

SUPPLY CURRENT (PER CHANNEL) vs SUPPLY VOLTAGE

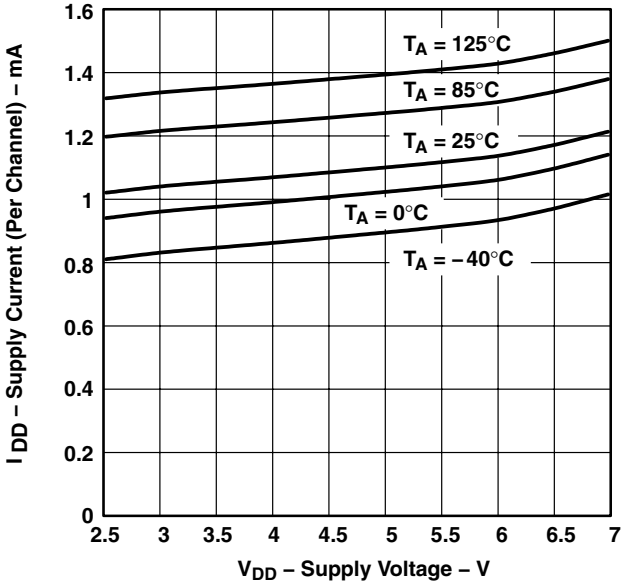


Figure 28

SLEW RATE vs LOAD CAPACITANCE

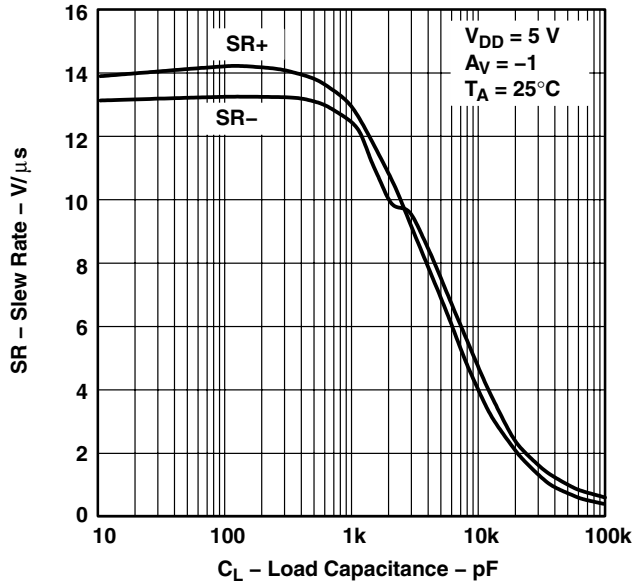


Figure 29

SLEW RATE vs FREE-AIR TEMPERATURE

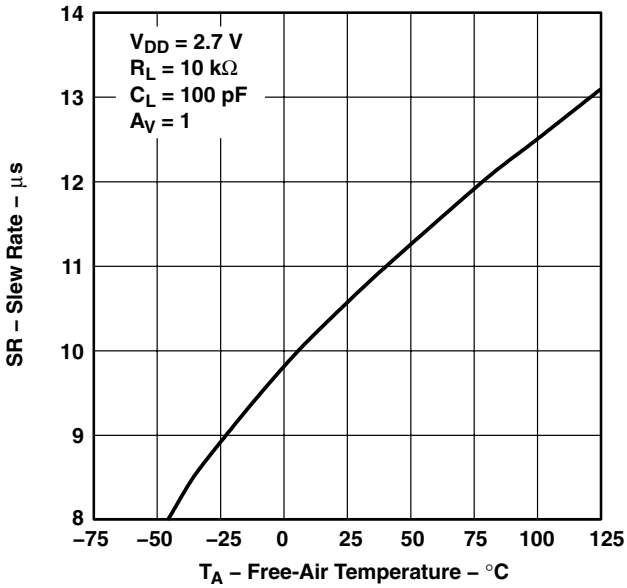


Figure 30

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

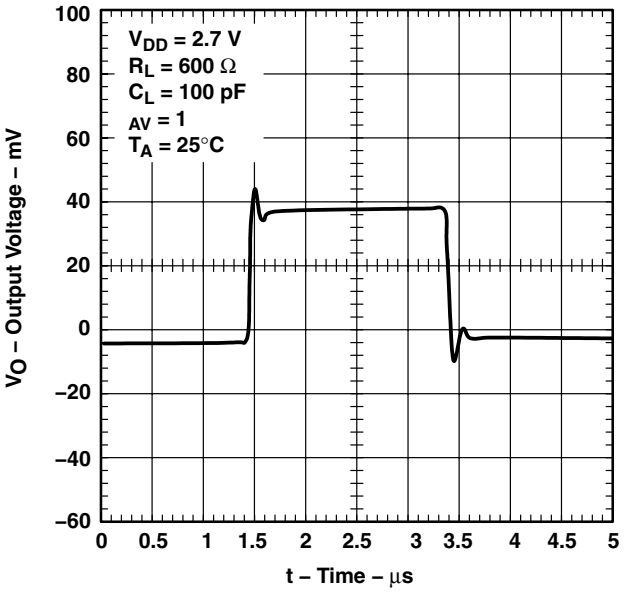


Figure 31

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

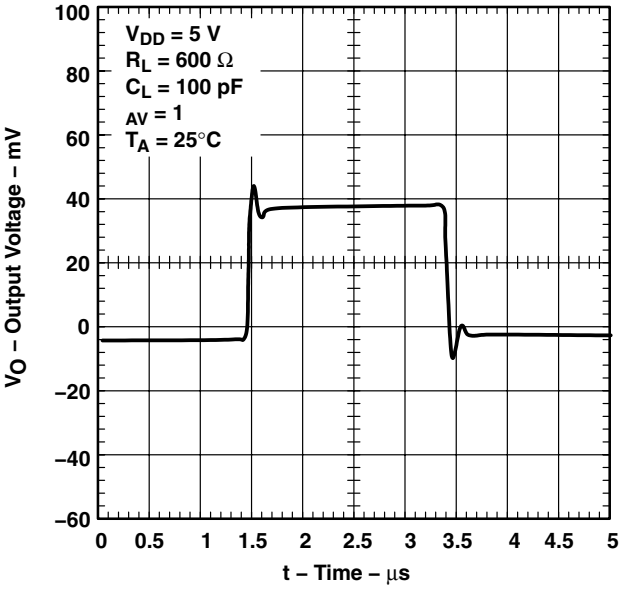


Figure 32

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

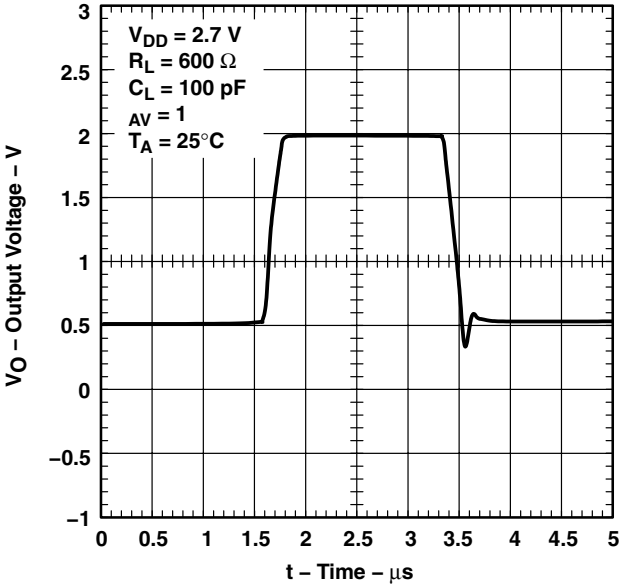


Figure 33

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

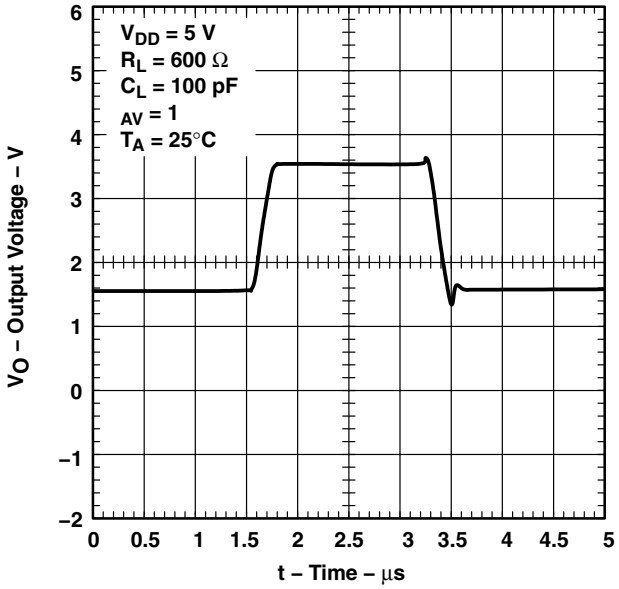


Figure 34

TYPICAL CHARACTERISTICS

INVERTING SMALL-SIGNAL PULSE RESPONSE

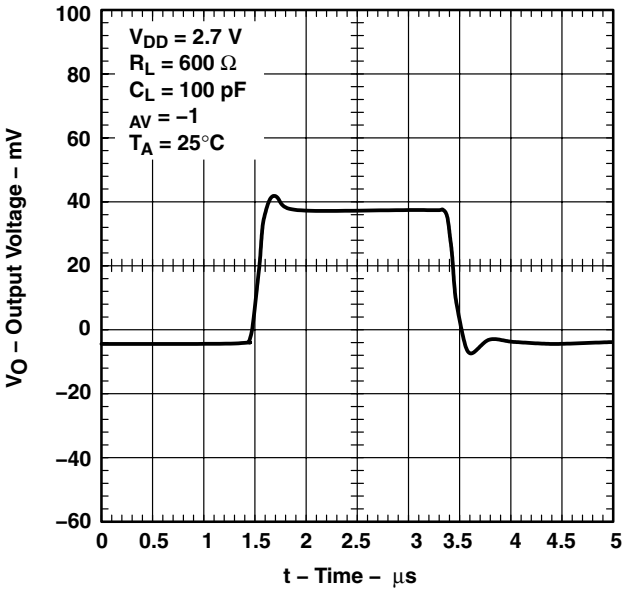


Figure 35

INVERTING SMALL-SIGNAL PULSE RESPONSE

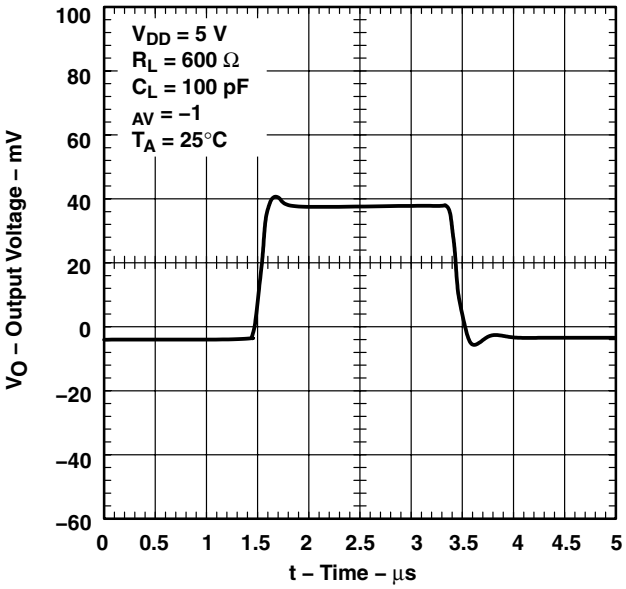


Figure 36

INVERTING LARGE-SIGNAL PULSE RESPONSE

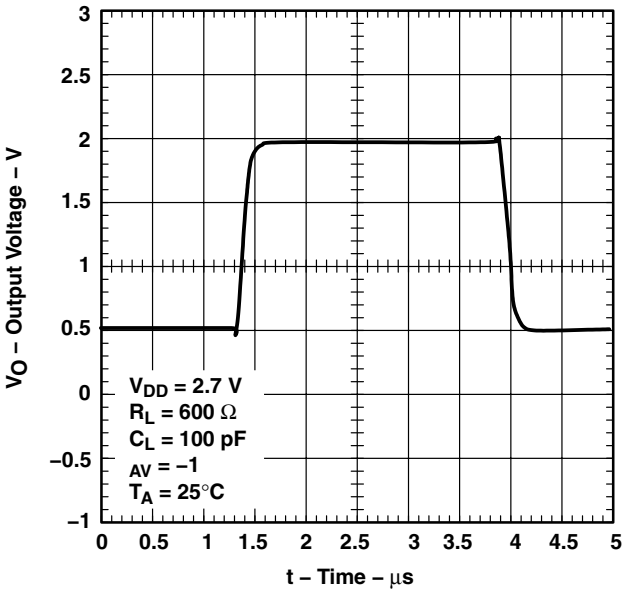


Figure 37

INVERTING LARGE-SIGNAL PULSE RESPONSE

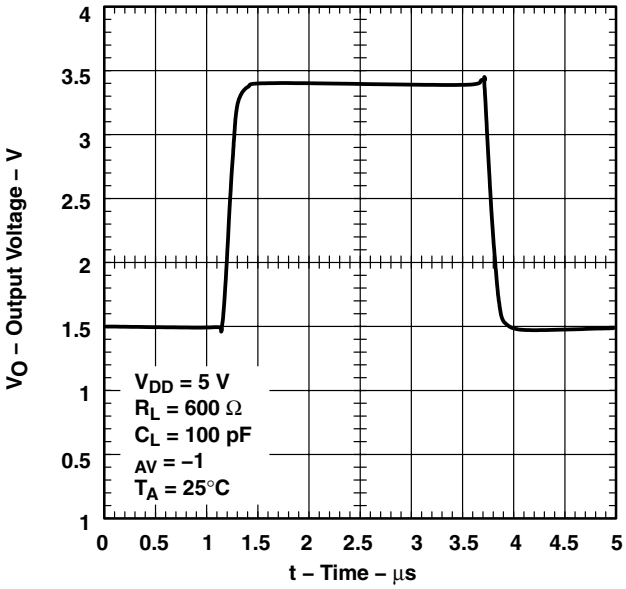


Figure 38

TYPICAL CHARACTERISTICS

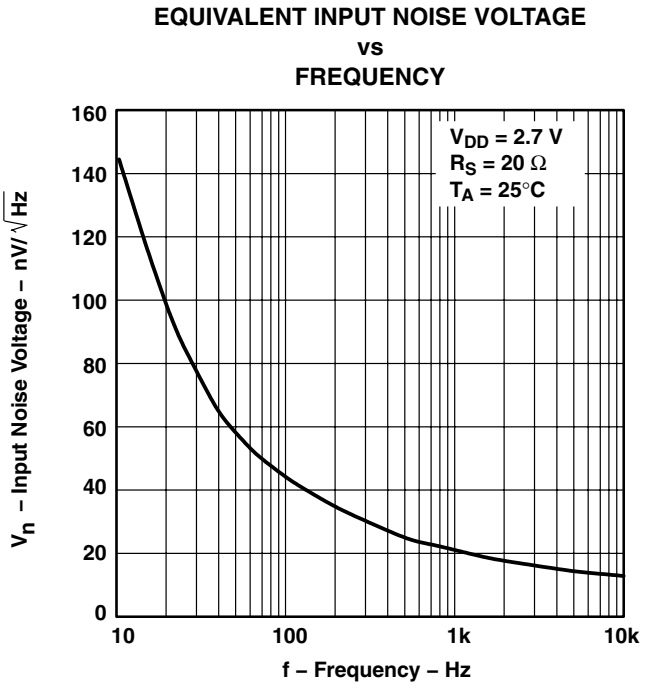


Figure 39

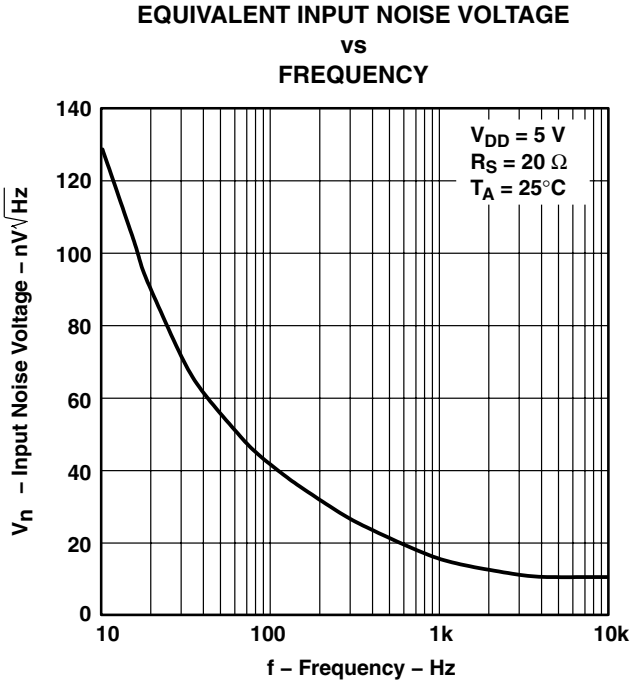


Figure 40

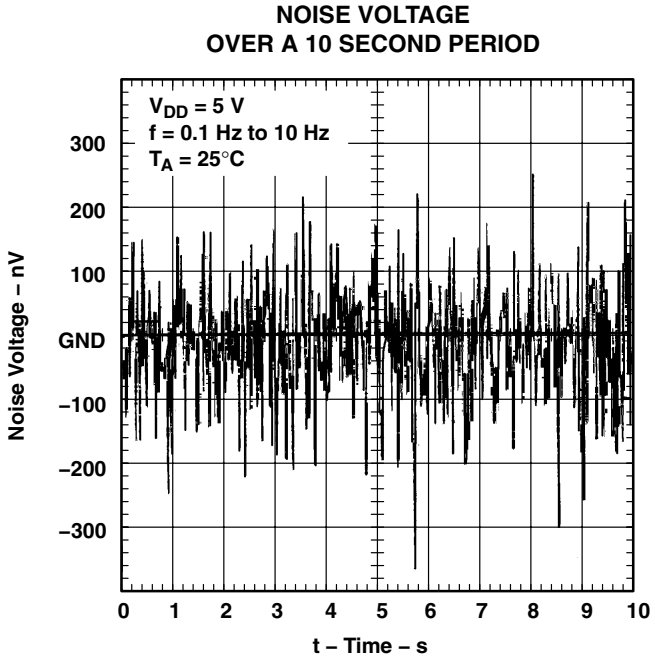


Figure 41

TYPICAL CHARACTERISTICS

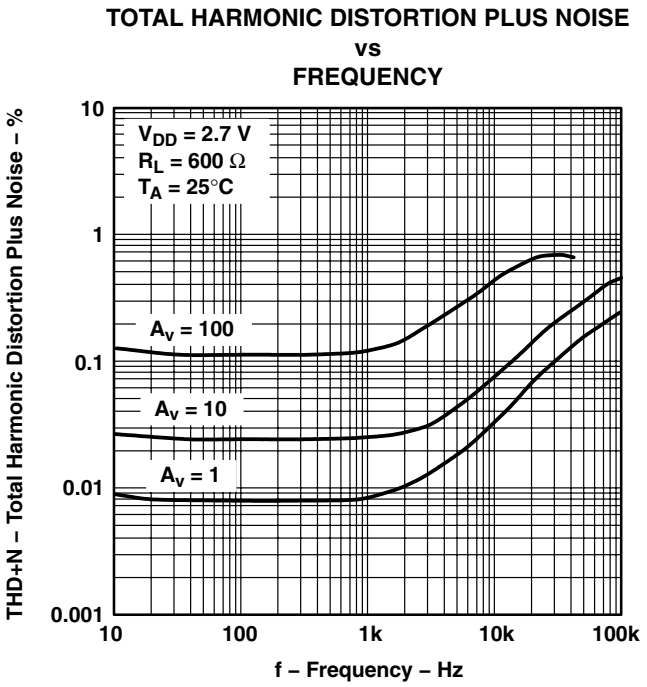


Figure 42

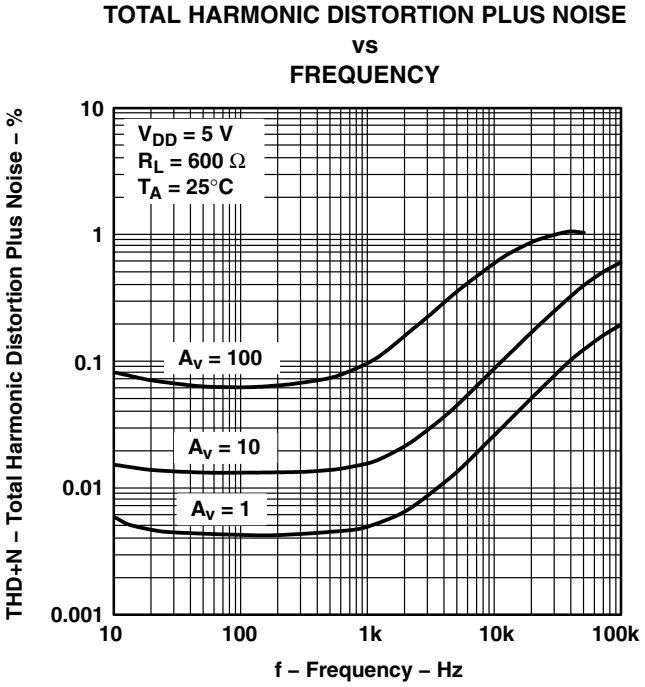


Figure 43

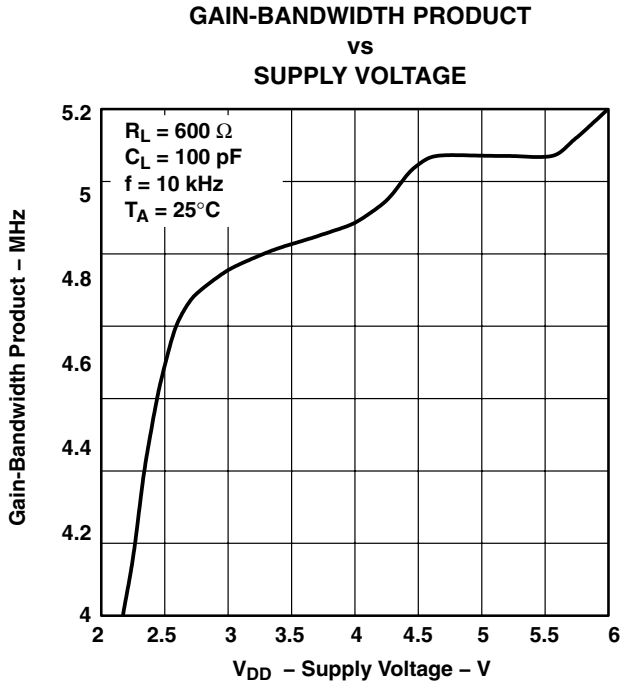


Figure 44

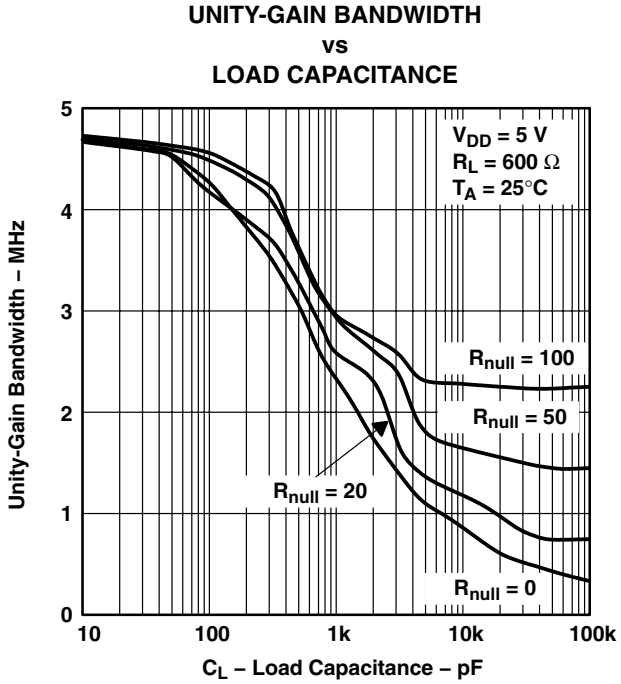


Figure 45

TYPICAL CHARACTERISTICS

PHASE MARGIN vs LOAD CAPACITANCE

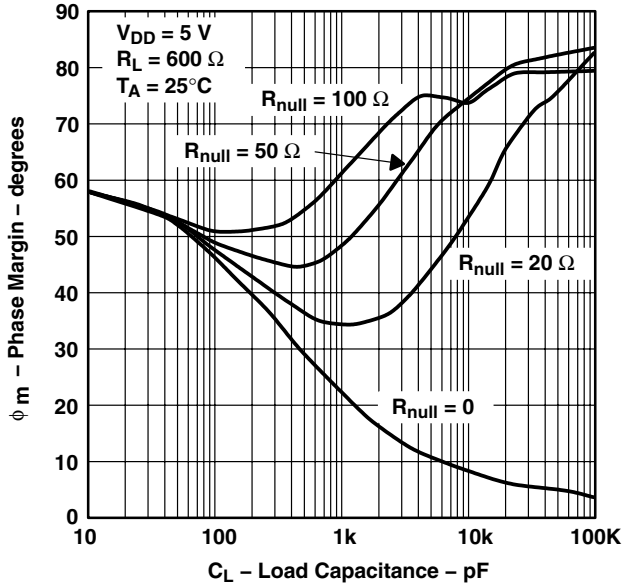


Figure 46

GAIN MARGIN vs LOAD CAPACITANCE

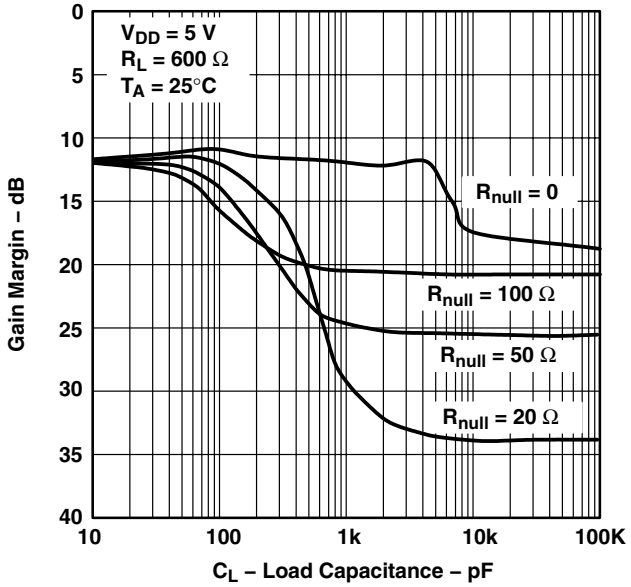


Figure 47

TLV2770 AMPLIFIER WITH SHUTDOWN PULSE TURNON/OFF CHARACTERISTICS

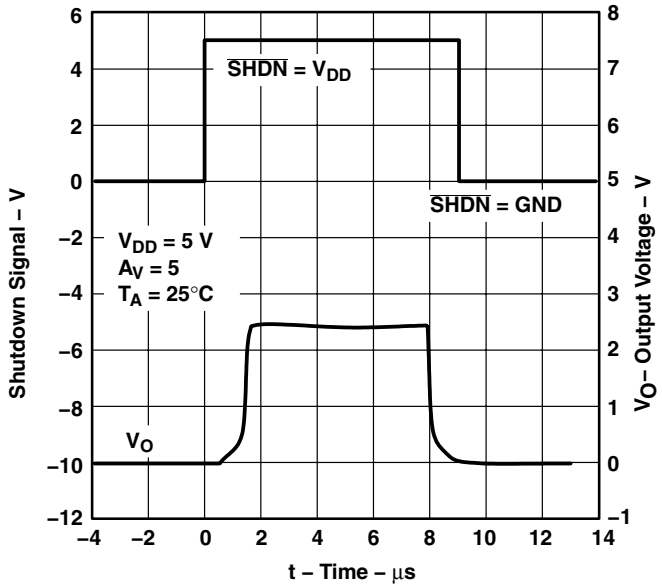


Figure 48

TLV2773 AMPLIFIER WITH SHUTDOWN PULSE TURNON/OFF CHARACTERISTICS

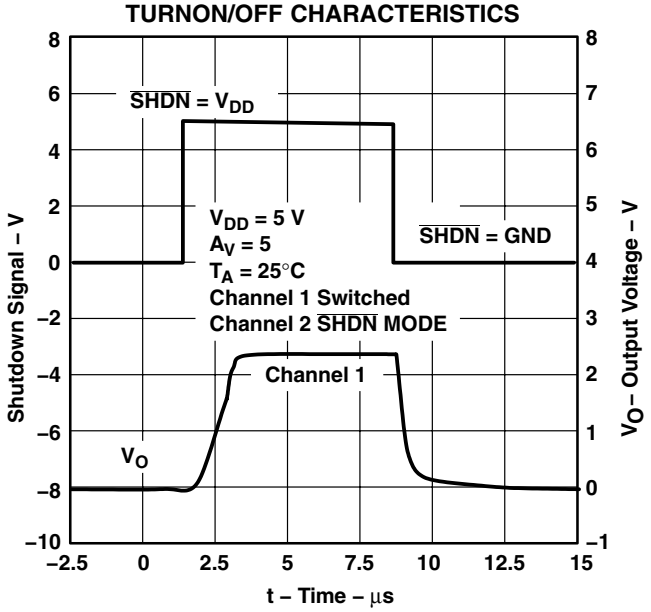


Figure 49

TYPICAL CHARACTERISTICS

TLV2775 – CHANNEL 1
AMPLIFIER WITH SHUTDOWN PULSE
TURNON/OFF CHARACTERISTICS

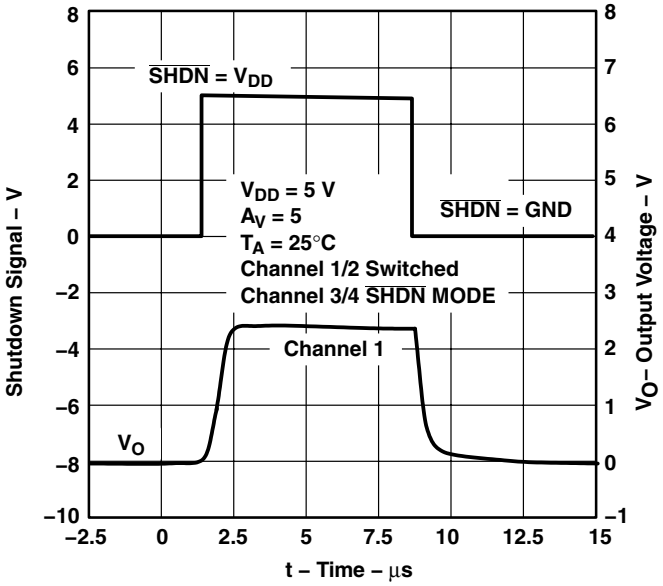


Figure 50

TLV2770
SUPPLY CURRENT WITH SHUTDOWN PULSE
TURNON/OFF CHARACTERISTICS

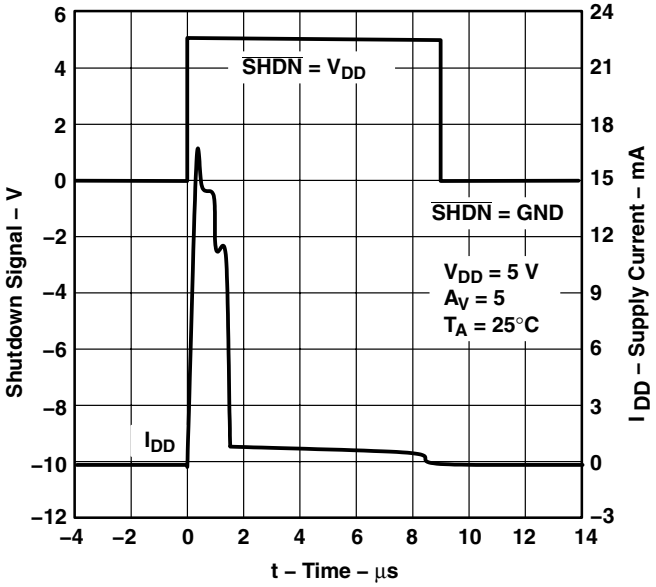


Figure 51

TLV2773
SUPPLY CURRENT WITH SHUTDOWN PULSE
TURNON/OFF CHARACTERISTICS

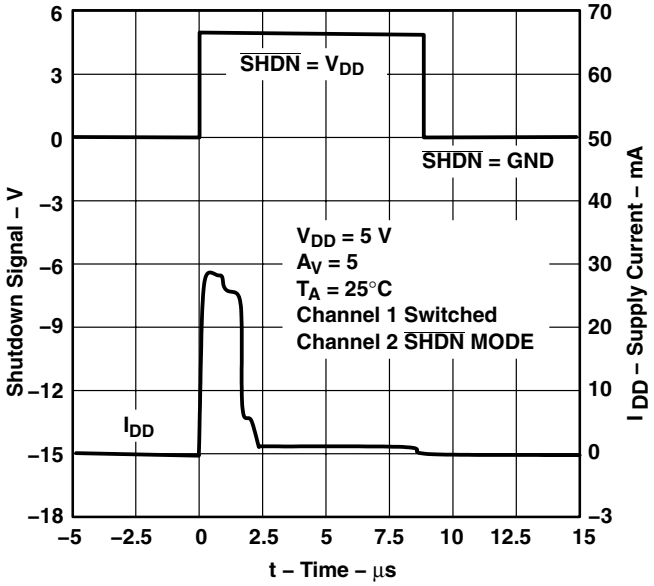


Figure 52

TLV2775
SUPPLY CURRENT WITH SHUTDOWN PULSE
TURNON/OFF CHARACTERISTICS

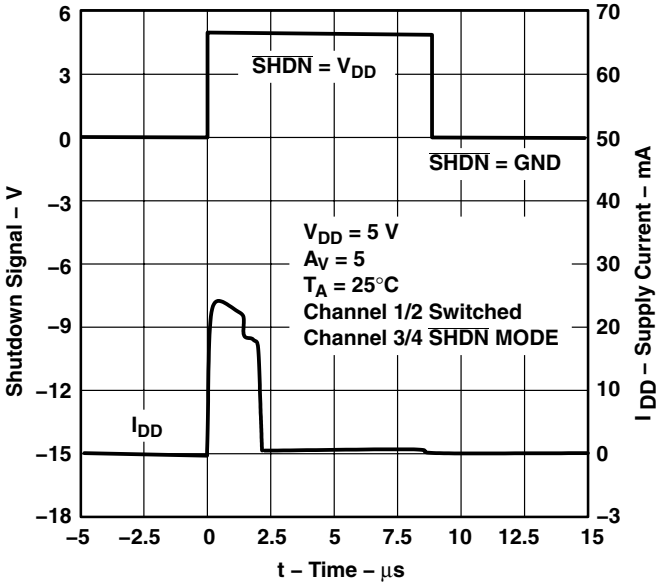


Figure 53

TYPICAL CHARACTERISTICS

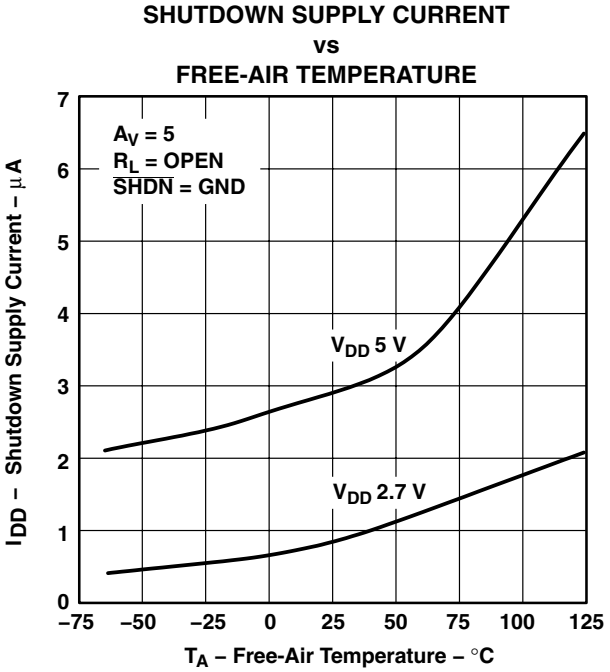


Figure 54

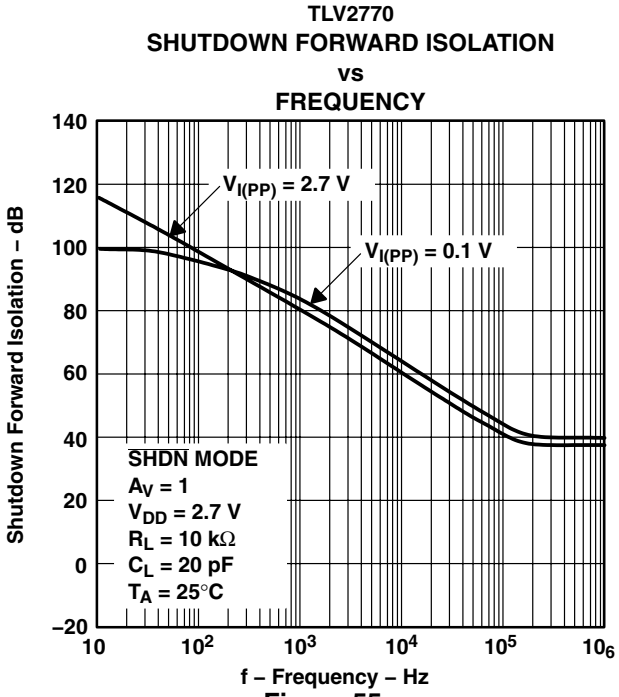


Figure 55

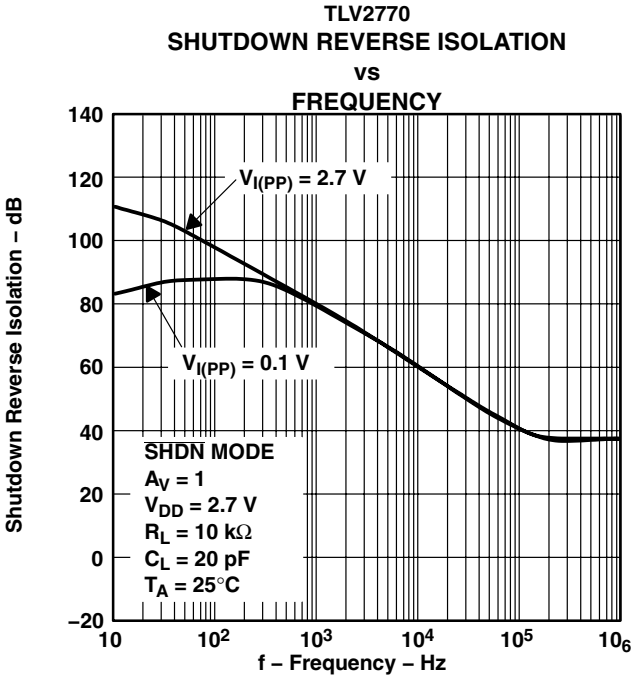


Figure 56

PARAMETER MEASUREMENT INFORMATION

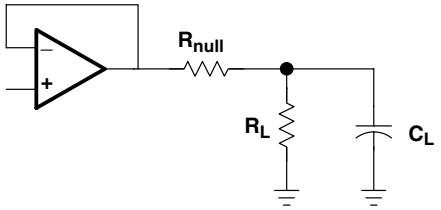


Figure 57

driving a capacitive load

When the amplifier is configured in this manner, capacitive loading directly on the output decreases the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series (R_{NULL}) with the output of the amplifier, as shown in Figure 58. A minimum value of 20 Ω should work well for most applications.

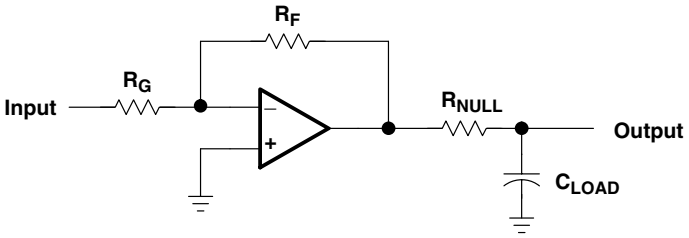
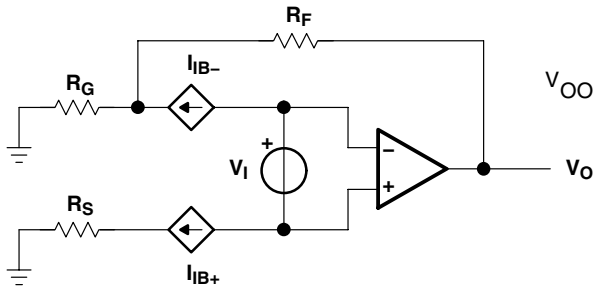


Figure 58. Driving a Capacitive Load

APPLICATION INFORMATION

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:

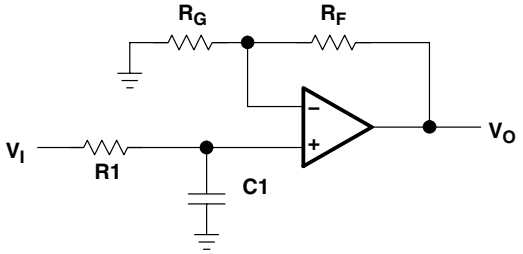


$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+} R_S \left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-} R_F$$

Figure 59. Output Offset Voltage Model

general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 60).

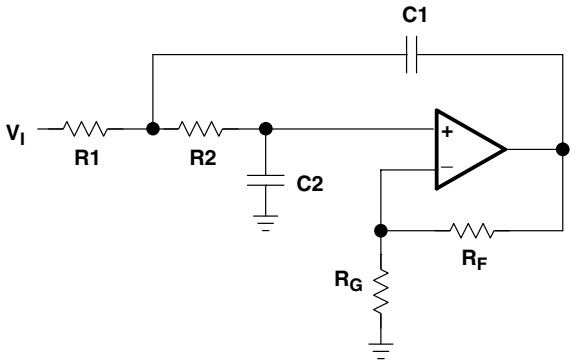


$$f_{-3dB} = \frac{1}{2\pi R1C1}$$

$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR1C1}\right)$$

Figure 60. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.



R1 = R2 = R
C1 = C2 = C
Q = Peaking Factor
(Butterworth Q = 0.707)

$$f_{-3dB} = \frac{1}{2\pi RC}$$

$$R_G = \frac{R_F}{\left(2 - \frac{1}{Q}\right)}$$

Figure 61. 2-Pole Low-Pass Sallen-Key Filter

APPLICATION INFORMATION

using the TLV2772 as an accelerometer interface

The schematic, shown in Figure 62, shows the ACH04-08-05 interfaced to the TLV1544 10-bit analog-to-digital converter (ADC).

The ACH04-08-05 is a shock sensor designed to convert mechanical acceleration into electrical signals. The sensor contains three piezoelectric sensing elements oriented to simultaneously measure acceleration in three orthogonal, linear axes (x, y, z). The operating frequency is 0.5 Hz to 5 kHz. The output is buffered with an internal JFET and has a typical output voltage of 1.80 mV/g for the x and y axis and 1.35 mV/g for the z axis.

Amplification and frequency shaping of the shock sensor output is done by the TLV2772 rail-to-rail operational amplifier. The TLV2772 is ideal for this application as it offers high input impedance, good slew rate, and excellent dc precision. The rail-to-rail output swing and high output drive are perfect for driving the analog input of the TLV1544 ADC.

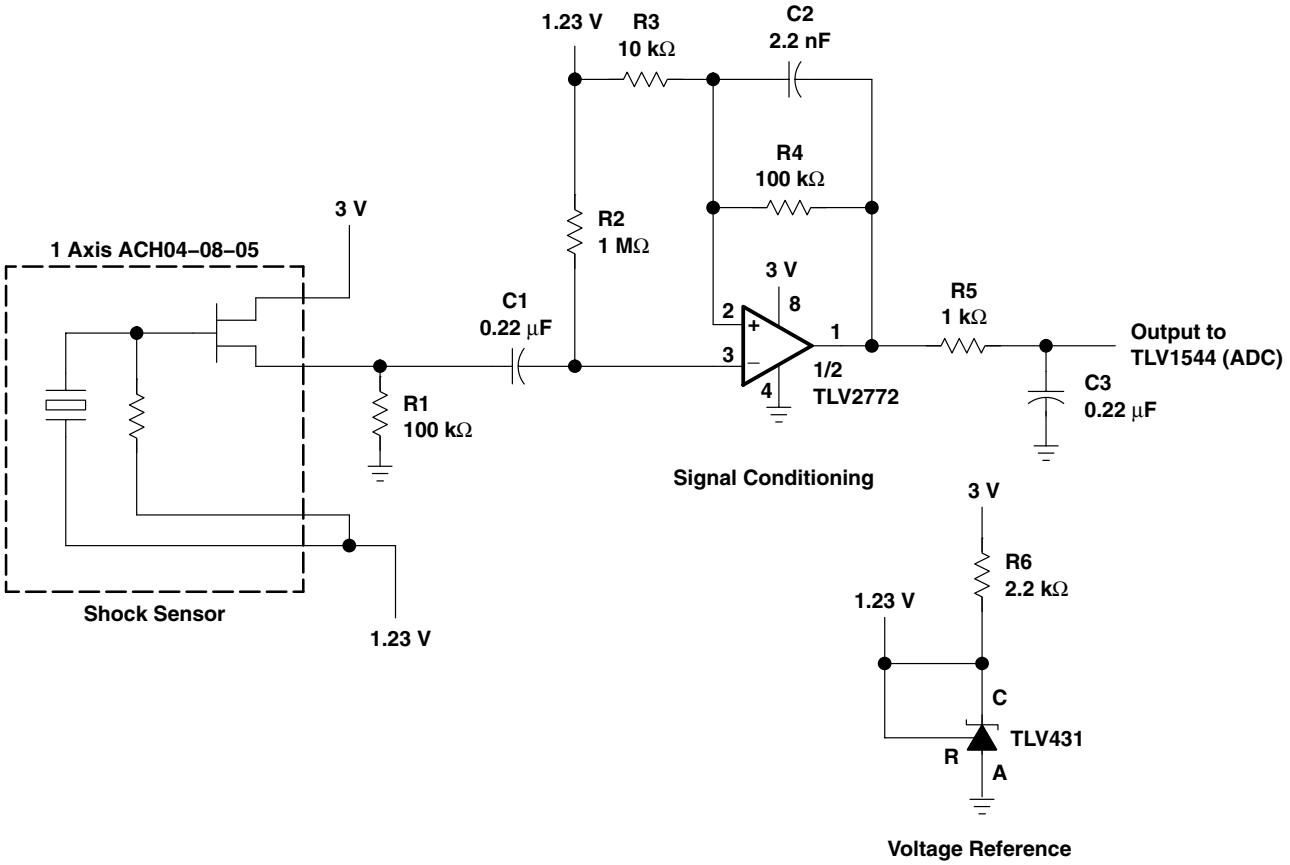


Figure 62. Accelerometer Interface Schematic

The sensor signal must be amplified and frequency-shaped to provide a signal the ADC can properly convert into the digital domain. Figure 62 shows the topology used in this application for one axis of the sensor. This system is powered from a single 3-V supply. Configuring the TLV431 with a 2.2-kΩ resistor produces a reference voltage of 1.23 V. This voltage is used to bias the operational amplifier and the internal JFETs in the shock sensor.

APPLICATION INFORMATION

gain calculation

Since the TLV2772 is capable of rail-to-rail output using a 3-V supply, V_O = 0 (min) to 3 V (max). With no signal from the sensor, nominal V_O = reference voltage = 1.23 V. Therefore, the maximum negative swing from nominal is 0 V – 1.23 V = –1.23 V and the maximum positive swing is 3 V – 1.23 V = 1.77 V. By modeling the shock sensor as a low impedance voltage source with output of 2.25 mV/g (max) in the x and y axis and 1.7 mV/g (max) in the z axis, the gain of the circuit is calculated by equation 1.

$$\text{Gain} = \frac{\text{Output Swing}}{\text{Sensor Signal} \times \text{Acceleration}} \tag{1}$$

To avoid saturation of the operational amplifier, the gain calculations are based on the maximum negative swing of –1.23 V and the maximum sensor output of 2.25 mV/g (x and y axis) and 1.70 mV/g (z axis).

$$\text{Gain (x, y)} = \frac{-1.23\ \text{V}}{2.25\ \text{mV/g} \times -50\ \text{g}} = 10.9 \tag{2}$$

and

$$\text{Gain (z)} = \frac{-1.23\ \text{V}}{1.70\ \text{mV/g} \times -50\ \text{g}} = 14.5 \tag{3}$$

By selecting R3 = 10 kΩ and R4 = 100 kΩ, in the x and y channels, a gain of 11 is realized. By selecting R3 = 7.5 kΩ and R4 = 100 kΩ, in the z channel, a gain of 14.3 is realized. The schematic shows the configuration for either the x- or y-axis.

bandwidth calculation

To calculate the component values for the frequency shaping characteristics of the signal conditioning circuit, 1 Hz and 500 Hz are selected as the minimum required 3-dB bandwidth.

To minimize the value of the input capacitor (C1) required to set the lower cutoff frequency requires a large value resistor for R2 is required. A 1-MΩ resistor is used in this example. To set the lower cutoff frequency, the required capacitor value for C1 is:

$$C1 = \frac{1}{2\pi\, f_{LOW}\, R_2} = 0.159\ \mu\text{F} \tag{4}$$

Using a value of 0.22 μF, a more common value of capacitor, the lower cutoff frequency is 0.724 Hz.

To minimize the phase shift in the feedback loop caused by the input capacitance of the TLV2772, it is best to minimize the value of the feedback resistor R4. However, to reduce the required capacitance in the feedback loop a large value for R4 is required. Therefore, a compromise for the value of R4 must be made. In this circuit, a value of 100 kΩ has been selected. To set the upper cutoff frequency, the required capacitor value for C2 is:

$$C2 = \frac{1}{2\pi\, f_{HIGH}\, R_4} = 3.18\ \mu\text{F} \tag{5}$$

Using a 2.2-nF capacitor, the upper cutoff frequency is 724 Hz.

R5 and C3 also cause the signal response to roll off. Therefore, it is beneficial to design this roll-off point to begin at the upper cutoff frequency. Assuming a value of 1 kΩ for R5, the value for C3 is calculated to be 0.22 μF.

APPLICATION INFORMATION

circuit layout considerations

To achieve the levels of high performance of the TLV277x, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- Ground planes—It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling—Use a 6.8-µF tantalum capacitor in parallel with a 0.1-µF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-µF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-µF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets—Sockets can be used but are not recommended. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements—Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This helps to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components—Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

APPLICATION INFORMATION

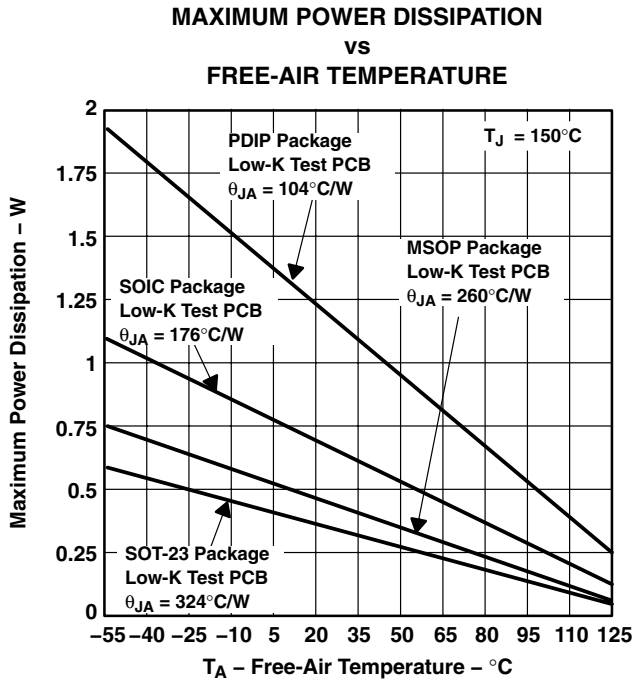
general power dissipation considerations

For a given θ_{JA}, the maximum power dissipation is shown in Figure 63 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}}\right)$$

Where:

P_D = Maximum power dissipation of TLV277x IC (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
θ_{JA} = $\theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction-to-case
θ_{CA} = Thermal coefficient from case to ambient air (°C/W)



NOTE A: Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 63.

APPLICATION INFORMATION

shutdown function

Three members of the TLV277x family (TLV2770/3/5) have a shutdown terminal for conserving battery life in portable applications. When the shutdown terminal is tied low, the supply current is reduced to 0.8 μA/channel, the amplifier is disabled, and the outputs are placed in a high impedance mode. To enable the amplifier, the shutdown terminal can either be left floating or pulled high. When the shutdown terminal is left floating, care needs to be taken to ensure that parasitic leakage current at the shutdown terminal does not inadvertently place the operational amplifier into shutdown. The shutdown terminal threshold is always referenced to $V_{DD}/2$. Therefore, when operating the device with split supply voltages (e.g. ±2.5 V), the shutdown terminal needs to be pulled to $V_{DD}-$ (not GND) to disable the operational amplifier.

The amplifier's output with a shutdown pulse is shown in Figure 48 through Figure 50. The amplifier is powered with a single 5-V supply and configured as a noninverting configuration with a gain of 5. The amplifier turnon and turnoff times are measured from the 50% point of the shutdown pulse to the 50% point of the output waveform. The times for the single, dual, and quad are listed in the data tables. The *bump* on the rising edge of the TLV2770 output waveform is due to the start-up circuit on the bias generator. For the dual and quad (TLV2773/5), this *bump* is attributed to the bias generator's start-up circuit as well as the crosstalk between the other channel(s), which are in shutdown.

Figure 55 and Figure 56 show the amplifier's forward and reverse isolation in shutdown. The operational amplifier is powered by ±1.35-V supplies and configured as a voltage follower (A_V = 1). The isolation performance is plotted across frequency for both 0.1-V_{PP} and 2.7-V_{PP} input signals. During normal operation, the amplifier would not be able to handle a 2.7-V_{PP} input signal with a supply voltage of ±1.35 V since it exceeds the common-mode input voltage range (V_{ICR}). However, this curve illustrates that the amplifier remains in shutdown even under a worst case scenario.

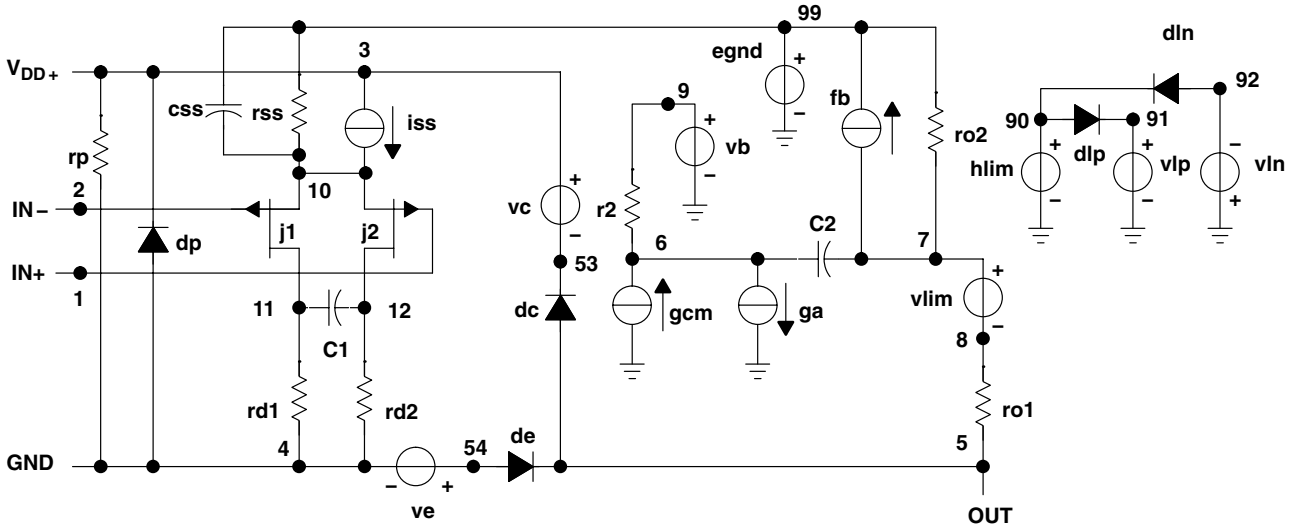
APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™ Release 8, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 4) and subcircuit in Figure 64 are generated using the TLV2772 typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 6: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, “Macromodeling of Integrated Circuit Operational Amplifiers”, *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).




```
* TLV2772 operational amplifier macromodel subcircuit
* created using Parts release 8.0 on 12/12/97 at 10:08
* Parts is a MicroSim product.
*
* connections:   noninverting input
*                |  inverting input
*                |  |  positive power supply
*                |  |  |  negative power supply
*                |  |  |  |  output
*                |  |  |  |  |
.subckt TLV2772  1  2  3  4  5
*
c1     11   12   2.8868E-12
c2     6    7    10.000E–12
css    10   99   2.6302E–12
dc     5    53   dy
de     54   5    dy
dlp    90   91   dx
dln    92   90   dx
dp     4    3    dx
egnd   99   0    poly(2) (3,0) (4,0) 0 .5 .5
fb     7    99   poly(5) vb vc ve vlp vln 0
                 15.513E6 –1E3 1E3 16E6 –16E6
ga     6    0    11   12   188.50E–6
gcm    0    6    10   99   9.4472E–9
iss    3    10   dc      145.50E–6
hlim   90   0    vlim 1K
j1     11   2    10 jx1
j2     12   1    10 jx2
r2     6    9    100.00E3
rd1    4    11   5.3052E3
rd2    4    12   5.3052E3
ro1    8    5    17.140
ro2    7    99   17.140
rp     3    4    4.5455E3
rss    10   99   1.3746E6
vb     9    0    dc 0
vc     3    53   dc .82001
ve     54   4    dc .82001
vlim   7    8    dc 0
vlp    91   0    dc 47
vln    0    92   dc 47
.model dx   D(Is=800.00E–18)
.model dy   D(Is=800.00E–18 Rs=1m Cjo=10p)
.model jx1  PJF(Is=2.2500E–12 Beta=244.20E–6
            + Vto=–.99765)
.model jx2  PJF(Is=1.7500E–12 Beta=244.20E–6
            + Vto=–1.002350)
.ends
*$
```

Figure 64. Boyle Macromodel and Subcircuit

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV2771QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VBPQ
TLV2771QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VBPQ
TLV2772AQDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2772AQ
TLV2772AQDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2772AQ
TLV2772AQPWRG4Q1	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-1-260C-UNLIM	-40 to 125	2772AQ
TLV2772AQPWRG4Q1.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2772AQ
TLV2772QDRG4Q1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2772Q1
TLV2772QDRG4Q1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2772Q1
TLV2772QPWRG4Q1	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-1-260C-UNLIM	-40 to 125	2772Q1
TLV2772QPWRG4Q1.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2772Q1
TLV2772QPWRQ1	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-1-260C-UNLIM	-40 to 125	2772Q1
TLV2772QPWRQ1.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2772Q1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV2771-Q1, TLV2772-Q1, TLV2772A-Q1 :

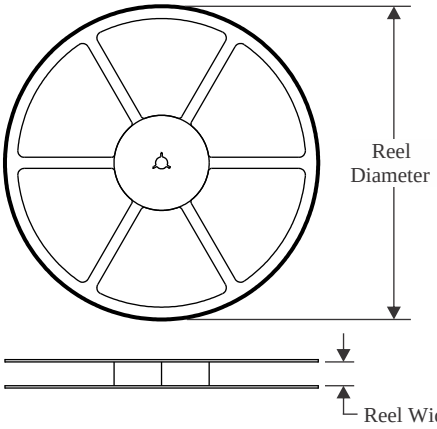
- Catalog : TLV2771, TLV2772, TLV2772A
- Enhanced Product : TLV2772A-EP
- Military : TLV2772AM

NOTE: Qualified Version Definitions:

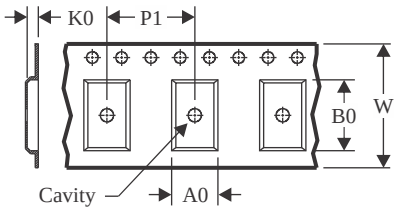
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

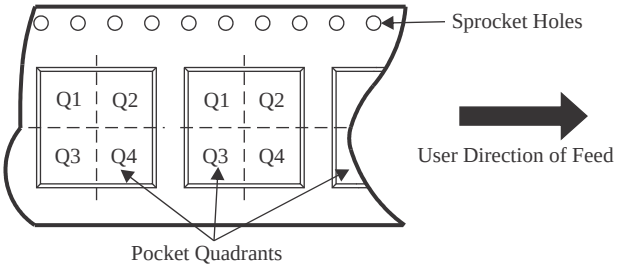


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

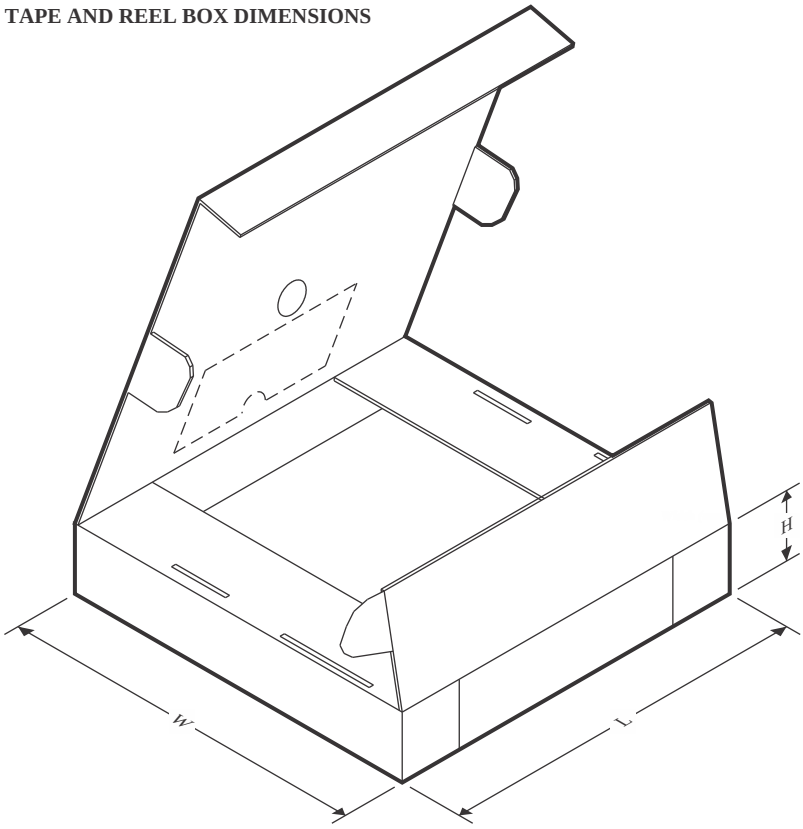
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

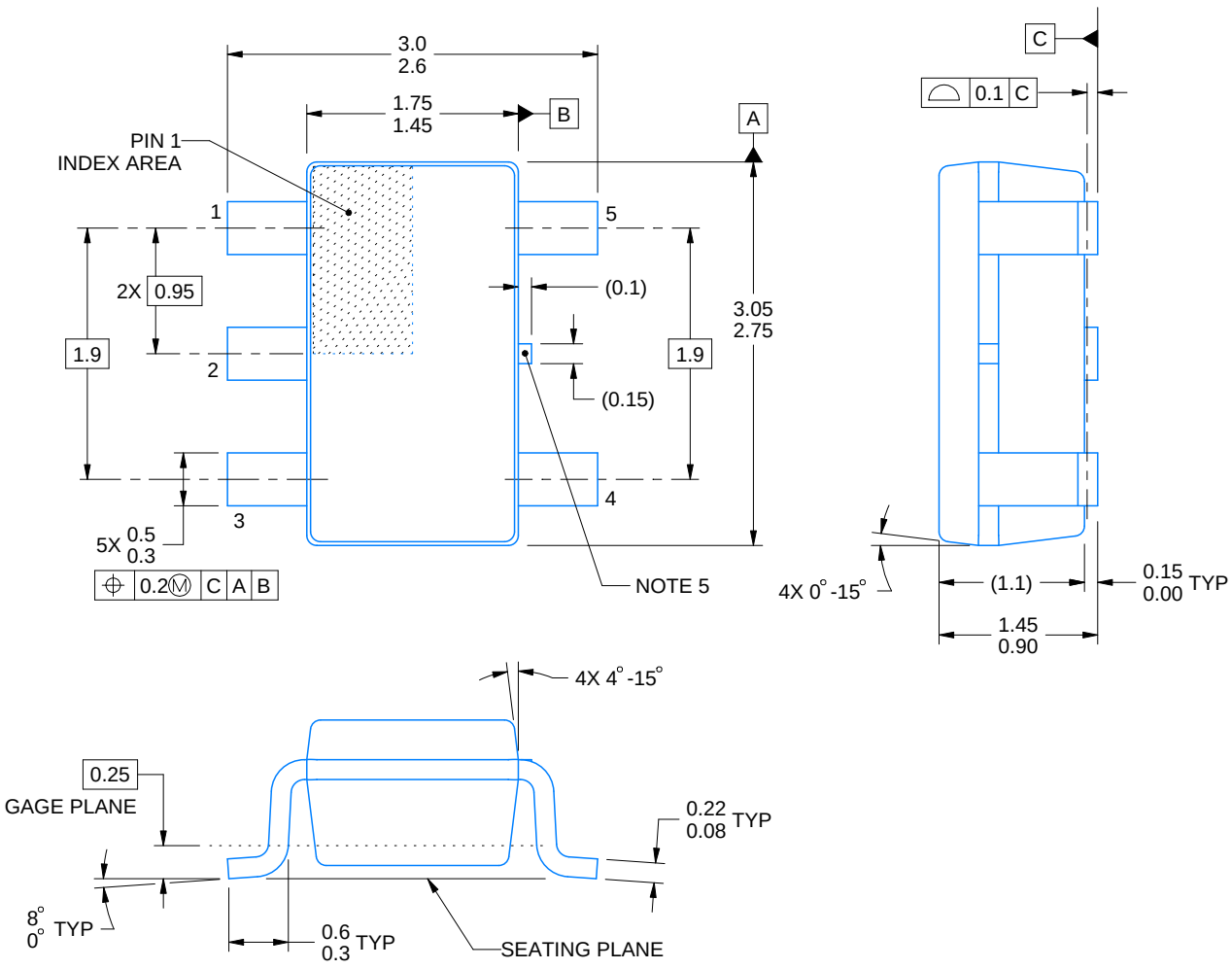
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2771QDBVRQ1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2772AQPWRG4Q1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV2772AQPWRG4Q1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV2772QPWRG4Q1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV2772QPWRG4Q1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV2772QPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV2772QPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

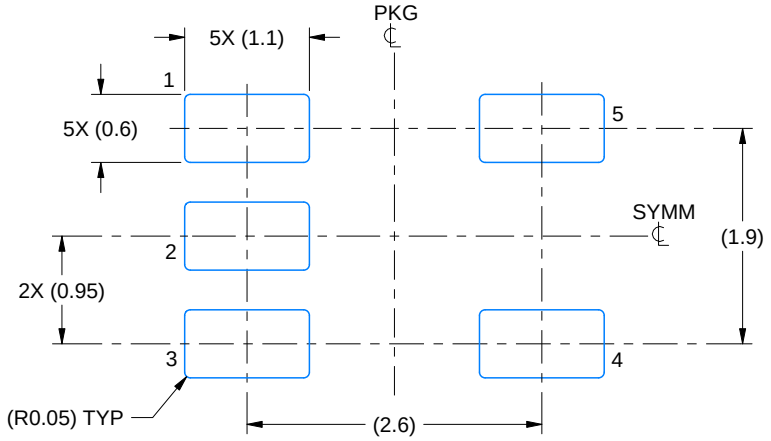
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2771QDBVRQ1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TLV2772AQPWRG4Q1	TSSOP	PW	8	2000	353.0	353.0	32.0
TLV2772AQPWRG4Q1	TSSOP	PW	8	2000	367.0	367.0	35.0
TLV2772QPWRG4Q1	TSSOP	PW	8	2000	367.0	367.0	35.0
TLV2772QPWRG4Q1	TSSOP	PW	8	2000	353.0	353.0	32.0
TLV2772QPWRQ1	TSSOP	PW	8	2000	356.0	356.0	35.0
TLV2772QPWRQ1	TSSOP	PW	8	2000	353.0	353.0	32.0



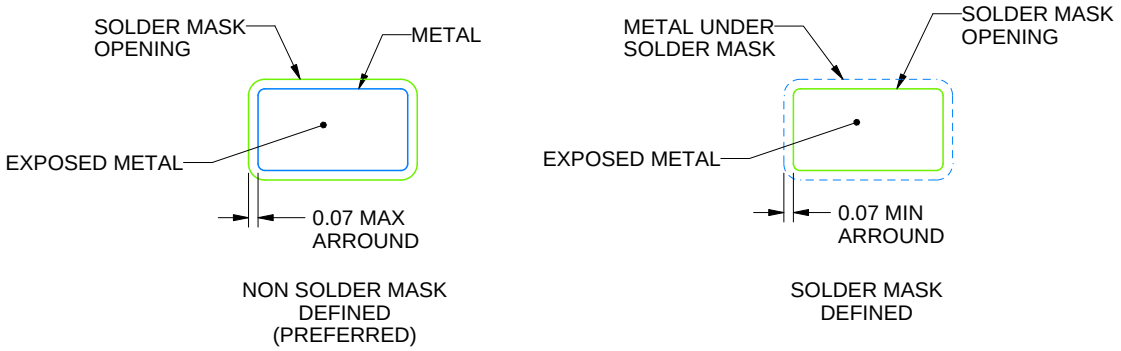
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

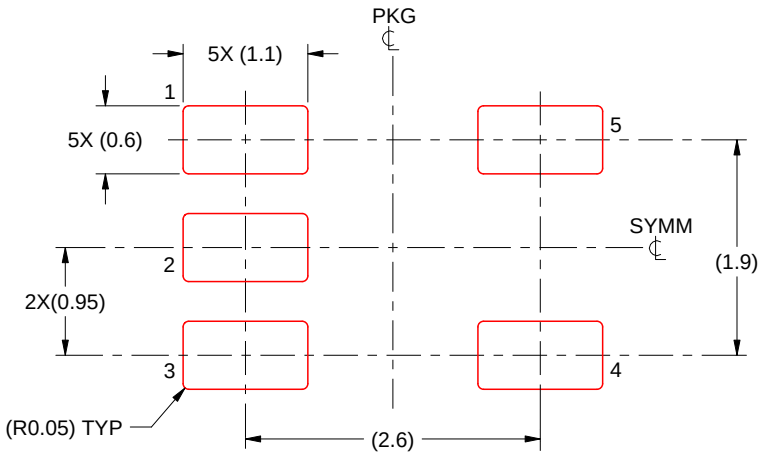


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

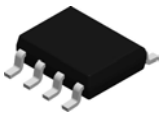


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

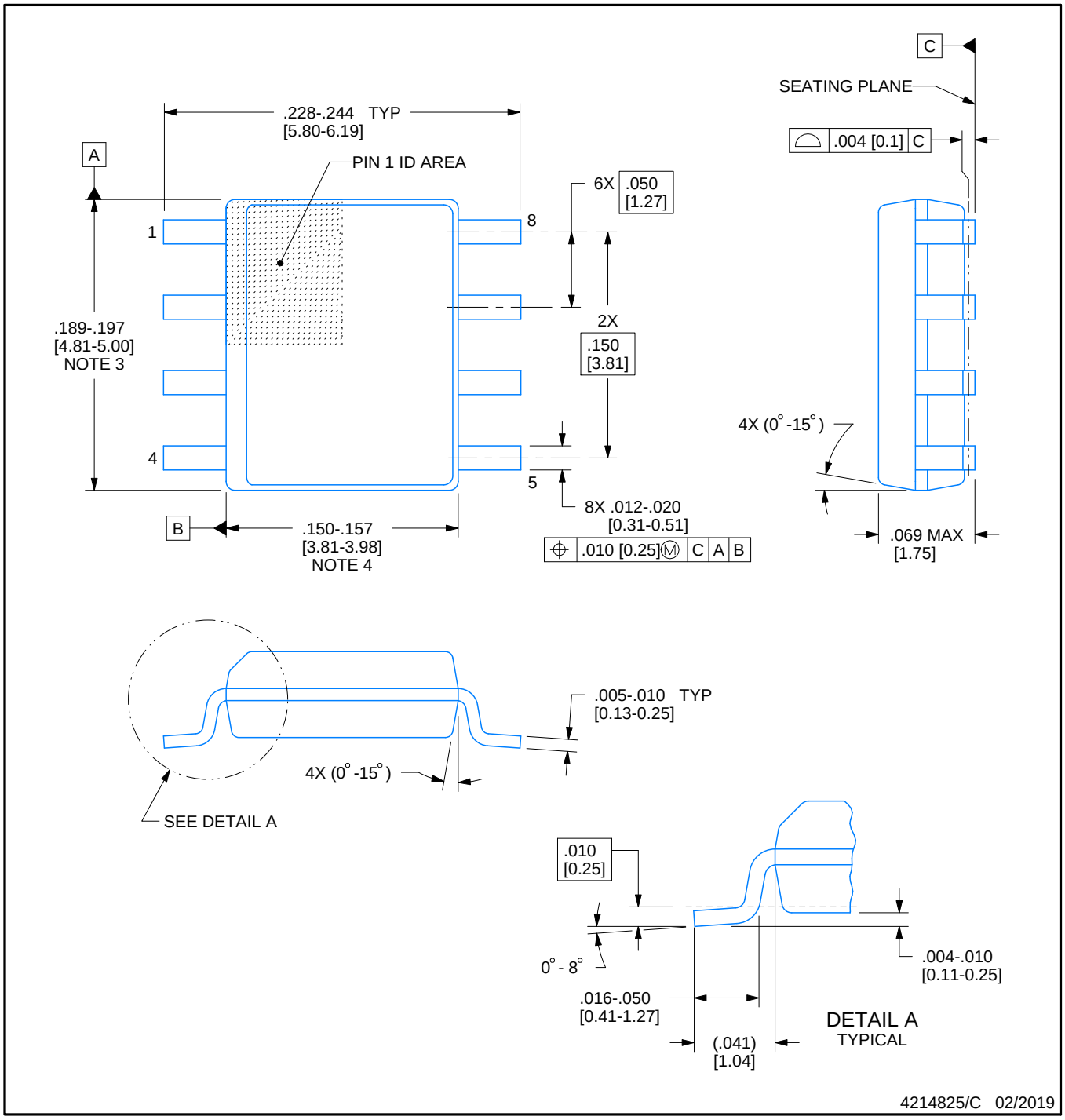


PACKAGE OUTLINE

D0008A

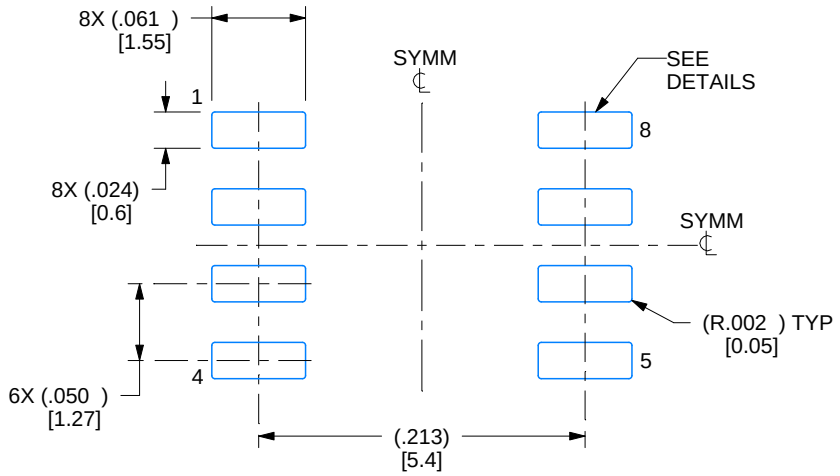
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

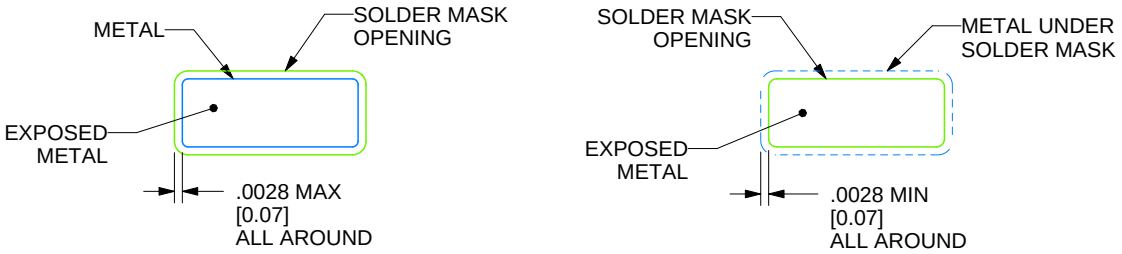


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

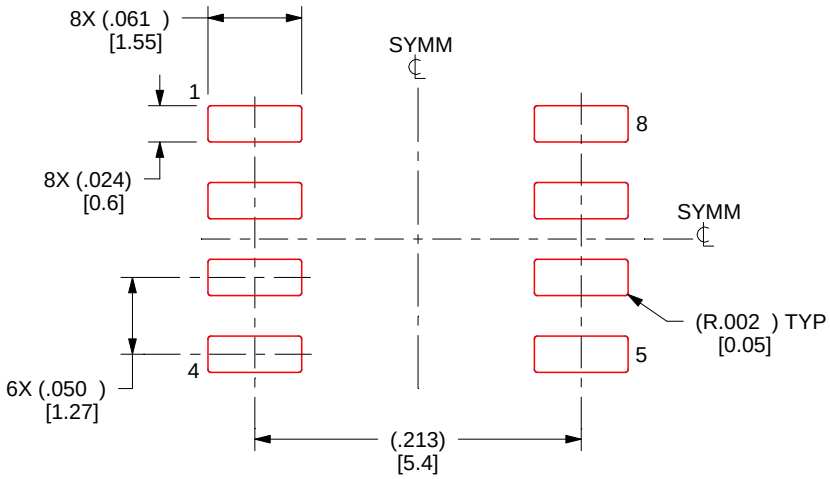


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

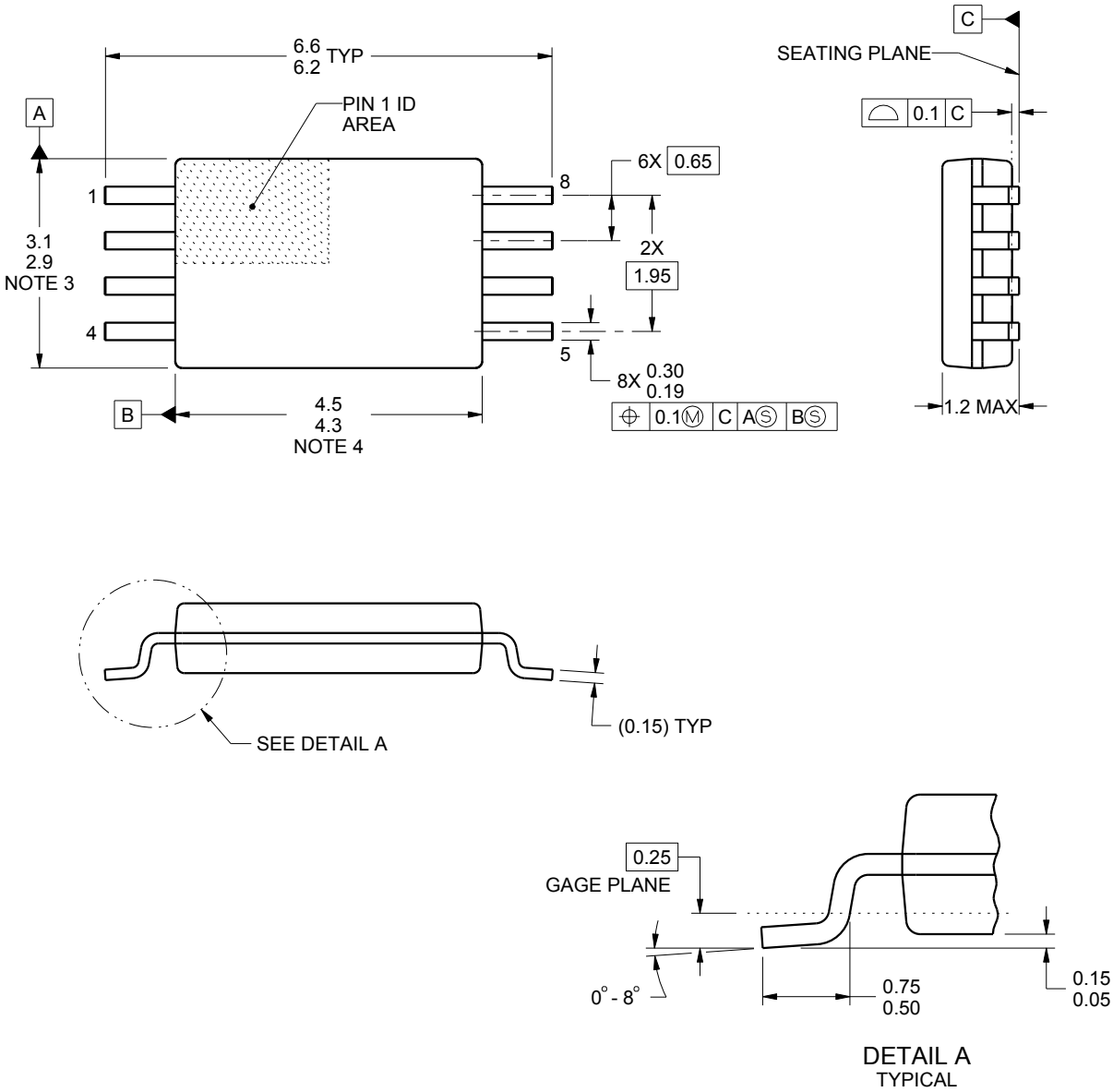


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

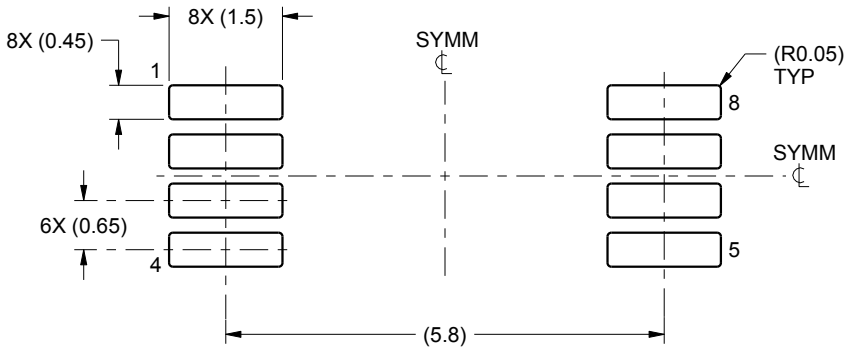
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

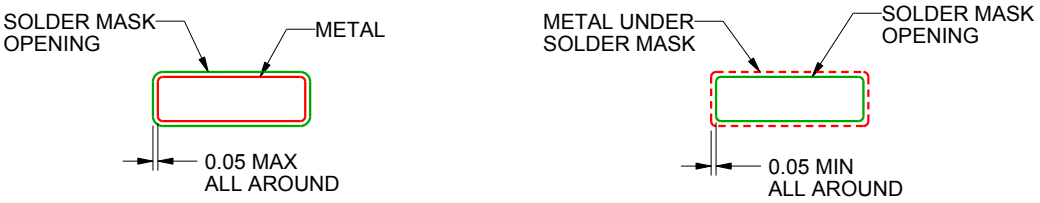


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X



NON SOLDER MASK
DEFINED

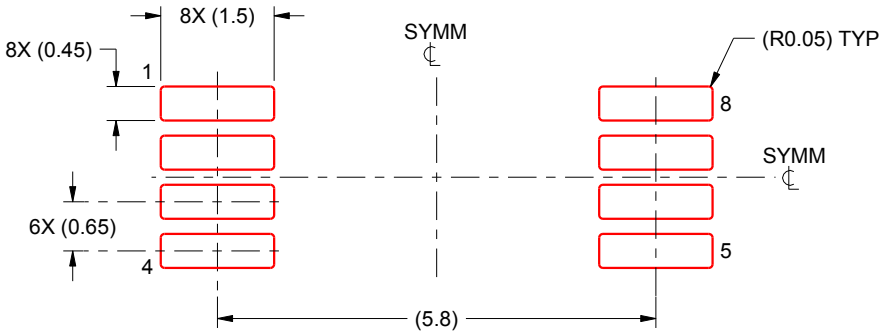
SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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