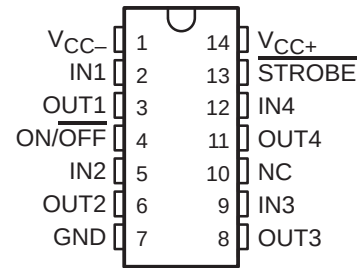


LT1030C QUADRUPLE LOW-POWER LINE DRIVER

SLLS048F – APRIL 1989 – REVISED APRIL 1998

- Low Supply Voltage . . . ± 5 V to ± 15 V
- Supply Current . . . 500 μ A Typical
- Zero Supply Current When Shut Down
- Outputs Can Be Driven ± 30 V
- Output Open When Off (3-State)
- 10-mA Output Drive
- Outputs of Several Devices Can Be Connected in Parallel
- Meets or Exceeds the Requirements of ANSI EIA/TIA-232-F Specifications
- Designed to Be Interchangeable With Linear Technology LT1030

D OR N PACKAGE
(TOP VIEW)



NC – No internal connection

description

The LT1030C is an EIA/TIA-232-F line driver that operates over a ± 5 -V to ± 15 -V supply-voltage range on low supply current. The device can be shut down to zero supply current. Current limiting fully protects the outputs from externally applied voltages of ± 30 V. Since the output swings to within 200 mV of the positive supply and to within 1 V of the negative supply, supply-voltage requirements are minimized.

A major advantage of the LT1030C is the high-impedance output state when the device is off or powered down. This feature allows several different drivers on the same bus.

The device can be used as an EIA/TIA-232-F driver, micropower interface, or level translator, among others.

The LT1030C is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

PACKAGE	
SMALL OUTLINE (D)	PLASTIC DIP (N)
LT1030CD	LT1030CN

The D package is available taped and reeled. Add the suffix R to the device type (i.e., LT1030CDR).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

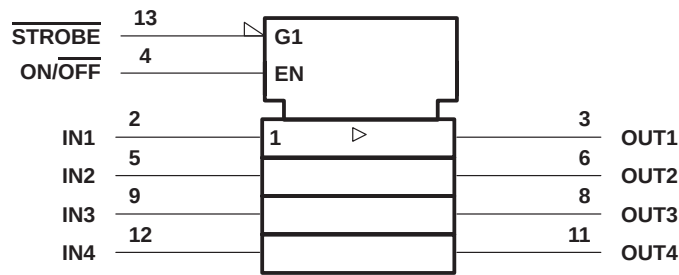
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LT1030C
QUADRUPLE LOW-POWER LINE DRIVER

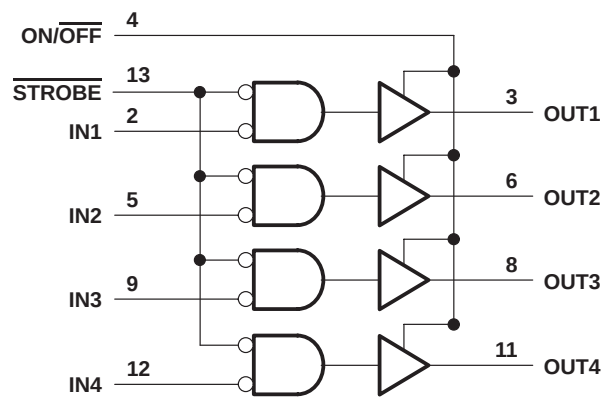
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



Terminal Functions

TERMINAL NAME	NO.	DESCRIPTION
GND	7	Ground terminal
IN1 IN2 IN3 IN4	2 5 9 12	Logic inputs. INx operate properly on TTL or CMOS levels. Output valid from $V_I = V_{CC-} + 2\text{ V}$ to 15 V. Connect to 5 V when not used.
ON/OFF	4	ON/OFF shuts down the entire circuit. It cannot be left open. For normally on operation, connect between 5 V and 10 V. If V_{IL} is at or near 0.8 V, significant settling time may be required.
OUT1 OUT2 OUT3 OUT4	3 6 8 11	Line driver outputs
STROBE	13	STROBE forces all outputs low. Drive with 3 V. Strobe terminal input impedance is approximately 2 k Ω to GND. Leave STROBE open when not used.
V _{CC+}	14	Positive supply
V _{CC-}	1	Negative supply

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC+} (see Note 1)	0 V to 15 V
Supply voltage range, V_{CC-}	0 V to -15 V
Input voltage range, logic inputs, V_I	V_{CC-} to 25 V
Input voltage range at ON/OFF, V_I	0 V to 12 V
Output voltage range, V_O (any output)	$V_{CC+} - 30$ V to $V_{CC-} + 30$ V
Duration of output short circuit to ± 30 V at (or below) 25°C (see Note 2)	Unlimited
Package thermal impedance, θ_{JA} (see Note 3): D package	127°C/W
N package	78°C/W
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, except differential voltages, are with respect to GND.
 2. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.
 3. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC+}	5	15	V
Supply voltage, V_{CC-}	-5	-15	V
High-level input voltage, V_{IH} (see Note 4)	2	15	V
Low-level input voltage, V_{IL} (see Note 4)		0.8	V
Operating free-air temperature, T_A	0	70	°C

NOTE 4: These V_{IH} and V_{IL} specifications apply only for inputs IN1–IN4. For operating levels for ON/OFF, see Figure 2.

electrical characteristics over operating free-air temperature range, $V_{CC\pm} = \pm 5$ V to ± 15 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP [‡]	MAX	UNIT
V_{OM+} Maximum positive peak output voltage swing	$I_O = -2$ mA, $T_A = 25^\circ\text{C}$	$V_{CC+} - 0.3$	$V_{CC+} - 0.1$		V
V_{OM-} Maximum negative peak output voltage swing	$I_O = 2$ mA, $T_A = 25^\circ\text{C}$		$V_{CC-} + 0.9$	$V_{CC-} + 1.4$	V
I_{IH} High-level input current	$V_I \geq 2$ V, $T_A = 25^\circ\text{C}$		2	20	μA
I_{IL} Low-level input current	$V_I \leq 0.8$ V, $T_A = 25^\circ\text{C}$		-10	-20	μA
I_I Input current, ON/OFF	$V_I = 0$		-0.1	-10	μA
	$V_I = 5$ V		30	65	
I_O Output current	$T_A = 25^\circ\text{C}$	5	12		mA
I_{OZ} Off-state output current	$V_O = \pm 15$ V, $T_A = 25^\circ\text{C}$, ON/OFF at 0.4 V		±2	±100	μA
I_{CC} Supply current (all outputs low)	$V_I \geq$ at 2.4 V, $I_O = 0$		500	1000	μA
$I_{CC(off)}$ Off-state supply current	ON/OFF at 0.4 V			10	μA
	ON/OFF at 0.1 V		10	150	

[‡] All typical values are at $V_{CC\pm} = \pm 12$ V, $T_A = 25^\circ\text{C}$.

LT1030C

QUADRUPLE LOW-POWER LINE DRIVER

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operating characteristics, $V_{CC\pm} = \pm 5\text{ V}$ to $\pm 15\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
SR Driver slew rate	$R_L = 3\text{ k}\Omega$, $C_L = 51\text{ pF}$	4	15	30	V/ μs

† All typical values are at $V_{CC\pm} = \pm 12\text{ V}$, $T_A = 25^\circ\text{C}$.

TYPICAL CHARACTERISTICS

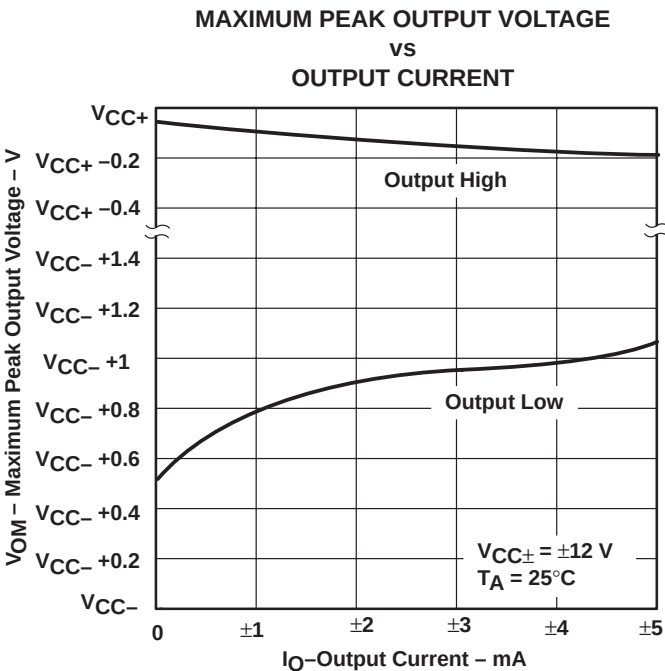


Figure 1

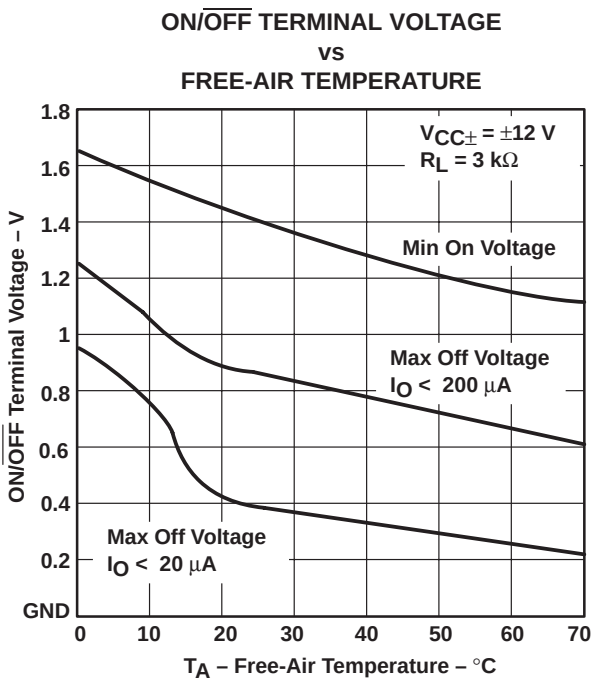


Figure 2

TYPICAL CHARACTERISTICS

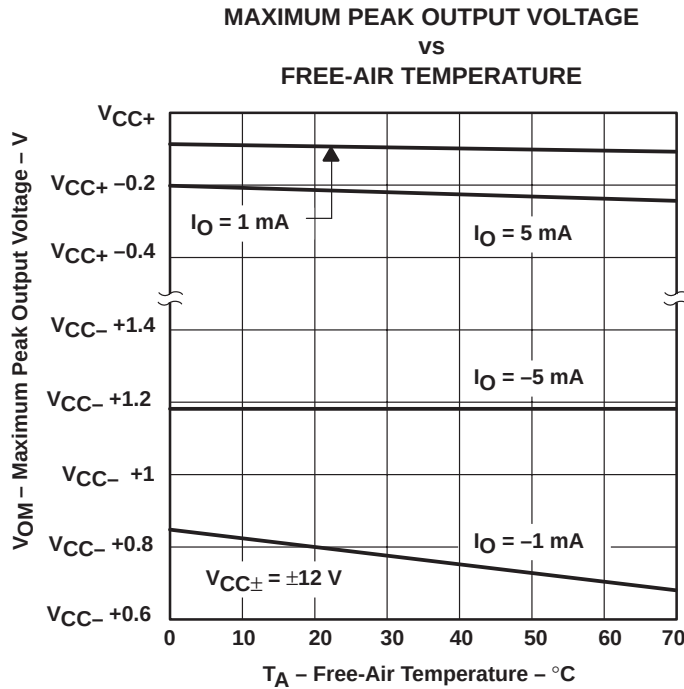


Figure 3

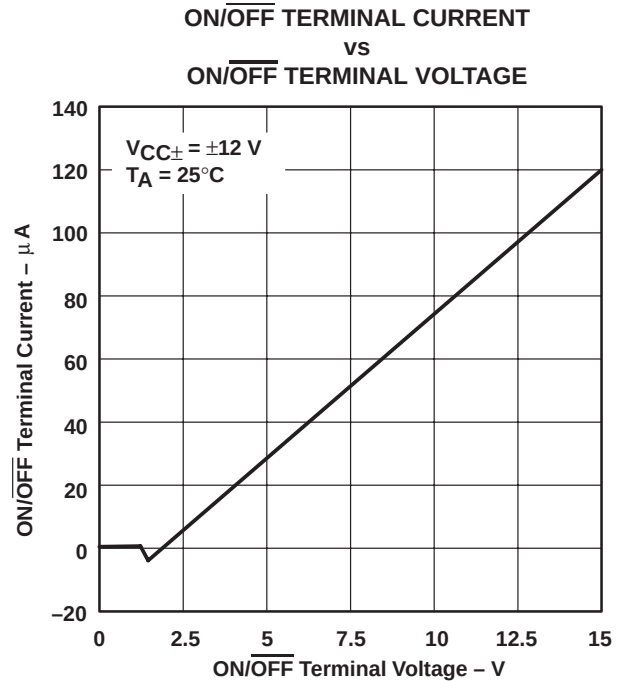


Figure 4

TYPICAL CHARACTERISTICS

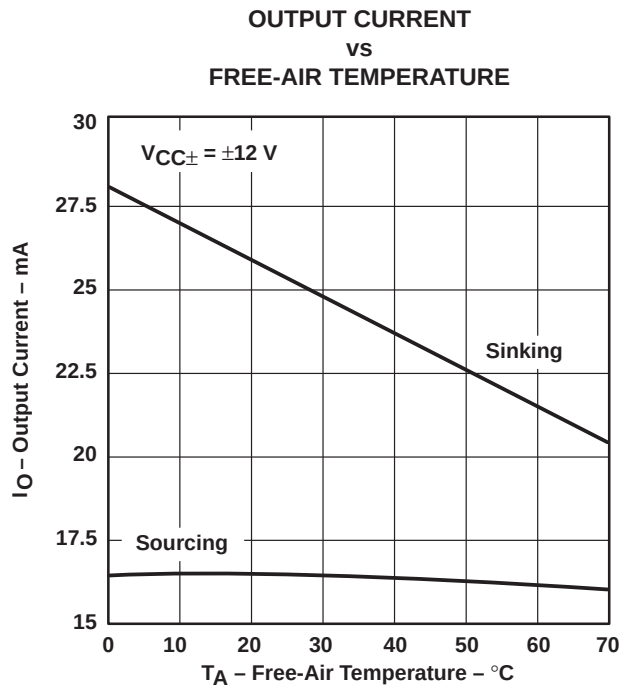


Figure 5

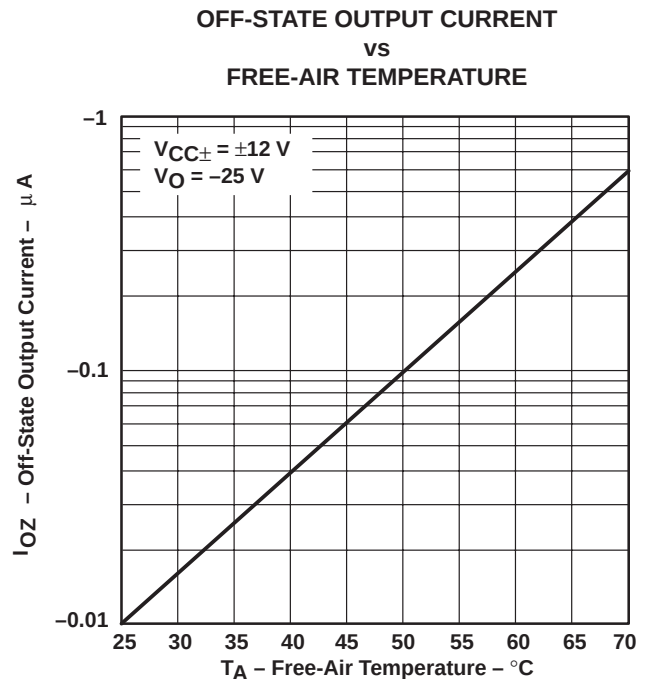


Figure 6

LT1030C QUADRUPLE LOW-POWER LINE DRIVER

SLLS048F – APRIL 1989 – REVISED APRIL 1998

TYPICAL CHARACTERISTICS

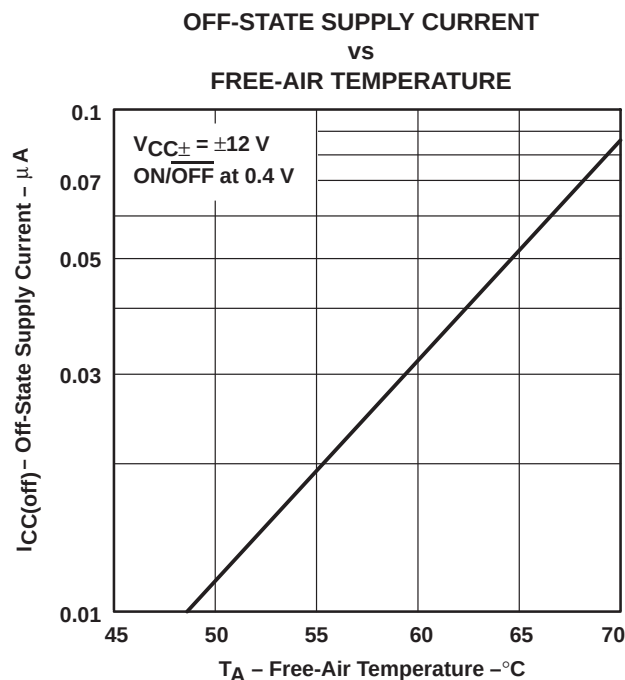


Figure 7

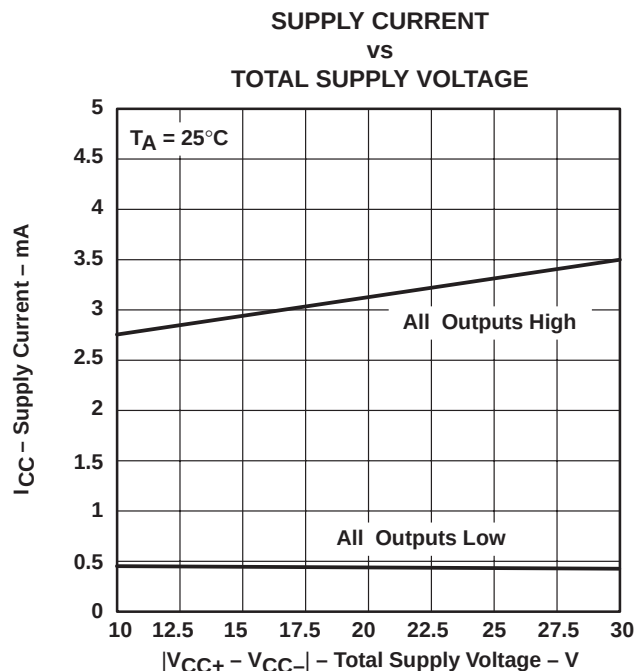


Figure 8

TYPICAL CHARACTERISTICS

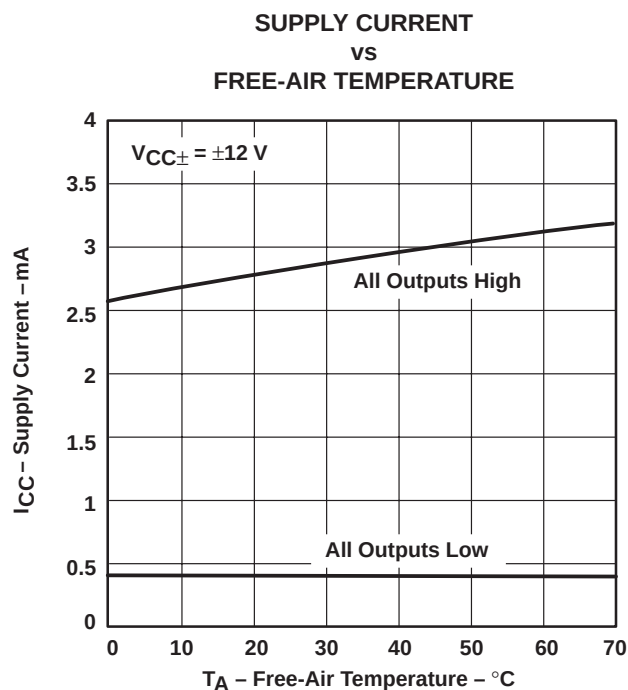


Figure 9

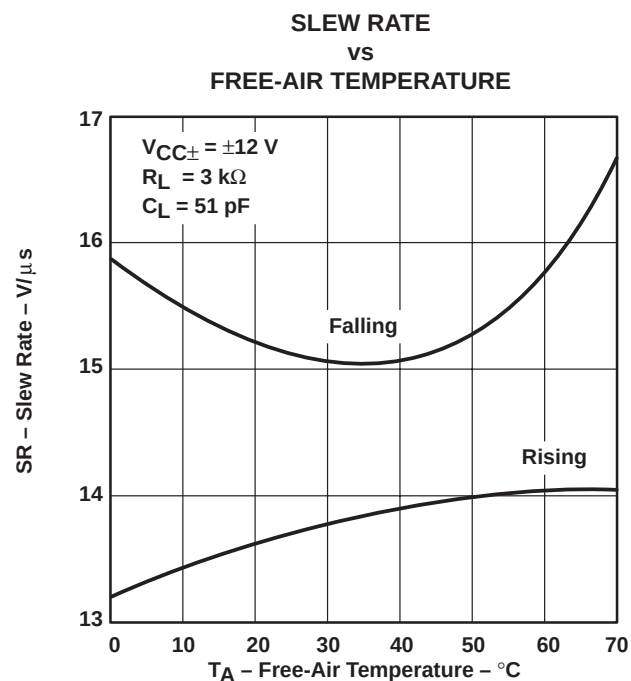


Figure 10

APPLICATION INFORMATION

forward biasing the substrate

As with other bipolar integrated circuits, forward biasing the substrate diode can cause problems. The LT1030C draws high current from V_{CC+} to GND when V_{CC-} is open circuited or pulled above ground. Connecting a diode from V_{CC-} to GND (if possible) prevents the high-current state. Any low-cost diode can be used (see Figure 11).

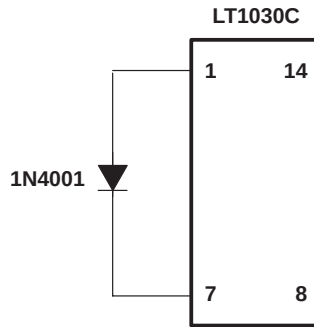


Figure 11. Connecting a Diode From V_{CC-} to GND

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LT1030CD	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	LT1030C
LT1030CD.A	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	LT1030C
LT1030CDR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	LT1030C
LT1030CDR.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	LT1030C
LT1030CN	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	LT1030CN
LT1030CN.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	LT1030CN

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

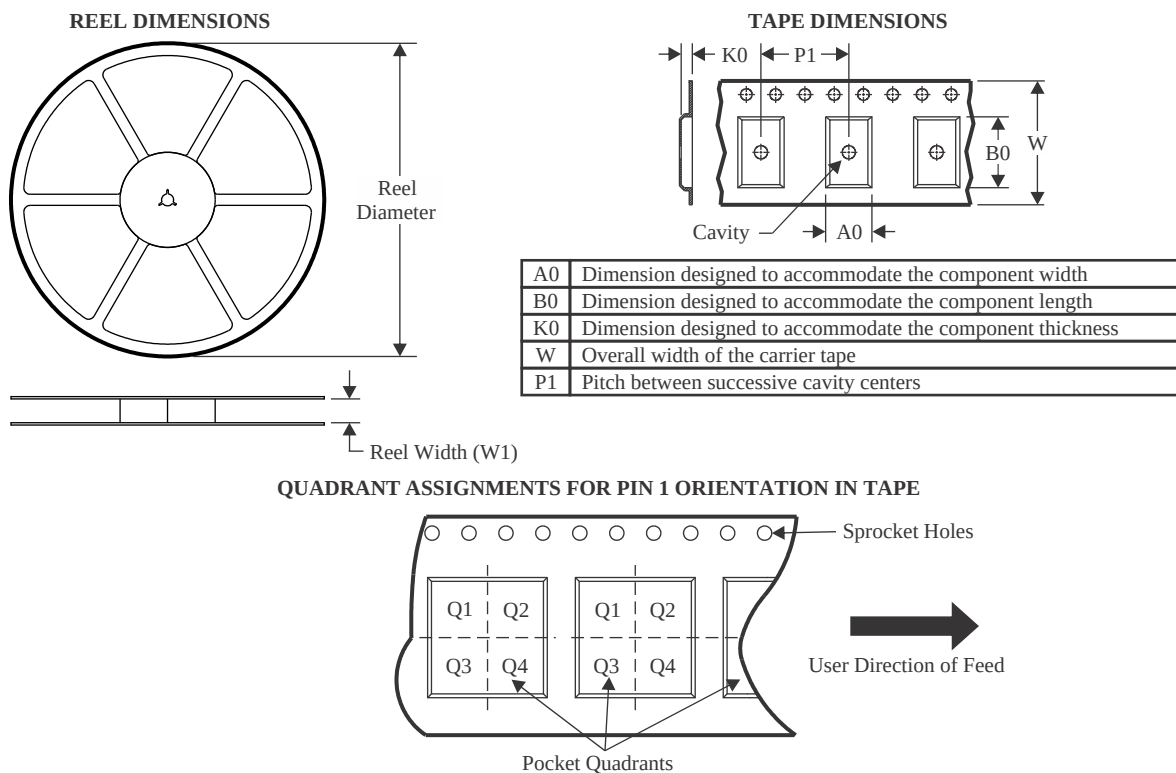
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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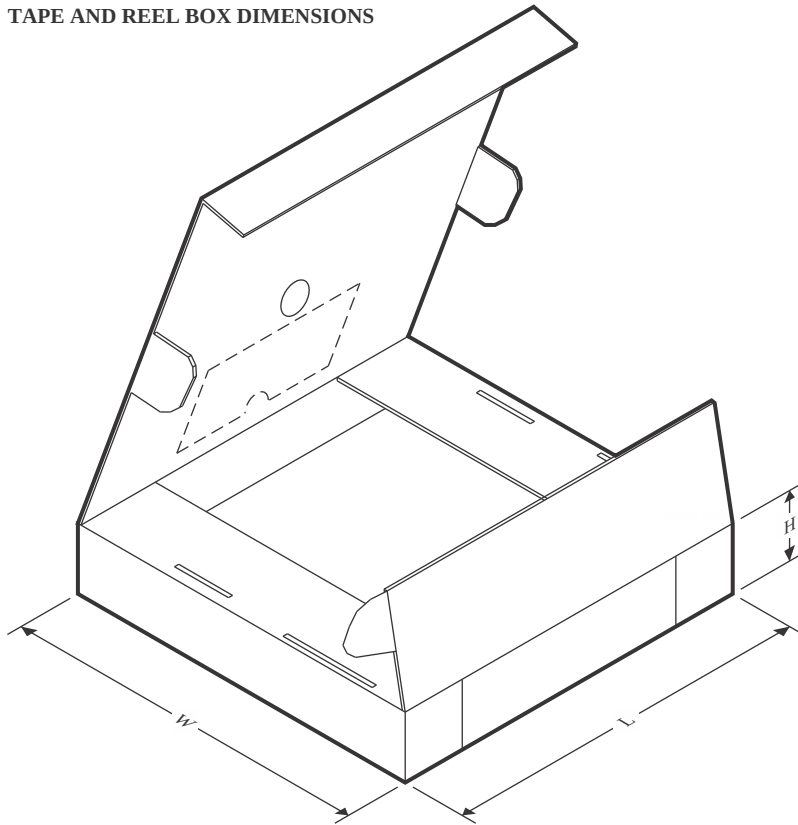
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LT1030CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

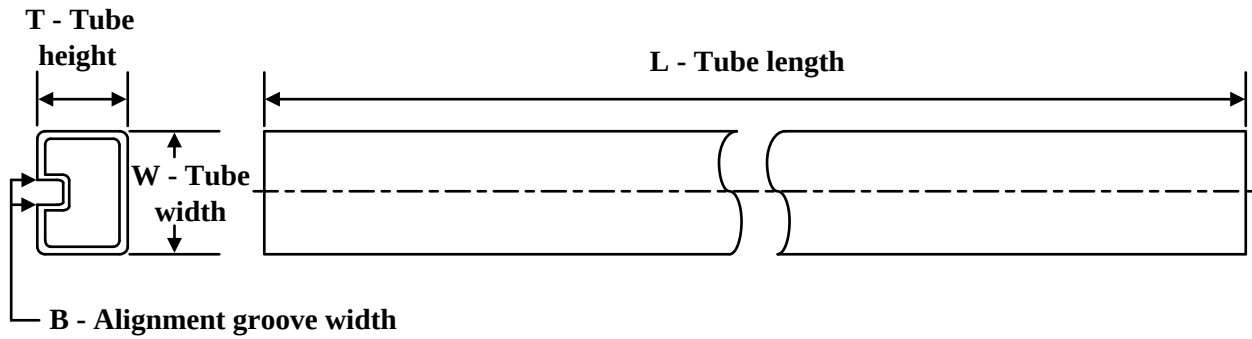
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LT1030CDR	SOIC	D	14	2500	356.0	356.0	35.0

TUBE



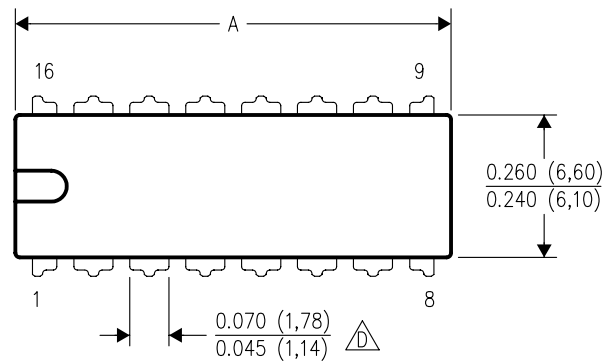
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
LT1030CD	D	SOIC	14	50	506.6	8	3940	4.32
LT1030CD.A	D	SOIC	14	50	506.6	8	3940	4.32
LT1030CN	N	PDIP	14	25	506	13.97	11230	4.32
LT1030CN.A	N	PDIP	14	25	506	13.97	11230	4.32

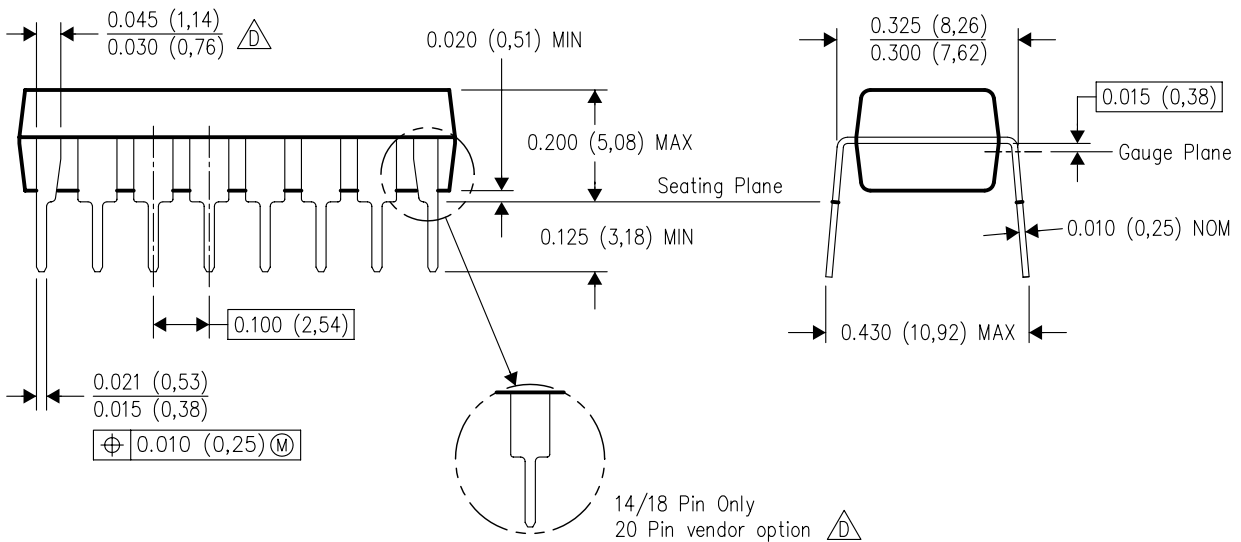
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE

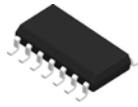


PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD

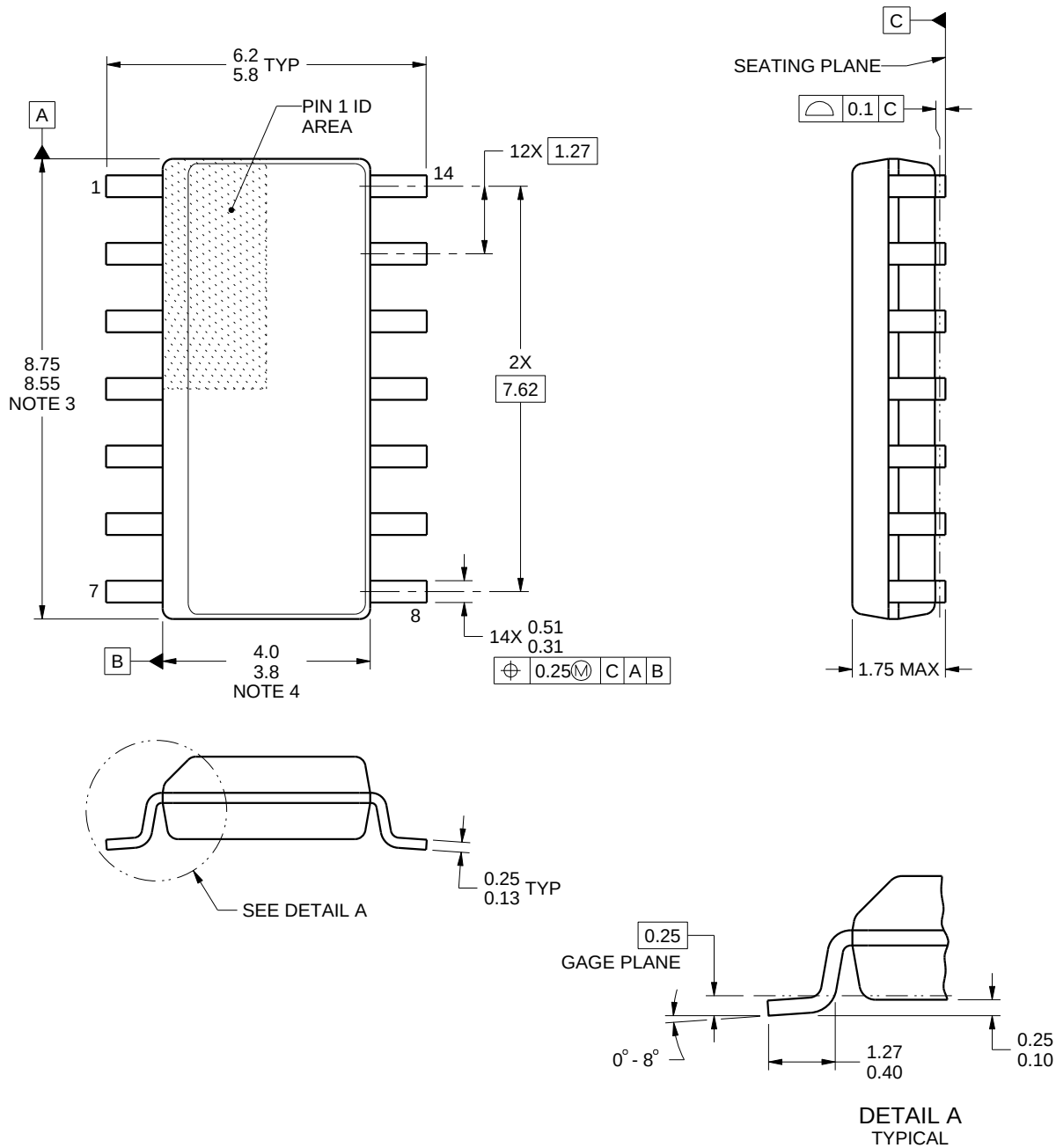


4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

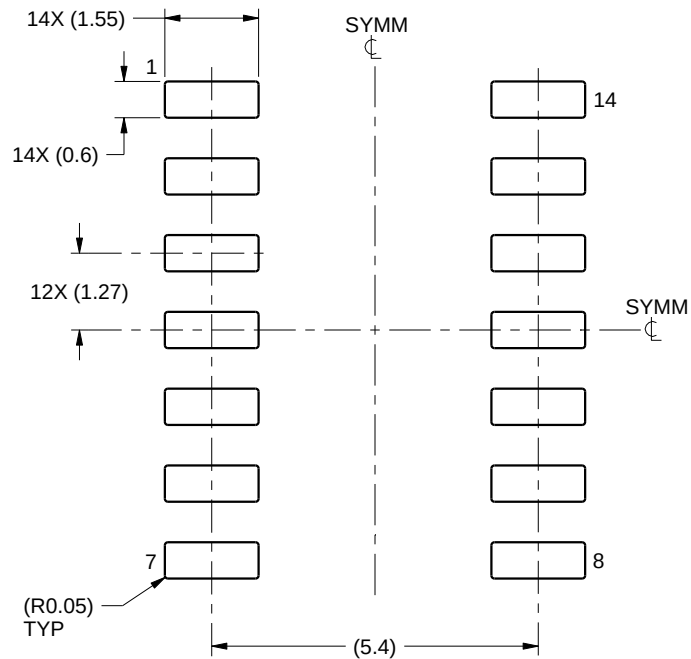
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

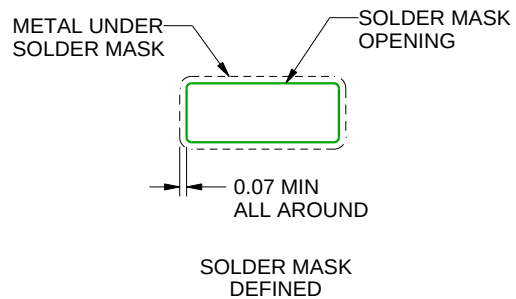
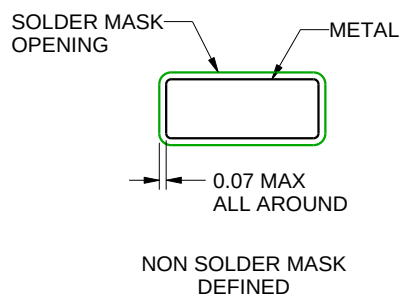
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

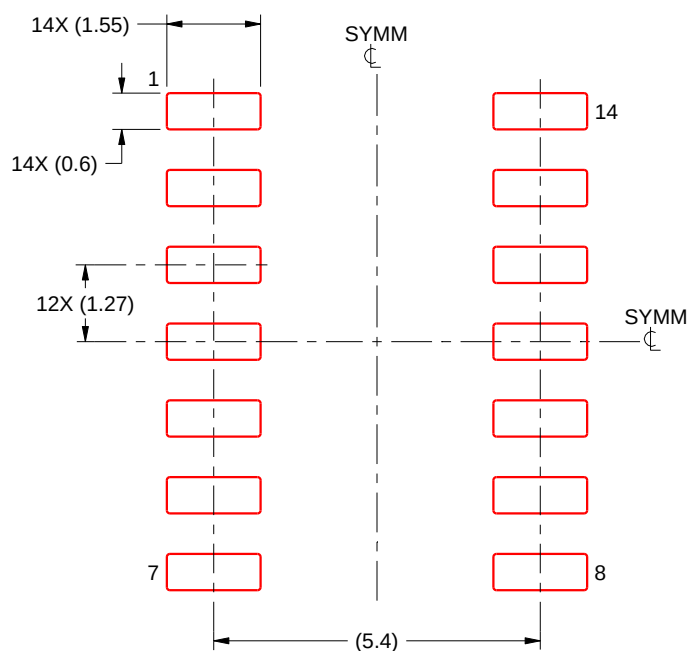
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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