

SN74SSTVF16859

13-BIT TO 26-BIT REGISTERED BUFFER WITH SSTL_2 INPUTS AND OUTPUTS

SCES429B – MARCH 2003 – REVISED FEBRUARY 2004

- Member of the Texas Instruments Widebus™ Family
- Operates at 2.3 V to 2.7 V for PC1600, PC2100, and PC2700
- Operates at 2.5 V to 2.7 V for PC3200 (QFN Package)
- Pinout and Functionality Compatible With JEDEC Standard SSTV16859
- 600 ps Faster (Simultaneous Switching) Than the JEDEC Standard SSTV16859 in PC2700 DIMM Applications
- 1-to-2 Outputs to Support Stacked DDR DIMMs
- Output Edge-Control Circuitry Minimizes Switching Noise in an Unterminated Line
- Outputs Meet SSTL_2 Class I Specifications
- Supports SSTL_2 Data Inputs
- Differential Clock (CLK and $\overline{\text{CLK}}$) Inputs
- Supports LVCMOS Switching Levels on the $\overline{\text{RESET}}$ Input
- $\overline{\text{RESET}}$ Input Disables Differential Input Receivers, Resets All Registers, and Forces All Outputs Low
- Pinout Optimizes DIMM PCB Layout
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DGG PACKAGE
(TOP VIEW)

Q13A	1	64	V _{DDQ}
Q12A	2	63	GND
Q11A	3	62	D13
Q10A	4	61	D12
Q9A	5	60	V _{CC}
V _{DDQ}	6	59	V _{DDQ}
GND	7	58	GND
Q8A	8	57	D11
Q7A	9	56	D10
Q6A	10	55	D9
Q5A	11	54	GND
Q4A	12	53	D8
Q3A	13	52	D7
Q2A	14	51	$\overline{\text{RESET}}$
GND	15	50	GND
Q1A	16	49	$\overline{\text{CLK}}$
Q13B	17	48	CLK
V _{DDQ}	18	47	V _{DDQ}
Q12B	19	46	V _{CC}
Q11B	20	45	V _{REF}
Q10B	21	44	D6
Q9B	22	43	GND
Q8B	23	42	D5
Q7B	24	41	D4
Q6B	25	40	D3
GND	26	39	GND
V _{DDQ}	27	38	V _{DDQ}
Q5B	28	37	V _{CC}
Q4B	29	36	D2
Q3B	30	35	D1
Q2B	31	34	GND
Q1B	32	33	V _{DDQ}

description/ordering information

This 13-bit to 26-bit registered buffer is designed for 2.3-V to 2.7-V V_{CC} operation.

ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	QFN – RGQ (Tin-Pb Finish)	Tape and reel	SN74SSTVF16859SR	SSF859
	QFN – RGQ (Matte-Tin Finish)		SN74SSTVF16859S8	
	TSSOP – DGG	Tape and reel	SN74SSTVF16859GR	SSTVF16859

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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WITH SSTL_2 INPUTS AND OUTPUTS

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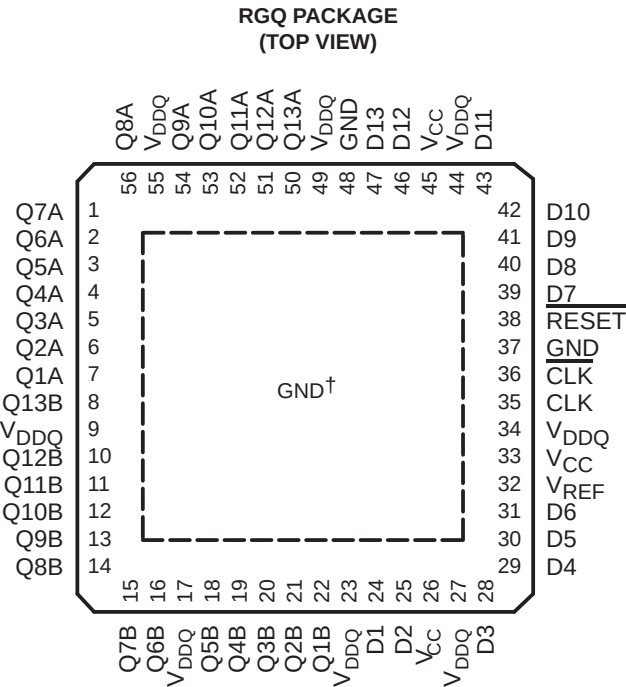
description/ordering information (continued)

All inputs are SSTL_2, except the LVCMOS reset ($\overline{\text{RESET}}$) input. All outputs are edge-controlled LVCMOS circuits optimized for unterminated DIMM loads.

The SN74SSTVF16859 operates from a differential clock (CLK and $\overline{\text{CLK}}$). Data are registered at the crossing of CLK going high and $\overline{\text{CLK}}$ going low.

The device supports low-power standby operation. When $\overline{\text{RESET}}$ is low, the differential input receivers are disabled, and undriven (floating) data, clock, and reference voltage (V_{REF}) inputs are allowed. In addition, when $\overline{\text{RESET}}$ is low, all registers are reset and all outputs are forced low. The LVCMOS $\overline{\text{RESET}}$ input always must be held at a valid logic high or low level.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the low state during power up.



[†] The center die pad must be connected to GND.

FUNCTION TABLE

INPUTS				OUTPUT Q
$\overline{\text{RESET}}$	CLK	$\overline{\text{CLK}}$	D	
H	↑	↓	H	H
H	↑	↓	L	L
H	L or H	L or H	X	Q ₀
L	X or floating	X or floating	X or floating	L

The diagram illustrates the internal logic of one of the 13 channels in the AD7714. It shows the following components and connections:

- Inputs:** RESET (51), CLK (48), CLK (49), VREF (45), and D1 (35).
- Logic:** The inputs are connected to a network of inverters and AND gates. The output of the logic is connected to a 1D C1 R flip-flop.
- Flip-flop:** The flip-flop has inputs 1D, C1, and R. The output of the flip-flop is connected to two comparators.
- Comparators:** The comparators have outputs Q1A (16) and Q1B (32).
- Output:** The outputs Q1A and Q1B are connected to the output pins 16 and 32.
- Label:** The diagram is labeled "One of 13 Channels" and "To 12 Other Channels".

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13-BIT TO 26-BIT REGISTERED BUFFER

WITH SSTL 2 INPUTS AND OUTPUTS

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recommended operating conditions (see Note 5)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		V_{DDQ}		2.7	V
V_{DDQ}	Output supply voltage	PC1600, PC2100, PC2700	2.3		2.7	V
		PC3200	2.5		2.7	V
V_{REF}	Reference voltage ($V_{REF} = V_{DDQ}/2$)	PC1600, PC2100, PC2700	1.15	1.25	1.35	V
		PC3200	1.25	1.3	1.35	V
V_I	Input voltage		0		V_{CC}	V
V_{IH}	AC high-level input voltage	Data inputs	$V_{REF}+310\text{mV}$			V
V_{IL}	AC low-level input voltage	Data inputs			$V_{REF}-310\text{mV}$	V
V_{IH}	DC high-level input voltage	Data inputs	$V_{REF}+150\text{mV}$			V
V_{IL}	DC low-level input voltage	Data inputs			$V_{REF}-150\text{mV}$	V
V_{IH}	High-level input voltage	$\overline{\text{RESET}}$	1.7			V
V_{IL}	Low-level input voltage	$\overline{\text{RESET}}$			0.7	V
V_{ICR}	Common-mode input voltage range	CLK, $\overline{\text{CLK}}$	0.97		1.53	V
$V_{I(PP)}$	Peak-to-peak input voltage	CLK, $\overline{\text{CLK}}$	360			mV
I_{OH}	High-level output current				-16	mA
I_{OL}	Low-level output current				16	mA
T_A	Operating free-air temperature		0		70	°C

NOTE 5: The $\overline{\text{RESET}}$ input of the device must be held at valid logic voltage levels (not floating) to ensure proper device operation. The differential inputs must not be floating unless $\overline{\text{RESET}}$ is low. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics for PC1600, PC2100, and PC2700 over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V _{CC} [†]	MIN	TYP [‡]	MAX	UNIT		
V _{IK}		I _I = −18 mA		2.3 V			−1.2	V		
V _{OH}		I _{OH} = −100 μA		2.3 V to 2.7 V	V _{DDQ} −0.2			V		
		I _{OH} = −8 mA		2.3 V	1.95					
V _{OL}		I _{OL} = 100 μA		2.3 V to 2.7 V	0.2			V		
		I _{OL} = 8 mA		2.3 V	0.35					
I _I	All inputs	V _I = V _{CC} or GND		2.7 V			±5	μA		
I _{CC}	Static standby	RESET = GND		2.7 V			10	μA		
	Static operating	RESET = V _{CC} , V _I = V _{IH} (AC) or V _{IL} (AC)					25	mA		
I _{CCD}	Dynamic operating – clock only	RESET = V _{CC} , V _I = V _{IH} (AC) or V _{IL} (AC), CLK and CLK switching 50% duty cycle		2.5 V			19	μA/MHz		
	Dynamic operating – per each data input	RESET = V _{CC} , V _I = V _{IH} (AC) or V _{IL} (AC), CLK and CLK switching 50% duty cycle, One data input switching at one-half clock frequency, 50% duty cycle					7	μA/clock MHz/D input		
C _i [§]	Data inputs	V _I = V _{REF} ± 310 mV		2.5 V			2.5	3	3.5	pF
	CLK, CLK	V _{ICR} = 1.25 V, V _I (PP) = 360mV					2.5	3	3.5	
	RESET	V _I = V _{CC} or GND					2.3	3	3.5	

† For this test condition, V_{DDQ} always is equal to V_{CC} .

‡ All typical values are at $V_{CC} = 2.5\text{ V}$, $T_A = 25^\circ\text{C}$.

§ Measured at 50-MHz input frequency



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electrical characteristics for PC3200 over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$V_{CC}^{\dagger}$	MIN	TYP [‡]	MAX	UNIT
V_{IK}		$I_I = -18 \text{ mA}$	2.5 V			-1.2	V
V_{OH}		$I_{OH} = -100 \mu\text{A}$	2.5 V to 2.7 V	$V_{DDQ} - 0.2$			V
		$I_{OH} = -8 \text{ mA}$	2.5 V	1.95			
V_{OL}		$I_{OL} = 100 \mu\text{A}$	2.5 V to 2.7 V			0.2	V
		$I_{OL} = 8 \text{ mA}$	2.5 V			0.35	
I_I	All inputs	$V_I = V_{CC}$ or GND	2.7 V			± 5	μA
I_{CC}	Static standby	$\overline{\text{RESET}} = \text{GND}$	2.7 V			10	μA
	Static operating	$\overline{\text{RESET}} = V_{CC}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$				25	mA
I_{CCD}	Dynamic operating – clock only	$\overline{\text{RESET}} = V_{CC}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and CLK switching 50% duty cycle	2.6 V			19	$\mu\text{A}/\text{MHz}$
	Dynamic operating – per each data input	$\overline{\text{RESET}} = V_{CC}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and CLK switching 50% duty cycle, One data input switching at one-half clock frequency, 50% duty cycle				7	$\mu\text{A}/\text{clock MHz}/\text{D input}$
$C_i^{\S}$	Data inputs	$V_I = V_{REF} \pm 310 \text{ mV}$	2.6 V	2.5	3	3.5	pF
	CLK, $\overline{\text{CLK}}$	$V_{ICR} = 1.25 \text{ V}$, $V_{I(PP)} = 360 \text{ mV}$		2.5	3	3.5	
	$\overline{\text{RESET}}$	$V_I = V_{CC}$ or GND		2.3	3	3.5	

[†] For this test condition, V_{DDQ} always is equal to V_{CC} .

[‡] All typical values are at $V_{CC} = 2.6 \text{ V}$, $T_A = 25^\circ\text{C}$.

[§] Measured at 50-MHz input frequency

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

				V _{CC} = 2.5 V ± 0.2 V†		V _{CC} = 2.6 V ± 0.1 V†		UNIT	
				MIN	MAX	MIN	MAX		
f _{clock}	Clock frequency			500		500		MHz	
t _w	Pulse duration, CLK, $\overline{\text{CLK}}$ high or low			1		1		ns	
t _{act}	Differential inputs active time (see Note 6)			22		22		ns	
t _{inact}	Differential inputs inactive time (see Note 7)			22		22		ns	
t _{su}	Setup time	Fast slew rate (see Notes 8 and 10)		Data before CLK↑, $\overline{\text{CLK}}$ ↓	0.65		0.65		ns
		Slow slew rate (see Notes 9 and 10)			0.75		0.75		
t _h	Hold time	Fast slew rate (see Notes 8 and 10)		Data after CLK↑, $\overline{\text{CLK}}$ ↓	0.65		0.65		ns
		Slow slew rate (see Notes 9 and 10)			0.8		0.8		

[†] For this test condition, V_{DDQ} always is equal to V_{CC} .

- NOTES: 6. V_{REF} must be held at a valid input level, and data inputs must be held low for a minimum time of t_{act} max, after $\overline{\text{RESET}}$ is taken high.
7. V_{REF} , data, and clock inputs must be held at valid voltage levels (not floating) for a minimum time of t_{inact} max, after $\overline{\text{RESET}}$ is taken low.
8. For data signal input slew rate $\geq 1 \text{ V/ns}$.
9. For data signal input slew rate $\geq 0.5 \text{ V/ns}$ and $< 1 \text{ V/ns}$.
10. CLK, $\overline{\text{CLK}}$ signals input slew rates are $\geq 1 \text{ V/ns}$.

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switching characteristics for TSSOP over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}^\dagger$		UNIT
			MIN	MAX	
$f_{\max}$			500		MHz
$t_{pd}^\ddagger$	CLK and $\overline{\text{CLK}}$	Q	1.1	2.5	ns
t_{PHL}	$\overline{\text{RESET}}$	Q		5	ns

[†] For this test condition, V_{DDQ} always is equal to V_{CC} .

[‡] Single-bit switching

switching characteristics for QFN over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}^\dagger$		$V_{CC} = 2.6\text{ V}$ $\pm 0.1\text{ V}^\dagger$		UNIT
			MIN	MAX	MIN	MAX	
$f_{\max}$			500		500		MHz
$t_{pd}^\ddagger$	CLK and $\overline{\text{CLK}}$	Q	1.1	2.5	1.1	2.2	ns
t_{PHL}	$\overline{\text{RESET}}$	Q		5		5	ns

[†] For this test condition, V_{DDQ} always is equal to V_{CC} .

[‡] Single-bit switching

output slew rates over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

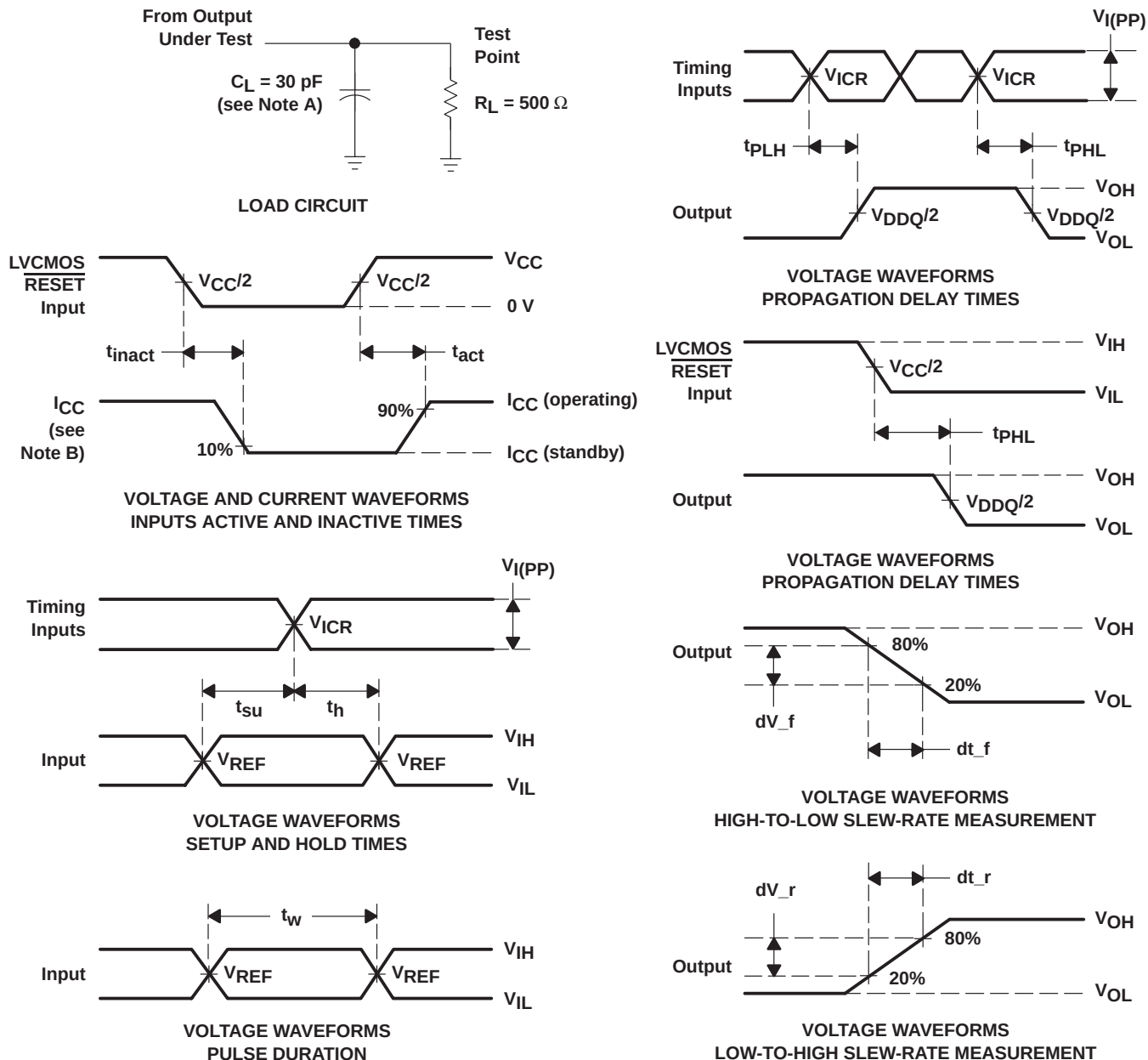
PARAMETER	FROM	TO	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}^\dagger$		$V_{CC} = 2.6\text{ V}$ $\pm 0.1\text{ V}^\dagger$		UNIT
			MIN	MAX	MIN	MAX	
dV/dt_r	20%	80%	1	4	1	4	V/ns
dV/dt_f	80%	20%	1	4	1	4	V/ns
$dV/dt_{\Delta}^\S$	20% or 80%	80% or 20%		1		1	V/ns

[†] For this test condition, V_{DDQ} always is equal to V_{CC} .

[§] Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate).

PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ AND $V_{CC} = 2.6\text{ V} \pm 0.1\text{ V}$



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. I_{CC} tested with clock and data inputs held at V_{CC} or GND, and $I_O = 0\text{ mA}$.
 - C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, input slew rate $= 1\text{ V/ns} \pm 20\%$ (unless otherwise noted).
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. $V_{TT} = V_{REF} = V_{DDQ}/2$
 - F. $V_{IH} = V_{REF} + 310\text{ mV}$ (ac voltage levels) for differential inputs. $V_{IH} = V_{CC}$ for LVC MOS input.
 - G. $V_{IL} = V_{REF} - 310\text{ mV}$ (ac voltage levels) for differential inputs. $V_{IL} = \text{GND}$ for LVC MOS input.
 - H. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74SSTVF16859G4R	OBSOLETE	VQFN	RGQ	56		TBD	Call TI	Call TI	0 to 70	SSF859	
SN74SSTVF16859GR	ACTIVE	TSSOP	DGG	64	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	SSTVF16859	Samples
SN74SSTVF16859S8	OBSOLETE	VQFN	RGQ	56		TBD	Call TI	Call TI	0 to 70	SSF859	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=100ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

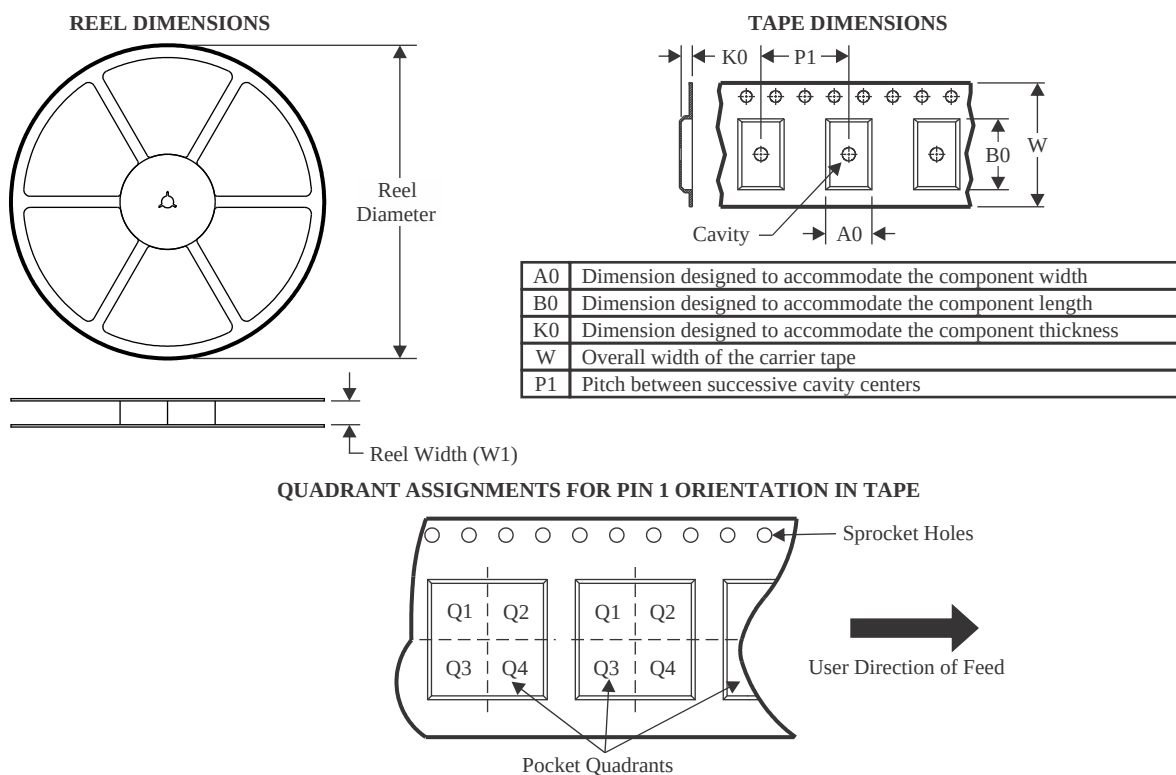
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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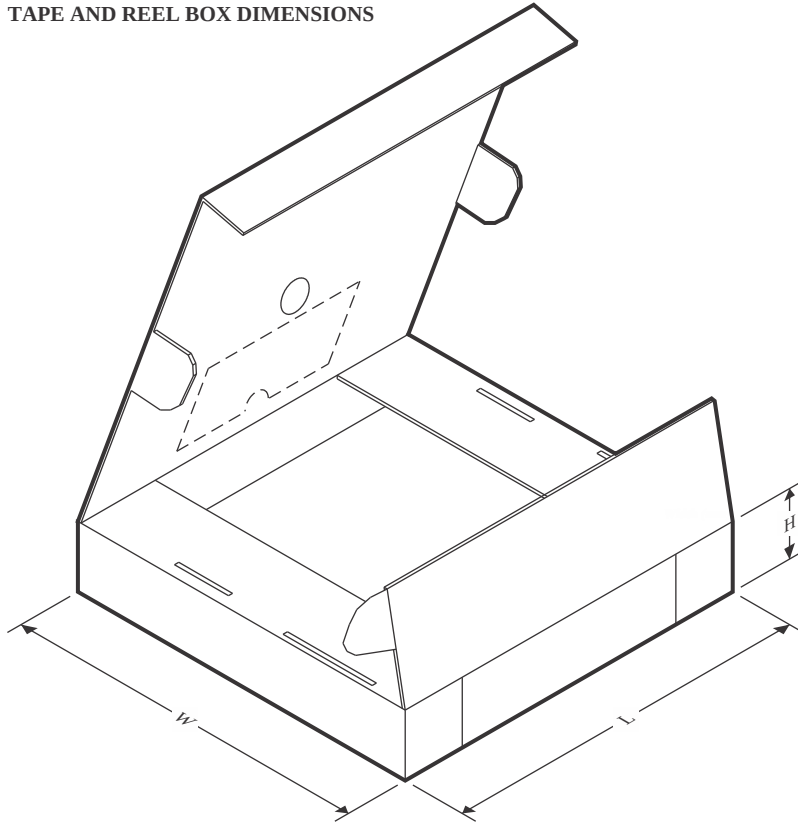
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74SSTVF16859GR	TSSOP	DGG	64	2000	330.0	24.4	8.4	17.3	1.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

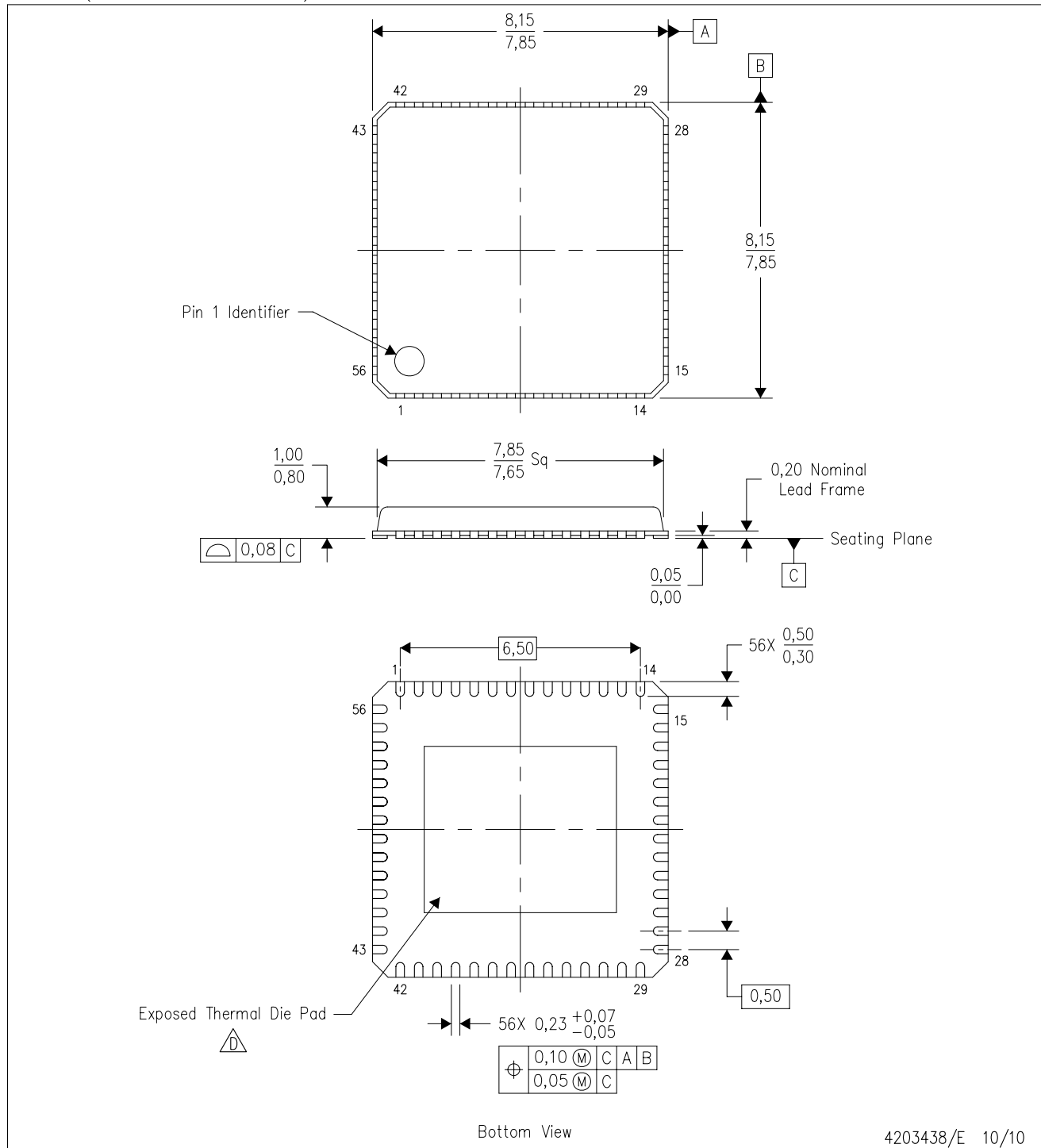


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74SSTVF16859GR	TSSOP	DGG	64	2000	367.0	367.0	45.0

RGQ (S-PVQFN-N56)

PLASTIC QUAD FLATPACK NO-LEAD

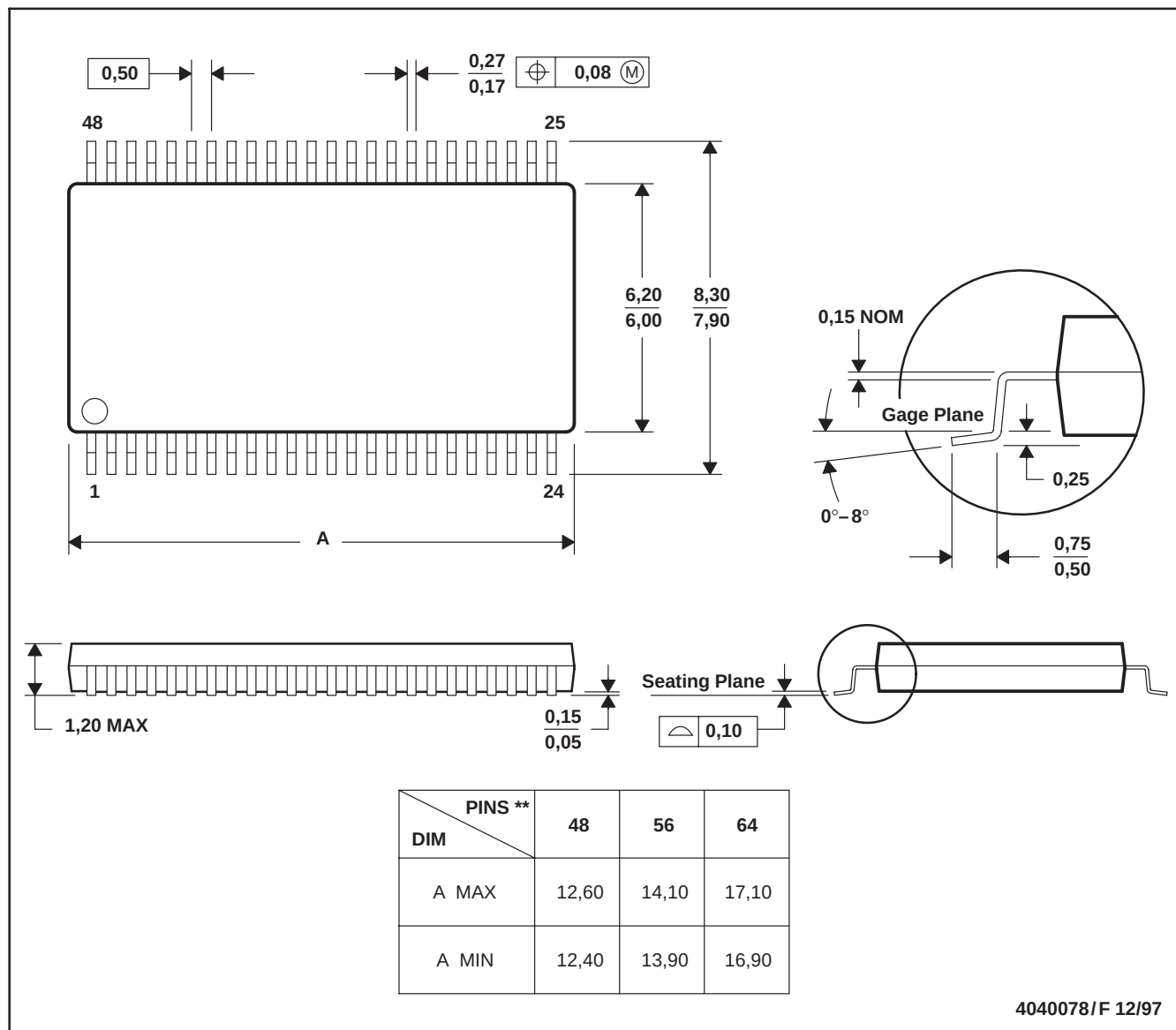


- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) Package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - E. Package complies to JEDEC MO-220 variation VLLD-2.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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