TPS25814 USB Type-C® Controller with Integrated Source Power Switch

1 Features

- USB Type-C specification compliant
  - Cable attach and orientation detection
  - Integrated VCONN switch
  - 26-V tolerant CC pins
  - Configurable current advertisement
- Integrated VBUS sourcing port power switch
  - 5-V, 3-A, 36-mΩ Sourcing switch
  - UL recognized component (E169910)
  - Undervoltage and overvoltage protection
  - Configurable current limit up to 3 A
- USB type-C connector system software interface (USCI) support
- Supports industrial temperature range
- Optional simple power management for multi-port systems

2 Applications

- Notebook and desktop computers
- 15-W USB-C chargers
- Docking stations and hubs

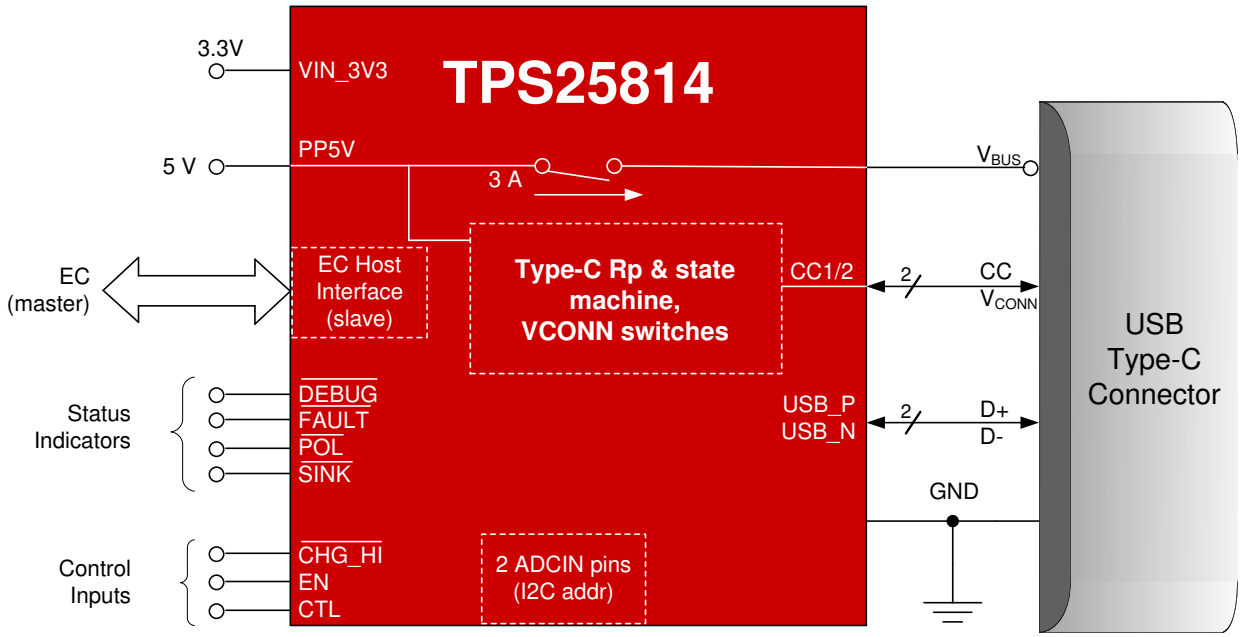
3 Description

The TPS25814 is a stand-alone USB Type-C controller providing cable plug and orientation detection for one USB Type-C connector. Upon cable attachment, the TPS25814 performs cable detection according to the USB Type-C specification. When cable detection is complete, the TPS25814 enables the internal power path. Status indicator pins may be used to control an external multiplexer.

Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
TPS25814	QFN (RSM)	4.0 mm x 4.0 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (July 2020) to Revision A (December 2020)	Page
• First public release	1

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5 Pin Configuration and Functions

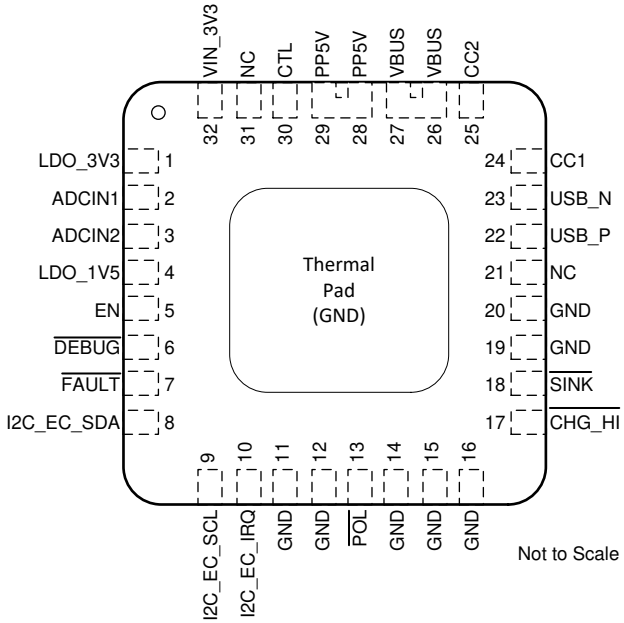

Figure 5-1. RSM Package 32-pin QFN Top View

Table 5-1. Pin Functions

PIN		TYPE(1)	RESET	Description
NAME	NO.			
ADCIN1	2	I	Hi-Z	Configuration input. Connect to a resistor divider to LDO_3V3.
ADCIN2	3	I	Hi-Z	Configuration input. Connect to a resistor divider to LDO_3V3.
CC1	24	I/O	Hi-Z	I/O for USB Type-C .
CC2	25	I/O	Hi-Z	I/O for USB Type-C .
$\overline{\text{CHG_HI}}$	17	I	Hi-Z	Charge logic input to select between minimum or maximum Type-C current advertisement.
CTL	30	I	Hi-Z	This pin controls which BC 1.2 mode is used. Pull to GND for CDP mode. Pull high for DCP mode.
$\overline{\text{DEBUG}}$	6	O	Hi-Z	Open-drain logic output that is asserted low when a Type-C debug accessory is detected.
EN	5	I	Low	When this pin is pulled low or left floating, the device will be disabled and remain in the Type-C Error Recovery state.
$\overline{\text{FAULT}}$	7	O	Hi-Z	Open-drain logic output that asserts when an over-current fault is detected.
GND	11,12,14,15,16, 19,20	—	—	Ground. Connect to ground plane.
I2C_EC_SCL	9	I	Hi-Z	I2C slave serial clock input. Tie to pullup voltage through a resistor when used or unused. Connect to Embedded Controller (EC).
I2C_EC_SDA	8	I/O	Hi-Z	I2C slave serial data. Open-drain output. Tie to pullup voltage through a resistor when used or unused. Connect to Embedded Controller (EC).
$\overline{\text{I2C_EC_IRQ}}$	10	O	Hi-Z	I2C slave interrupt. Active low. Connect to external voltage through a pull-up resistor. May also be used as a general purpose digital output. Connect to Embedded Controller (EC).
LDO_1V5	4	O	—	Output of the CORE LDO. Bypass with capacitance C_{LDO_1V5} to GND. This pin cannot source current to external circuits.

Table 5-1. Pin Functions (continued)

PIN		TYPE[(1)]	RESET	Description
NAME	NO.			
LDO_3V3	1	O	—	Output of supply switched from VIN_3V3 or VBUS LDO. Bypass with capacitance C_{LDO_3V3} to GND.
$\overline{POL}$	13	O	Hi-Z	Open-drain logic output that gives the information needed to mux the superspeed lines. It is asserted low when CC2 is connected to the cable CC line.
PP5V	28,29	I	—	5-V System Supply to VBUS, supply for CCy pins as VCONN.
$\overline{SINK}$	18	O	Hi-Z	Open-drain logic output that asserts low when a Type-C Sink is identified on the CC lines.
USB_N	23	I/O	Hi-Z	I/O for BC 1.2 functionality. Connect to the USB D- line.
USB_P	22	I/O	Hi-Z	I/O for BC 1.2 functionality. Connect to the USB D+ line.
VBUS	26,27	I/O		5-V to 20-V input. Bypass with capacitance C_{VBUS} to GND.
VIN_3V3	32	I	—	Supply for core circuitry and I/O. Bypass with capacitance CVIN_3V3 to GND.
NC	21,31	—	—	This pin has no functionality. Leave floating.

(1) I = input, O = output, I/O = input and output, GPIO = general purpose digital input and output

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Input voltage range [2]	PP5V	–0.3	6	V
	VIN_3V3	–0.3	4	
	ADCIN1, ADCIN2	–0.3	4	
	VBUS[4]	–0.3	28	V
	CC1, CC2 [4]	–0.5	26	
	$\overline{\text{SINK}}$, $\overline{\text{FAULT}}$, $\overline{\text{CHG_HI}}$, USB_P, USB_N, CTL, $\overline{\text{POL}}$, $\overline{\text{DEBUG}}$, EN	-0.3	6.0	
	I2C_EC_SDA, I2C_EC_SCL, $\overline{\text{I2C_EC_IRQ}}$	–0.3	4	
Output voltage range [2]	LDO_1V5[3]	–0.3	2	V
	LDO_3V3[3]	–0.3	4	
Source current	Source or sink current VBUS		internally limited	A
	Positive source current on CC1, CC2		1	
	Positive sink current on CC1, CC2 while VCONN switch is enabled		1	
	positive sink current for I2C_EC_SDA, I2C_EC_SCL		internally limited	
	positive source current for LDO_3V3, LDO_1V5		internally limited	
T_J Operating junction temperature		–40	175	°C
T_{STG} Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network GND. Connect the GND pin directly to the GND plane of the board.
(3) Do not apply voltage to these pins.
(4) A TVS with a break down voltage falling between the Recommended max and the Abs max value is recommended such as TVS2200.

6.2 ESD Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±1000	V
		Charged device model (CDM), per JEDEC specificationJESD22-C101, all pins[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_I	Input voltage range [1]	VIN_3V3	3.0	3.6	V
		PP5V	4.9	5.5	
		VBUS	4	22	

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{IO}	I/O voltage range [1]	I2C_EC_SDA, I2C_EC_SCL, $\overline{\text{I2C_EC_IRQ}}$, ADCIN1, ADCIN2	0	3.6	V
		$\overline{\text{SINK}}$, $\overline{\text{FAULT}}$, $\overline{\text{CHG_HI}}$, USB_P, USB_N, CTL, $\overline{\text{POL}}$, $\overline{\text{DEBUG}}$, EN	0	5.5	
		CC1, CC2	0	5.5	
I_O	Output current (from PP5V)	VBUS		3	A
		CC1, CC2		315	mA
I_O	Output current (from VBUS LDO)	current from LDO_3V3		5	mA
T_A	Ambient operating temperature	$I_{PP_5V} \leq 1.5$ A, $I_{PP_CABLE} \leq 315$ mA	–40	105	°C
		$I_{PP_5V} \leq 3$ A, $I_{PP_CABLE} \leq 315$ mA	–40	85	
T_J	Operating junction temperature		–40	125	°C

(1) All voltage values are with respect to network GND. All GND pins must be connected directly to the GND plane of the board.

6.4 Recommended Capacitance

over operating free-air temperature range (unless otherwise noted)

PARAMETER[1]		VOLTAGE RATING	MIN	NOM	MAX	UNIT
C_{VIN_3V3}	Capacitance on VIN_3V3	6.3 V	5	10		µF
C_{LDO_3V3}	Capacitance on LDO_3V3	6.3 V	5	10	25	µF
C_{LDO_1V5}	Capacitance on LDO_1V5	4 V	4.5		12	µF
C_{VBUS}	Capacitance on VBUS	25 V	1	4.7	10	µF
C_{PP5V}	Capacitance on PP5V	10 V	120			µF

(1) Capacitance values do not include any derating factors. For example, if 5.0 µF is required and the external capacitor value reduces by 50% at the required operating voltage, then the required external capacitor value would be 10 µF.

6.5 Thermal Information

THERMAL METRIC[1]		TPS25814 QFN (RSM) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.5	°C/W
$R_{\theta JC}$ (top)	Junction-to-case (top) thermal resistance	24.5	°C/W
$R_{\theta JC}$	Junction-to-board (bottom) thermal resistance	2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Power Supply Characteristics

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN_3V3, VBUS						
V_{VBUS_UVLO}	VBUS UVLO threshold.	rising	3.6		3.9	V
		falling	3.5		3.8	
		hysteresis		0.1		

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Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VIN3V3_UVLO}	voltage required on VIN_3V3 for power on	rising, V_{VBUS}=0	2.56	2.66	2.76	V
		falling, V_{VBUS}=0	2.44	2.54	2.64	
		hysteresis		0.12		
LDO_3V3, LDO_1V5						
V_{LDO_3V3}	voltage on LDO_3V3	V_{VIN_3V3} = 0V, 10 µA ≤ I_{LOAD} ≤ 18 mA, V_{VBUS} ≥ 3.9V	3.0	3.4	3.6	V
R_{LDO_3V3}	Rdson of VIN_3V3 to LDO_3V3	I_{LDO_3V3}=50mA			1.4	Ω
V_{LDO_1V5}	voltage on LDO_1V5	up to maximum internal loading condition.	1.49	1.5	1.65	V

6.7 Power Consumption

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V, no GPIO loading

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{VIN_3V3,ActSrc}$	current into VIN_3V3	Active Source mode: V_{VBUS}=5.0V, V_{VIN_3V3}=3.3V		3		mA
$I_{VIN_3V3,IdlSrc}$	current into VIN_3V3	Idle Source mode: V_{VBUS}=5.0V, V_{VIN_3V3}=3.3V		1.0		mA
$P_{MstbySrc}$	Power drawn into PP5V and VIN_3V3 in Modern Standby Source Mode	CCm floating, CCn tied to GND through 5.1kΩ, V_{PP5V} = 5V, V_{VIN_3V3}=3.3V, I_{VBUS}=0, T_J=25ºC		4.5		mW
$I_{VIN_3V3,SleepSrc}$	current into VIN_3V3	Sleep source mode: V_{VBUS}=0V, V_{VIN_3V3}=3.3V		61		µA
$I_{PP5V,Sleep}$	current into PP5V	Sleep mode: V_{VBUS}=0V, V_{VIN_3V3}=3.3V		2		µA
$I_{PP5V,ActSrc}$	current into PP5V	Active Source mode: V_{VBUS}=5.0V, V_{VBUS}=5.0V, V_{VIN_3V3}=3.3V. No external load on VBUS.		0.5		mA

6.8 PP_5V Power Switch Characteristics

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{PP_5V}	Resistance from PP5V to VBUS	I_{LOAD} = 3 A, T_J=25ºC		36	38	mΩ
R_{PP_5V}	Resistance from PP5V to VBUS	I_{LOAD} = 3 A, T_J=125ºC		36	53	mΩ
I_{PP5V_REV}	VBUS to PP5V leakage current	V_{PP5V} = 0V, V_{VBUS} = 5.5V, PP_5V disabled, T_J≤85ºC, measure I_{PP5V}			5	µA
I_{PP5V_FWD}	PP5V to VBUS leakage current	V_{PP5V} = 5.5V, V_{VBUS} = 0V, PP_5V disabled, T_J≤85ºC, measure I_{VBUS}			15	µA
I_{LIM5V}	Current limit setting	1.5A setting	2.3		2.70	A
I_{LIM5V}	Current limit setting	3.0A setting	3.22		3.78	A
I_{VBUS}	PP5V to VBUS current sense accuracy	3.64A ≥ I_{VBUS} ≥ 1A	3.05	3.5	3.75	A/V
$V_{PP_5V_RCP}$	RCP clears and PP_5V starts turning on when V_{VBUS} – V_{PP5V} < $V_{PP_5V_RCP}$. Measure V_{VBUS} – V_{PP5V}		10		20	mV
$t_{iOS_PP_5V}$	response time to VBUS short circuit	VBUS to GND through 10mΩ, C_{VBUS}=0		1.15		µs
$t_{PP_5V_ovp}$	response time to V_{VBUS} > $V_{OVP4RCP}$	Enable PP_5V, I_{RpDef} being drawn from PP5V, configure $V_{OVP4RCP}$ to setting 2, ramp V_{VBUS} from 4V to 20V at 100 V/ms, C_{PP5V} = 2.5 µF, measure time from OVP detection until reverse current < 100 mA		4.5		µs

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Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PP_5V_uvlo}$	response time to V_{PP5V} < V_{PP5V_UVLO}, PP_VBUS is deemed off when V_{VBUS} < 0.8V	R_L = 100 Ω, no external capacitance on VBUS		4		µs
$t_{PP_5V_rcp}$	response time to V_{PP5V} < V_{VBUS} +$V_{PP_5V_RCP}$	V_{PP5V}=5.5V, I_{RpDef} being drawn from PP5V, enable PP_5V, configure $V_{OVP4RCP}$ to setting 2, ramp V_{VBUS} from 4V to 21.5V at 10 V/µs, measure V_{PP5V}. C_{PP5V} = 104 µF, C_{VBUS}=10µF, measure time from RCP detection until reverse current < 100 mA.		0.7		µs
t_{ILIM}	Current limit deglitch time			5.1		ms
t_{ON}	from enable signal to VBUS at 90% of final value	R_L = 100Ω, V_{PP5V} = 5V, C_L=0	2.3	3.3	4.3	ms
t_{OFF}	from disable signal to VBUS at 10% of final value	R_L = 100Ω, V_{PP5V} = 5V, C_L=0	0.30	0.45	0.6	ms
t_{RISE}	VBUS from 10% to 90% of final value	R_L = 100Ω, V_{PP5V} = 5V, C_L=0	1.2	1.7	2.2	ms
t_{FALL}	VBUS from 90% to 10% of initial value	R_L = 100Ω, V_{PP5V} = 5V, C_L=0	0.06	0.1	0.14	ms

6.9 Power Path Supervisory

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OVP4RCP}$	VBUS over voltage protection	OVP detected when V_{VBUS} > $V_{OVP4RCP}$ (rising)	5.54	5.8	6.08	V
$V_{OVP4RCP}$	VBUS over voltage protection	falling	5.44		5.94	V
V_{PP5V_UVLO}	Voltage required on PP5V	rising	3.9	4.1	4.3	V
		falling	3.8	4.0	4.2	
		hysteresis		0.1		
I_{DSCH}	VBUS discharge current	V_{VBUS} = 22V, measure I_{VBUS}	4		15	mA

6.10 CC Cable Detection Parameters

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Type-C Source (Rp pull-up)						
$V_{OC_3.3}$	Unattached CCy open circuit voltage while Rp enabled, no load	V_{LDO_3V3} > 2.302 V, R_{CC} = 47 kΩ	1.85			V
V_{OC_5}	Attached CCy open circuit voltage while Rp enabled, no load	V_{PP5V} > 3.802 V, R_{CC} = 47 kΩ	2.95			V
I_{Rev}	Unattached reverse current on CCy	V_{CCy} = 5.5V, V_{CCx} = 0V, $V_{LDO_3V3_UVLO}$ < V_{LDO_3V3} < 3.6 V, V_{PP5V} = 3.8 V , measure current into CCy			10	µA
		V_{CCy} = 5.5V, V_{CCx} = 0V, $V_{LDO_3V3_UVLO}$ < V_{LDO_3V3} < 3.6 V, V_{PP5V} = 0, T_J≤85°C, measure current into CCy			10	
I_{RpDef}	current source - USB Default	0 < V_{CCy} < 1.0 V, measure I_{CCy}	64	80	96	µA
$I_{Rp1.5}$	current source - 1.5A	4.75 V < V_{PP5V} < 5.5 V, 0 < V_{CCy} < 1.5 V, measure I_{CCy}	166	180	194	µA

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Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{Rp3.0}$	current source - 3.0A	4.75 V < V_{PP5V} < 5.5 V, 0 < V_{CCy} < 2.45 V, measure I_{CCy}	304	330	356	µA

6.11 CC VCONN Parameters

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{PP_CABLE}	Rdson of the VCONN path	V_{PP5V}=5V, I_L = 250 mA, measure resistance from PP5V to CCy			1.2	Ω
I_{LIMVC}	short circuit current limit	V_{PP5V}=5V, R_L=10mΩ , measure I_{CCy}	540	600	660	mA
$I_{CC2PP5V}$	Reverse leakage current through VCONN FET	VCONN disabled, T_J ≤ 85 °C, V_{CCy} = 5.5 V, V_{PP5V}=0 V, V_{VBUS}=5V, LDO forced to draw from VBUS, measure I_{CCy}			10	µA
V_{VC_OVP}	Over-voltage protection threshold for PP_CABLE	V_{PP5V} rising	5.6	5.9	6.2	V
V_{VC_RCP}	Reverse current protection threshold for PP_CABLE, sourcing VCONN through CCx	V_{PP5V} ≥ 4.9 V, V_{CCy} = V_{PP5V}, V_{CCx} rising	60	200	340	mV
		V_{PP5V} ≥ 4.9 V, V_{CCy} ≤ 4 V, V_{CCx} rising	210	340	470	mV
t_{VCILIM}	Current clamp deglitch time			1.3		ms
$t_{PP_CABLE_FSD}$	Time to disable PP_CABLE after V_{PP5V} > V_{VC_OVP} or V_{CCx} - V_{PP5V} > V_{VC_RCP}	C_L=0		0.5		µs
$t_{PP_CABLE_off}$	from disable signal to CCy at 10% of final value	I_L = 250 mA, V_{PP5V} = 5V, C_L=0	100	200	300	µs
$t_{iOS_PP_CABLE}$	response time to short circuit	V_{PP5V}=5V, for short circuit R_L = 10mΩ.		2		µs

6.12 Thermal Shutdown Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{SD_MAIN}	Temperature shutdown threshold	Temperature rising	145	160	175	°C
		hysteresis		20		°C
T_{SD_PP5V}	Temperature controlled shutdown threshold. The PP_5V and PP_CABLE power paths have local sensors that disables them when this temperature is exceeded.	Temperature rising	135	150	165	°C
		hysteresis		10		°C

6.13 Input/Output (I/O) Characteristics

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CHG_HI, CTL, EN						
GPIO_VIH	GPIOx high-Level input voltage	V_{LDO_3V3} = 3.3V	1.3			V
GPIO_VIL	GPIOx low-level input voltage	V_{LDO_3V3} = 3.3V			0.54	V
GPIO_HYS	GPIOx input hysteresis voltage	V_{LDO_3V3} = 3.3V	0.09			V
GPIO_ILKG	GPIOx leakage current	V_{GPIOx} = 3.45 V	–1		1	µA
GPIO_RPD	GPIOx internal pull-down	pull-down enabled	50	100	150	kΩ
GPIO_DG	GPIOx input deglitch			20		ns

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Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Status Outputs						
GPIO_VOL	GPIOx output low voltage	V_{LDO_3V3} = 3.3V, I_{GPIOx}=2mA			0.4	V
ADCIN1, ADCIN2						
ADCIN_ILKG	ADCINx leakage current	V_{ADCINx} = 3.45 V, V_{VIN_3V3} = 3.3	–1		1	µA
t_{BOOT}	time from LDO_3V3 going high until ADCINx is read for configuration			10		ms

6.14 BC1.2 Characteristics

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Advertisement						
V_{DX_SRC}	Source voltage	C_{USB_P} ≤ 600 pF	0.55	0.6	0.65	V
V_{DX_ILIM}	VDX_SRC current limit		250		400	µA
I_{DX_SNK}	Sink Current	V_{USB_P} ≥ 250 mV	25	75	125	µA
I_{DX_SNK}	Sink Current	V_{USB_N} ≥ 250 mV	25	75	125	µA
R_{DCP_DAT}	Dedicated Charging Port Resistance	0.5 V ≤ V_{USB_P} ≤ 0.7 V, 25 µA ≤ I_{USB_N} ≤ 175 µA			200	Ω

6.15 I2C Requirements and Characteristics

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\overline{\text{I2C_EC_IRQ}}$						
OD_VOL_IRQ	Low level output voltage	I_{OL} = 2 mA			0.4	V
OD_LKG_IRQ	Leakage Current	Output is Hi-Z, V_{I2Cx_IRQ} = 3.45 V	–1		1	µA
SDA and SCL Common Characteristics (Slave)						
V_{IL}	Input low signal	V_{LDO_3V3}=3.3V,			0.54	V
V_{IH}	Input high signal	V_{LDO_3V3}=3.3V,	1.3			V
V_{HYS}	Input hysteresis	V_{LDO_3V3}=3.3V	0.165			V
V_{OL}	Output low voltage	I_{OL}=3 mA			0.36	V
I_{LEAK}	Input leakage current	Voltage on pin = V_{LDO_3V3}	–3		3	µA
I_{OL}	Max output low current	V_{OL}=0.4 V	15			mA
I_{OL}	Max output low current	V_{OL}=0.6 V	20			mA
t_f	Fall time from 0.7*V_{DD} to 0.3*V_{DD}	V_{DD} = 1.8V, 10 pF ≤ C_b ≤ 400 pF	12		80	ns
t_f	Fall time from 0.7*V_{DD} to 0.3*V_{DD}	V_{DD} = 3.3V, 10 pF ≤ C_b ≤ 400 pF	12		150	ns
t_{SP}	I2C pulse width surpressed				50	ns
C_I	pin capacitance (internal)				10	pF
C_b	Capacitive load for each bus line (external)				400	pF
SDA and SCL Standard Mode Characteristics (Slave)						
f_{SCLS}	Clock frequency for slave	V_{DD} = 1.8V or 3.3V			100	kHz
$t_{VD;DAT}$	Valid data time	Transmitting Data, V_{DD} = 1.8V or 3.3V, SCL low to SDA output valid			3.45	µs
$t_{VD;ACK}$	Valid data time of ACK condition	Transmitting Data, V_{DD} = 1.8V or 3.3V, ACK signal from SCL low to SDA (out) low			3.45	µs
SDA and SCL Fast Mode Characteristics (Slave)						
f_{SCLS}	Clock frequency for slave	V_{DD} = 1.8V or 3.3V	100		400	kHz

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Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{VD;DAT}$	Valid data time	Transmitting data, V_{DD} = 1.8V, SCL low to SDA output valid			0.9	µs
$t_{VD;ACK}$	Valid data time of ACK condition	Transmitting data, V_{DD} = 1.8V or 3.3V, ACK signal from SCL low to SDA (out) low			0.9	µs

6.16 Typical Characteristics

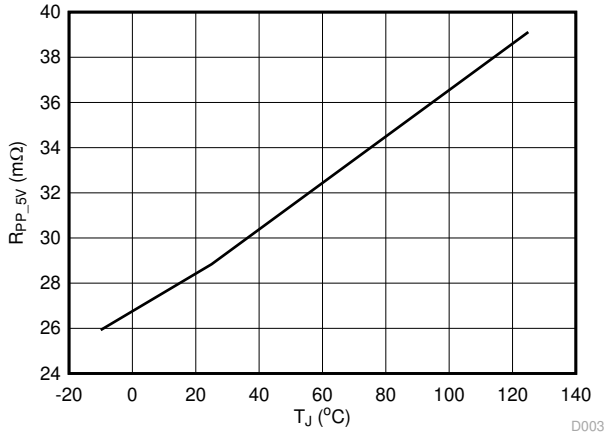

Figure 6-1. PP_5Vx Rdson vs. Temperature

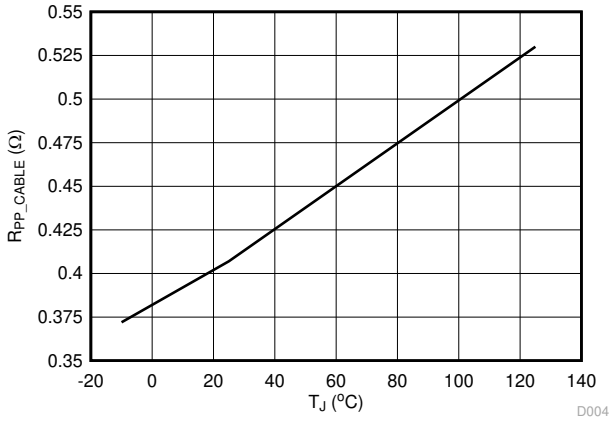

Figure 6-2. PP_CABLEx Rdson vs. Temperature

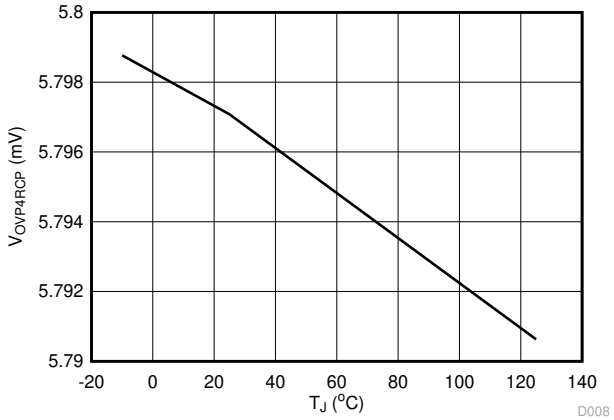

Figure 6-3. $V_{OVP4RCP}$ vs. Temperature

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7 Parameter Measurement Information

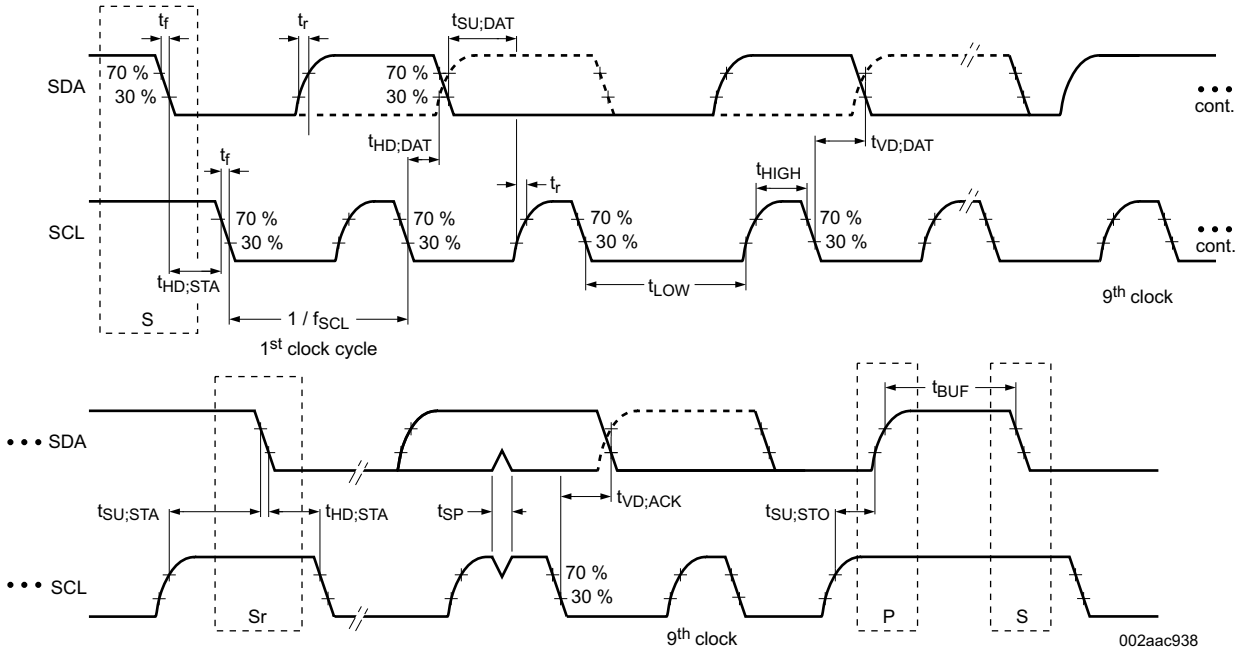

Figure 7-1. I²C Slave Interface Timing

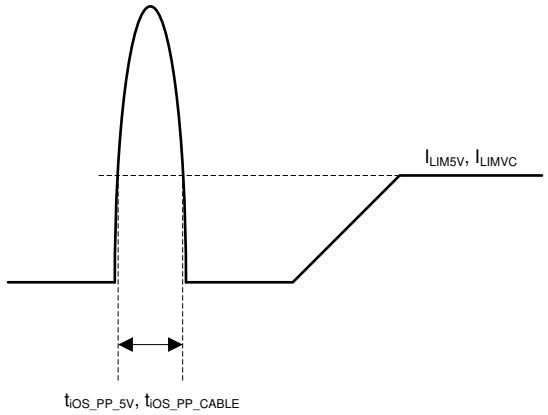

Figure 7-2. Short-Circuit Response Time for Internal Power Paths PP_5V and PP_CABLE

8 Detailed Description

8.1 Overview

The TPS25814 is a fully-integrated USB Type-C Source management device providing cable plug and orientation detection for USB Type-C receptacle. The TPS25814 may also control an attached super-speed multiplexer to simultaneously support USB data .

The TPS25814 is divided into several main sections: the cable plug and orientation detection circuitry, the port power switches, the power management circuitry and the digital core.

The cable plug and orientation detection analog circuitry automatically detects a USB Type-C cable plug insertion and also automatically detects the cable orientation. For a high-level block diagram of cable plug and orientation detection, a description of its features and more detailed circuitry, see the *Cable Plug and Orientation Detection*.

The port power switches provide power to the VBUS pin and also to the CC1 or CC2 pins based on the detected plug orientation. For a high-level block diagram of the port power switches, a description of its features and more detailed circuitry, see the *Power Paths*.

The TPS25814 has a I^2C slave port to be controlled by host processor (see the *I^2C Interface*).

The TPS25814 also integrates a thermal shutdown mechanism and runs off of accurate clocks provided by the integrated oscillator.

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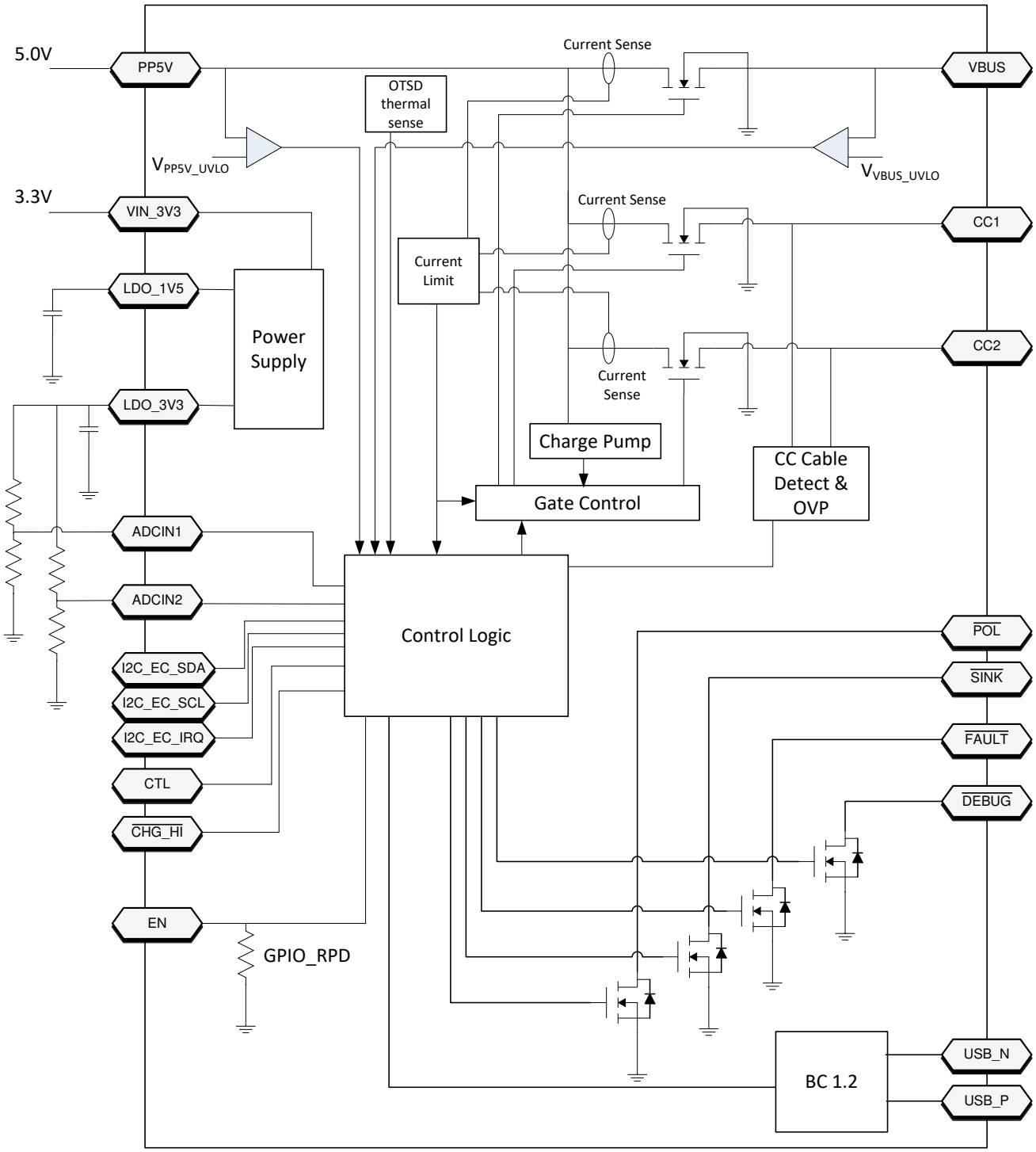
8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Power Paths

The TPS25814 has internal power paths: PP_5V and PP_CABLE. Each power path is described in detail in this section.

8.3.1.1 Internal Sourcing Power Paths

Figure 8-1 shows the TPS25814 internal sourcing power paths. The TPS25814 features two internal 5-V sourcing power paths. The path from PP5V to VBUS is called PP_5V. The path from PP5V to CCx is called PP_CABLE. Each path contains current clamping protection, overvoltage protection, UVLO protection and temperature sensing circuitry. PP_5V may conduct up to 3 A continuously, while PP_CABLE may conduct up to 315 mA continuously. When disabled, the blocking FET protects the PP5V rail from high-voltage that may appear on VBUS.

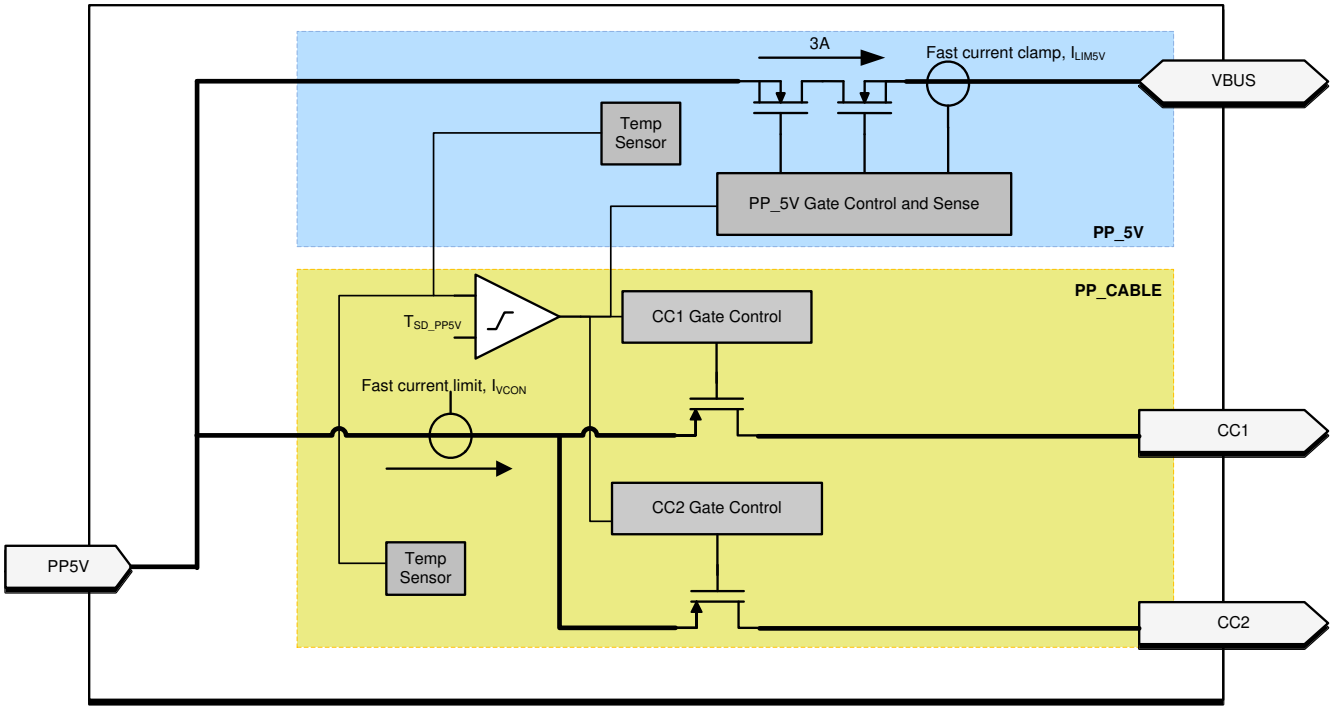


Figure 8-1. Port Power Switches

8.3.1.1.1 PP_5V Current Clamping

The current through the internal PP_5V path are current limited to I_{LIM5V}. The I_{LIM5V} value is configured by the CHG_HI pin as well as ADCIN1 and ADCIN2 pin strapping. When the current through the switch exceeds I_{LIM5V}, the current limiting circuit activates within $t_{iOS_PP_5V}$ and the path behaves as a constant current source. If the duration of the overcurrent event exceeds t_{ILIM}, the PP_5V switch is disabled.

8.3.1.1.2 PP_5V Local Overtemperature Shut Down (OTSD)

When PP_5V clamps the current, the temperature of the switch will begin to increase. When the local temperature sensors of PP_5V or PP_CABLE detect that $T_J > T_{SD_PP5V}$ the PP_5V switch is disabled and the affected port enters the USB Type-C ErrorRecovery state.

8.3.1.1.3 PP_5V OVP

When the voltage on a port's VBUS pin exceeds $V_{OVP4RCP}$ while PP_5V is enabled, then PP_5V is disabled within $t_{PP_5V_ovp}$ and the port enters into the Type-C ErrorRecovery state.

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8.3.1.1.4 PP_5V UVLO

If the PP5V pin voltage falls below its undervoltage lock out threshold (V_{PP5V_UVLO}) while PP_5V is enabled, then PP_5V is disabled within $t_{PP_5V_uvlo}$ and the port that had PP_5V enabled enters into the Type-C ErrorRecovery state.

8.3.1.1.5 PP_5Vx Reverse Current Protection

If V_{VBUS} - V_{PP5V} > $V_{PP_5V_RCP}$, then the PP_5V path is automatically disabled within $t_{PP_5V_rcp}$. If the RCP condition clears, then the PP_5V path is automatically enabled within t_{ON}.

8.3.1.1.6 PP_CABLE Current Clamp

When enabled and providing VCONN power the TPS25814 PP_CABLE power switch clamps the current to I_{VCON}. When the current through the PP_CABLE switch exceeds I_{VCON}, the current clamping circuit activates within $t_{iOS_PP_CABLE}$ and the switch behaves as a constant current source.

8.3.1.1.7 PP_CABLE Local Overtemperature Shut Down (OTSD)

When PP_CABLE clamps the current, the temperature of the switch will begin to increase. When the local temperature sensors of PP_5V or PP_CABLE detect that T_J>T_{SD_PP5V} the PP_CABLE switch is disabled and latched off within $t_{PP_CABLE_off}$. The port then enters the USB Type-C ErrorRecovery state.

8.3.1.1.8 PP_CABLE UVLO

If the PP5V pin voltage falls below its undervoltage lock out threshold (V_{PP5V_UVLO}), then the PP_CABLE switch is automatically disabled within $t_{PP_CABLE_off}$.

8.3.2 Cable Plug and Orientation Detection

Figure 8-2 shows the plug and orientation detection block at each CCy pin (CC1, CC2). Each pin has identical detection circuitry.

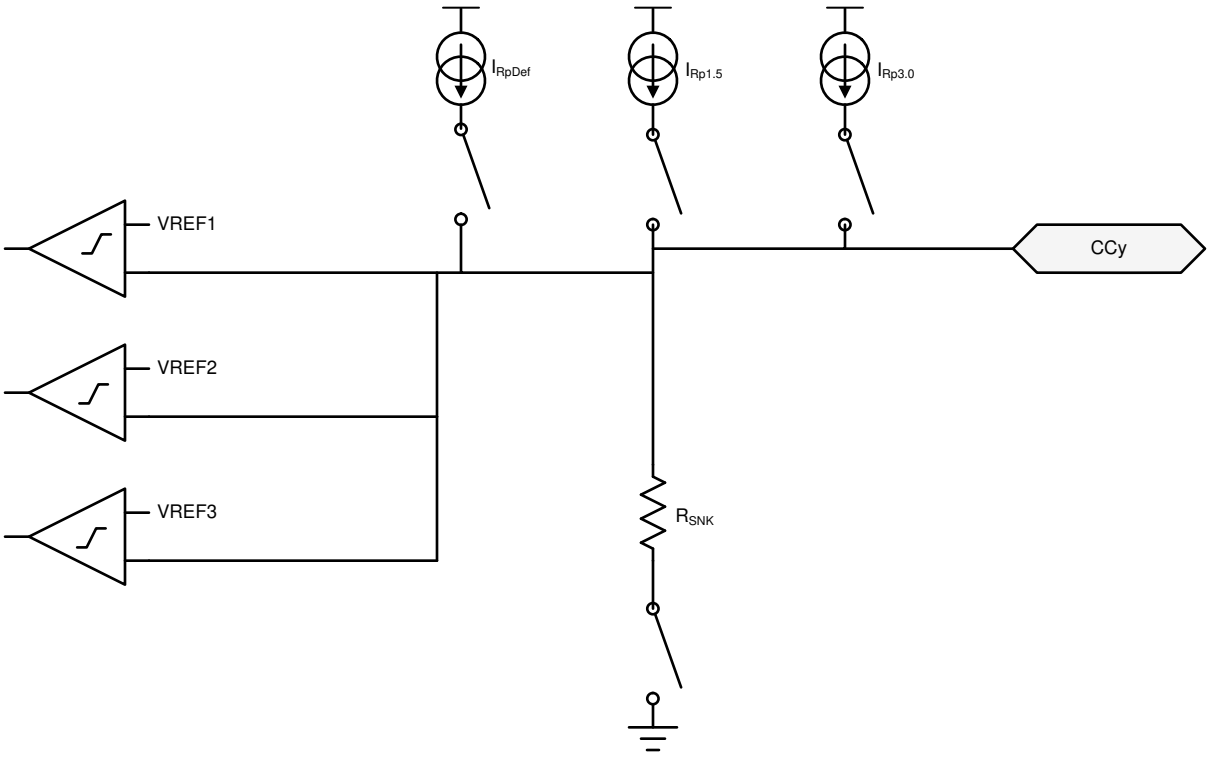

Figure 8-2. Plug and Orientation Detection Block

8.3.2.1 Configured as a Source

When configured as a source, the TPS25814 detects when a cable or a Sink is attached using the CC1 and CC2 pins. When in a disconnected state, the TPS25814 monitors the voltages on these pins to determine what, if anything, is connected. See *USB Type-C Specification* for more information.

Table 8-1 shows the Cable Detect States for a Source.

Table 8-1. Cable Detect States for a Source

CC1	CC2	CONNECTION STATE	RESULTING ACTION
Open	Open	Nothing attached	Continue monitoring both CCy pins for attach. Power is not applied to VBUS or VCONN.
Rd	Open	Sink attached	Monitor CC1 for detach. Power is applied to VBUS but not to VCONN (CC2).
Open	Rd	Sink attached	Monitor CC2 for detach. Power is applied to VBUS but not to VCONN (CC1).
Ra	Open	Powered Cable-No UFP attached	Monitor CC2 for a Sink attach and CC1 for cable detach. Power is not applied to VBUS or VCONN (CC1).
Open	Ra	Powered Cable-No UFP attached	Monitor CC1 for a Sink attach and CC2 for cable detach. Power is not applied to VBUS or VCONN (CC1).
Ra	Rd	Powered Cable-UFP Attached	Provide power on VBUS and VCONN (CC1) then monitor CC2 for a Sink detach. CC1 is not monitored for a detach.
Rd	Ra	Powered Cable-UFP attached	Provide power on VBUS and VCONN (CC2) then monitor CC1 for a Sink detach. CC2 is not monitored for a detach.
Rd	Rd	Debug Accessory Mode attached	Sense either CCy pin for detach.
Ra	Ra	Audio Adapter Accessory Mode attached	Sense either CCy pin for detach.

When a TPS25814 port is configured as a Source, a current I_{RpDef} is driven out each CCy pin and each pin is monitored for different states. When a Sink is attached to the pin a pull-down resistance of Rd to GND exists. The current I_{RpDef} is then forced across the resistance Rd generating a voltage at the CCy pin. The TPS25814 applies I_{RpDef} until it closes the switch from PP5V to VBUS, at which time it may change to $I_{Rp1.5A}$ or $I_{Rp3.0A}$.

When the CCy pin is connected to an active cable VCONN input, the pull-down resistance is different (Ra). In this case the voltage on the CCy pin will be lower and the TPS25814 recognizes it as an active cable.

The voltage on CCy is monitored to detect a disconnection depending upon which Rp current source is active. When a connection has been recognized and the voltage on CCy subsequently rises above the disconnect threshold for t_{CC}, the system registers a disconnection.

8.3.3 Overvoltage Protection (CC1, CC2)

The TPS25814 detects when the voltage on the CC1 or CC2 pin is too high or there is reverse current into the PP5V pin and takes action to protect the system. The protective action is to disable PP_CABLE within $t_{PP_CABLE_FSD}$ and disable the USB PD transmitter.

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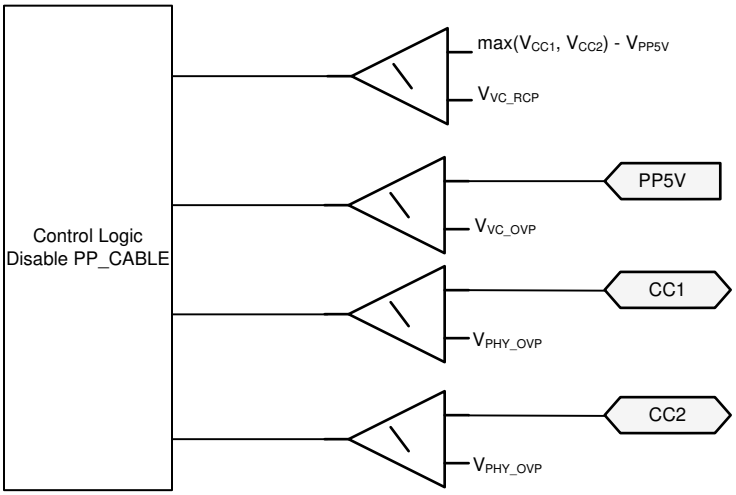

Figure 8-3. Overvoltage and Reverse Current Protection for CC1 and CC2

8.3.4 Default Behavior Configuration (ADCIN1, ADCIN2)

The ADCINx pins must be externally tied to the LDO_3V3 pin via a resistive divider as shown in the following figure. At power-up the ADC converts the ADCINx voltage and the digital core uses these two values to determine the I^{2}C slave address.

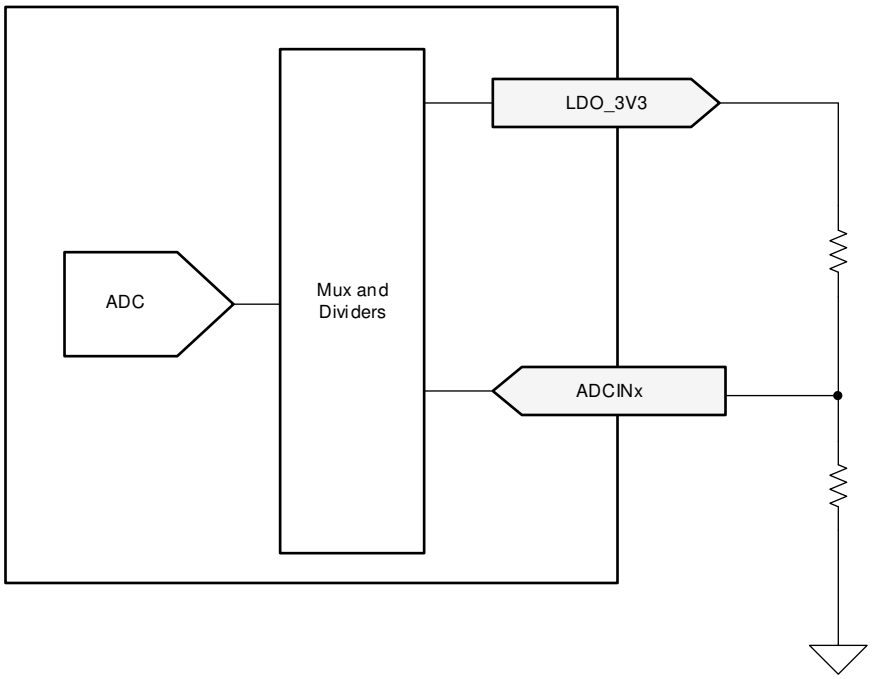

Figure 8-4. ADCINx Resistor Divider

The device behavior is determined in several ways depending upon the decoded value of the ADCIN1 and ADCIN2 pins. The following table shows the decoded values for different resistor divider ratios. See *Pin Strapping to Configure Default Behavior* for details on how the ADCINx configurations determine default device behavior. See *I^{2}C Address Setting* for details on how ADCINx decoded values affects default I^{2}C slave address.

Table 8-2. Decoding of ADCIN1 and ADCIN2 Pins

DIV = R_{DOWN} / (R_{UP} + R_{DOWN})			Without Using R_{UP} or R_{DOWN}	ADCINx Decoded Value		
MIN	Target	MAX		ADCINx[2]	ADCINx[1]	ADCINx[0]
0	0.0114	0.0228	tie to GND	0	0	0

Table 8-2. Decoding of ADCIN1 and ADCIN2 Pins (continued)

DIV = R_{DOWN} / (R_{UP} + R_{DOWN})			Without Using R_{UP} or R_{DOWN}	ADCINx Decoded Value		
MIN	Target	MAX		ADCINx[2]	ADCINx[1]	ADCINx[0]
0.0229	0.0475	0.0722	N/A	0	0	1
0.0723	0.1074	0.1425	N/A	0	1	0
0.1425	0.1899	0.2372	N/A	0	1	1
0.2373	0.3022	0.3671	N/A	1	0	0
0.3672	0.5368	0.7064	tie to LDO_1V5	1	0	1
0.7065	0.8062	0.9060	N/A	1	1	0
0.9061	0.9530	1.0	tie to LDO_3V3	1	1	1

8.3.5 BC 1.2 (USB_P, USB_N)

The TPS25814 supports BC 1.2 as a Downstream Port using the hardware shown in the following figure.

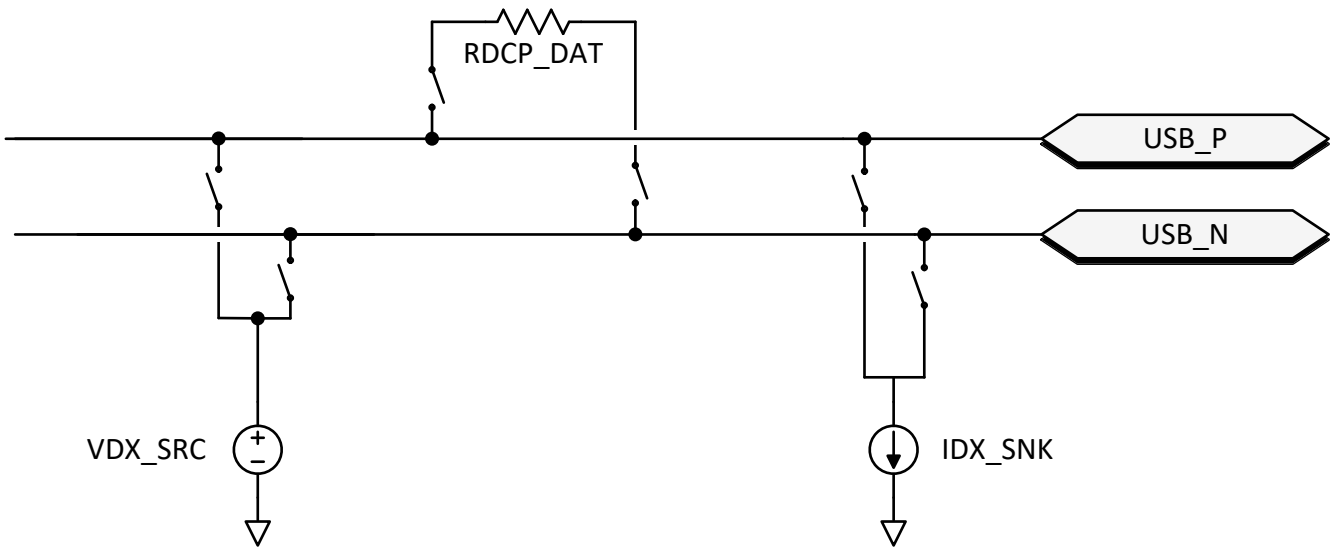

Figure 8-5. BC1.2 Hardware Components

8.3.6 Digital Interfaces

The TPS25814 contains several different digital interfaces which may be used for communicating with other devices. The available interfaces include one I^2C Slave, and additional inputs and outputs.

8.3.6.1 Fault Indicators ($\overline{FAULT}$)

When the PP_5Vx power path is clamping the current, the $\overline{FAULT}$ pin is asserted. It is de-asserted when the sink is unplugged or when the TPS25814 enters the Error Recovery state due to an OTSD event.

8.3.6.2 Sink Attachment Indicator ($\overline{SINK}$)

When the TPS25814 detects a valid sink attachment it asserts the $\overline{SINK}$ pin. The pin is de-asserted when the sink is detached or the TPS25814 enters the Error Recovery state due to an OTSD event.

8.3.6.3 Polarity Indicator ($\overline{POL}$)

When the $\overline{SINK}$ pin is asserted, the TPS25814 will also assert the $\overline{POL}$ pin if CC2 is connected to the CC wire in the plug. This pin will be de-asserted upon detachment of the sink. $\overline{POL}$ can connect to the FLIP pin of the TUSB1046 for example.

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8.3.6.4 Power Management ($\overline{\text{CHG_HI}}$)

The TPS25814 will adjust its current advertisement and its current limit when the $\overline{\text{CHG_HI}}$ pin changes state. When the $\overline{\text{CHG_HI}}$ pin is high, the TPS25814 will limit its current advertisement to the minimum current value. When the pin is low, the maximum current is advertised. The ADCIN2 pin is used to configure the minimum and maximum current (see *Pin Strapping to Configure Default Behavior*). To enable this behavior, the ADCIN1 must be set to enable SPM (see Pin Strapping to Configure Default Behavior). Note that until the $\overline{\text{SINK}}$ pin is asserted, the TPS25814 will set its Type-C current advertisement to USB default current.

Table 8-3. $\overline{\text{CHG_HI}}$ usage

ADCIN1[0]	$\overline{\text{CHG_HI}}$ pin state	Current Advertisement and Current Limit
1	Low	Maximum Current (1.5 A or 3.0 A depending on ADCIN2)
1	High	Minimum Current (USB default or 1.5 A depending on ADCIN2)
0	High or Low	Maximum Current (1.5 A or 3.0 A depending on ADCIN2)

8.3.6.5 Battery Charging Control (CTL)

The system can control the mode of the BC 1.2 charging used. The TPS25814 will implement the Dedicated Charging Port (DCP) mode or the Charging Data Port (CDP) mode.

Table 8-4. BC 1.2 Mode Control (CTL)

CTL pin state	ADCIN2[0] Decoded Value	BC 1.2 Charging Mode
Low	0 or 1	CDP
High	0	DCP
High	1	DCP Auto Mode1

8.3.6.6 Debug Accessory Detection ($\overline{\text{DEBUG}}$)

If the TPS25814 detects the attachment of a Type-C debug accessory (Rd, Rd), then it will assert the $\overline{\text{DEBUG}}$ pin low. Otherwise this pin is Hi-Z.

8.3.6.7 Disable the Port (EN)

The system may force the TPS25814 to disable the port by forcing the EN pin low. This forces the TPS25814 into the Type-C Error Recovery state. Note that the TPS25814 has an internal pull-down on this pin (GPIO_RPD).

8.3.6.8 I^2C Interface

The TPS25814 features an I^2C interface that each use an I^2C I/O driver like the one shown in Figure 8-6. This I/O consists of an open-drain output and in input comparator with de-glitching.

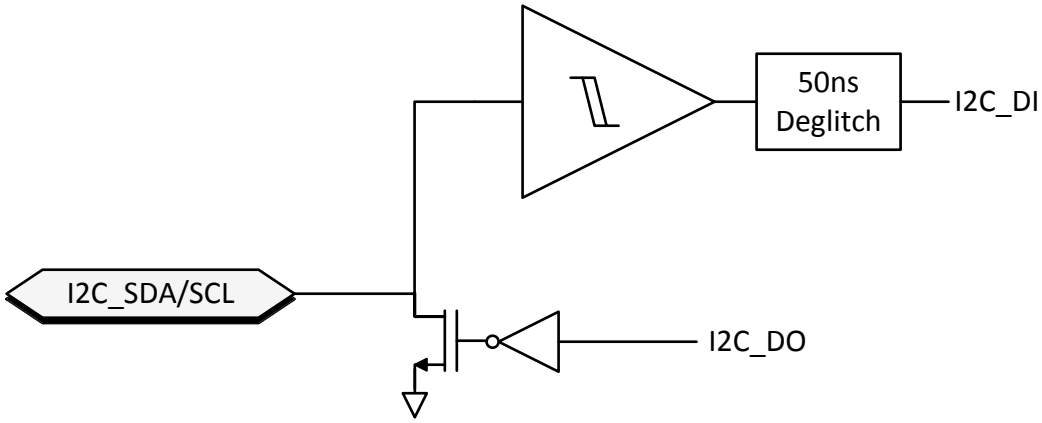

Figure 8-6. I^2C Buffer

8.3.7 I²C Interface

The TPS25814 has an I²C slave interface port: I2C_EC . I²C port I2C_EC is comprised of the I2C_EC_SDA, I2C_EC_SCL, and $\overline{\text{I2C_EC_IRQ}}$ pins. These interfaces provide general status information about the TPS25814, as well as the ability to control the TPS25814 behavior, and providing information about connections detected at the USB-C receptacle.

Table 8-5. I²C Summary

I2C Bus	Type	Typical Usage
I2C_EC	Slave	Connect to an Embedded Controller (EC).

8.3.7.1 I²C Interface Description

The TPS25814 supports Standard and Fast mode I²C interfaces. The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a supply through a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

A master sending a Start condition, a high-to-low transition on the SDA input and output, while the SCL input is high initiates I²C communication. After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/W).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period as changes in the data line at this time are interpreted as control commands (Start or Stop). The master sends a Stop condition, a low-to-high transition on the SDA input and output while the SCL input is high.

Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period. When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. The master receiver holding the SDA line high does this. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.

Figure 8-7 shows the start and stop conditions of the transfer. Figure 8-8 shows the SDA and SCL signals for transferring a bit. Figure 8-9 shows a data transfer sequence with the ACK or NACK at the last clock pulse.

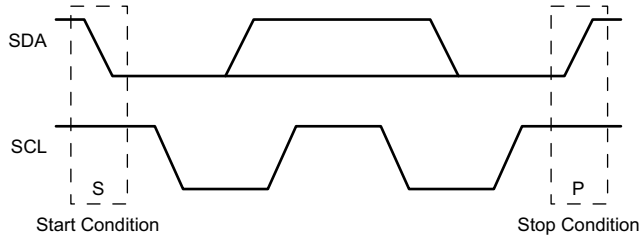

Figure 8-7. I²C Definition of Start and Stop Conditions

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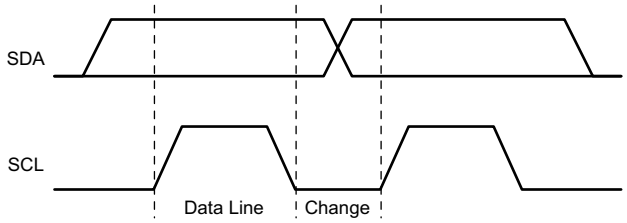

Figure 8-8. I²C Bit Transfer

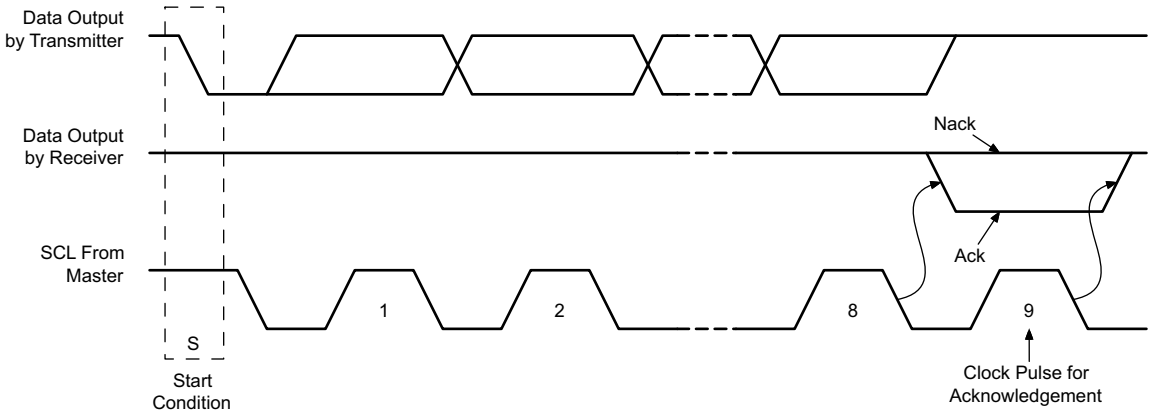

Figure 8-9. I²C Acknowledgment

8.3.7.2 I²C Clock Stretching

The TPS25814 features clock stretching for the I²C protocol. The TPS25814 slave I²C port may hold the clock line (SCL) low after receiving (or sending) a byte, indicating that it is not yet ready to process more data. The master communicating with the slave must not finish the transmission of the current bit and must wait until the clock line actually goes high. When the slave is clock stretching, the clock line remains low.

The master must wait until it observes the clock line transitioning high plus an additional minimum time (4 µs for standard 100-kbps I²C) before pulling the clock low again.

Any clock pulse may be stretched but typically it is the interval before or after the acknowledgment bit.

8.3.7.3 I²C Address Setting

The host should only use I2C_EC_SCL/SDA for loading a patch bundle. Once the boot process is complete, each port has a unique slave address on the I2C_EC_SCL/SDA bus as selected by the ADCINx pins.

Table 8-6. I²C Default Slave Address for I2C_EC_SCL/SDA.

ADCIN1 Decoding		Slave Address							
ADCIN1[1]	ADCIN1[0]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	1	0	0	0	0	0	R/W
0	1	0	1	0	0	0	0	1	R/W
1	0	0	1	0	0	0	1	0	R/W
1	1	0	1	0	0	0	1	1	R/W

8.3.7.4 Unique Address Interface

The Unique Address Interface allows for complex interaction between an I²C master and a single TPS25814. The I²C Slave sub-address is used to receive or respond to Host Interface protocol commands. Figure 8-10 and Figure 8-11 show the write and read protocol for the I²C slave interface, and a key is included in Figure 8-12 to explain the terminology used. The key to the protocol diagrams is in the SMBus Specification and is repeated here in part.

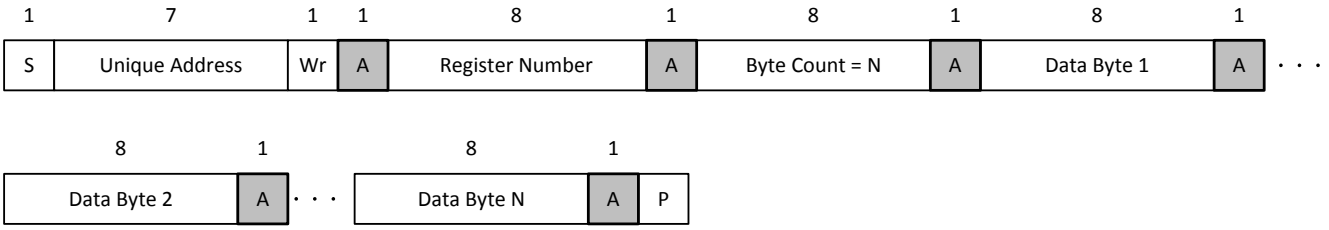

Figure 8-10. I²C Unique Address Write Register Protocol

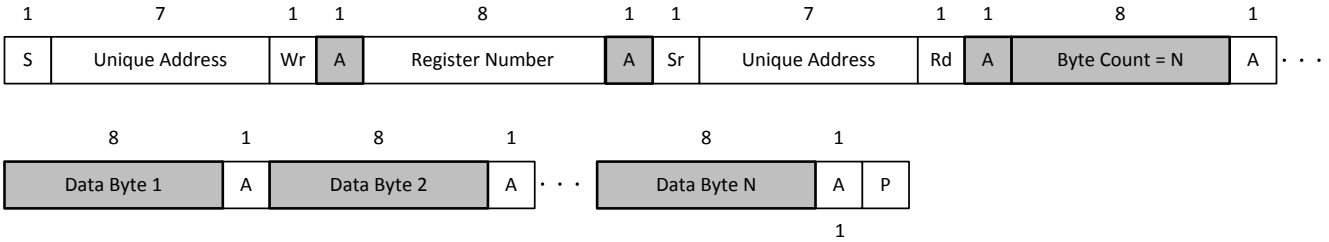

Figure 8-11. I²C Unique Address Read Register Protocol

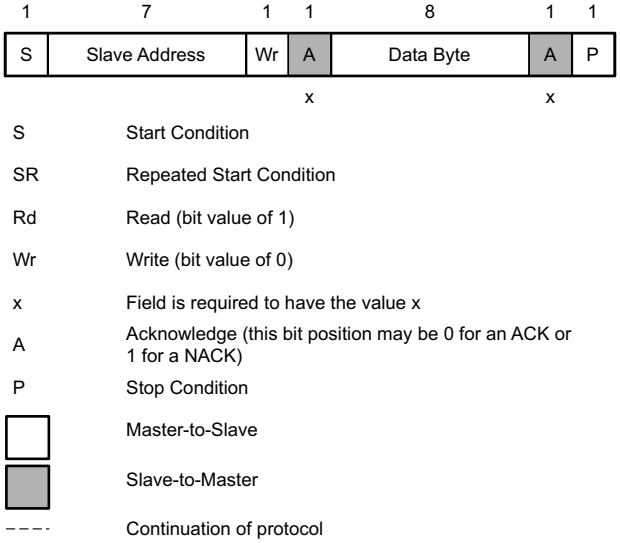

Figure 8-12. I²C Read/Write Protocol Key

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8.4 Device Functional Modes

8.4.1 Pin Strapping to Configure Default Behavior

During the boot procedure, the device will read the ADCINx pins and set the configurations based on the table below.

Table 8-7. Device Configuration using ADCIN1

ADCIN1 Decoded Value (1)			I²C Address Index (2)	SPM Enabled
ADCIN1[2]	ADCIN1[1]	ADCIN1[0]		
0	0	0	#1	no
0	0	1	#2	
0	1	0	#3	
0	1	1	#4	
1	0	0	#1	yes
1	0	1	#2	
1	1	0	#3	
1	1	1	#4	

(1) See Table 8-6 to see the exact meaning of I²C Address Index.
(2) See Table 8-2 for how to configure a given ADCINx decoded value.

Table 8-8. Device Configuration using ADCIN2

ADCIN2 Decoded Value (1)			Minimum Current(2)	Maximum Current	DCP Mode
ADCIN2[2]	ADCIN2[1]	ADCIN2[0]			
0	0	0	USB Default	1.5A	DCP
0	0	1			DCP Auto Mode 1
0	1	0		3A	DCP
0	1	1			DCP Auto Mode 1
1	0	0	1.5A	1.5A	DCP
1	0	1			DCP Auto Mode 1
1	1	0		3A	DCP
1	1	1			DCP Auto Mode 1

(1) See Table 8-2 for how to configure a given ADCINx decoded value.
(2) Requires SPM to be enabled via ADCIN1.

8.4.2 Power States

The TPS25814 may operate in one of three different power states: Active, Idle, or Sleep. The Modern Standby mode is a special case of the Idle mode. The functionality available in each state is summarized in the following table. The device will automatically transition between the three power states based on the circuits that are active and required, see the following figure. In the Sleep State the TPS25814 will detect a Type-C connection. Transitioning between the Active mode to the Idle mode requires a period of time (T) without any of the following activity:

- Change in CC status.
- GPIO input event.
- I²C transactions.
- Voltage alert.
- Fault alert.

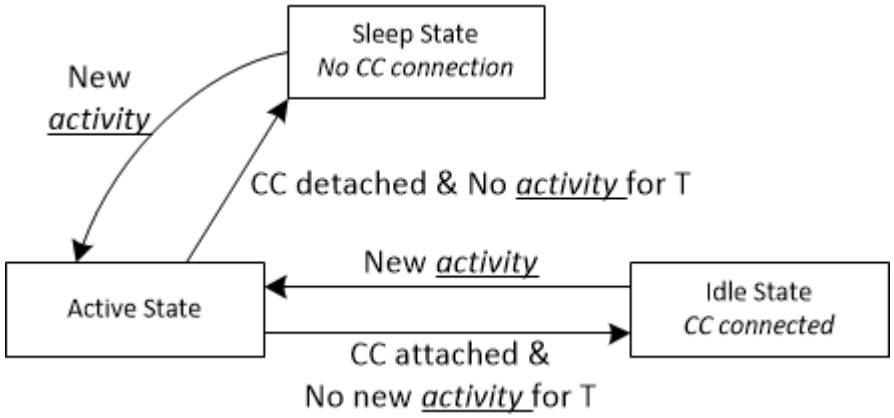

Figure 8-13. Flow Diagram For Power States

Table 8-9. Power Consumption States.

	Active Source Mode(1)	Idle Source Mode(2)	Modern Standby Source Mode(4)	Sleep Mode(3)
PP_5V	enabled	enabled	enabled	disabled
PP_CABLE	enabled	enabled	disabled	disabled
external CC1 termination	Rd	Rd	Rd	open
external CC2 termination	open	open	open	open

(1) This mode is used for: $I_{VIN_3V3,ActSrc}$
(2) This mode is used for: $I_{VIN_3V3,IdlSrc}$
(3) This mode is used for: $I_{VIN_3V3,SleepSrc}$
(4) This mode is used for: $P_{MstbySrc}$

8.4.3 Schottky for Current Surge Protection

To prevent the possibility of large ground currents into the TPS25814 during sudden disconnects due to inductive effects in a cable, it is recommended that a Schottky diode be placed from VBUS to ground as shown in Figure 8-14.

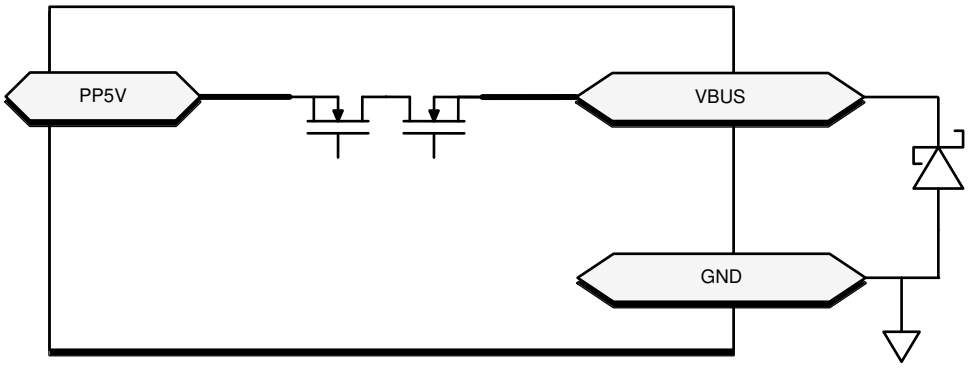

Figure 8-14. Schottky for Current Surge Protection

8.4.4 Thermal Shutdown

The TPS25814 features a central thermal shutdown as well as independent thermal sensors for each internal power path. The central thermal shutdown monitors the overall temperature of the die and disables all functions except for supervisory circuitry when die temperature goes above a rising temperature of T_{SD_MAIN}. The temperature shutdown has a hysteresis of T_{SDH_MAIN} and when the temperature falls back below this value, the device resumes normal operation.

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The power path thermal shutdown monitors the temperature of each internal PP5V-to-VBUS power path and disables both power paths and the VCONN power path when either exceeds T_{SD_PP5V}. Once the temperature falls by at least T_{SDH_PP5V} the path can be configured to resume operation or remain disabled until re-enabled by firmware.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS25814 is a Type-C DFP controller that supports all Type-C DFP required functions. The TPS25814 Only applies power to VBUS when it detects that a UFP is attached and removes power when it detects the UFP is detached. The device exposes its identity via its CC pin advertising its current capability based on the CHG_HI pin settings. The TPS25814 also limits its advertised current internally and provides robust protection to a fault on the system VBUS power rail.

After a connection is established by the TPS25814, the device is capable of providing VCONN to power circuits in the cable plug on the CC pin that is not connected to the CC wire in the cable. VCONN is internally current limited and is supplied by PP5V.

The TPS25814 is also capable of supporting BC 1.2 compliant charging schemes of a Charging Data Port (CDP) and a Dedicated Charging Port (DCP). The CTL pin changes which charging modes are activated to the connected portable device.

The following design procedure can be used to implement a full featured Type-C DFP.

9.2 Typical Application

9.2.1 Type C DFP Port Implementation with Embedded Controller

Figure 9-1 shows a Type-C DFP implementation where the TPS25814 is connected to an embedded controller. The embedded controller will have the ability to communicate with the TPS25814 via I^2C, as well as change the charge current advertisement and BC 1.2 charging scheme.

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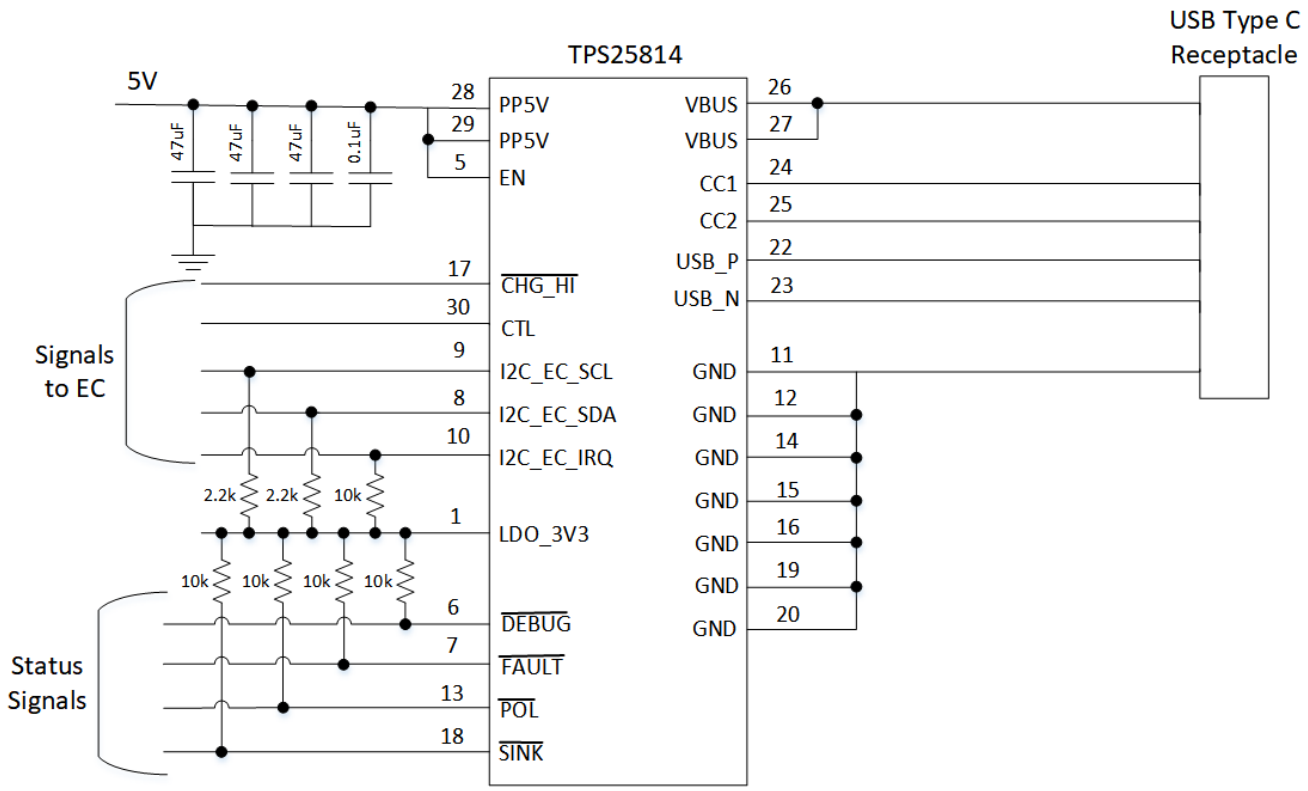

Figure 9-1. Type C DFP Port Implementation

9.2.1.1 Detailed Design Procedure

9.2.1.1.1 Type-C Connector VBUS Capacitors

The first level of protection starts at the Type-C connector and the VBUS pin capacitors. These capacitors help filter out high frequency noise but can also help absorb short voltage transients. Each VBUS pin should have a 10-nF capacitor rated at or above 25 V and placed as close to the pin as possible. The GND pin on the capacitors should have very short path to GND on the connector. The derating factor of ceramic capacitors should be taken into account as they can lose more than 50% of their effective capacitance when biased. Adding the VBUS capacitors can help reduce voltage spikes by 2 V to 3 V.

9.2.1.1.2 VBUS Schottky and TVS Diodes

Schottky diodes are used on VBUS to help absorb large GND currents when a Type-C cable is removed while drawing high current. The inductance in the cable will continue to draw current on VBUS until the energy stored is dissipated. Higher currents could cause the body diodes on IC devices connected to VBUS to conduct. When the current is high enough it could damage the body diodes of IC devices. Ideally, a VBUS Schottky diode should have a lower forward voltage so it can turn on before any other body diodes on other IC devices. Schottky diodes on VBUS also help during hard shorts to GND which can occur with a faulty Type-C cable or damaged Type-C PD device. VBUS could ring below GND which could damage devices hanging off of VBUS. The Schottky diode will start to conduct once VBUS goes below the forward voltage. When the TPS25814 is the only device connected to VBUS, place the Schottky Diode close to the VBUS pin of the TPS25814.

TVS Diodes help suppress and clamp transient voltages. Most TVS diodes can fully clamp around 10 ns and can keep the VBUS at their clamping voltage for a period of time. Looking at the clamping voltage of TVS diodes after they settle during a transient will help decide which TVS diode to use. The peak power rating of a TVS diode must be able to handle the worst case conditions in the system.

9.2.1.1.3 VBUS Snubber Circuit

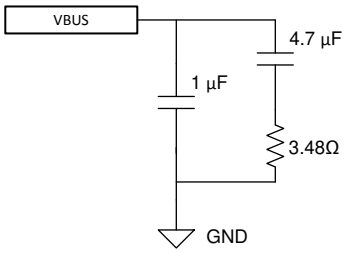

Figure 9-2. VBUS Snubber

Another method of clamping the USB Type-C VBUS is to use a VBUS RC Snubber. An RC Snubber is smaller than a TVS diode, and typically more cost effective as well. An RC Snubber works by modifying the characteristic of the total RLC response in the USB Type-C cable hot-plug from being under-damped to critically-damped or over-damped. So rather than clamping the overvoltage directly, it changes the hot-plug response from under-damped to critically-damped, so the voltage on VBUS does not ring at all; so the voltage is limited, but without requiring a clamping element like a TVS diode.

However, the USB Type-C and Power Delivery specifications limit the range of capacitance that can be used on VBUS for the RC snubber. VBUS capacitance must have a minimum 1 µF and a maximum of 10 µF. The RC snubber values chosen support up to 4 m USB Type-C cable (maximum length allowed in the USB Type-C specification) being hot plugged, is to use 4.7-µF capacitor in series with a 3.48-Ω resistor. In parallel with the RC Snubber a 1-µF capacitor is used, which always ensures the minimum USB Type-C VBUS capacitance specification is met. This circuit is shown in Figure 9-2.

9.2.1.2 Application Curves

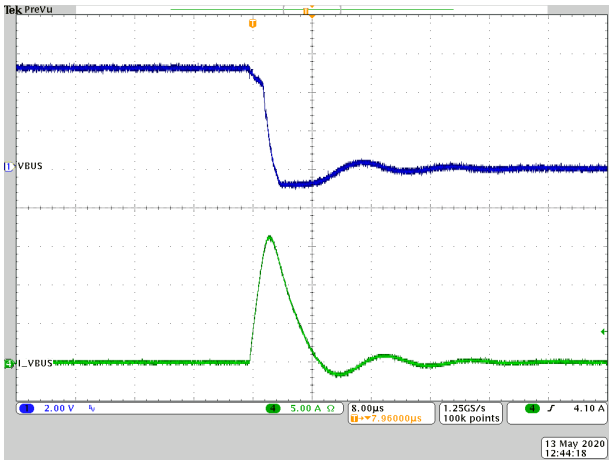

Figure 9-3. VBUS Short to Ground (Zoomed In)

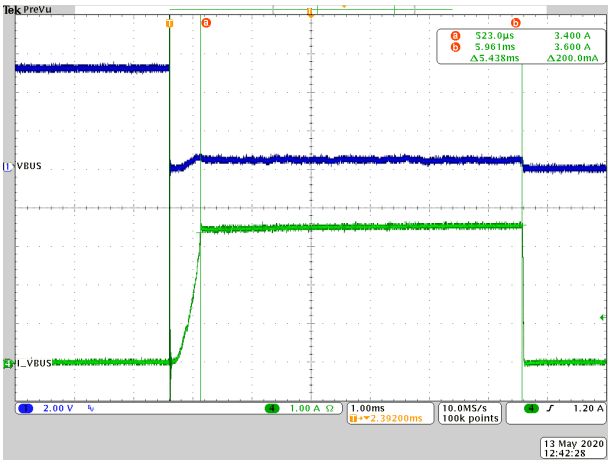

Figure 9-4. VBUS Short to Ground (Zoomed Out)

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10 Power Supply Recommendations

10.1 3.3-V Power

10.1.1 VIN_3V3 Input Switch

The VIN_3V3 input is the main supply of the TPS25814 device. The VIN_3V3 switch is a uni-directional switch from VIN_3V3 to LDO_3V3, not allowing current to flow backwards from LDO_3V3 to VIN_3V3. This switch is on when the 3.3 V supply is available. The recommended capacitance C_{VIN_3V3} (see the Recommended Capacitance in the *Specifications* section) should be connected from the VIN_3V3 pin to the GND pin).

10.2 1.5-V Power

The internal circuitry is powered from 1.5 V. The 1.5-V LDO steps the voltage down from LDO_3V3 to 1.5 V. The 1.5-V LDO provides power to all internal low-voltage digital circuits which includes the digital core, and memory. The 1.5-V LDO also provides power to all internal low-voltage analog circuits. Connect the recommended capacitance C_{LDO_1V5} (see the Recommended Capacitance in the *Specifications* section) from the LDO_1V5 pin to the GND pin.

10.3 Recommended Supply Load Capacitance

The Recommended Capacitance in the *Specifications* section lists the recommended board capacitances for the various supplies. The typical capacitance is the nominally rated capacitance that must be placed on the board as close to the pin as possible. The maximum capacitance must not be exceeded on pins for which it is specified. The minimum capacitance is minimum capacitance allowing for tolerances and voltage derating ensuring proper operation.

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11 Layout

11.1 Layout Guidelines

Proper routing and placement will maintain signal integrity for high speed signals and improve the heat dissipation from the TPS25814 power path. The combination of power and high speed data signals are easily routed if the following guidelines are followed. It is a best practice to consult with board manufacturing to verify manufacturing capabilities.

11.1.1 Top TPS25814 Placement and Bottom Component Placement and Layout

When the TPS25814 is placed on top and its components on bottom the solution size will be at its smallest.

11.2 Layout Example

Follow the differential impedances for Super / High Speed signals defined by their specifications (DisplayPort - AUXN/P and USB2.0). All I/O will be fanned out to provide an example for routing out all pins, not all designs will utilize all of the I/O on the TPS25814.

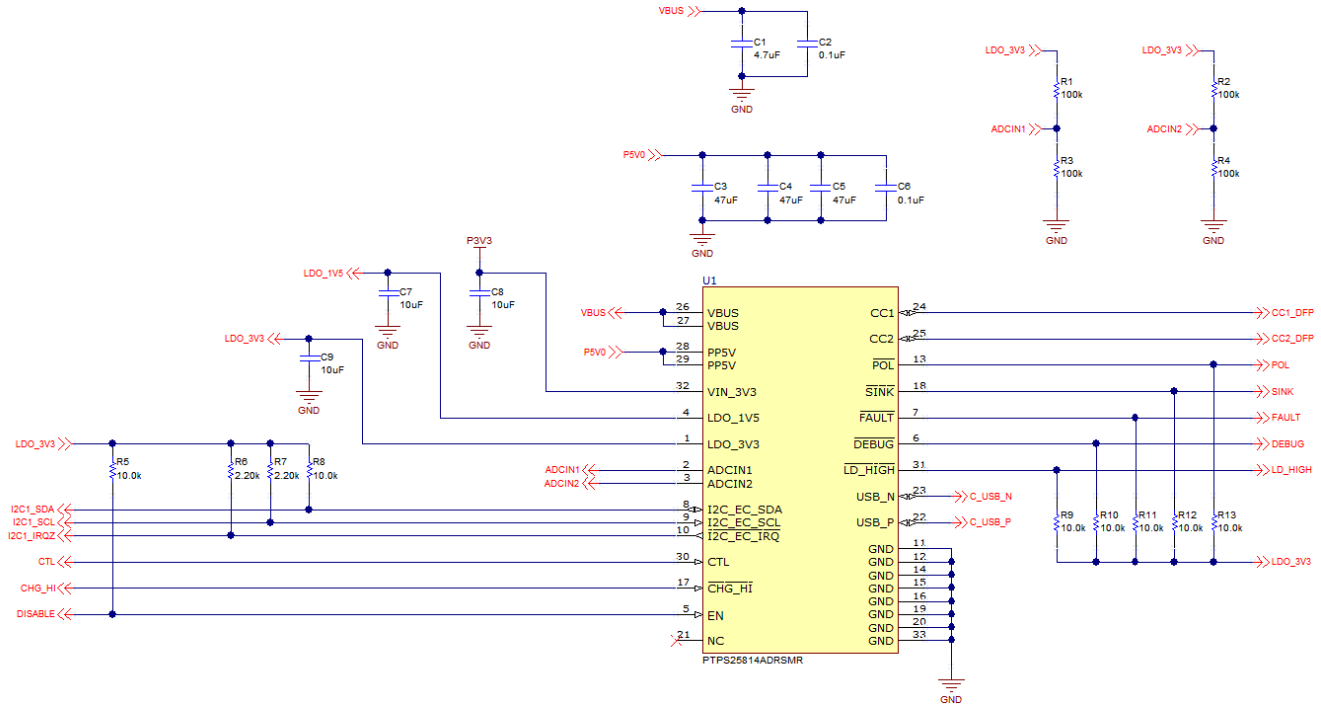

Figure 11-1. Example Schematic

11.3 Component Placement

Top and bottom placement is used for this example to minimize solution size. The TPS25814 is placed on the top side of the board and the majority of its components are placed on the bottom side. When placing the components on the bottom side, it is recommended that they are placed directly under the TPS25814. When placing the VBUS and PPHV capacitors it is easiest to place them with the GND terminal of the capacitors to face outward from the TPS25814 or to the side since the drain connection pads on the bottom layer should not be connected to anything and left floating. All other components that are for pins on the GND pad side of the TPS25814 should be placed where the GND terminal is underneath the GND pad.

The CC capacitors should be placed on the same side as the TPS25814 close to the respective CC1 and CC2 pins. Do NOT via to another layer in between the CC pins to the CC capacitor, placing a via after the CC capacitor is recommended.

The ADCIN1/2 voltage divider resistors can be placed where convenient.

The figures below show the placement in 2-D and 3-D.

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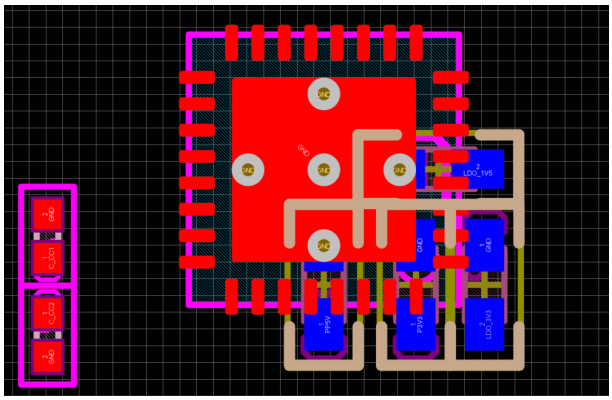

Figure 11-2. Top View Layout

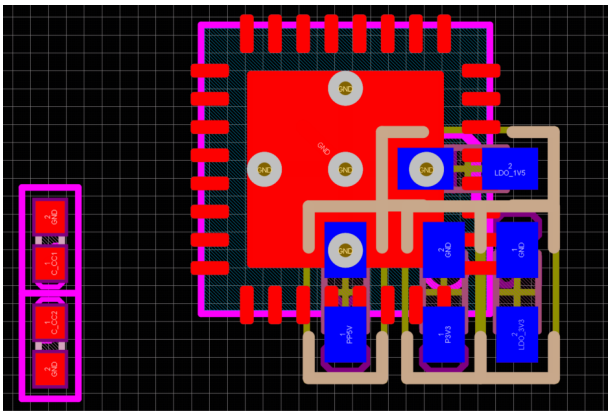

Figure 11-3. Bottom View Layout

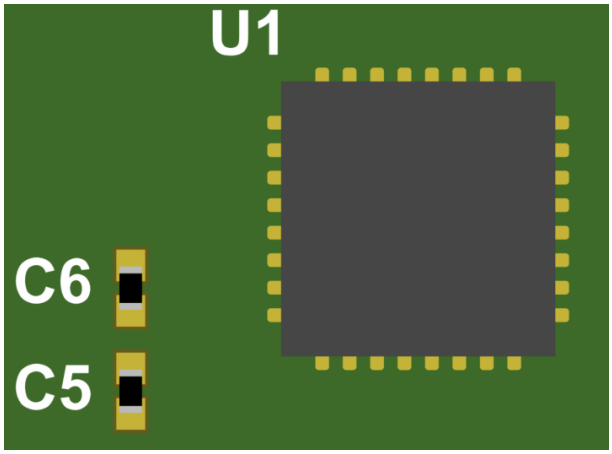

Figure 11-4. Top View 3-D

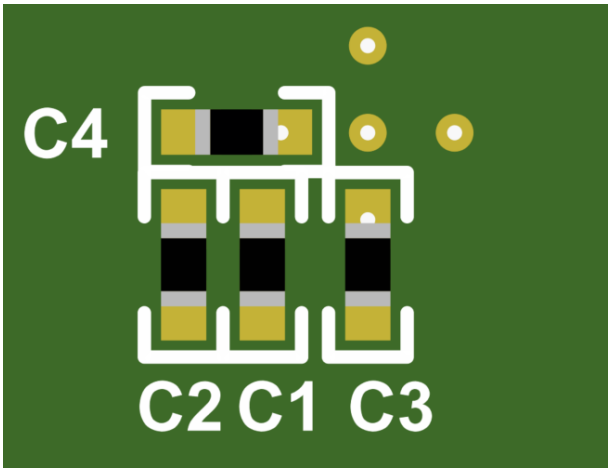

Figure 11-5. Bottom View 3-D

11.4 Routing and View Placement

On the top side, create pours for PP5V and VBUS. Connect PP5V and VBUS from the top layer to the bottom layer using at least 6, 8-mil hole and 16-mil diameter vias. See Figure 11-6 for the recommended via sizing. The via placement and copper pours are highlighted in Figure 11-7.

Figure 11-6. Recommended Minimum Via Sizing

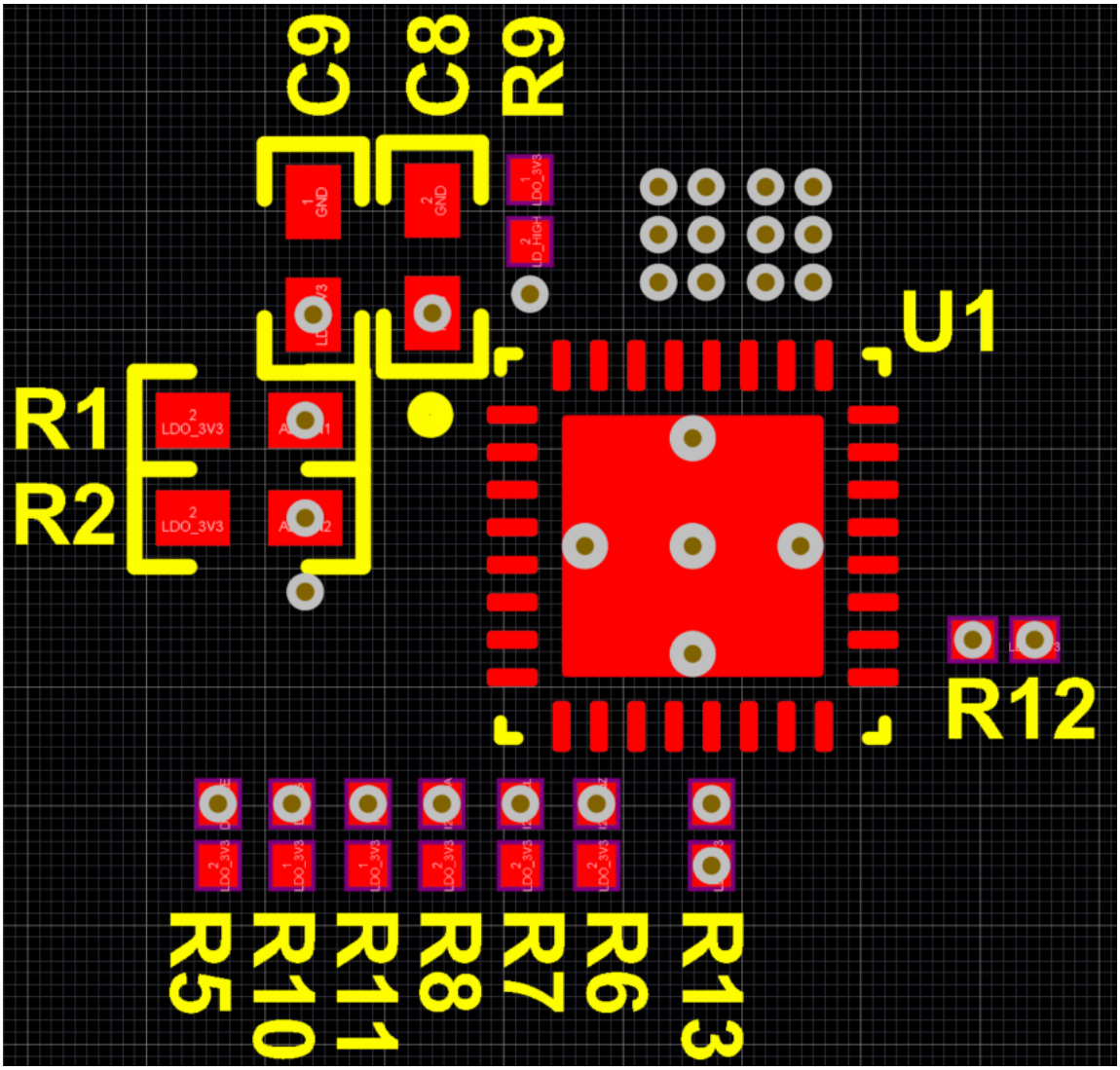

Figure 11-7. Via Placement - Top Layer

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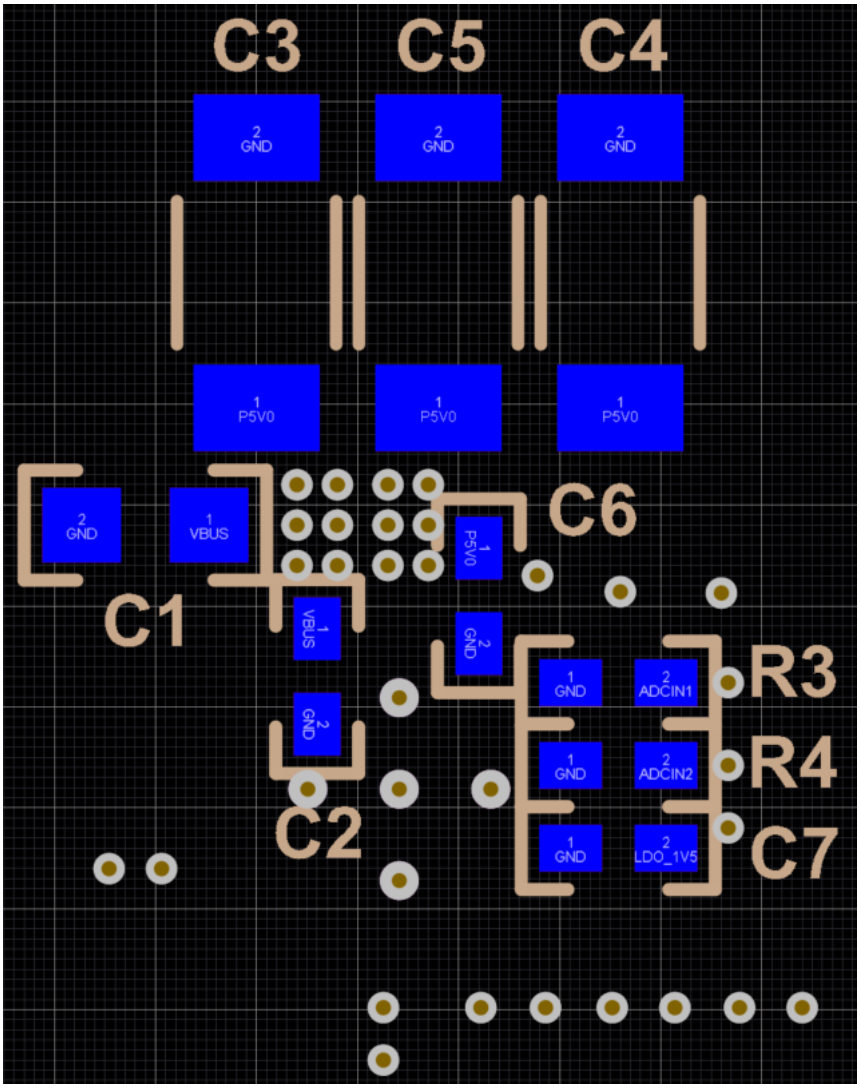

Figure 11-8. Via Placement - Bottom Layer

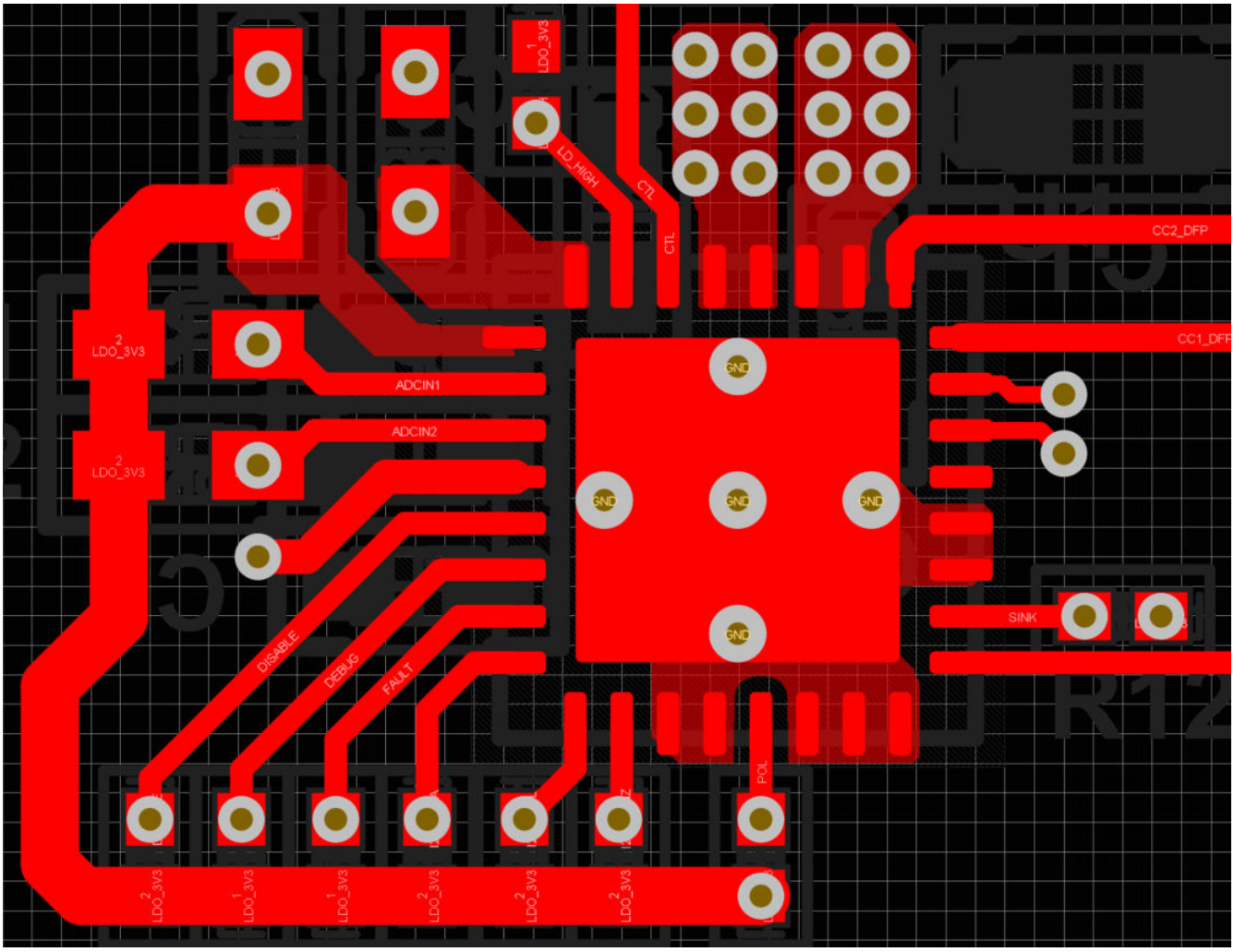

Figure 11-9. Routing - Top Layer

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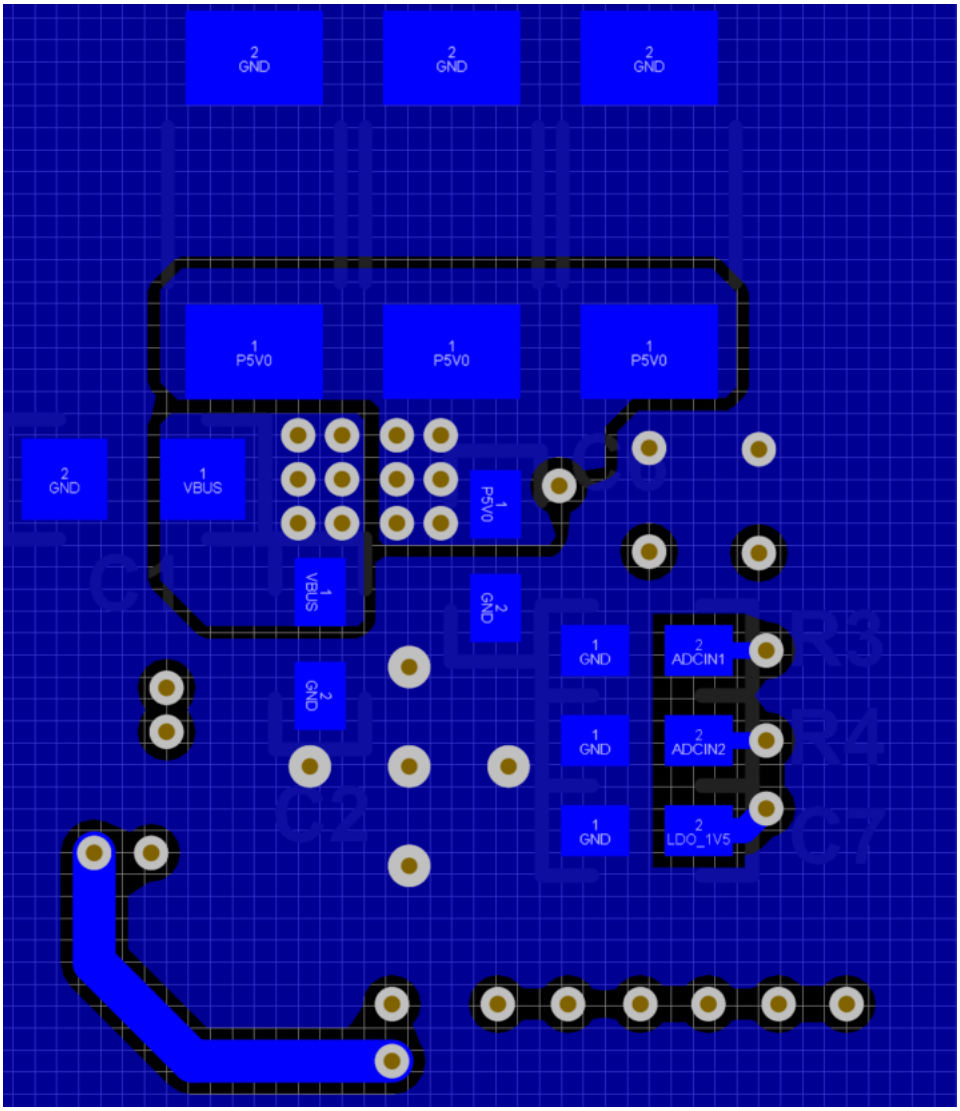

Figure 11-10. Routing - Bottom Layer

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Documentation Support

12.2.1 Related Documentation

- *USB-PD Specifications*
- *USB Power Delivery Specification*

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS25814RSMR	Active	Production	VQFN (RSM) | 32	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	25814
TPS25814RSMR.A	Active	Production	VQFN (RSM) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	25814
TPS25814RSMR.B	Active	Production	VQFN (RSM) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	25814

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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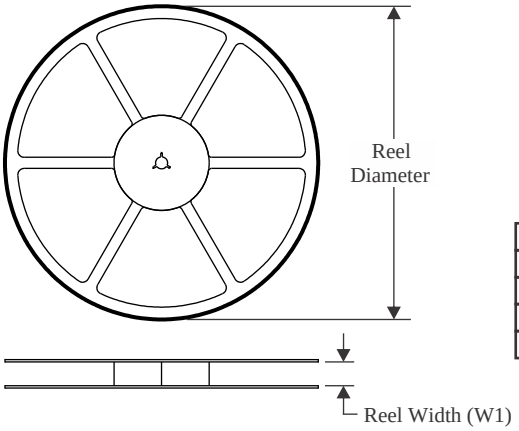
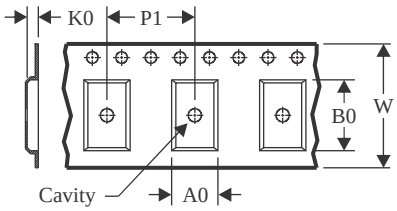
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

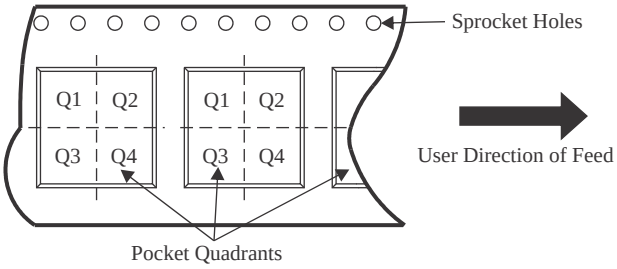


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

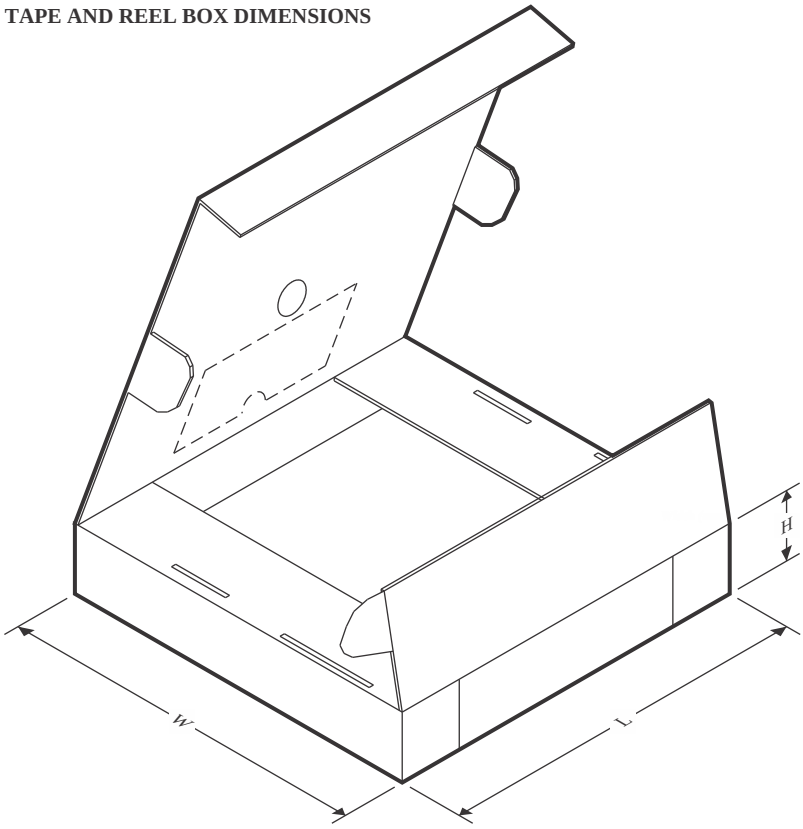
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS25814RSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS25814RSMR	VQFN	RSM	32	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

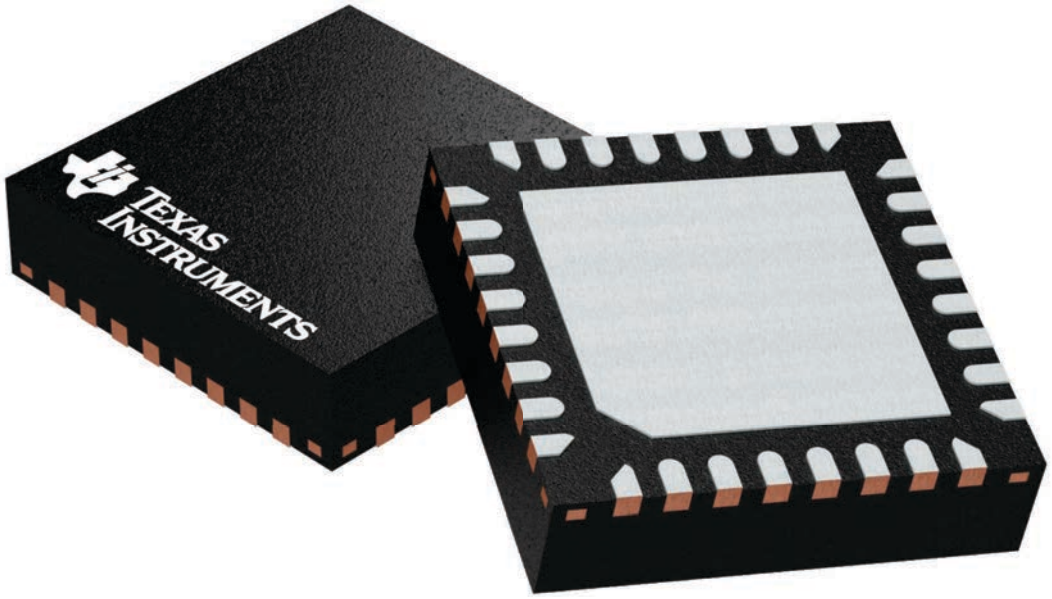
RSM 32

VQFN - 1 mm max height

4 x 4, 0.4 mm pitch

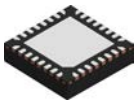
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224982/A

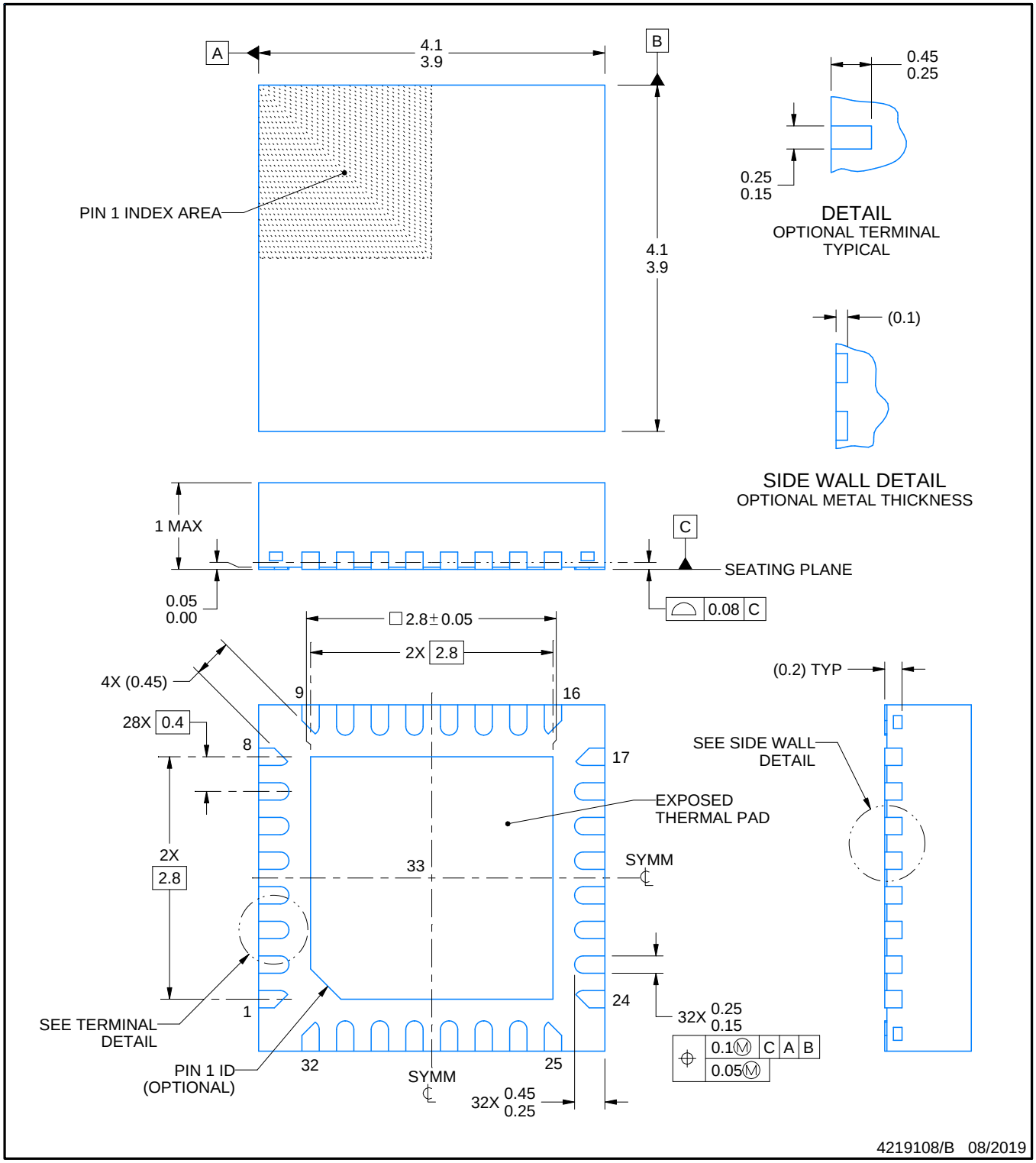
RSM0032B



PACKAGE OUTLINE

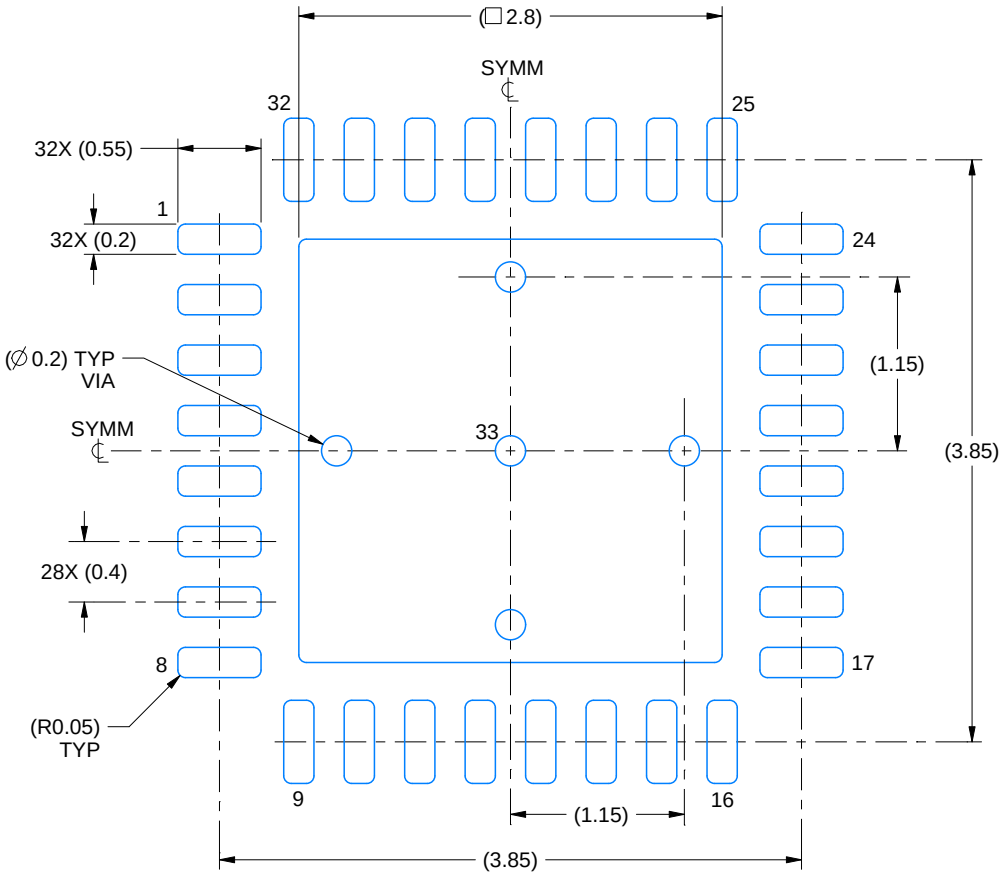
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

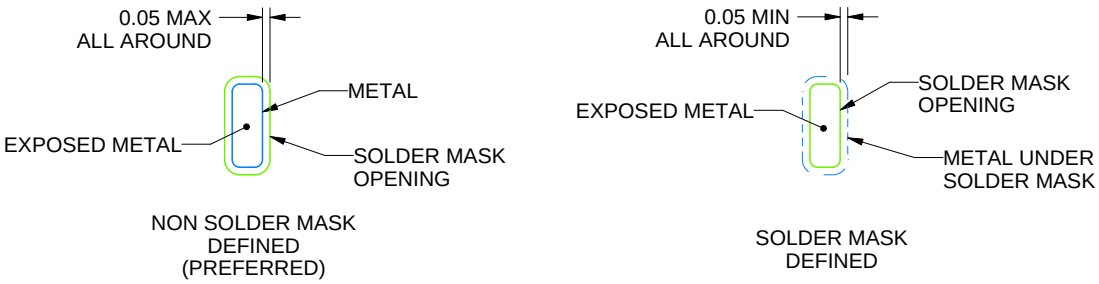


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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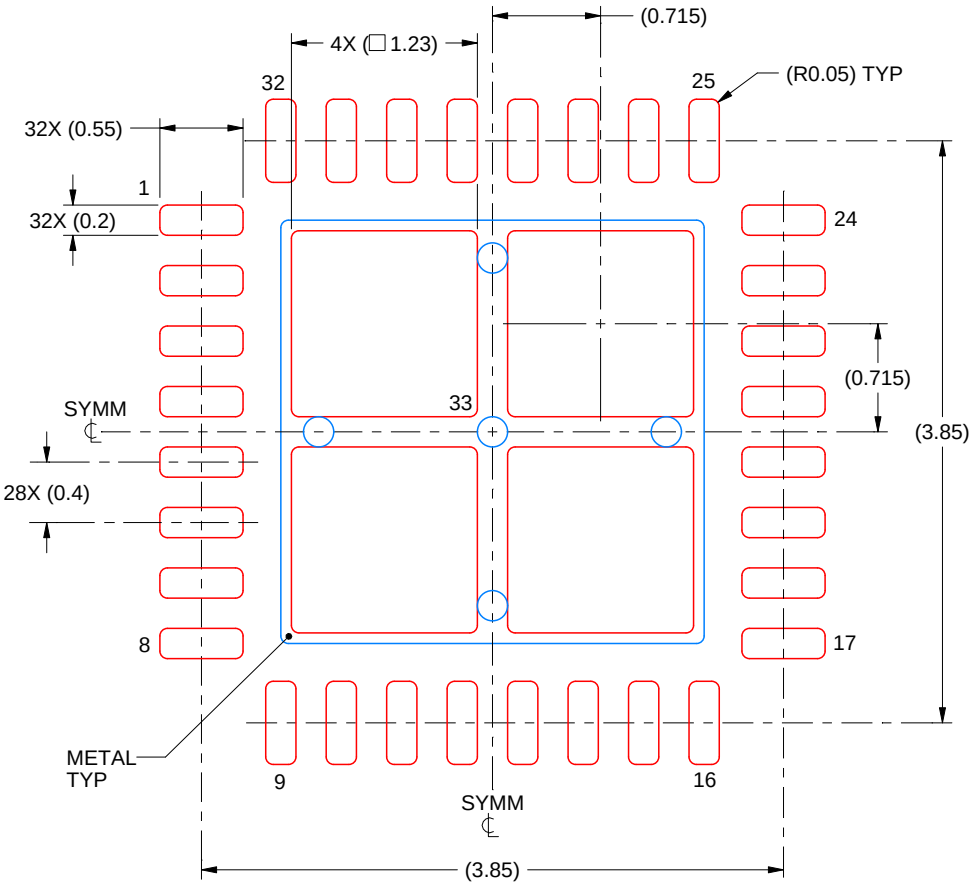
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 33:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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