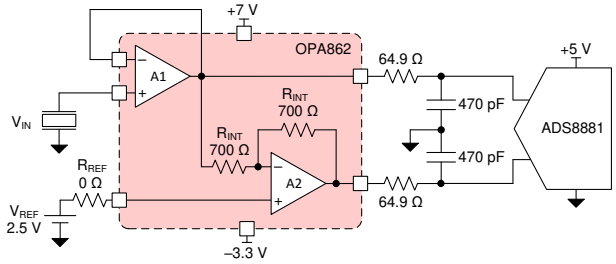
# OPA862 High Input Impedance, Single-Ended to Differential ADC Driver

## 1 Features

- Wide Supply Range: 3 V to 12.6 V
- High Input Impedance: 325 MΩ
- Voltage Noise:
  - Input-Referred (f ≥ 5 kHz): 2.3 nV/√ Hz
  - Output-Referred (f ≥ 10 kHz): 8.3 nV/√ Hz
- Differential Output Offset: ±700 µV (Maximum)
- Output Offset Drift: ±1.5 µV/°C (Typical)
- A2 Bias Current Cancellation, $I_B$: ±5 nA (Typical)
- Gain-Bandwidth Product: 400 MHz
- Small-Signal Bandwidth: 44 MHz (G = 2 V/V)
- Slew Rate: 140 V/µs
- HD2, HD3 ($V_{OD}$ = 10 $V_{PP}$, 50 kHz): –122 dBc, –140 dBc
- Rail-to-Rail Output:
  - High Linear Output Current: 60 mA (Typical)
- Quiescent Current: 3.1 mA
- Disable mode: 12-µA Quiescent Current
- Extended Temperature Operation: –40°C to +125°C

## 2 Applications

- 16-bit and 18-bit ADC Drivers
- Memory and LCD Testers
- Data Acquisition (DAQ)
- Test and Measurement
- Transimpedance Amplifiers (TIA)
- Class-D audio Amplifier Drivers
- Piezoelectric Sensor Interface
- Medical Instrumentation




**Single-Ended High-Input Impedance Sensor Interface**

## 3 Description

The OPA862 is a single-ended to differential analog-to-digital converter (ADC) driver with high input impedance for directly interfacing with sensors. The device only consumes 3.1-mA quiescent current for an output-referred noise density of 8.3 nV/√ Hz in a gain of 2-V/V configuration. A fully differential amplifier configured in a gain of 1 V/V with 1-kΩ resistors must be less than 1 nV/√ Hz to achieve the OPA862 equivalent output-referred noise density of 8.3 nV/√ Hz. The OPA862 can be configured for other gains using external resistors. The device has a large gain-bandwidth product of 400 MHz and a slew rate of 140 V/µs. This yields exceptional linearity and fast-settling, 18-bit performance over comparable single-ended-to-differential ADC drivers. The device includes a reference input pin for setting the output common-mode voltage.

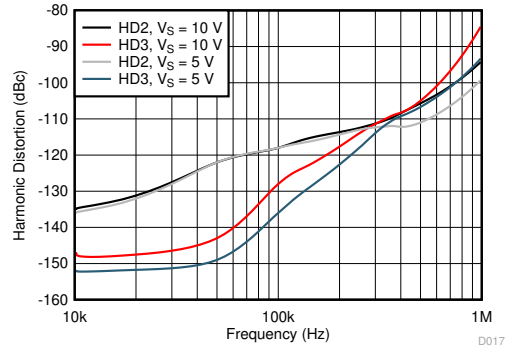
The OPA862 is fully characterized to operate over a wide supply range of 3 V to 12.6 V, and features a rail-to-rail output stage. The device is fabricated using Texas Instruments' proprietary, high-speed, silicon-germanium (SiGe) process and achieves exceptional distortion performance for 18-bit systems. The device includes a disable mode that consumes only 12-µA quiescent current in power-down state.

The OPA862 is rated to work over the extended industrial temperature range of –40°C to +125°C.

**Device Information**(1)

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| OPA862 | SOIC (8) | 4.90 mm × 3.90 mm |
| | WSON (8) | 3.00 mm × 3.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.




**Harmonic Distortion vs Frequency**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision B (Feburary 2020) to Revision C (August 2020) | Page |
|---|---|
| • Updated the numbering format for tables, figures, and cross-references throughout the document | 1 |
| • Changed the status of OPA862 WSON package From: *Preview* To: *Active* | 1 |

| Changes from Revision A (September 2019) to Revision B (February 2020) | Page |
|---|---|
| • Changed document status from advance information to production data | 1 |


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## 5 Pin Configuration and Functions

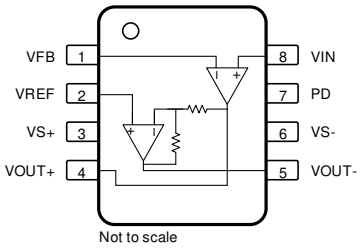


**Figure 5-1. D Package, 8-Pin SOIC (Top View)**

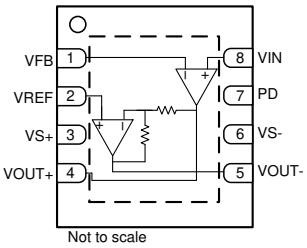


**Figure 5-2. DTK Package, 8-Pin WSON (Top View)**

**Table 5-1. Pin Functions**

| PIN[1] | | TYPE[2] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| PD | 7 | I | Power down (low = enable, high = disable), cannot be floated |
| VFB | 1 | I | Amplifier 1 inverting (feedback) input |
| VIN | 8 | I | Amplifier 1 noninverting (signal) input |
| VOUT+ | 4 | O | Noninverting output |
| VOUT– | 5 | O | Inverting output |
| VREF | 2 | I | Amplifier 2 noninverting (reference) input |
| VS+ | 3 | P | Positive power supply |
| VS– | 6 | P | Negative power supply |

(1) Solder the exposed DTK package thermal pad to a heatspreading power or ground plane. This pad is electrically isolated from the die, but must be connected to a power or ground plane and not floated.
(2) I = input, O = output, and P = power.

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage | Supply voltage, $(V_{S+}) – (V_{S–})$ | | 13 | V |
| | Supply turn-on/turn-off maximum dV/dT[2] | | 1 | V/µs |
| | Input-output voltage range | $(V_{S–}) – 0.5$ | $(V_{S+}) + 0.5$ | V |
| | Differential input voltage | | 0.7 | |
| Current | Continuous input current[3] | | ±10 | mA |
| | Continuous output current[4] | | ±20 | |
| Temperature | Continuous power dissipation | See *Thermal Information* | | |
| | Junction, $T_J$ | | 150 | °C |
| | Operating free-air, $T_A$ | –40 | 125 | |
| | Storage, $T_{stg}$ | –65 | 150 | |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Stay below this ± supply turn-on edge rate to make sure that the edge-triggered ESD absorption device across the supply pins remains off.
(3) Continuous input current limit for both the ESD diodes to supply pins and amplifier differential input clamp diode. The differential input clamp diode limits the voltage across it to 0.7 V with this continuous input current flowing through it.
(4) Long-term continuous current for electromigration limits.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±2500 | V |
| | | Charged device model (CDM), per JEDEC specificationJESD22-C101[2] | ±1500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{S+}$ | Single-supply positive voltage | 3 | 10 | 12.6 | V |
| $T_A$ | Ambient temperature | –40 | 25 | 125 | °C |

## 6.4 Thermal Information

| THERMAL METRIC[1] | | OPA862 | | UNIT |
|---|---|---|---|---|
| | | D (SOIC) | DTK (WSON) | |
| | | 8 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 125.7 | 65.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 65.9 | 56.7 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 69.1 | 34.4 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 18 | 1.6 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 68.3 | 34.4 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | 8.8 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.


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## 6.5 Electrical Characteristics: $V_S$ = ±2.5 V to ±5 V

$T_A$ ≈ 25°C, A1 input common-mode voltage ($V_{CM}$) = midsupply, $V_{REF}$ = midsupply, $R_F$ (connected between VOUT+ and VFB) = 0 Ω, $R_G$ = open, differential gain (G) = 2 V/V, $R_L$ (differential load) = 2 kΩ, $R_{REF}$ = 0 Ω, and $V_S$ = ±5 V for $V_{OD}$ = 10 $V_{PP}$ condtions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **AC PERFORMANCE** | | | | | | | |
| SSBW | Differential small-signal bandwidth | $V_{OD}$ = 20 $mV_{PP}$ | | | 44 | | MHz |
| | | $V_{OD}$ = 20 $mV_{PP}$, G = 4 V/V, $R_F$ = 700 Ω | | | 48 | | |
| | | $V_{OD}$ = 20 $mV_{PP}$, G = –2 V/V, $R_F$ = 700 Ω | | | 48 | | |
| LSBW | Differential large-signal bandwidth | $V_{OD}$ = 1 $V_{PP}$ | | | 42 | | MHz |
| | | $V_S$ = ±2.5 V, $V_{OD}$ = 5 $V_{PP}$ | | | 14 | | |
| | | $V_{OD}$ = 10 $V_{PP}$ | | | 7.5 | | |
| GBWP | Differential gain-bandwidth product | $V_{OD}$ = 40 $mV_{PP}$, G = 200 V/V, $R_F$ = 700 Ω | | | 400 | | MHz |
| | Bandwidth for 0.1-dB flatness | $V_{OD}$ = 20 $mV_{PP}$, G = 2 V/V | | | 6.5 | | MHz |
| | Output balance ($\Delta V_{OD}$ / $\Delta V_{OCM}$) | $V_{OD}$ = 5 $V_{PP}$, f = 1 MHz | | | 41 | | dB |
| SR | Slew rate[(1)] (20% – 80%) | $V_{OD}$ = 10 $V_{PP}$ | | | 140 | | V/µs |
| | Overshoot, undershoot | $V_{OD}$ = 10-V step | | | 0.2% | | |
| $t_r$, $t_f$ | Rise and fall time | $V_{OD}$ = 200-mV step | | | 8.5 | | ns |
| | Settling time | To 0.0015% of final value, $V_{OD}$ = 10-V step | | | 100 | | ns |
| | Input overdrive recovery | $V_{IN}$ = $V_S$ ± 0.5 V, $V_{REF}$ = midsupply | | | 100 | | ns |
| | Output overdrive recovery | G = –4 V/V, $V_{OD}$ = 2x overdrive | | | 120 | | ns |
| HD2 | Second-order harmonic distortion | $V_{OD}$ = 10 $V_{PP}$, f = 15 kHz | | | –133 | | dBc |
| | | $V_{OD}$ = 10 $V_{PP}$, f = 50 kHz | | | –122 | | |
| | | $V_{OD}$ = 10 $V_{PP}$, f = 350 kHz | | | –110 | | |
| HD3 | Third-order harmonic distortion | $V_{OD}$ = 10 $V_{PP}$, f = 15 kHz | | | –148 | | dBc |
| | | $V_{OD}$ = 10 $V_{PP}$, f = 50 kHz | | | –140 | | |
| | | $V_{OD}$ = 10 $V_{PP}$, f = 350 kHz | | | –110 | | |
| $e_n$ | Differential output noise | f ≥ 10 kHz | | | 8.3 | | nV/√Hz |
| | Input voltage noise of A1 and A2 | f ≥ 5 kHz | | | 2.3 | | |
| $e_i$ | Input current noise of A1 | f ≥ 100 kHz | | | 0.7 | | pA/√Hz |
| | Input current noise of A2 | f ≥ 100 kHz | | | 0.9 | | |
| **DC PERFORMANCE** | | | | | | | |
| $V_{OS}$ | Differential output offset voltage | | | | ±50 | ±700 | µV |
| | Input offset voltage for A1, A2 | | | | ±50 | ±325 | |
| | Differential output offset drift | $T_A$ = 0°C to 85°C, $T_A$ = –40°C to 125°C | SOIC | | ±1.5 | ±9 | µV/°C |
| | | | WSON | | ±1.5 | ±7 | |
| | Input offset voltage drift for A1, A2 | $T_A$ = 0°C to 85°C, $T_A$ = –40°C to 125°C | SOIC | | ±0.5 | ±3 | |
| | | | WSON | | ±0.5 | ±2.5 | |
| $I_B$ | Input bias current, A1 | | | | 1 | 3.1 | µA |
| | Input bias current, A2 | VREF pin | | | ±5 | ±90 | nA |
| | Input bias current drift, A1 | $T_A$ = –40°C to 125°C | | | 13 | | nA/°C |
| | Input bias current drift, A2 | VREF pin, $T_A$ = –40°C to 125°C | | | ±65 | | pA/°C |
| $I_{OS}$ | Input offset current, A1 | | | | ±4 | ±110 | nA |
| G | Differential gain | | | | 2 | | V/V |
| | Differnetial gain error | | | | ±0.1 | ±0.25 | % |
| | Differential gain error drift | $T_A$ = –40°C to 125°C | | | ±0.02 | | ppm/°C |

## 6.5 Electrical Characteristics: $V_S$ = ±2.5 V to ±5 V (continued)

$T_A$ ≈ 25°C, A1 input common-mode voltage ($V_{CM}$) = midsupply, $V_{REF}$ = midsupply, $R_F$ (connected between VOUT+ and VFB) = 0 Ω, $R_G$ = open, differential gain (G) = 2 V/V, $R_L$ (differential load) = 2 kΩ, $R_{REF}$ = 0 Ω, and $V_S$ = ±5 V for $V_{OD}$ = 10 $V_{PP}$ condtions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $R_{INT}$ | Internal resistors | | | 700 | | Ω |
| **INPUT** | | | | | | |
| CMIR | Input common-mode range, A1 | | $V_{S–}$ + 0.5 | | $V_{S+}$ – 1.1 | V |
| | VREF pin common-mode range | | $V_{S–}$ + 1.3 | | $V_{S+}$ – 1.1 | |
| | $\Delta V_{OS}$ (2) at CMIR specification, A1 | $V_{CM}$ = $V_{S+}$ – 1.1 V and $V_{CM}$ = $V_{S–}$ + 0.5 V | | | ±25 | µV |
| | $\Delta V_{OS}$ (2) at CMIR specification | $V_{REF}$ = $V_{S+}$ – 1.1 V and $V_{REF}$ = $V_{S–}$ + 1.3 V | | | ±50 | µV |
| CMRR | Common-mode rejection ratio | CMRR = $V_{OD}$ / $V_{IN}$, $V_{IN}$ = $V_{REF}$, $V_{CM}$ = ±1 V, $R_{REF}$ = 0 Ω | 100 | 120 | | dB |
| | Input impedance common-mode, A1 | | | 325 \|\| 0.6 | | MΩ \|\| pF |
| | Input impedance differential-mode, A1 | | | 35 \|\| 1.9 | | kΩ \|\| pF |
| | Input impedance, A2 | VREF pin | | 2.3 \|\| 3.5 | | GΩ \|\| pF |
| **OUTPUT** | | | | | | |
| $V_{OL}$ | Output voltage range low | Each output, single-ended | | $V_{S–}$ + 0.15 | $V_{S–}$ + 0.25 | V |
| $V_{OH}$ | Output voltage range high | Each output, single-ended | $V_{S+}$ – 0.25 | $V_{S+}$ – 0.15 | | V |
| | Linear output current | $V_S$ = ±5 V, $V_{OD}$ = ±2.65 V, $\Delta V_{OCM}$ < ±10 mV relative to no-load condition | 40 | 60 | | mA |
| **POWER SUPPLY** | | | | | | |
| $V_S$ | Specified operating voltage | Single-supply referred to GND | 3 | 10 | 12.6 | V |
| $I_Q$ | Quiescent current | $V_S$ = ±5 V, $T_A$ = 25°C | 2.8 | 3.1 | 3.3 | mA |
| | Quiescent current drift | $V_S$ = ±5 V, $T_A$ = –40°C to 125°C | | 9 | | µA/°C |
| PSRR | Power-supply rejection ratio | $V_{IN}$ = $V_{REF}$ = 0 V, $\Delta V_S$ = 2 V | 105 | 115 | | dB |
| **POWER DOWN** | | | | | | |
| | Disable voltage threshold | Disabled above specified voltage | | | $V_{S–}$ + 1.5 | V |
| | Enable voltage threshold | Enabled below specified voltage | $V_{S–}$ + 1 | | | V |
| | Disable pin bias current | | –10 | | 10 | nA |
| | Power-down quiescent current | | | 12 | 20 | µA |
| | Turn-on time delay | | | 1.3 | | µs |
| | Turn-off time delay | | | 2.5 | | µs |

(1) Average of rising and falling slew rate.
(2) $\Delta V_{OS}$ = $V_{OS}$ at specified CMIR $V_{CM}$ – $V_{OS}$ at midsupply $V_{CM}$.


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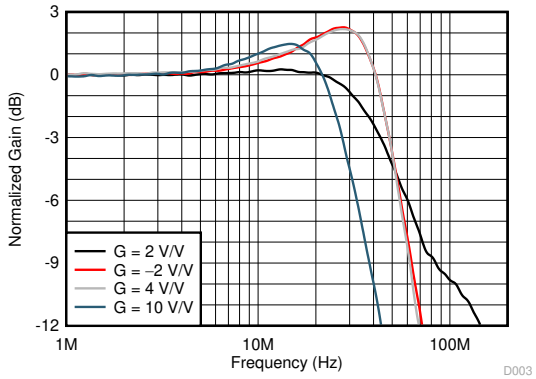
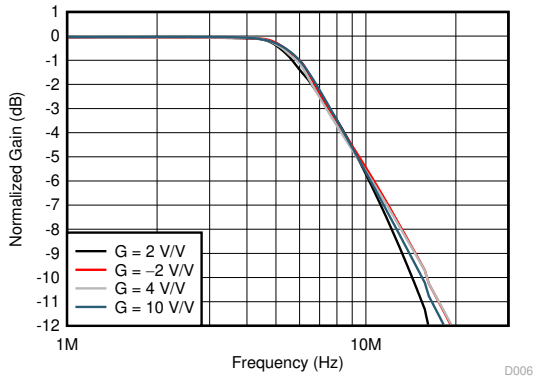
## 6.6 Typical Characteristics: $V_S$ = ±5 V

$T_A$ ≈ 25°C, A1 input common-mode voltage ($V_{CM}$) = midsupply, $V_{REF}$ = midsupply, $R_F$ (connected between VOUT+ and VFB) = 0 Ω, $R_G$ = open, differential gain (G) = 2 V/V, $R_L$ (differential load) = 2 kΩ, and $R_{REF}$ = 0 Ω (unless otherwise noted).



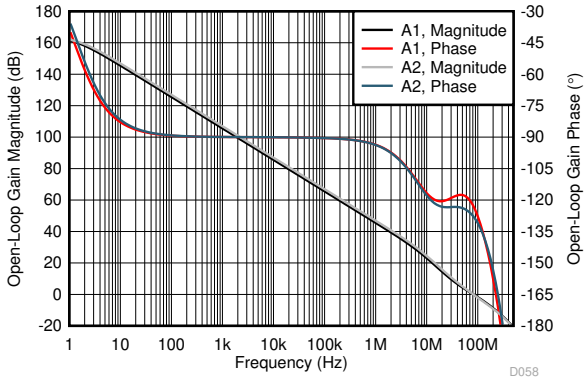

$V_{OD}$ = 20 $mV_{PP}$

**Figure 6-1. Small-Signal Frequency Response**



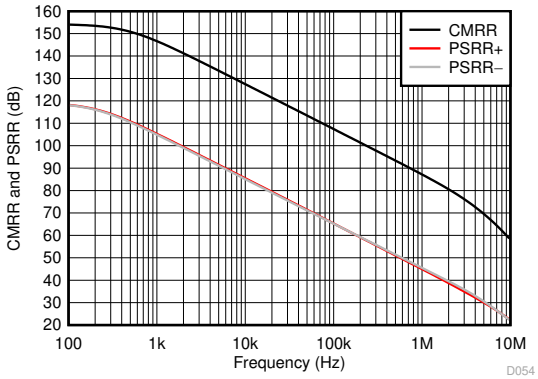

$V_{OD}$ = 10 $V_{PP}$

**Figure 6-2. Large-Signal Frequency Response**



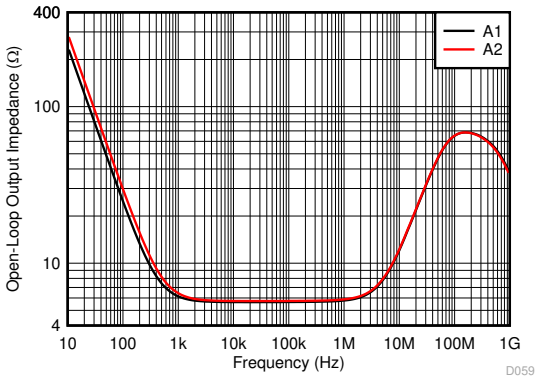

Simulation

**Figure 6-3. Open-Loop Gain And Phase vs Frequency**



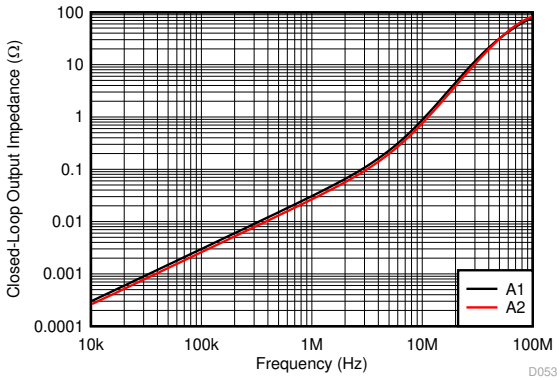

Simulation, A1 and A2

**Figure 6-4. CMRR and PSRR vs Frequency**




Simulation

**Figure 6-5. Open-Loop Output Impedance vs Frequency**

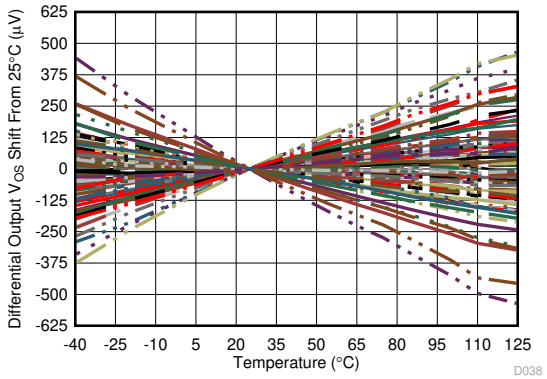



Simulation

**Figure 6-6. Closed-Loop Output Impedance vs Frequency**

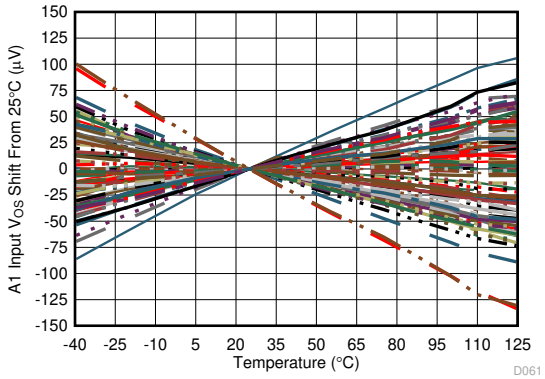
## 6.6 Typical Characteristics: $V_S$ = ±5 V (continued)

$T_A$ ≈ 25°C, A1 input common-mode voltage ($V_{CM}$) = midsupply, $V_{REF}$ = midsupply, $R_F$ (connected between VOUT+ and VFB) = 0 Ω, $R_G$ = open, differential gain (G) = 2 V/V, $R_L$ (differential load) = 2 kΩ, and $R_{REF}$ = 0 Ω (unless otherwise noted).



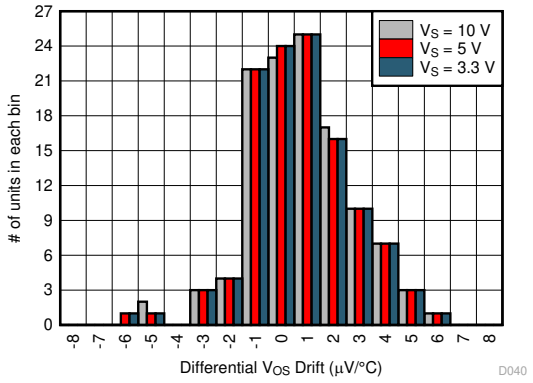

99 units

**Figure 6-7. Differential Output Offset Voltage vs Temperature**



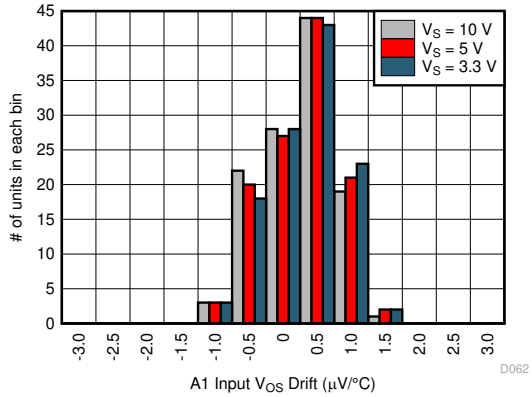

99 units

**Figure 6-8. A1 Input Offset Voltage vs Temperature**



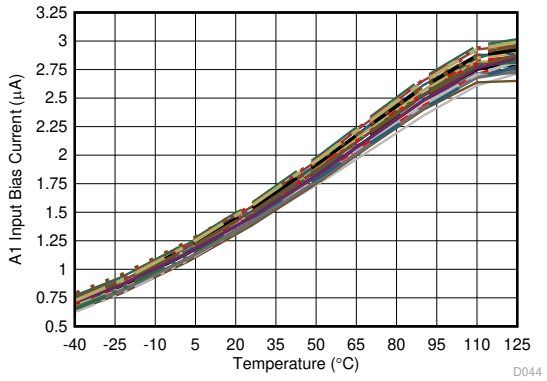

–40°C to +125°C, over 115 units

**Figure 6-9. Differential Output Offset Voltage Drift Histogram**



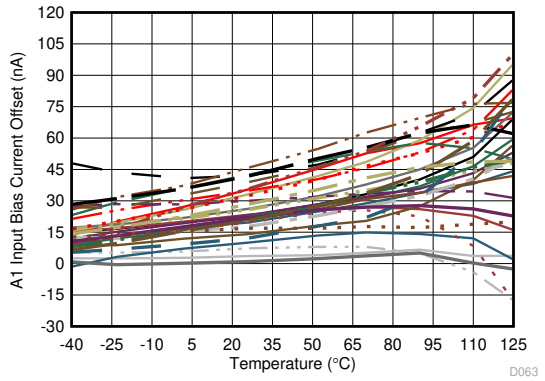

–40°C to +125°C, over 115 units

**Figure 6-10. A1 Input Offset Voltage Drift Histogram**




32 units

**Figure 6-11. A1 Input Bias Current vs Temperature**




32 units

**Figure 6-12. A1 Input Offset Current vs Temperature**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## 6.6 Typical Characteristics: $V_S$ = ±5 V (continued)

$T_A$ ≈ 25°C, A1 input common-mode voltage ($V_{CM}$) = midsupply, $V_{REF}$ = midsupply, $R_F$ (connected between VOUT+ and VFB) = 0 Ω, $R_G$ = open, differential gain (G) = 2 V/V, $R_L$ (differential load) = 2 kΩ, and $R_{REF}$ = 0 Ω (unless otherwise noted).

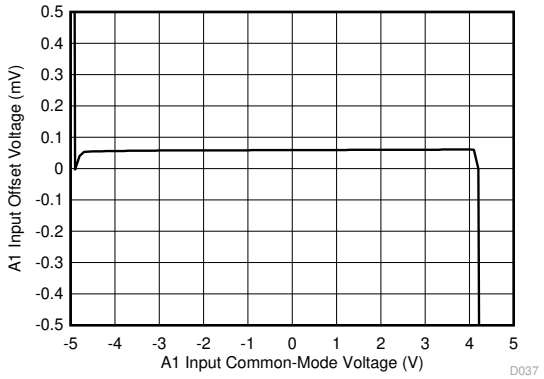



**Figure 6-13. A1 Input Offset Voltage vs Input Common-Mode Voltage**

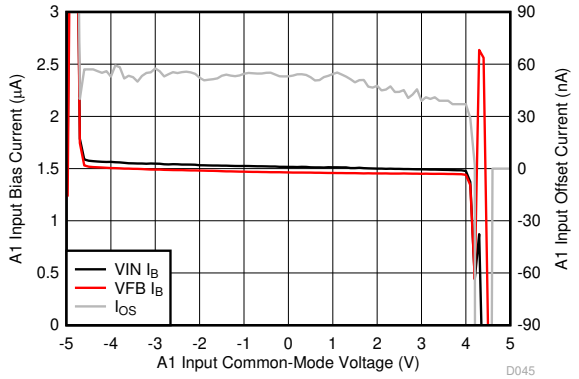
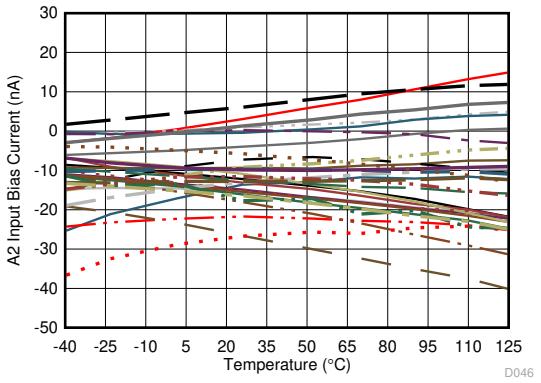



**Figure 6-14. A1 Input Bias Current and Input Offset Current vs Input Common-Mode Voltage**




32 units

**Figure 6-15. A2 Input Bias Current vs Temperature**

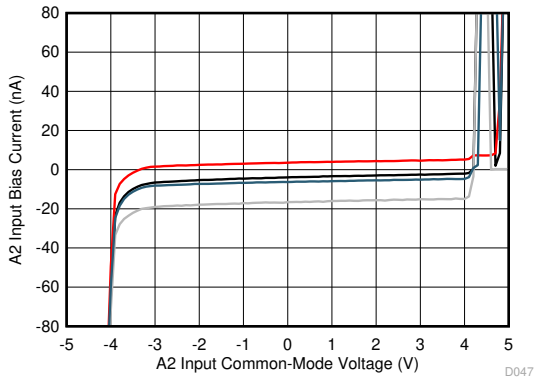



**Figure 6-16. A2 Input Bias Current vs Input Common-Mode Voltage**

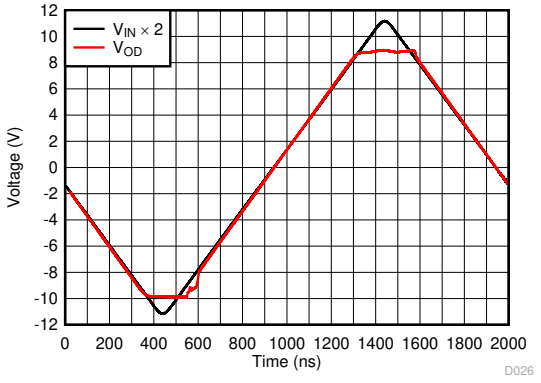
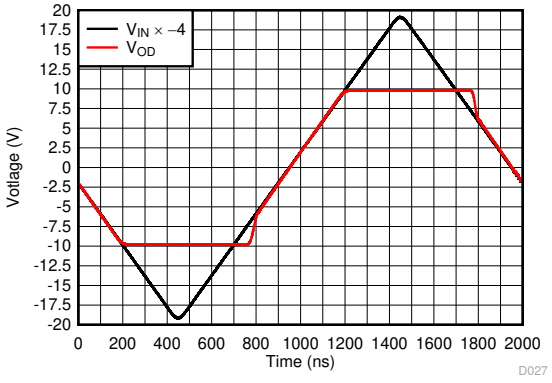



**Figure 6-17. Input Overdrive Recovery**

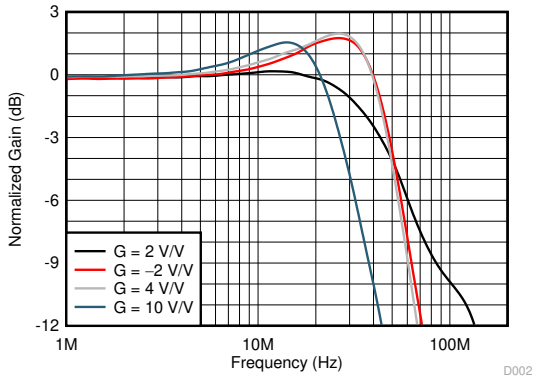



G = –4 V/V

**Figure 6-18. Output Overdrive Recovery**

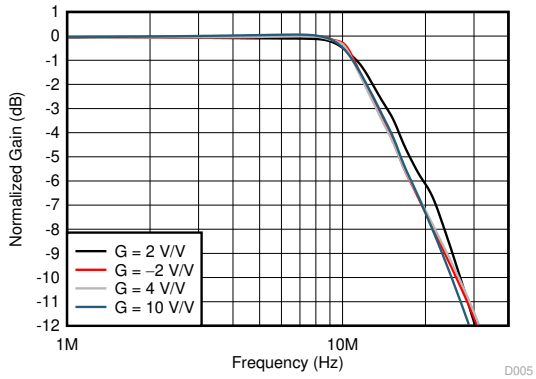
## 6.7 Typical Characteristics: $V_S$ = ±2.5 V

$T_A$ ≈ 25°C, A1 input common-mode voltage ($V_{CM}$) = midsupply, $V_{REF}$ = midsupply, $R_F$ (connected between VOUT+ and VFB) = 0 Ω, $R_G$ = open, differential gain (G) = 2 V/V, $R_L$ (differential load) = 2 kΩ, and $R_{REF}$ = 0 Ω (unless otherwise noted).



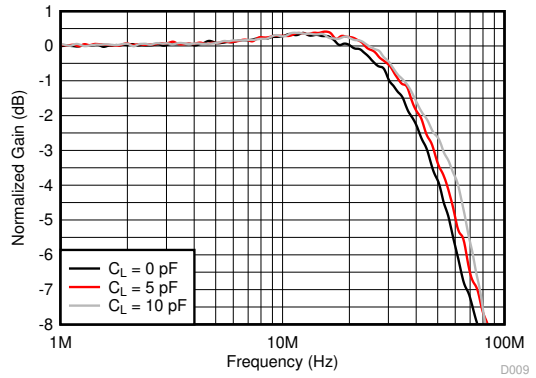

$V_{OD}$ = 20 $mV_{PP}$

**Figure 6-19. Small-Signal Frequency Response**



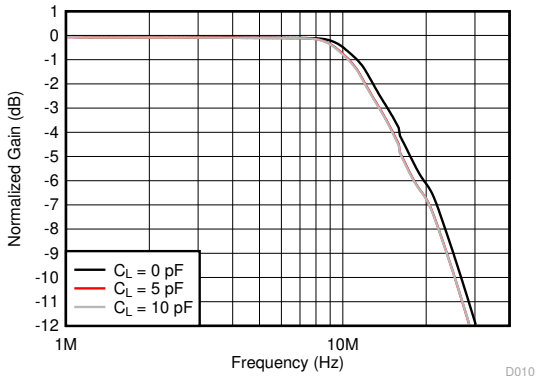

$V_{OD}$ = 5 $V_{PP}$

**Figure 6-20. Large-Signal Frequency Response**




$V_{OD}$ = 20 $mV_{PP}$

**Figure 6-21. Small-Signal Frequency Response Over $C_L$**




$V_{OD}$ = 5 $V_{PP}$

**Figure 6-22. Large-Signal Frequency Response Over $C_L$**

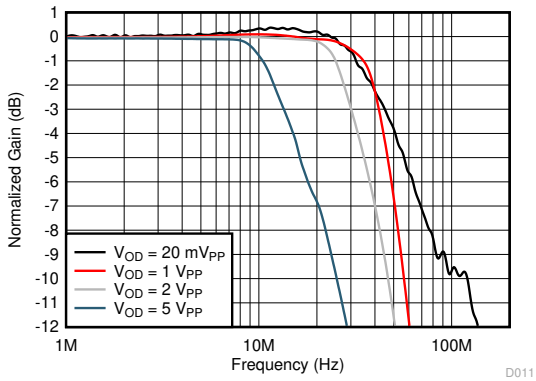



**Figure 6-23. Frequency Response Over Differential Output Voltage, $V_{OD}$**

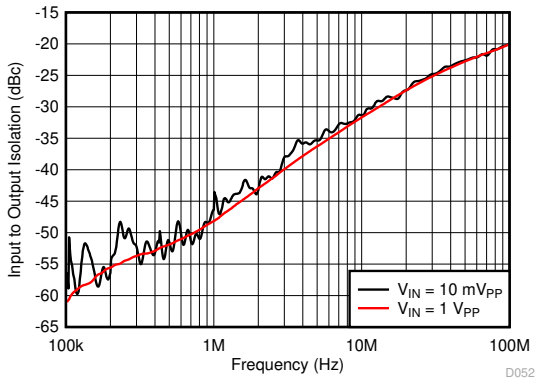



**Figure 6-24. Input-to-Output Disable Mode Isolation**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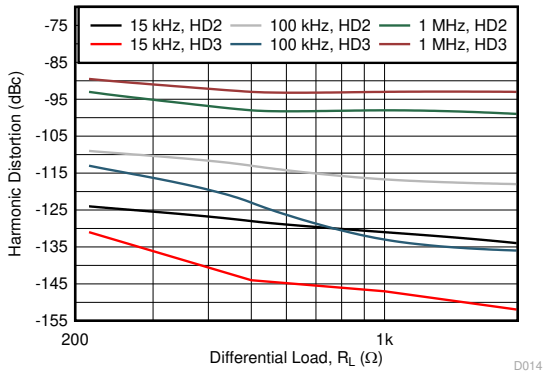
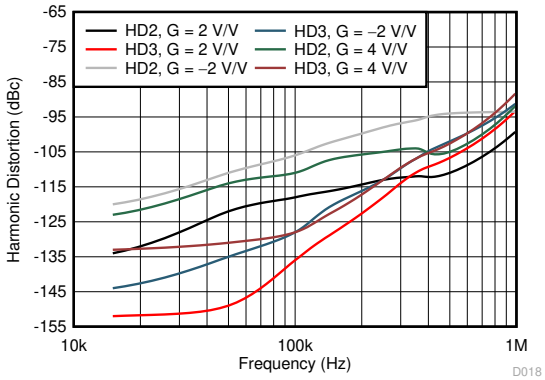
## 6.7 Typical Characteristics: $V_S$ = ±2.5 V (continued)

$T_A$ ≈ 25°C, A1 input common-mode voltage ($V_{CM}$) = midsupply, $V_{REF}$ = midsupply, $R_F$ (connected between VOUT+ and VFB) = 0 Ω, $R_G$ = open, differential gain (G) = 2 V/V, $R_L$ (differential load) = 2 kΩ, and $R_{REF}$ = 0 Ω (unless otherwise noted).



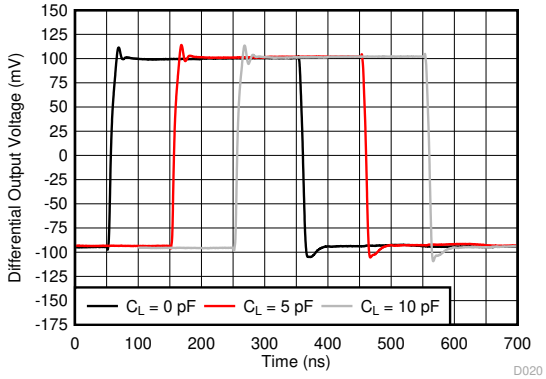

$V_{OD}$ = 5 $V_{PP}$

**Figure 6-25. Harmonic Distortion vs Differential Load**



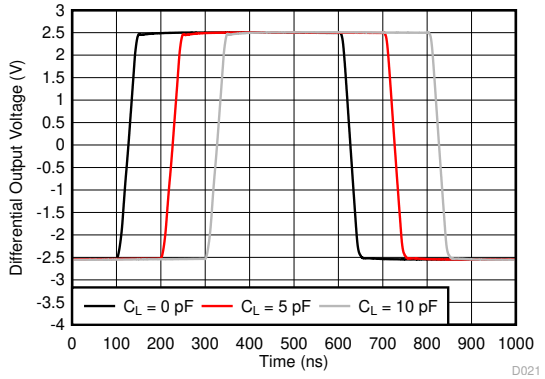

$V_{OD}$ = 5 $V_{PP}$

**Figure 6-26. Harmonic Distortion vs Frequency and Gain**




$V_{OD}$ = 200 $mV_{PP}$

**Figure 6-27. Small-Signal Step Response Over $C_L$**




$V_{OD}$ = 5 $V_{PP}$

**Figure 6-28. Large-Signal Step Response Over $C_L$**

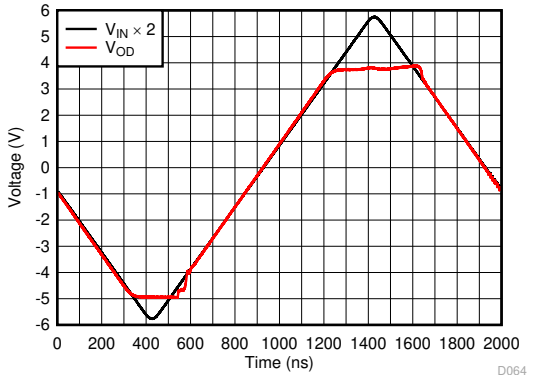
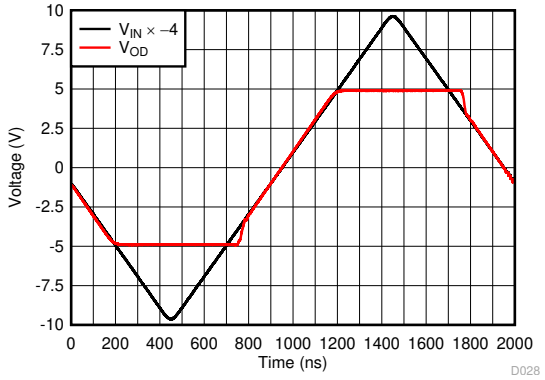



**Figure 6-29. Input Overdrive Recovery**

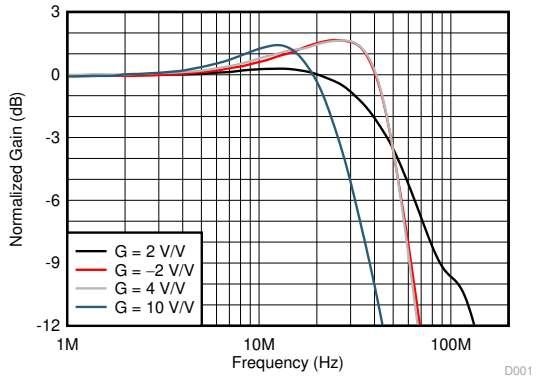



G = –4 V/V

**Figure 6-30. Output Overdrive Recovery**

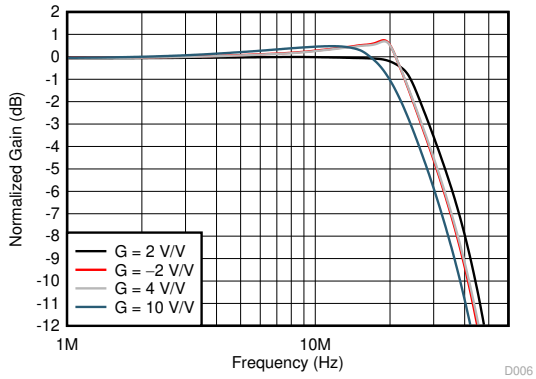
## 6.8 Typical Characteristics: $V_S$ = 1.9 V, –1.4 V

$T_A$ ≈ 25°C, A1 input common-mode voltage ($V_{CM}$) = midsupply, $V_{REF}$ = midsupply, $R_F$ (connected between VOUT+ and VFB) = 0 Ω, $R_G$ = open, differential gain (G) = 2 V/V, $R_L$ (differential load) = 2 kΩ, and $R_{REF}$ = 0 Ω (unless otherwise noted).




$V_{OD}$ = 20 $mV_{PP}$

**Figure 6-31. Small-Signal Frequency Response**




$V_{OD}$ = 2 $V_{PP}$

**Figure 6-32. Large-Signal Frequency Response**

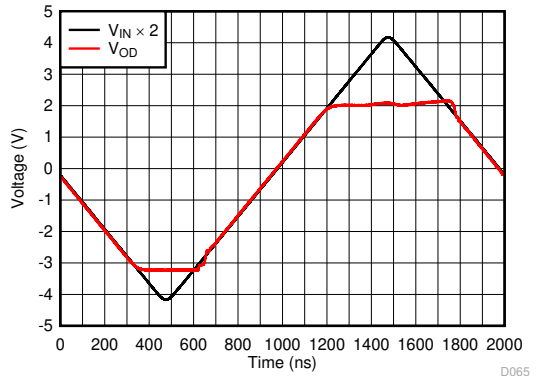
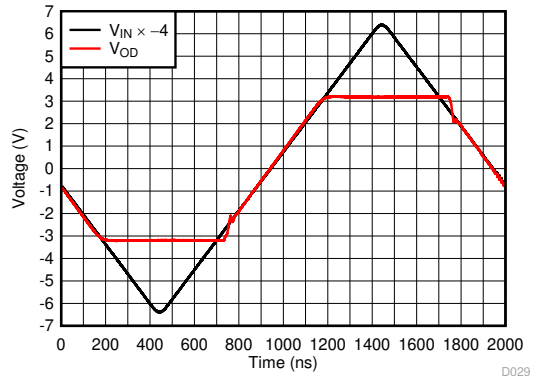



**Figure 6-33. Input Overdrive Recovery**




G = –4 V/V

**Figure 6-34. Output Overdrive Recovery**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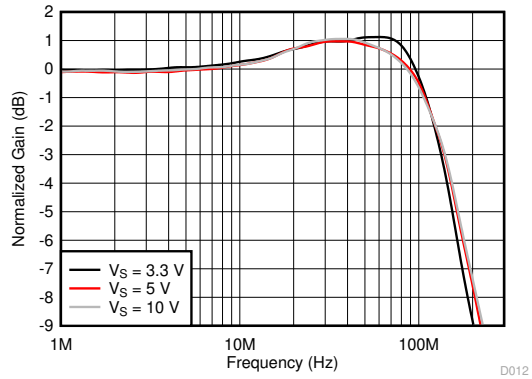
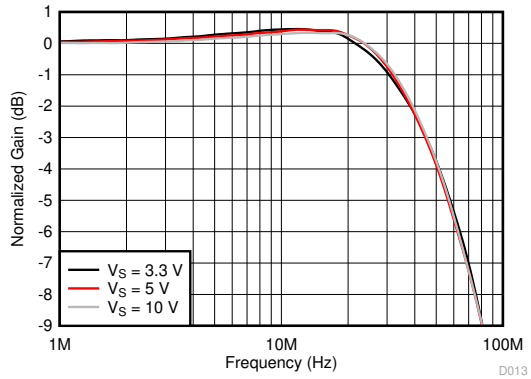
## 6.9 Typical Characteristics: $V_S$ = 1.9 V, –1.4 V to ±5 V

$T_A$ ≈ 25°C, A1 input common-mode voltage ($V_{CM}$) = midsupply, $V_{REF}$ = midsupply, $R_F$ (connected between VOUT+ and VFB) = 0 Ω, $R_G$ = open, differential gain (G) = 2 V/V, $R_L$ (differential load) = 2 kΩ, and $R_{REF}$ = 0 Ω (unless otherwise noted).



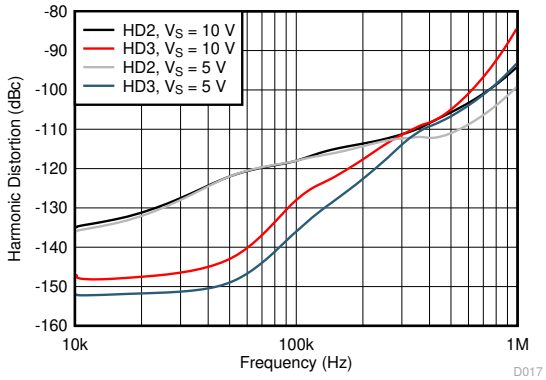

$V_{IN}$ = 10 $mV_{PP}$, $V_{REF}$ = 0 V, measured at VOUT+

**Figure 6-35. A1 Small-Signal Frequency Response**



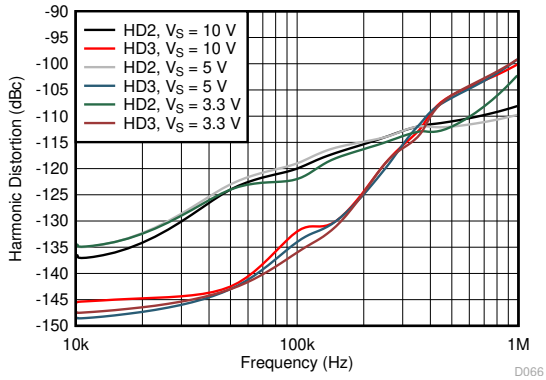

$V_{IN}$ = 0 V, $V_{REF}$ = 20 $mV_{PP}$, measured at VOUT–

**Figure 6-36. $V_{REF}$ Small-Signal Frequency Response**



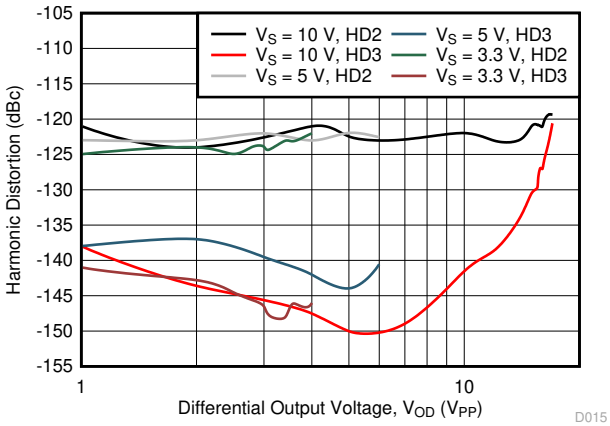

$V_{OD}$ = 10 $V_{PP}$ for 10-V supply, $V_{OD}$ = 5 $V_{PP}$ for 5-V supply

**Figure 6-37. Harmonic Distortion vs Frequency**



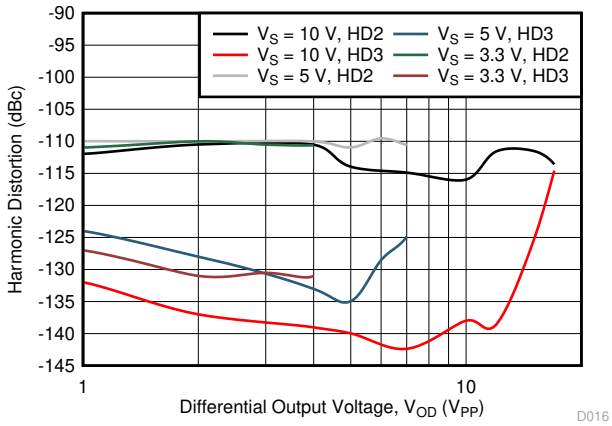

$V_{OD}$ = 2 $V_{PP}$

**Figure 6-38. Harmonic Distortion vs Frequency**




Frequency = 50 kHz

**Figure 6-39. Harmonic Distortion vs Differential Output Voltage**

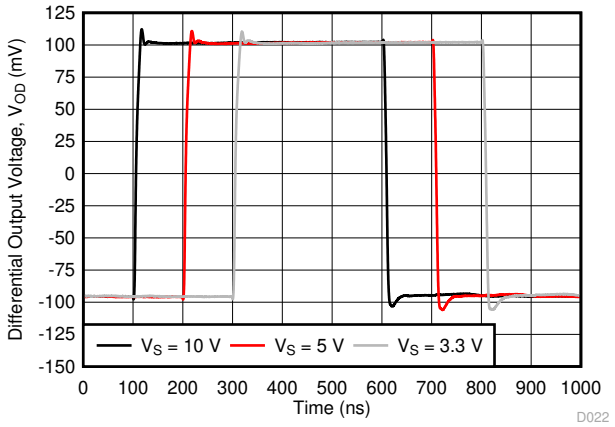



Frequency = 50 kHz, G = –2 V/V

**Figure 6-40. Harmonic Distortion vs Differential Output Voltage**

## 6.9 Typical Characteristics: $V_S$ = 1.9 V, –1.4 V to ±5 V (continued)

$T_A$ ≈ 25°C, A1 input common-mode voltage ($V_{CM}$) = midsupply, $V_{REF}$ = midsupply, $R_F$ (connected between VOUT+ and VFB) = 0 Ω, $R_G$ = open, differential gain (G) = 2 V/V, $R_L$ (differential load) = 2 kΩ, and $R_{REF}$ = 0 Ω (unless otherwise noted).




$V_{OD}$ = 200 $mV_{PP}$

**Figure 6-41. Small-Signal Step Response**

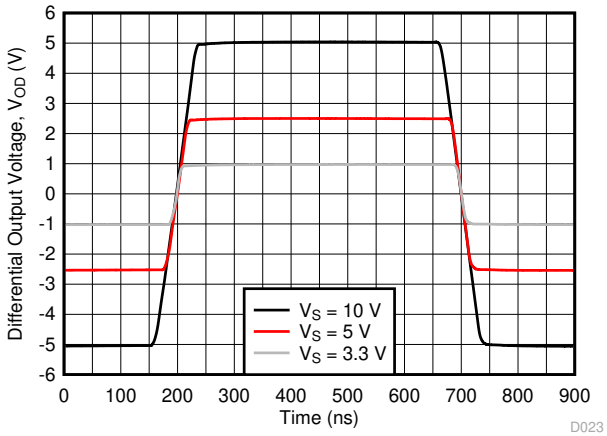
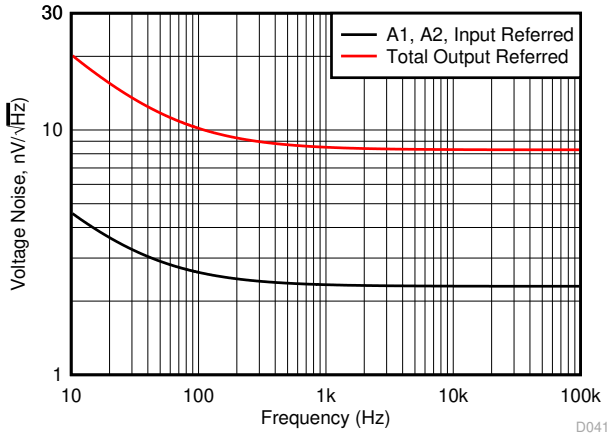
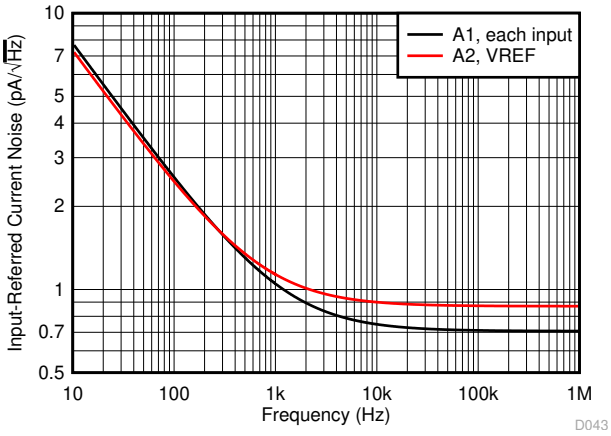



**Figure 6-42. Large-Signal Step Response**




1/f corner (A1, A2) = 30 Hz, 1/f corner (output) = 49 Hz

**Figure 6-43. Voltage Noise Density vs Frequency**




1/f corner (A1) = 1.2 kHz, 1/f corner (A2) = 700 Hz

**Figure 6-44. Current Noise Density vs Frequency**

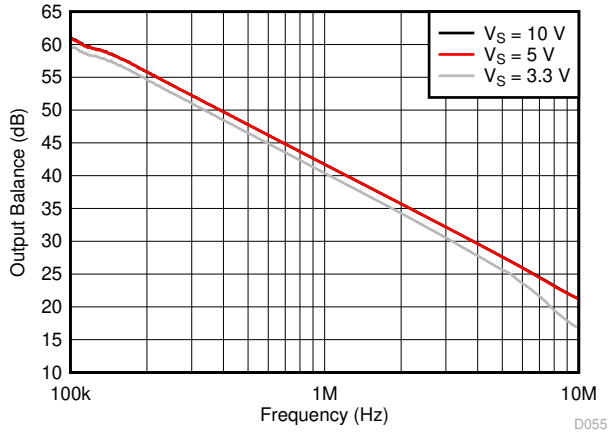
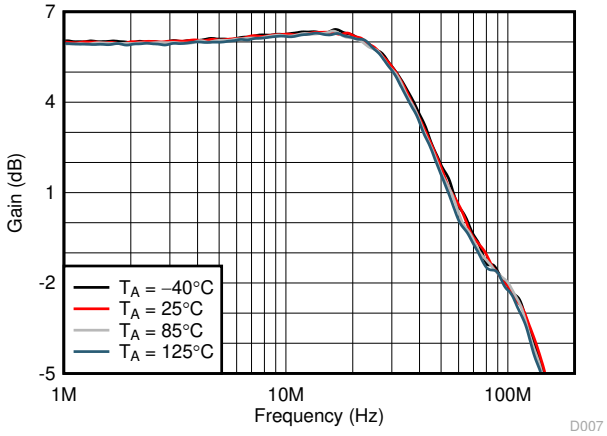



**Figure 6-45. Output Balance vs Frequency**




$V_S$ = 5 V, $V_{OD}$ = 20 $mV_{PP}$

**Figure 6-46. Small-Signal Frequency Response vs Temperature**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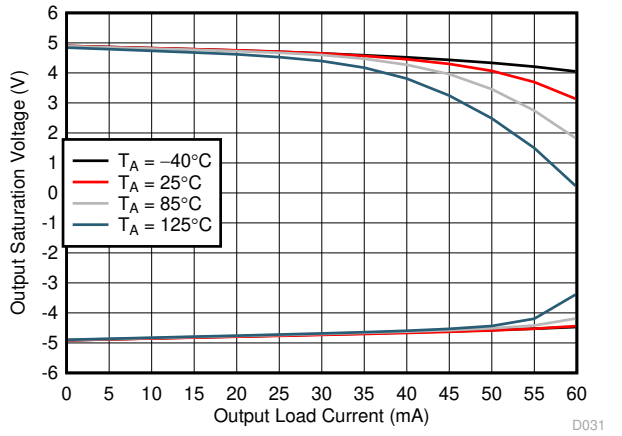
## 6.9 Typical Characteristics: $V_S$ = 1.9 V, –1.4 V to ±5 V (continued)

$T_A$ ≈ 25°C, A1 input common-mode voltage ($V_{CM}$) = midsupply, $V_{REF}$ = midsupply, $R_F$ (connected between VOUT+ and VFB) = 0 Ω, $R_G$ = open, differential gain (G) = 2 V/V, $R_L$ (differential load) = 2 kΩ, and $R_{REF}$ = 0 Ω (unless otherwise noted).




$V_S$ = 10 V, single-ended output voltage and load current for A1 and A2

**Figure 6-47. Output Saturation Voltage vs Output Load Current**

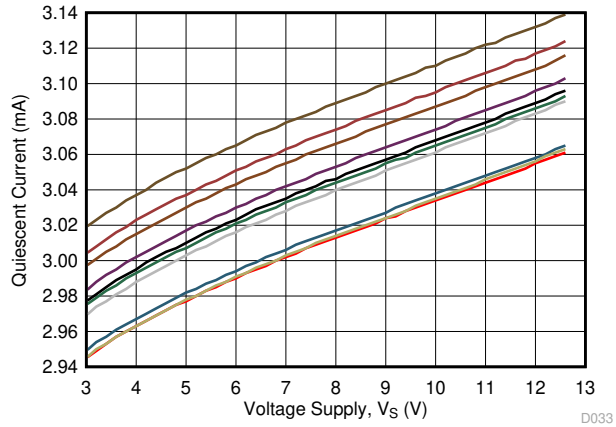



**Figure 6-48. Quiescent Current vs Voltage Supply**

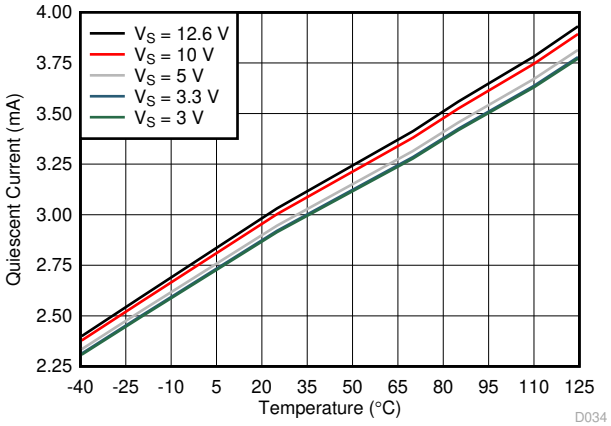



**Figure 6-49. Quiescent Current vs Temperature**

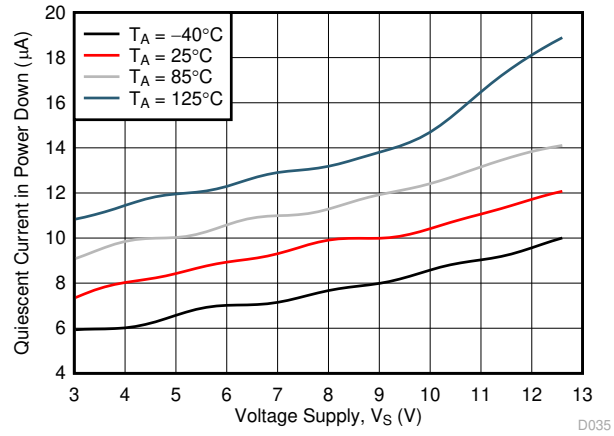
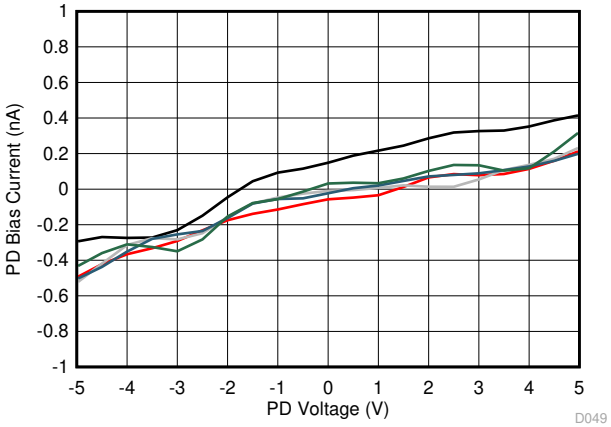
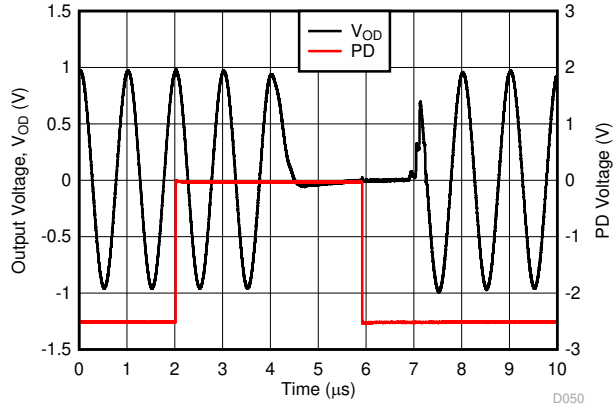



**Figure 6-50. Power-Down Quiescent Current vs Voltage Supply**




$V_S$ = 10 V

**Figure 6-51. Power-Down Bias Current vs Power-Down Voltage**




$V_S$ = 5 V

**Figure 6-52. Turnon and Turnoff Timing**

# 7 Detailed Description

## 7.1 Overview

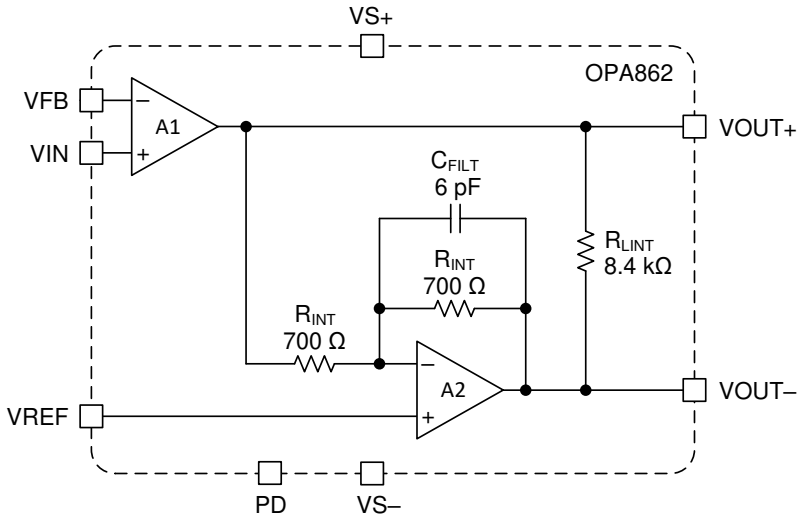
The OPA862 is a 44-MHz, single-ended-to-differential amplifier suitable for use in high-input impedance analog front-ends. This device offers a gain-bandwidth product (GBWP) of 400 MHz with a low output-referred voltage noise of 8.3 nV/√ Hz while consuming only 3.1 mA of quiescent current. The OPA862 includes a REF pin for output common-mode voltage control using amplifier 2 and a shutdown pin for low-power mode operation that consumes only 12 µA of quiescent current.

The OPA862 can be configured for a single-ended-to-differential gain of 2 V/V without using any external resistors. The device can be configured in gains other than 2 V/V by using only two external resistors in the feedback loop of amplifier 1 (A1) and requires fewer external gain-setting resistors compared to a fully differential amplifier (FDA). The noninverting input of A1 offers high input impedance (325 MΩ typical) for interfacing single-ended sensors that often have a non-zero output impedance to differential input analog-to-digital converters (ADCs). A combination of large 140-V/µs slew rate, 400-MHz GBWP, and nonlinearity cancellation in the output stages of the two amplifiers results in exceptional distortion and settling performance for 18-bit systems.

The OPA862 includes an internal capacitor $C_{FILT}$ in the feedback circuit of amplifier 2 (A2) that limits the device bandwidth to approximately 44 MHz. Although the individual amplifiers have a GBWP of 200 MHz, because of the architecture of the OPA862, the input and output signal bandwidth must not exceed approximately 44 MHz to achieve good linearity. High GBWP amplifiers generally have high linearity because they can maintain high loop gain. The simple architecture of the OPA862 (as compared to an FDA) has an inherent delay between the outputs VOUT+ and VOUT– that primarily limits the linearity performance versus the high GBWP of the individual amplifiers. The benefit of the $C_{FILT}$ capacitor is that the $C_{FILT}$ filters and minimizes the noise at the output beyond the usable frequency of the OPA862.

The VREF pin can be used to set the output common-mode to a desired value. Section 7.4 describes various configurations that the OPA862 can be used in.

## 7.2 Functional Block Diagram





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## 7.3 Feature Description

### 7.3.1 Input and ESD Protection

The OPA862 is built using a high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in Section 6.1. As shown in Figure 7-1 all device pins are protected with internal ESD protection diodes to the power supplies.

These diodes provide moderate protection to input overdrive voltages beyond the supplies as well. The protection diodes can typically support 10-mA continuous current. Where higher currents are possible (for example, in systems with ±12-V supply parts driving into the OPA862), add current limiting series resistors in series with the inputs to limit the current. Keep these resistor values as low as possible because high values can degrade both noise performance and frequency response. The OPA862 has back-to-back ESD diodes between the VIN and VFB pins. As a result, the differential input voltage between the VIN and VFB pins must be limited to 0.7 V or less to keep from forward biasing these back-to-back ESD diodes. The diodes are robust enough to survive transient conditions such as those common during slew conditions. In the event the differential input voltage exceeds 0.7 V, these back-to-back diodes forward bias and protect the amplifier but the current must be limited per the specifications in Section 6.1 to avoid permanent damage to these diodes or the amplifier.

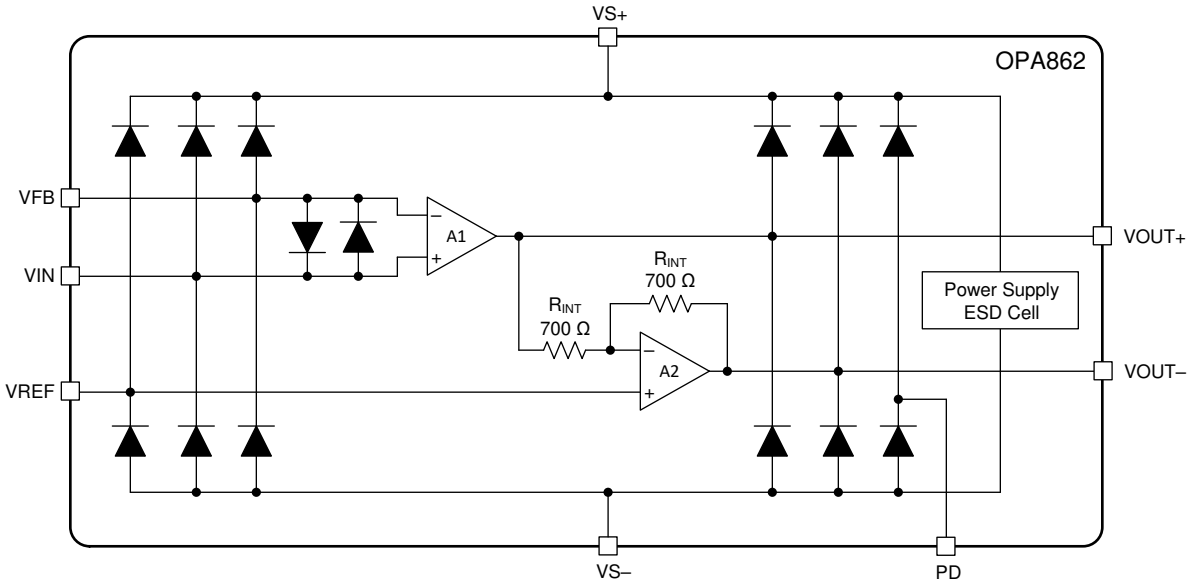


**Figure 7-1. Internal ESD Protection**

### 7.3.2 Anti-Phase Reversal Protection

When the input common-mode voltage approaches or exceeds $V_{S-}$, the base-collector junction of the input transistors forward biases. This condition creates an output path parallel to the normal $g_m$ path of the transistors that is opposite in phase to the $g_m$ path. When this parallel path starts to dominate, phase inversion occurs. To protect against phase inversion, the OPA862 features anti-phase reversal (APR) protection Schottky diodes on the input transistors. The Schottky diodes turn on at a voltage lower than the forward bias voltage of the base-collector junction, thus preventing the forward bias and the phase-inversion at the base-collector junction of the input transistors. Figure 7-2 shows a diagram of APR protection within the OPA862.

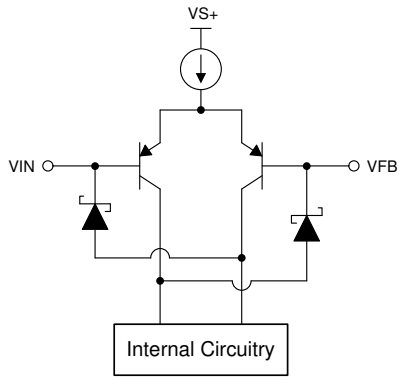


**Figure 7-2. Anti-Phase Reversal Protection**

### 7.3.3 Precision and Low Noise

The OPA862 is laser trimmed for high DC precision. An important factor that reduces the DC precision of the system that uses the OPA862 is the errors introduced by the bias currents of A2 flowing through the internal feedback resistors, $R_{INT}$; see Section 7.2. To minimize the error contribution from $I_B$, the A2 amplifier of the OPA862 features a unique $I_B$ cancellation mechanism. This $I_B$ cancellation mechanism is the reason why the $I_B$ of A2 is orders of magnitude lower than the $I_B$ of A1. The DC errors are negligible for most applications because of the nanoamperes of $I_B$ and very low $I_B$ drift of A2. However, despite being very low, if the $I_B$ errors of A2 are significant for an application, a 348-Ω $R_{REF}$ resistor can be used on the VREF input to cancel out the $I_B$ errors. The tradeoff of using the $R_{REF}$ is that this resistor introduces noise that is amplified by a factor of two at VOUT– because of the noise gain of two of A2. The $C_{FILT}$ capacitor (see Section 7.2) also helps filter out the flat band noise contribution of $R_{REF}$. The 700-Ω internal resistors were carefully chosen to balance low noise while keeping the total power dissipation low by taking advantage of the low 3.1-mA quiescent current of the OPA862. As shown in Figure 7-3, to get the equivalent 8.3-nV/√ Hz noise of the OPA862 with a typical FDA configuration, the FDA must be less than 1 nV/√ Hz; such FDAs are often difficult to find or expensive. When $R_{REF}$ equals 0 Ω, the typical error resulting from the $I_B$ of A2 appears as an input-referred offset of 3.5 µV at the VREF input, and when $R_{REF}$ is 348 Ω, the differential output-referred noise increases from 8.3 nV/√ Hz to 9.6 nV/√ Hz.

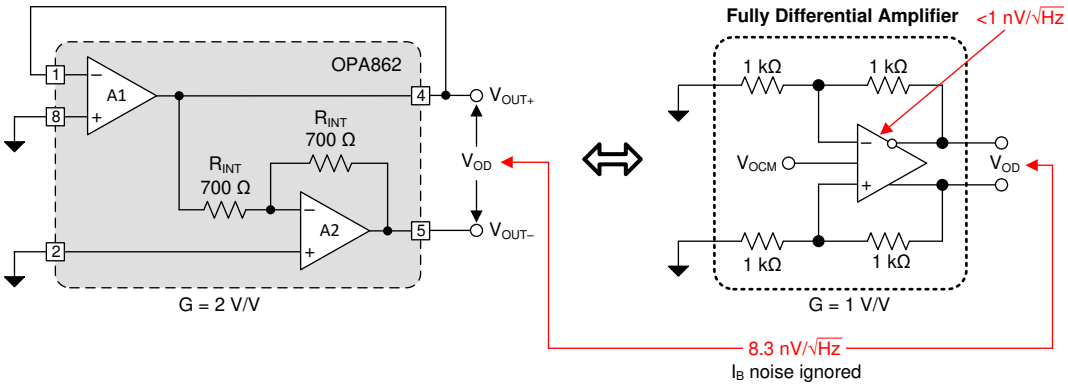


**Figure 7-3. Equivalent Voltage Noise FDA to OPA862**


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## 7.4 Device Functional Modes

### 7.4.1 Split-Supply Operation (±1.5 V to ±6.3 V)

To facilitate testing with common lab equipment, the OPA862 can be configured to allow for split-supply operation. This configuration eases lab testing because the mid-point between the power rails is ground, and most signal generators, network analyzers, oscilloscopes, spectrum analyzers, and other lab equipment reference the inputs and outputs to ground. For split-supply operation referenced to ground, the power supplies $V_{S+}$ and $V_{S–}$ are symmetrical around ground and generally $V_{REF}$ is also set equal to ground. Split-supply operation is preferred in systems where the signals swing around ground because of the ease-of-use; however, the system requires two supply rails.

### 7.4.2 Single-Supply Operation (3 V to 12.6 V)

Many newer systems use a single power supply to improve efficiency and reduce the cost of the extra power supply. The OPA862 can be used with a single supply (negative supply set to ground), as shown in Figure 7-4, with no change in performance if the input and output are biased within the linear operation of the device. To change the circuit from split supply to a single-supply configuration, level shift all the voltages by half the difference between the power-supply rails. In the single-supply configuration, a voltage must be set on the VREF pin, typically midsupply, such that VREF does not violate the common-mode input range (CMIR) specification or the output voltage range of A2. An additional advantage of configuring an amplifier for single-supply operation is that the effects of PSRR are minimized because the low-supply rail is grounded. See the *Single-Supply Op Amp Design Techniques* application report for examples of single-supply designs.

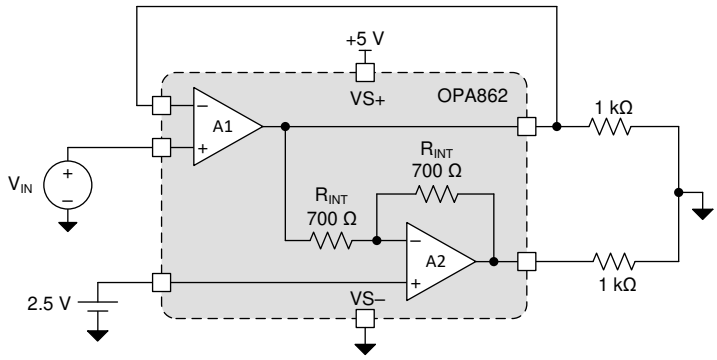


**Figure 7-4. Typical Single-Supply Configuration**

# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

### 8.1.1 Single-Ended-to-Differential Gain of 4 V/V

Figure 8-1 shows the configuration that can be used for a single-ended-to-differential gain of 4 V/V. Amplifier A1 follows all the conventional equations of a regular voltage-feedback amplifier for inverting and noninverting gains. With the fixed inverting gain of –1 V/V for the configuration of A2, the primary role of A2 is to invert the output of A1 so that a differential signal is available at the output pins, VOUT+ and VOUT–. In the configuration shown in Figure 8-1, $V_{OUT+}$ is always in phase with $V_{IN}$ and equal to $V_{IN}$ times two. $V_{OUT-}$ has the same swing as $V_{OUT+}$ but 180° out of phase. The common-mode voltage at A1 is equal to $V_{IN}$ and the common-mode voltage at A2 is equal to the voltage on the VREF pin, which in the case of Figure 8-1 is GND.

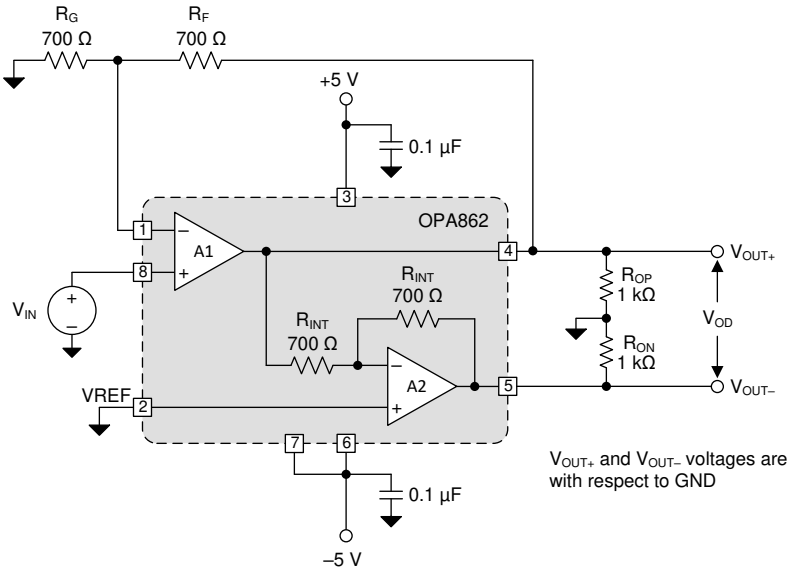


**Figure 8-1. Single-Ended To Differential Gain of 4 V/V Configuration**

Equation 1 through Equation 4 can be derived from the configuration in Figure 8-1. The output common-mode voltage, $V_{OCM}$, is the average of $V_{OUT+}$ and $V_{OUT-}$, and is equal to the voltage on the VREF pin as given by Equation 4.

$$V_{OUT+} = V_{IN}\left(1+\frac{R_F}{R_G}\right) \tag{1}$$

$$V_{OUT-} = -V_{OUT+} + 2\times V_{REF} = -V_{IN}\left(1+\frac{R_F}{R_G}\right) + 2\times V_{REF} \tag{2}$$

$$V_{OD} = V_{OUT+} - V_{OUT-} = 2\times V_{IN}\left(1+\frac{R_F}{R_G}\right) - 2\times V_{REF} \tag{3}$$


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$$V_{OCM} = \frac{V_{OUT+} + V_{OUT-}}{2} = V_{REF} \quad (4)$$

## 8.2 Typical Applications

### 8.2.1 Single-Ended to Differential with 2.5-V Output Common-Mode Voltage

Most real-world signals are single ended. Often, fully differential amplifiers (FDAs) are used for single-ended-to-differential conversions but the low-impedance input of the FDA configuration can be a challenge for digital acquisition systems (DAQs). The high input impedance input of the OPA862, coupled with its ability to convert single-ended inputs to differential outputs, makes the device an excellent choice for DAQs.

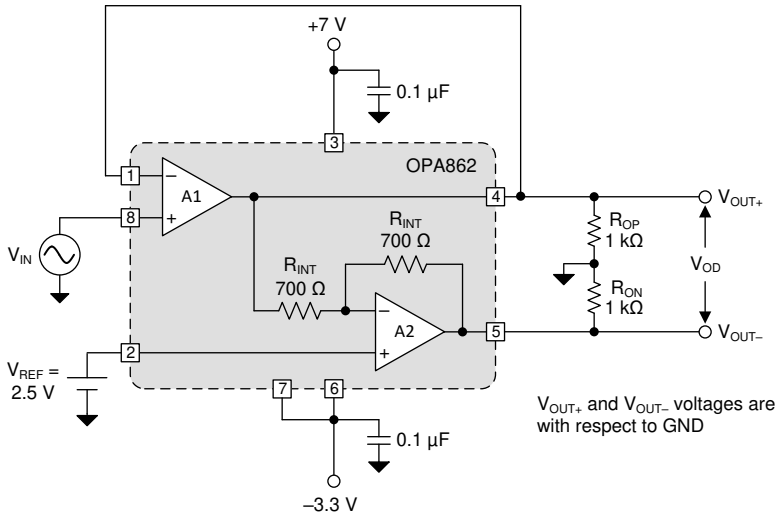


**Figure 8-2. Single-Ended to Differential, G = 2 V/V With 2.5-V $V_{OCM}$ Configuration**

#### *8.2.1.1 Design Requirements*

Use the design requirements shown in Table 8-1 to design a single-ended-to-differential output circuit block.

**Table 8-1. Design Requirements**

| DESIGN PARAMETER | VALUE |
|---|---|
| Input signal, $V_{IN}$ | 1-MHz, 0-5 V, sinusoidal signal |
| Output common-mode voltage, $V_{OCM}$ | 2.5 V |
| Differential gain, G | 2 V/V |
| Differential load | 2 kΩ |

#### *8.2.1.2 Detailed Design Procedure*

For $R_F$ = 0 Ω, with the VFB pin shorted to VOUT+, use Equation 3 to determine that the OPA862 is in a differential gain of 2 V/V configuration. Equation 4 describes how setting $V_{REF}$ equal to 2.5 V results in a $V_{OCM}$ of 2.5 V, as required per the design criteria. When designing a front-end stage with the OPA862, the input common-mode voltage and the output voltage range of the input and output pins, respectively, must be considered carefully. Choose the supplies such that none of these voltage ranges are violated and that the single-ended output voltages at each output do not exceed the maximum allowed voltages of the subsequent stage that the OPA862 is driving. Simulate the transfer characteristics of this circuit to ensure the output voltages are within the desired operation limits. Figure 8-3 illustrates the transfer characteristics for the OPA862 configuration in Figure 8-2. The output waveforms of the circuit in Figure 8-2 are described in Figure 8-4 and meets the design requirements of Table 8-1.

#### 8.2.1.3 Application Curves

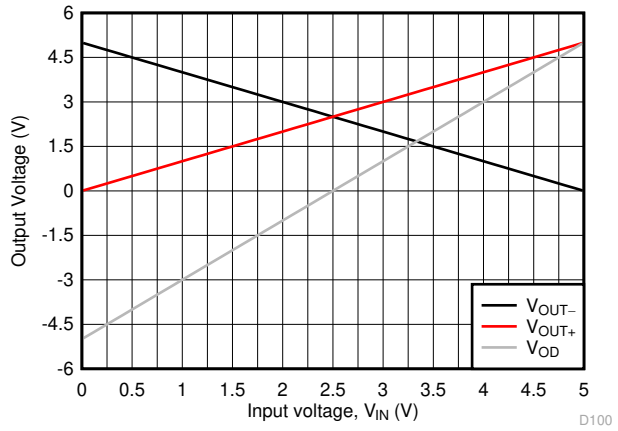


**Figure 8-3. DC Transfer Characteristics**

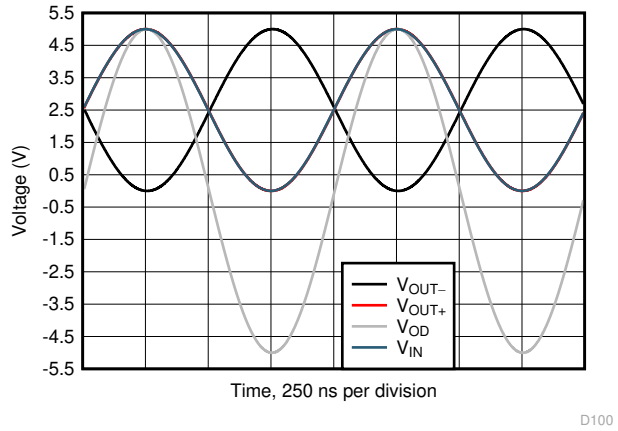


**Figure 8-4. Transient Output Response**

### 8.2.2 Transimpedance Amplifier Configuration

With recent advancements in light-sensing technology, transimpedance (TIA) applications are becoming popular, ranging in signal bandwidth needs from tens of kHz to hundreds of MHz. Because the current output of the photodiode in these TIA applications is unipolar, a key challenge in interfacing with the fully differential input analog-to-digital converters (ADCs) is maximizing the differential signal to the ADC in order to maximize the signal-to-noise ratio (SNR).

As illustrated in the output waveform of Figure 8-6, only half the differential output signal swing of the FDA is available. On the contrary, by using the OPA862 as the TIA stage, a single-device interface to the ADC can be designed that also allows the full differential swing to the ADC and set the desired output common-mode as shown in Figure 8-5. $V_{REF}$ is used to set the output common-mode voltage and $V_{DC}$ is used to DC shift the outputs such that for a zero photodiode current, $V_{OD}$ (equal to $V_{OUT+} - V_{OUT-}$) is at one of the peaks of the desired differential peak-to-peak swing. Whether the $V_{OD}$ peak at the zero photodiode current is at a high or low peak is determined by the direction of current through $R_F$ in the presence of the photodiode signal current.

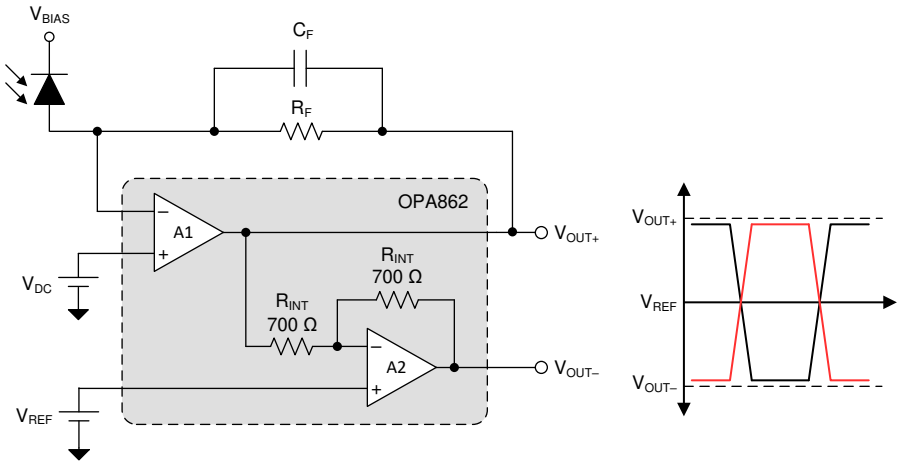


**Figure 8-5. Improved TIA Signal Chain With the OPA862**


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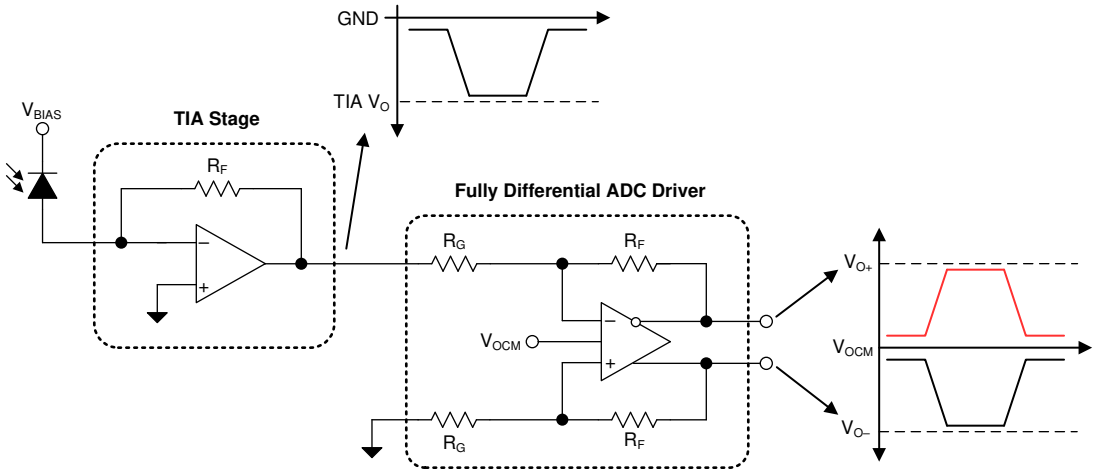


**Figure 8-6. Conventional TIA Signal Chain**

### *8.2.2.1 Design Requirements*

Use the design requirements shown in Table 8-2 to design the TIA circuit block.

**Table 8-2. Design Requirements**

| DESIGN PARAMETER | VALUE |
|---|---|
| Photodiode current, $I_{IN}$ | 0 mA to 5 mA |
| Photodiode Capacitance, $C_D$ | 50 pF |
| Signal bandwidth | 9 MHz |
| Output common-mode voltage, $V_{OCM}$ | 2.5 V |

### *8.2.2.2 Detailed Design Procedure*

In most TIA designs, selecting the right photodiode for the application is the most important decision because the photodiode determines the $I_{IN}$ and $C_D$ parameters that in turn determine the bandwidth required from the amplifier, the realizable TIA gain, and the signal bandwidth. Signal bandwidth also determines the rise time of the pulses. Choosing the photodiode with as low a capacitance as possible maximizes the TIA signal bandwidth for a given amplifier. Similarly, choosing a low TIA gain ($R_F$) allows for higher signal bandwidth but having a $R_F$ as high as possible maximizes the SNR of the signal chain.

In order to take advantage of the increased SNR by using the OPA862 as described in Figure 8-5, the amplifier is already chosen. Using the design methodology explained at *What You Need To Know About Transimpedance Amplifiers – Part 1* and the design parameters in Table 8-2, $R_F$ can be determined to be 1 kΩ and the required feedback capacitor, $C_F$, is 22 pF. Because the range of $I_{IN}$ is 0 mA to 5 mA and $R_F$ is 1 kΩ, the range of a single-ended output voltage at $V_{OUT+}$ is 0 V to 5 V ($I_{IN} \times R_F$). In the cathode bias configuration of the photodiode condition in Figure 8-7, when the photodiode is excited the current flows towards $V_{OUT+}$ through $R_F$, resulting in a voltage pulse that goes lower from the zero current value. Thus, setting $V_{OUT+}$ = 5 V and $V_{OUT-}$ = 0 V ($V_{OD}$ = +5 V) is desirable when the current is zero so that when the maximum current pulse of 5 mA occurs, $V_{OUT+}$ goes to 0 V and $V_{OUT-}$ reaches 5 V ($V_{OD}$ = –5 V). The $V_{OCM}$ target of 2.5 V, which is a typical mid-reference voltage for differential input ADCs, can be set by choosing $V_{REF} = V_{OCM}$. The values of $V_{DC}$ and $V_{REF}$ can be determined by setting the values of $V_{OUT+}$ and $V_{OUT-}$ to appropriate values at the zero photo-current in the following equations:

- $V_{DC} = V_{OUT+}$
- $V_{REF} = (V_{OUT-} + V_{DC}) / 2 = V_{OCM}$

Figure 8-8 and Figure 8-9 show the small-signal bandwidth and large-signal step response TINA simulation results of the circuit in Figure 8-7.

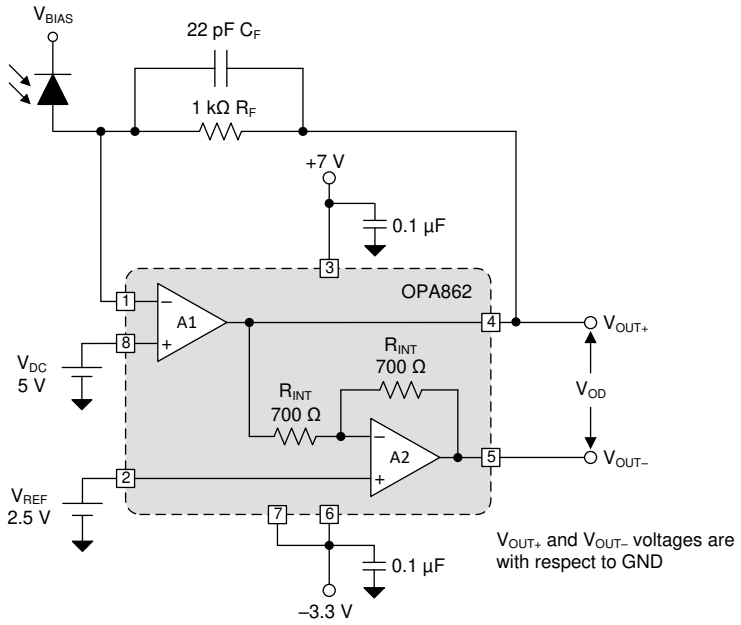


**Figure 8-7. TIA Circuit With the OPA862**

### *8.2.2.3 Application Curves*

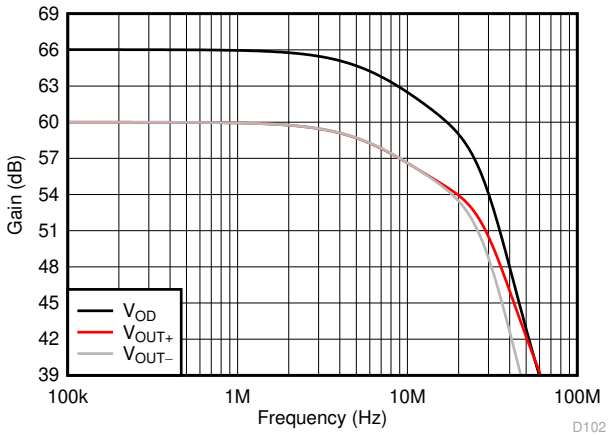


**Figure 8-8. Small-Signal Bandwidth**

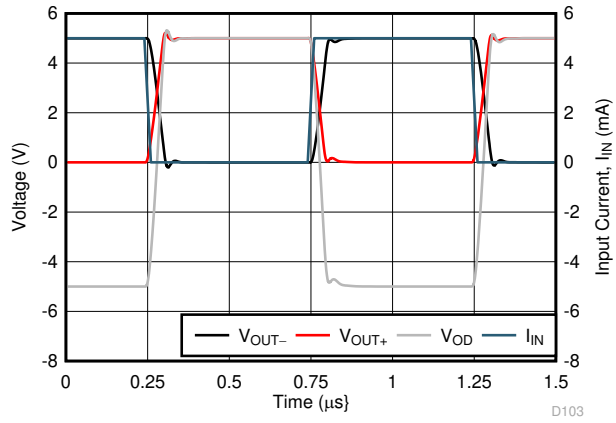


**Figure 8-9. Large-Signal Transient Response**


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### 8.2.3 DC Level-Shifting

Often, applications must level-shift a ground-referenced signal to a non-ground voltage. Configurations in Figure 8-10 and Figure 8-11 show two different ways of level-shifting a signal by using the OPA862 without having to use external resistors, saving board cost and space. These configurations leverage the fixed noninverting gain-of-2 configuration of A2 and the summing configuration of A1 to level-shift the signal at VOUT–. The internal resistors of the OPA862 are extremely well-matched to maintain the gain-of-2 accuracy of A2. Similarly matched external resistors can add significant cost to the system and often are more expensive than the amplifier itself.

Apart from the polarity of the $V_{DC}$-shift at the output, a key difference between the configurations of Figure 8-10 and Figure 8-11 is that in the case of Figure 8-10, $V_{DC}$ only must be capable of driving the $I_B$ of A1 but in the case of Figure 8-11, $V_{DC}$ must be capable of driving higher currents, as given by $I = V_{DC} / R_G$ when a noninverting input of A1 is grounded.

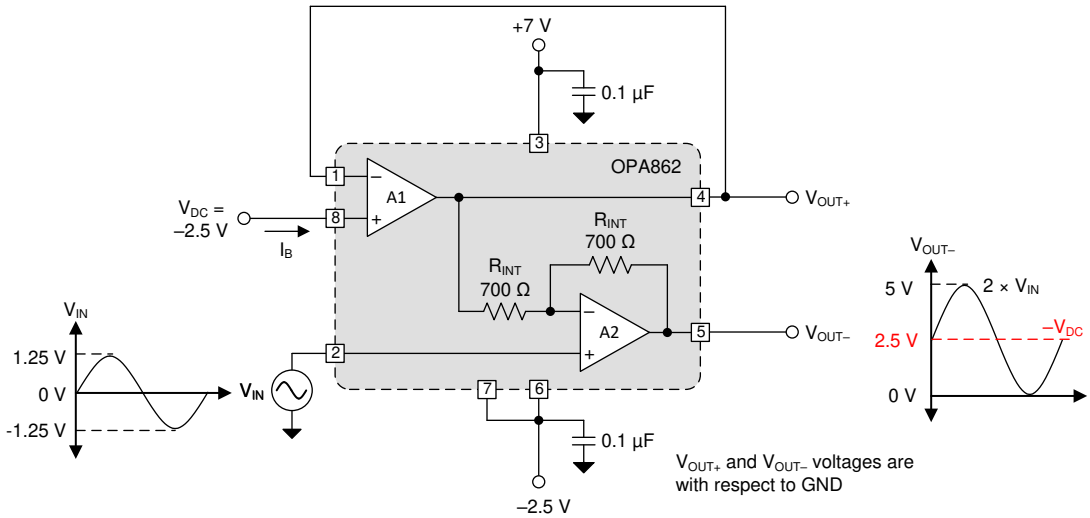


**Figure 8-10. Level-Shifting With a DC Source of Polarity Opposite to the Desired DC Shift**

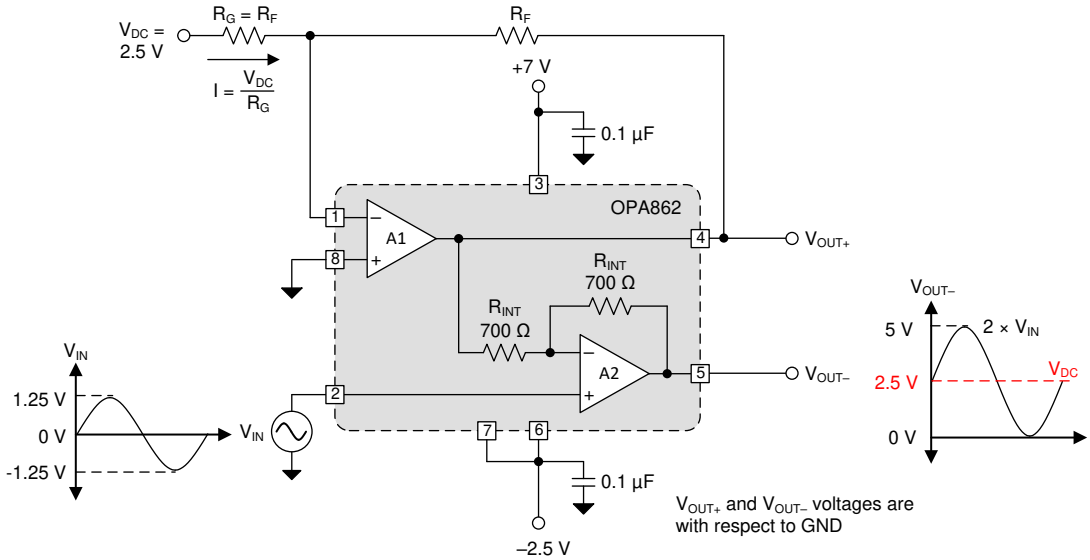


**Figure 8-11. Level-Shifting With a DC Source of Polarity Same as the Desired DC Shift**

# 9 Power Supply Recommendations

The OPA862 is intended to work in a supply range of 3 V to 12.6 V. The OPA862 can be used in single-supply operation, or in a balanced or unbalanced split-supply operation. Good power-supply bypassing is recommended for best AC performance and distortion in particular. Minimize the distance (less than 0.1 inch) from the power-supply pins to high-frequency, 0.1-µF decoupling capacitors. A larger capacitor (2.2 µF or 10 µF is typical) is used with a high-frequency, 0.1-µF supply decoupling capacitor at the device supply pins. For single-supply operation, only the positive supply has these capacitors. When a split-supply is used, use these capacitors for each supply to ground. If necessary, place the larger capacitors further from the device and share these capacitors among several devices in the same area of the printed circuit board (PCB). Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. An optional 0.1-µF supply decoupling capacitor across the two power supplies (for bipolar operation) reduces second-order harmonic distortion.

# 10 Layout

## 10.1 Layout Guidelines

Achieving optimum AC performance with a fast amplifier such as the OPA862 requires careful attention to board layout parasitics and external component types. The OPA862EVM can be used as a reference when designing the circuit board. Recommendations that optimize performance include:

1. **Minimize parasitic capacitance** to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and input pins can cause instability. On the noninverting input, VIN, the device can react with the source impedance to cause unintentional band limiting. To reduce unwanted capacitance, open a plane cutout around the signal I/O pins in the ground and power planes below those pins. Otherwise, ground and power planes must be unbroken elsewhere on the board.
2. **Minimize the distance** (< 0.1") from the power-supply pins to high-frequency, 0.01-µF or 0.1-µF decoupling capacitors. At the device pins, do not allow the ground and power plane layout to be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections must always be decoupled with these capacitors. Larger (2.2-µF to 10-µF) decoupling capacitors, effective at lower frequencies, must also be used on the supply pins. These capacitors can be placed somewhat farther from the device and shared among several devices in the same area of the PC board.
3. **Careful selection and placement of external components preserve the AC performance of the OPA862.** Resistors must be a low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film and carbon composition axially leaded resistors can also provide good high frequency performance. Again, keep their leads and PCB trace length as short as possible. Because the VOUT+ pin and the VFB pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the VFB and VOUT+ pins, respectively.
4. **Connections to other wideband devices** on the board can be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 mils to 100 mils) must be used, preferably with ground and power planes opened up around them.
5. **Socketing a high-speed part such as the OPA862 is not recommended.** The additional lead length and pin-to-pin capacitance introduced by the socket can create troublesome parasitic network that can make achieving a smooth, stable frequency response difficult. Best results are obtained by soldering the OPA862 to the board.


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## 10.2 Layout Examples

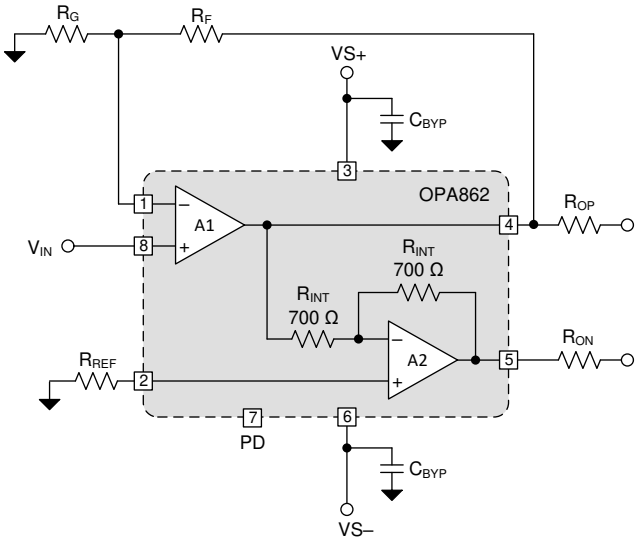


**Figure 10-1. Representative Schematic for Layout in**

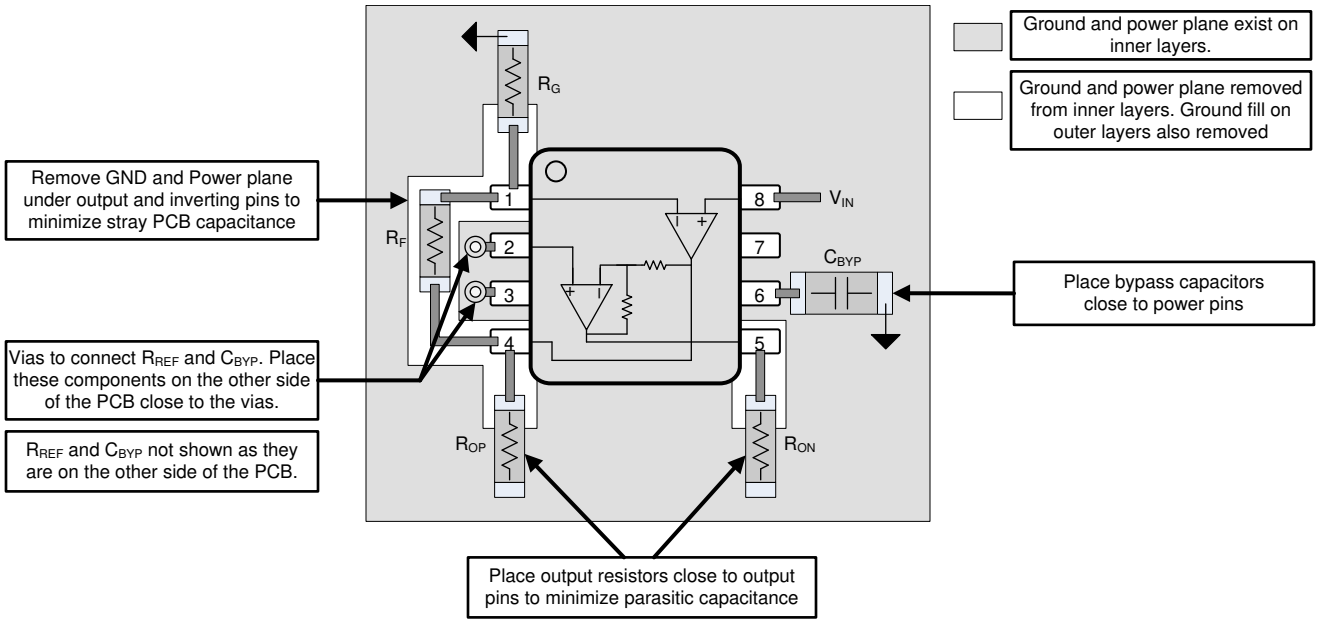


**Figure 10-2. Layout Recommendations**

# 11 Device and Documentation Support

## 11.1 Documentation Support

### 11.1.1 Related Documentation

For related documentation see the following:

Texas Instruments, *Single-Supply Op Amp Design Techniques* application report

## 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| OPA862IDR | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 862 |
| OPA862IDR.B | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 862 |
| OPA862IDT | Active | Production | SOIC (D) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 862 |
| OPA862IDT.B | Active | Production | SOIC (D) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 862 |
| OPA862IDTKR | Active | Production | WSON (DTK) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 862 |
| OPA862IDTKR.B | Active | Production | WSON (DTK) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 862 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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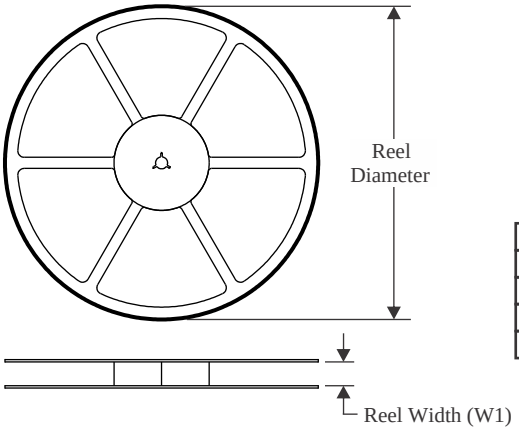
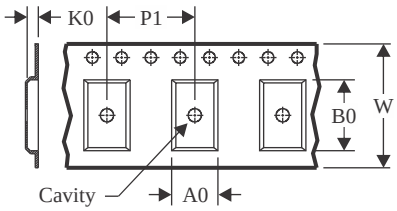
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

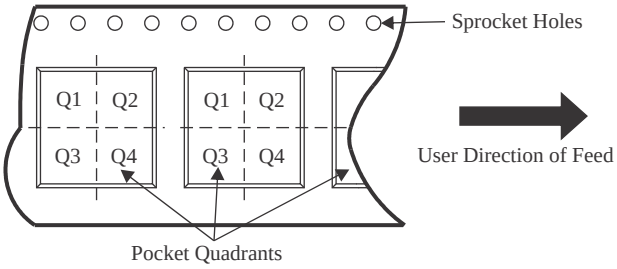



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

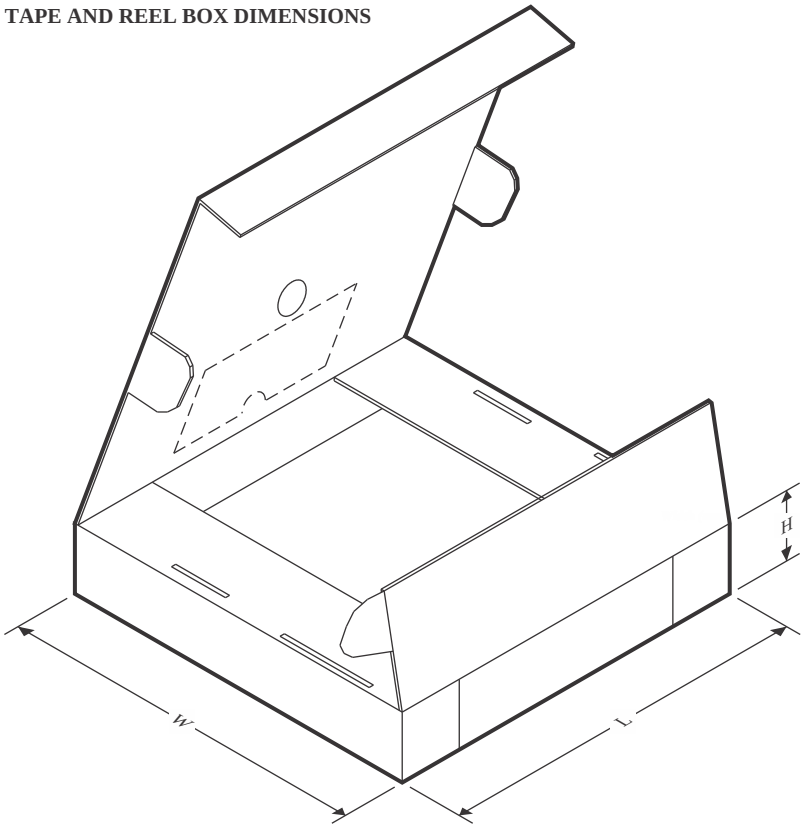
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

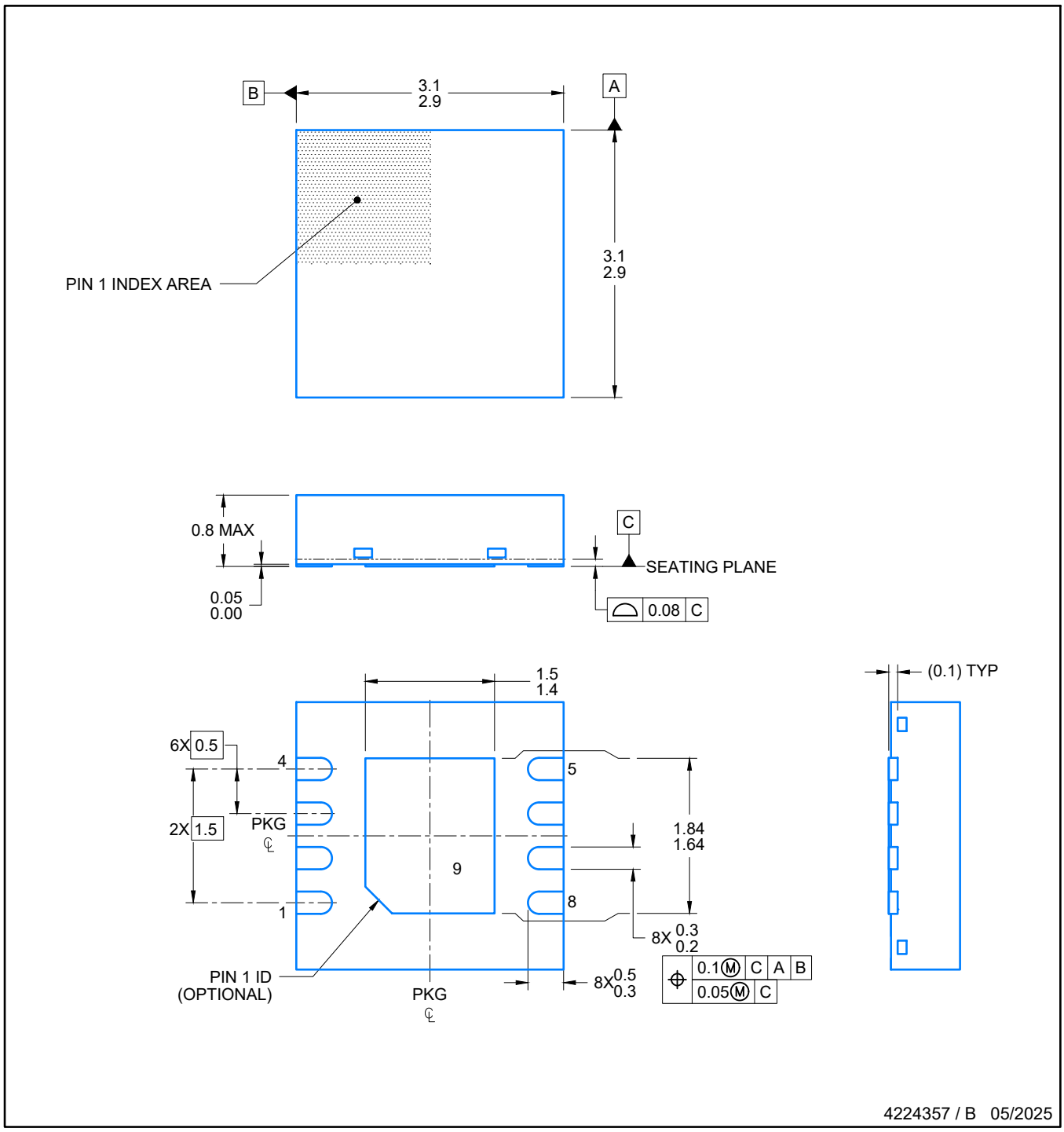
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA862IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| OPA862IDT | SOIC | D | 8 | 250 | 180.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| OPA862IDTKR | WSON | DTK | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS



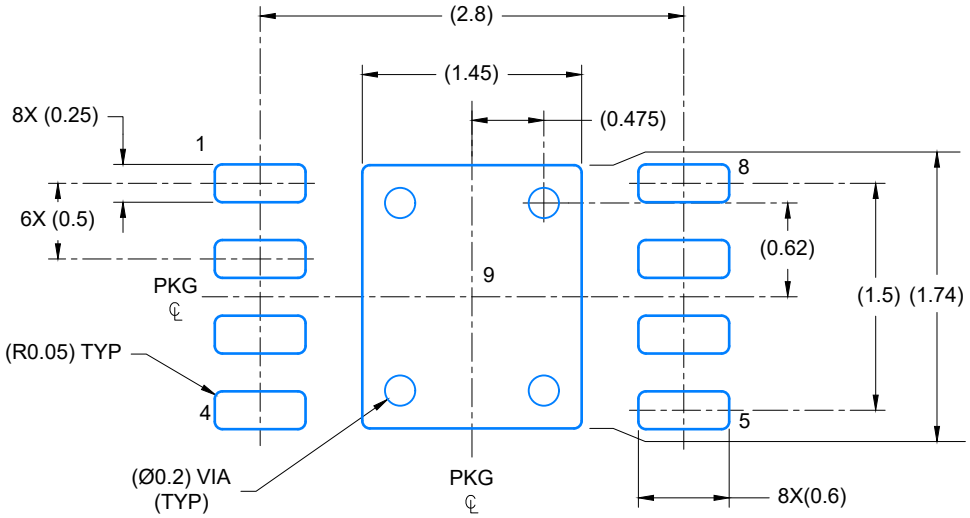

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| OPA862IDR | SOIC | D | 8 | 2500 | 356.0 | 356.0 | 35.0 |
| OPA862IDT | SOIC | D | 8 | 250 | 210.0 | 185.0 | 35.0 |
| OPA862IDTKR | WSON | DTK | 8 | 3000 | 367.0 | 367.0 | 35.0 |

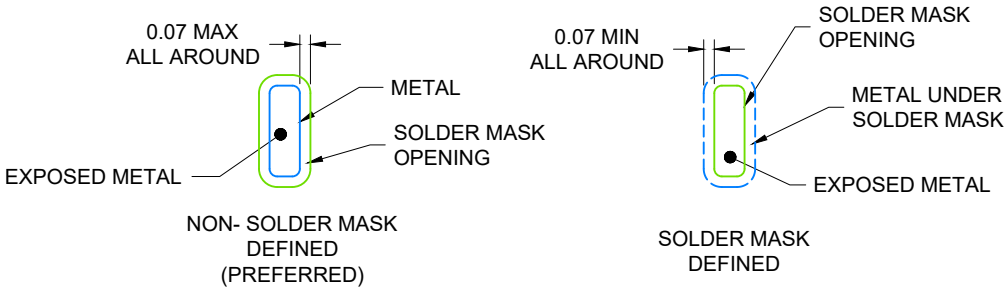



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

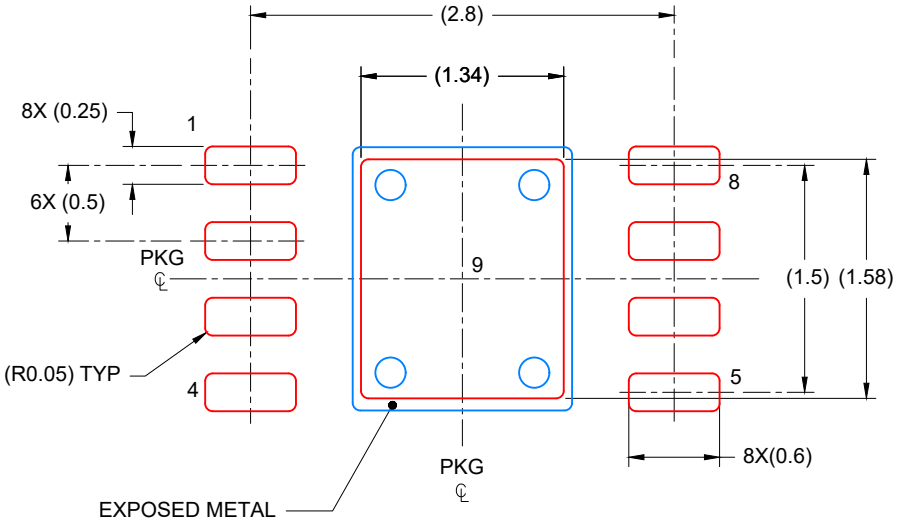



SOLDER MASK DETAILS

4224357 / B 05/2025

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



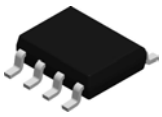

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 9: 84%
SCALE: 20X

4224357 / B 05/2025

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

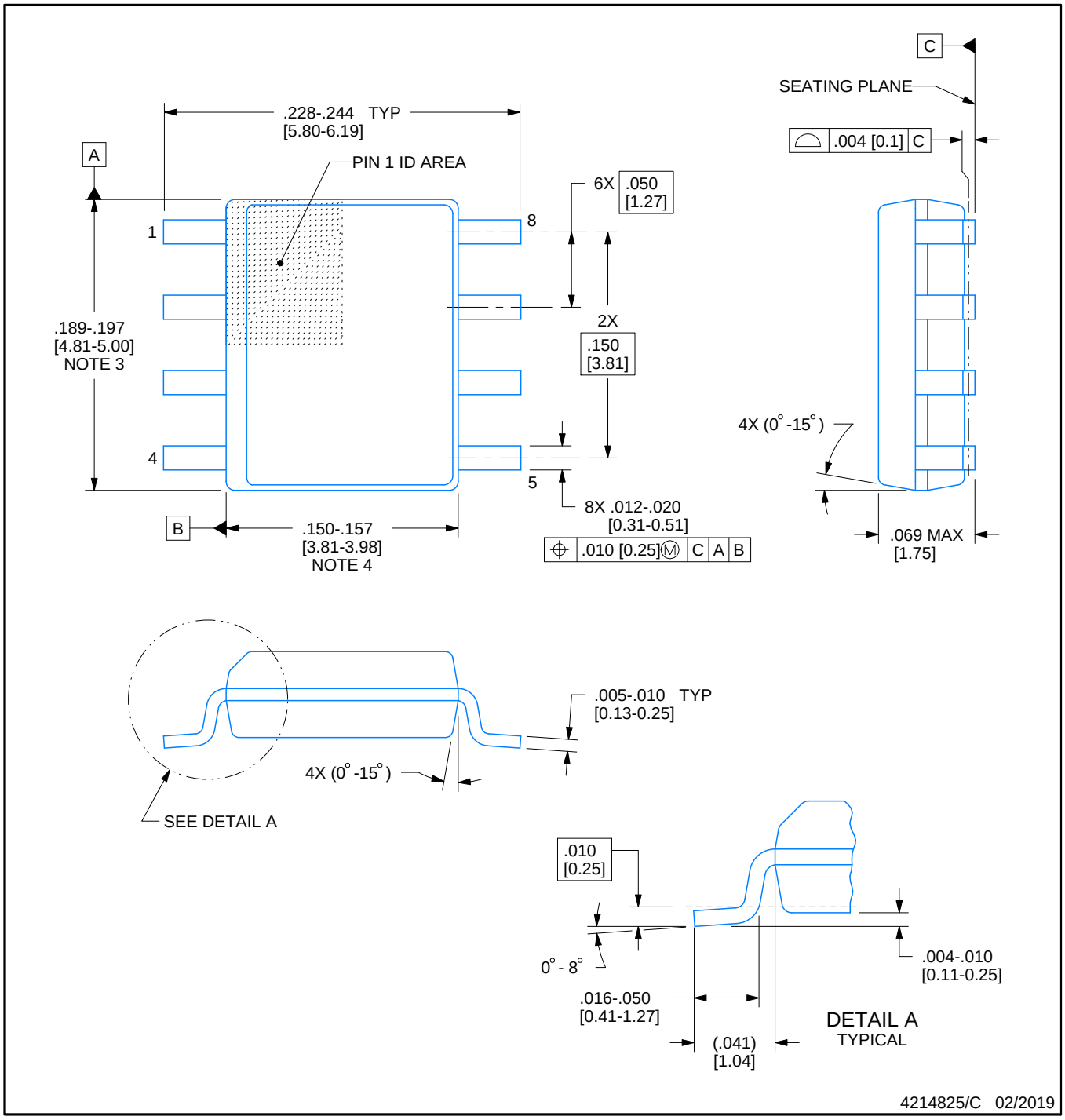


# PACKAGE OUTLINE

## D0008A

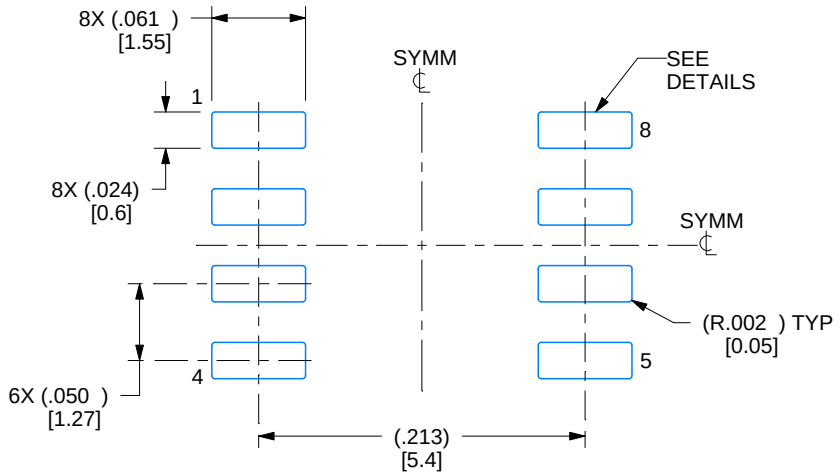
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

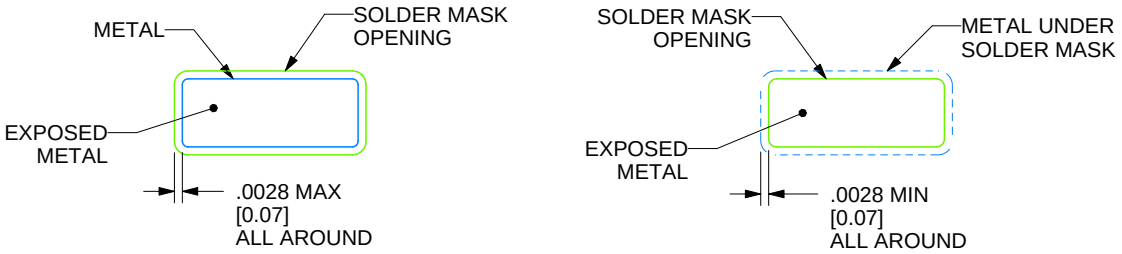



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

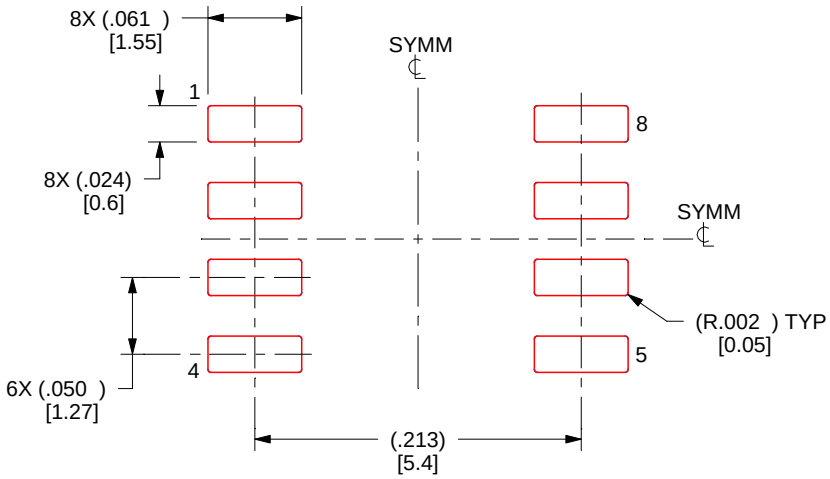



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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