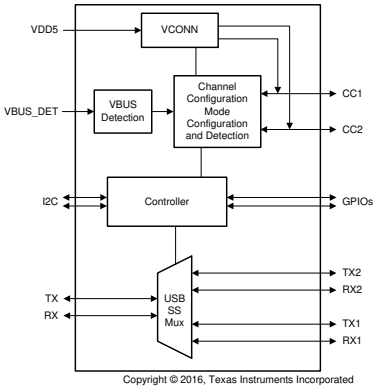
HD3SS3220 USB Type-C DRP Port Controller with SuperSpeed 2:1 MUX

1 Features

- USB Type-C Port Controller with Integrated 2:1 SuperSpeed Mux
- Compatible to USB Type-C™ Specifications
- Supports USB 3.1 G1 and G2 up to 10 Gbps
- Supports up to 15 W of Power Delivery with 3-A Current Advertisement and Detection
- Mode Configuration
  - Host Only – DFP/Source
  - Device Only – UFP/Sink
  - Dual Role Port - DRP
- Channel Configuration (CC)
  - Attach of USB Port Detection
  - Cable Orientation Detection
  - Role Detection
  - Type-C Current Mode (Default, Mid, High)
- $V_{(BUS)}$ Detection and VCONN Support for Active Cables
- Audio and Debug Accessory Support
- Supports for Try.SRC and Try.SNK DRP Modes
- Configuration Control through GPIO and I^2C
- Low Active and Standby Current Consumptions
- Industrial Temperature Range of –40 to 85°C

2 Applications

- USB Host, Device, Hub
- Mobile Phones, Tablets and Notebooks
- USB Peripherals such as Thumb Drives, Portable Hard Disks, Set Top Box



Simplified Schematic

3 Description

HD3SS3220 is a USB SuperSpeed (SS) 2:1 mux with DRP port controller. The device provides Channel Configuration (CC) logic and 5V VCONN sourcing for ecosystems implementing USB Type-C. The HD3SS3220 can be configured as a Downstream Facing Port (DFP), Upstream Facing Port (UFP) or a Dual Role Port (DRP) making it ideal for any application.

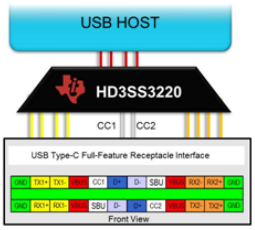
The HD3SS3220, in DRP mode, alternates presenting itself as a DFP or UFP according to the Type-C specifications. The CC logic block monitors the CC1 and CC2 pins for pull-up or pull-down resistances to determine when a USB port has been attached and its port role. Once a USB port has been attached, the CC logic also determines the orientation of the cable and configures the USB SS mux accordingly. Finally, CC logic advertises or detects Type-C current mode – Default, Mid, or High in DFP and UFP modes respectively.

Excellent dynamic characteristics of the integrated mux allow switching with minimum attenuation to the SS signal eye diagram and very little added jitter. The device's switch paths deploy adaptive common mode voltage tracking resulting identical channel despite different common mode voltage for RX and TX channels.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
HD3SS3220	VQFN RNH (30)	2.50 mm x 4.50 mm
HD3SS3220I		

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision C (May 2017) to Revision D (September 2020) — **Page**

- Changed VDD to VDD5....3
- In Control Pins row of *Absolute Maximum Ratings*, DIR was in both VDD5 and VCC33. Removed DIR from VDD5....5
- Deleted $C_{(bus,I2c)}$ from the *Recommended Operating Conditions* table....5
- From: When using 3.3 V for I^2C, customer must ensure VDD is above 3 V at all times. To: When using 3.3 V for I^2C, customer must ensure VDD5 is above 3 V at all times....6
- Changed the "I2C (SDA, SCL)" section of the *Timing Requirements* table....8
- Added t_{ENnCC_HI} parameter in section of the *Timing Requirements* table....8
- Added t_{VDD5V_PG} parameter in section of the *Timing Requirements* table....8
- Added note in section *DFP/Source – Downstream Facing Port* that ID pin will remain high until VBUS is at VSafe0V....14
- From: When a voltage level within the proper threshold is detected on CC1, the DIR pin is pulled low. To: When a voltage level within the proper threshold is detected on CC1, the DIR pin is high....15
- From: When a voltage level within the proper threshold is detected on CC2, the DIR pin is high. To: When a voltage level within the proper threshold is detected on CC2, the DIR pin is pulled low....15
- From: HD3SS3220 supports audio and debug accessories in UFP, DFP and DRP mode. To: HD3SS3220 supports audio and debug accessories in UFP, DFP and DRP mode by default....16
- Added note that UFP accessory support can be disabled by setting DISABLE_UFP_ACCESSORY register....16
- Added section on VDD5 and VCC33 power-on requirements....17
- Removed the Note about non-failsafe pins from *Dead Battery* section as this information is in the *VDD5 and VCC33 Power-On Requirements* section....19

Changes from Revision B (September 2016) to Revision C (May 2017) — **Page**

- Added R_{VBUS} values: MIN = 855, TYP = 887, MAX = 920 KΩ....6

Changes from Revision A (August 2016) to Revision B (September 2016) — **Page**

- Changed pins CC1 and CC2 values From: MIN = –0.3 MAX = VDD5 +0.3 To: MIN –0.3 MAX = 6 in the *Absolute Maximum Ratings*....5

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Changes from Revision * (December 2016) to Revision A (August 2016) **Page**

- *Absolute Maximum Ratings*, Deleted "ENn_MUX" from the Control Pins..... 5
- *ESD Ratings*, Deleted text "Pins listed as ±XXX V may actually have higher performance." from Note 1.....5
- *Recommended Operating Conditions*, Added "VDD5 supply ramp time" 5
- *Recommended Operating Conditions*, Changed "External resistor on VBUS_DET pin" MIN value From: 890 KΩ To: 880 KΩ.....5
- Switch the position of CC1 and CC2 in Figure 8-1 26
- Switch the position of CC1 and CC2 in Figure 8-2 28
- Switch the position of CC1 and CC2 in Figure 8-3 30

5 Pin Configuration and Functions

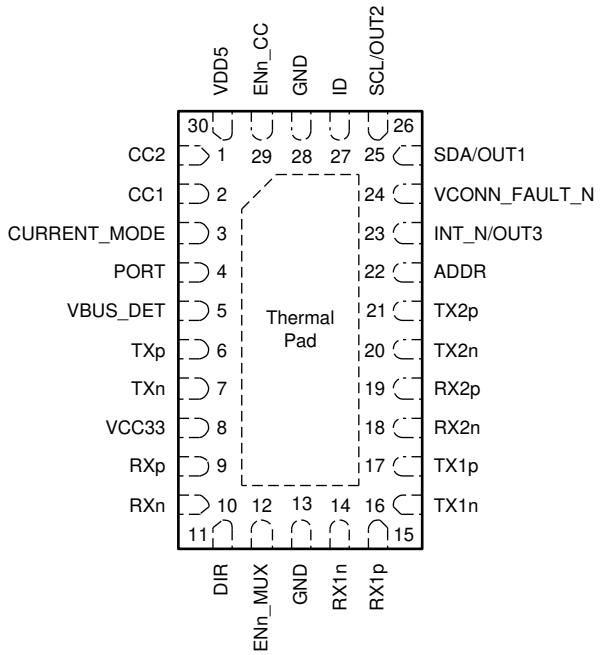

Figure 5-1. RNH Package 30 Pin (VQFN) Top View

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CC2	1	I/O	Type-C Configuration channel signal 2
CC1	2	I/O	Type-C Configuration channel signal 1
CURRENT_MODE	3	I	Tri-level input pin to indicate current advertisement in DFP (or DFP in DRP) mode while in GPIO mode. Don't care in UFP mode. Provides the flexibility to advertise higher current without I^2C. The pin has 250 K internal pull-down. L – Low - Default – 900 mA M - Medium (Install 500 K to VDD5 on the PCB) – 1.5 A H - High (Install 10 K to VDD5 on the PCB) – 3 A
PORT	4	I	Tri-level input pin to indicate port mode. The state of this pin is sampled when HD3SS3220's ENn_CC is asserted low, and VDD5 is active. This pin is also sampled following a I2C_SOFT_RESET. H - DFP (Pull-up to VDD5 if DFP mode is desired) NC - DRP (Leave unconnected if DRP mode is desired) L - UFP (Pull-down or tie to GND if UFP mode is desired)
VBUS_DET	5	I	5-28V VBUS input voltage. VBUS detection determines UFP attachment. One 900K external resistor required between system VBUS and VBUS_DET pin.
TXp	6	I/O	Host/Device USB SuperSpeed differential Signal TX positive
TXn	7	I/O	Host/Device USB SuperSpeed differential Signal TX negative

PIN		I/O	DESCRIPTION
NAME	NO.		
VCC33	8	P	3.3-V Power supply
RXp	9	I/O	Host/Device USB SuperSpeed differential Signal RX positive
RXn	10	I/O	Host/Device USB SuperSpeed differential Signal RX negative
DIR	11	O	Type-C plug orientation. Open drain output. A pull-up resistor (that is, 200 K) must be installed for proper operation of the device.
ENn_MUX	12	I	Active Low MUX Enable: L - Normal operation, and H - Shutdown.
GND	13, 28	G	Ground
RX1n	14	I/O	Type-C Port - USB SuperSpeed differential Signal RX1 negative
RX1p	15	I/O	Type-C Port - USB SuperSpeed differential Signal RX1 positive
TX1n	16	I/O	Type-C Port - USB SuperSpeed differential Signal TX1 negative
TX1p	17	I/O	Type-C Port - USB SuperSpeed differential Signal TX1 positive
RX2n	18	I/O	Type-C Port - USB SuperSpeed differential Signal RX2 negative
RX2p	19	I/O	Type-C Port - USB SuperSpeed differential Signal RX2 positive
TX2n	20	I/O	Type-C Port - USB SuperSpeed differential Signal TX2 negative
TX2p	21	I/O	Type-C Port - USB SuperSpeed differential Signal TX2 positive
ADDR	22	I	Tri-level input pin to indicate I^2C address or GPIO mode: H (connect to VDD5) - I^2C is enabled and I2C 7-bit address is 0x67. NC - GPIO mode (I2C is disabled) L (connect to GND) - I^2C is enabled and I2C 7-bit address is 0x47. ADDR pin should be pulled up to VDD5 if high configuration is desired
INT_N/OUT3	23	O	The INT_N/OUT3 is a dual-function pin. When used as the INT_N, the pin is an open drain output in I^2C control mode and is an active low interrupt signal for indicating changes in I^2C registers. When used as OUT3, the pin is in audio accessory detect in GPIO mode: H - no detection, and L - audio accessory connection detected.
VCONN_FAULT_N	24	O	Open drain output. Asserted low when VCONN overcurrent detected.
SDA/OUT1	25	I/O	The SDA/OUT1 is a dual-function pin. When I2C is enabled (ADDR pin is high or low), this pin is the I^2C communication data signal. When in GPIO mode (ADDR pin is NC), this pin is an open drain output for communicating Type-C current mode detect when the device is in UFP mode: H – Default (900 mA) current mode detected, and L – Medium (1.5 A) or High (3 A) Current Mode detected.
SCL/OUT2	26	I/O	The SCL/OUT2 is a dual function pin. When I^2C is enabled (ADDR pin is high or low), this pin is the I^2C communication clock signal. When in GPIO mode (ADDR pin is NC), this pin is an open drain output for communicating Type-C current mode detect when the device is in UFP mode: H – Default or Medium current mode detected, and L – High current mode detected.
ID	27	O	Open drain output. Asserted low when CC pin detected device attachment when port is a source (DFP), or dual-role (DRP) acting as source (DFP).
ENn_CC	29	I	Enable signal for CC controller. Enable is active low.
VDD5	30	P	5-V Power supply
Thermal Pad	–	–	The thermal PAD must be connected to GND, see the Thermal Pad connection techniques (SLMA002).

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
5-V Supply Voltage	VDD5	–0.3	6	V
3.3-V Supply Voltage	VCC33	–0.3	4	V
Control Pins	ADDR, PORT, ID, INT_N/OUT3, ENn_CC, SDA/OUT1, SCL/OUT2	–0.3	VDD5 +0.3	V
	CC1, CC2	–0.3	6	V
	ENn_MUX, DIR	–0.3	VCC33 +0.3	V
	VBUS_DET	–0.3	4	V
Super-speed Differential Signal Pins	[RX/TX] [p/n], [RX/TX][2/1][p/n]	–0.3	2.5	V
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process..

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD5}	5-V Supply Voltage range	4.5[1]		5.5	V
V_{CC33}	3.3-V Supply Voltage range	3		3.6	V
V_{DD}	Supply range for I2C (SDA, SCL) pins	1.65		3.6	V
$V_{DD5(ramp)}$	VDD5 supply ramp time			25	ms
$V_{(diff)}$	High speed signal pins differential voltage	0		1.8	V_{PP}
$V_{(cm)}$	High speed signal pins common mode voltage	0		2	V
T_A	Operating free-air/ambient temperature (HD3SS3220)	0		70	°C
T_A	Operating free-air/ambient temperature (HD3SS3220I)	–40		85	°C
$V_{(BUS)}$	System $V_{(BUS)}$ input voltage through 900-K resistor	4	5	28	V
$C_{(BULK)}$	Bulk capacitance on VCONN. Only when VCONN is on. Disconnected when VCONN is off. Shall be placed on VDD5.	10		200	µF
$R_{(p_ODext)}$	External Pull up resistor on Open Drain IOs (OUT1, OUT2, INT/OUT3, ID, VCONN_FAULT_N, and DIR pins)		200		KΩ
$R_{(p_TLext)}$	Tri-level input external pull-up resistor (PORT and ADDR pins)		4.7		KΩ
$R_{(p_15A)}$	External pull up resistor to advertise 1.5 A (CURRENT_MODE pin)		500		KΩ
$R_{(p_3A)}$	External pull up resistor to advertise 3 A (CURRENT_MODE pin)		10		KΩ
$R_{(p_i2c_ext)}$	External Pull up resistance on I^2C bus (Could be 4.7 K or higher. Nominal value listed)		2.2		KΩ

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$R_{(VBUS)}$	External resistor on VBUS_DET pin	880	900	910	KΩ

(1) With 200 mA VCONN current for VCONN ≥ 4.75 V at connector, VDD5 ≥ 5 V is recommended

6.4 Thermal Information

THERMAL METRIC[1]		HD3SS3220 RNH (VQFN) 30 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	12.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Consumption						
$I_{(ACTIVE)}$	Current consumption in active mode- both CC controller and SS mux on	ENn_CC/Mux = L		0.7	0.9	mA
I_{CC}	Current consumption in active mode – CC controller on and SS mux off	ENn_CC = L, ENn_Mux = H		0.2		mA
$I_{(SHUTDOWN)}$	Current consumption in shutdown mode	ENn_CC/Mux = H		5		µA
CC PINS						
$R_{(CC_DB)}$	Pulldown resistor when in dead-battery mode.		4.1	5.1	6.1	kΩ
$R_{(CC_D)}$	Pulldown resistor when in UFP or DRP mode.		4.6	5.1	5.6	kΩ
$V_{(UFP_CC_USB)}$	Voltage level for detecting a DFP attach when configured as a UFP and DFP is advertising default current source capability.		0.25		0.61	V
$V_{(UFP_CC_MED)}$	Voltage level for detecting a DFP attach when configured as a UFP and DFP is advertising medium (1.5 A) current source capability.		0.7		1.16	V
$V_{(UFP_CC_HIGH)}$	Voltage level for detecting a DFP attach when configured as a UFP and DFP is advertising high (3 A) current source capability.		1.31		2.04	V
$V_{(DFP_CC_USB)}$	Voltage level for detecting a UFP attach when configured as a DFP and advertising default current source capability.		1.51	1.6	1.64	V
$V_{(DFP_CC_MED)}$	Voltage level for detecting a UFP attach when configured as a DFP and advertising 1.5-A current source capability.		1.51	1.6	1.64	V
$V_{(DFP_CC_HIGH)}$	Voltage level for detecting a UFP attach when configured as a DFP and advertising 3-A current source capability.		2.46	2.6	2.74	V
$V_{(AC_CC_USB)}$	Voltage level for detecting an active cable attach when configured as a DFP and advertising default current source capability.		0.15	0.2	0.25	V
$V_{(AC_CC_MED)}$	Voltage level for detecting an active cable attach when configured as a DFP and advertising 1.5-A current source capability.		0.35	0.4	0.45	V
$V_{(DFP_CC_HIGH)}$	Voltage level for detecting an active cable attach when configured as a DFP and advertising 3-A current source capability.		0.75	0.8	0.84	V

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over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CC(DEFAULT_P)}$	Default mode pull-up current source when operating in DFP or DRP mode.		64	80	96	µA
$I_{CC(MED_P)}$	Medium (1.5 A) mode pull-up current source when operating in DFP or DRP mode.		166	180	194	µA
$I_{CC(HIGH_P)}$	High (3 A) mode pull-up current source when operating in DFP or DRP mode.		34	330	356	µA
3-Level Input Pins: PORT, ADDR, ENn_CC and CURRENT_MODE						
V_{IL}	Low-level input voltage				0.4	V
V_M	Mid-Level (Floating) voltage (PORT, ADDR and CURRENT_MODE pins)		0.28 x VDD5		0.56 x VDD5	V
V_{IH}	High-level input voltage		VDD5 - 0.3		VDD5	V
I_{IH}	High-level input current		20		20	µA
I_{IL}	Low-level input current		–10		10	µA
$I_{ID(LKG)}$	Current Leakage on ID pin	VDD5 = 0 V, ID = 5 V			10	µA
$R_{(pu)}$	Internal pull-up resistance (PORT and ADDR pins)			588		kΩ
$R_{(pd)}$	Internal pull-down resistance (PORT and ADDR pins)			1.1		MΩ
$R_{(pd_CURRENT)}$	Internal pull-down resistance (CURRENT_MODE pin)			275		kΩ
$R_{(ENn_CC)}$	Internal pull-up resistance (ENn_CC pin)			1.1		MΩ
Input Pins: ENn_MUX						
V_{IL}	Low-level input voltage				0.3 x VCC33	V
V_{IH}	High-level input voltage		0.7 x VCC33			V
I_{IH}	High-level input current		–1		1	µA
I_{IL}	Low-level input current		–1		1	µA
Open Drain Output Pins: OUT1, OUT2, INT_N/OUT3, ID, VCONN_FAULT_N, DIR						
V_{OL}	Low-level signal output voltage	I_{OL} = –1.6 mA			0.4	V
I2C– SDA/OUT1, SCL/OUT2 can Operate from 1.8/3.3 V (±10%)(1)						
V_{IH}	High-level input voltage		1.05			V
V_{IL}	Low-level input voltage				0.4	V
V_{OL}	Low-level output voltage (open-drain)	I_{OL} = –1.6 mA			0.4	V
VBUS_DET IO Pin (Connected to System VBUS Signal)						
$V_{(BUS_THR)}$	VBUS threshold range		2.95	3.3	3.8	V
R_{VBUS}	External resistor between V_{BUS} and VBUS_DET pin		855	887	920	KΩ
$R_{(VBUS_DET_INT)}$	Internal pull-down resistor at VBUS_DET pin			95		kΩ
VCONN						
R_{ON}	On resistance of the VCONN power FET				1.25	Ω
$V_{(TOL)}$	Voltage tolerance on VCONN power FET				5.5	V
$V_{(pass)}$	Voltage to pass through VCONN power FET				5.5	V
$I_{(VCONN)}$	VCONN current limit. VCONN will be disconnected above this value		225	300	375	mA
MUX High Speed Performance Parameters						
I_L	Differential Insertion Loss	f = 0.3 Mhz		–0.43		dB
		f = 2.5 Ghz		–1.07		
		f = 5 Ghz		–1.42		
BW	Bandwidth			8		Ghz
R_L	Differential return loss	f = 0.3 Mhz		–27		dB
		f = 2.5 Ghz		–9		
		f = 5 Ghz		–9		

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
O_{IRR}	Differential OFF isolation	f = 0.3 Mhz		–79		dB
		f = 2.5 Ghz		–23		
		f = 5 Ghz		–20		
X_{TALK}	Differential Cross Talk	f = 0.3 Mhz		–89		dB
		f = 2.5 Ghz		–34		
		f = 5 Ghz		–30		
R_{ON}	On resistance				8	Ω

(1) When using 3.3 V for I^2C, customer must ensure VDD5 is above 3 V at all times.

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
I2C (SDA, SCL)					
$t_{SU:DAT}$	Data setup time	100			ns
$t_{HD:DAT}$	Data setup time	10			ns
$t_{SU;STA}$	Set-up time, SCL to start condition	0.6			µs
$t_{HD,STA}$	Hold time,(repeated) start condition to SCL	0.6			µs
$t_{SU:STO}$	Set up time for STOP condition	0.6			µs
$t_{VD;DAT}$	Data valid time			0.9	µs
$t_{VD;ACK}$	Data valid acknowledge time			0.9	µs
t_{BUF}	Bus free time between a STOP and START condition	1.3			µs
f_{SCL}	SCL clock frequency; I^2C mode for local I^2C control			400	ns
t_r	Rise time of both SDA and SCL signals			300	ns
t_f	Fall time of both SDA and SCL signals			300	ns
C_{BUS_100KHZ}	Total capacitive load for each bus line when operating at ≤ 100 KHz			400	pF
C_{BUS_400KHZ}	Total capacitive load for each bus line when operating at 400 KHz.			100	pF
SS MUX					
t_{PD}	Switch propagation delay See Figure 6-3			80	ps
t_{SW_ON}	Switching time DIR-to-Switch ON See Figure 6-2			0.5	µs
t_{SW_OFF}	Switching time DIR-to-Switch OFF See Figure 6-2			0.5	µs
t_{SK_INTRA}	Intra-pair output skew See Figure 6-3			5	ps
t_{SK_INTER}	Inter-pair output skew See Figure 6-3			20	ps
Power-On Timings					
t_{ENnCC_HI}	ENn_CC high after both VDD5 and VCC33 supplies are stable. Refer to Figure 7-3.	2			ms
t_{VDD5V_PG}	VDD5 stable before VCC33. Refer to Figure 7-2.	2			ms

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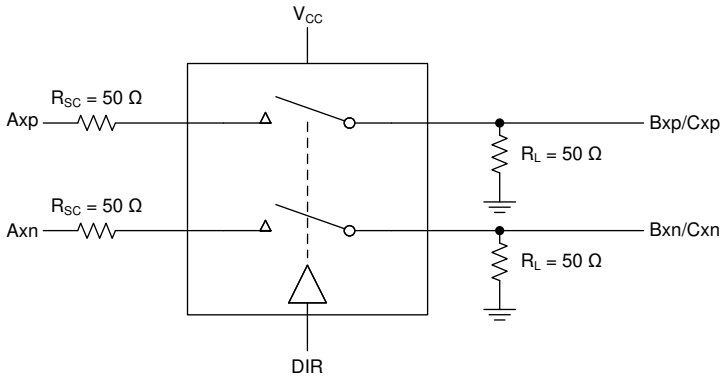

Figure 6-1. Test Setup

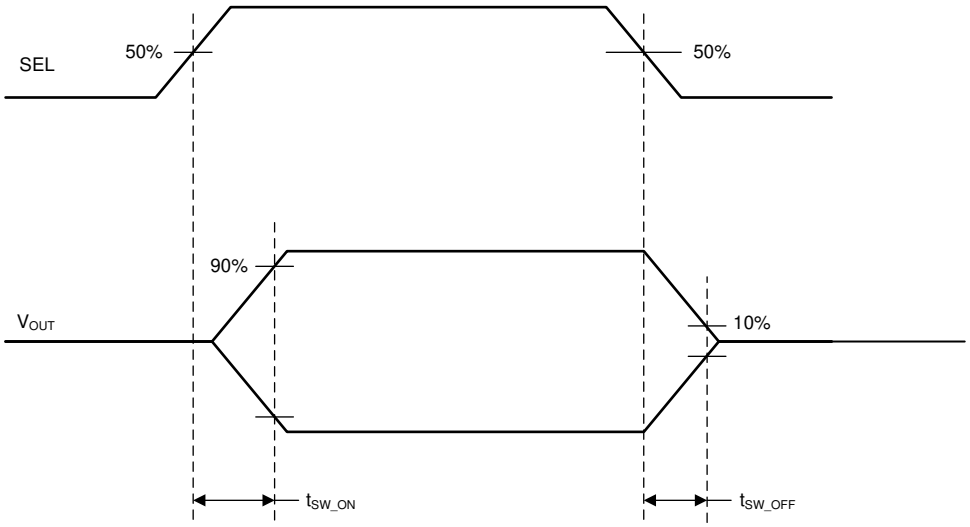

Figure 6-2. Switch On and Off Timing Diagram

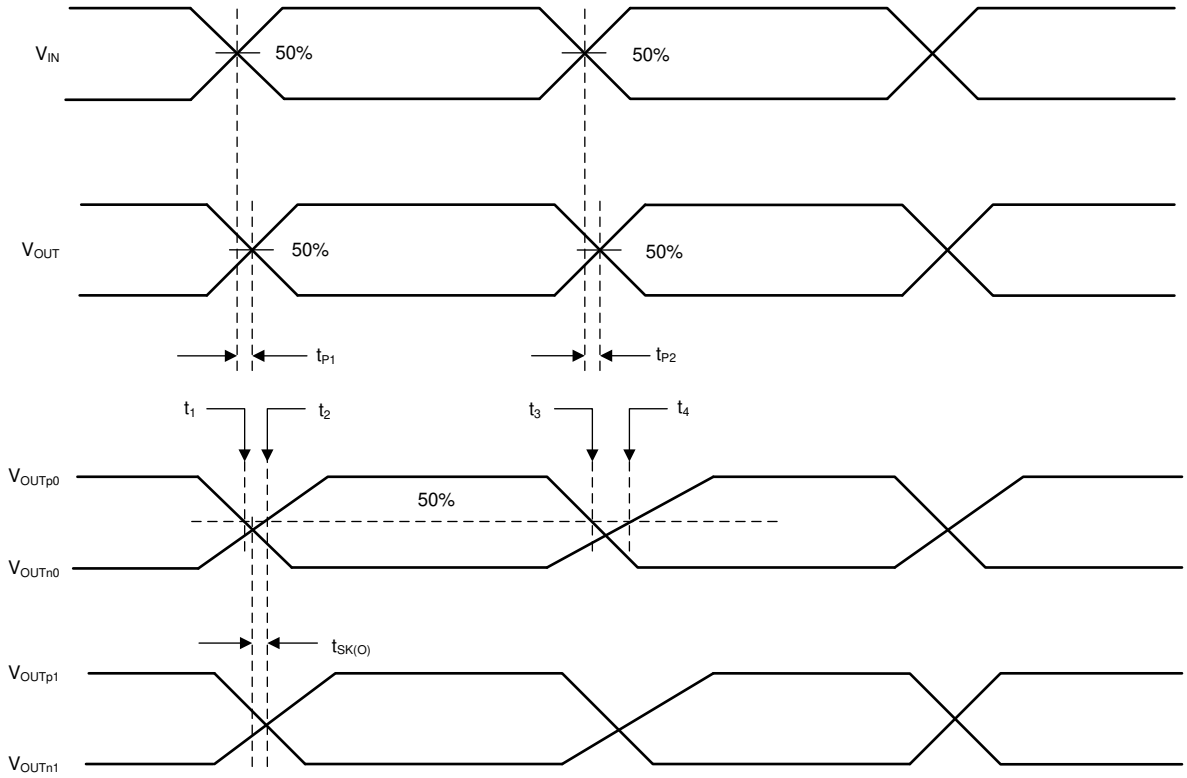

Figure 6-3. Timing Diagrams and Test Setup

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7 Detailed Description

7.1 Overview

The USB Type-C ecosystem operates around a small form factor connector and cable that is flippable and reversible. Due to the nature of the connector, a scheme is needed to determine the connector orientation. Additional schemes are needed to determine when a USB port is attached, determine the acting role of the USB port (DFP, UFP, DRP), and communicate Type-C current capabilities. These schemes are implemented over the CC pins according to the USB Type-C specifications. The HD3SS3220 provides Configuration Channel (CC) logic for determining USB port attach/detach, role detection, cable orientation, and Type-C current mode. The HD3SS3220 also contains several features such as VCONN sourcing, audio and debug accessory modes, Try.SRC and Try.SNK DRP configurations which make this device ideal for source, sink or dual role applications with USB 2.0 or USB 3.1.

HD3SS3220 has integrated USB 3.0/3.1 SS/SS+ MUX with 2 channel 2:1 switching required to handle cable flips. The CC controller determines the orientation of the cable and controls the MUX selection. The device also provides this orientation signal as a GPIO signal DIR that can be used in the system for increased flexibility and features.

7.1.1 Cables, Adapters, and Direct Connect Devices

Type-C Specification defines several cables, plugs and receptacles to be used to attach ports. The HD3SS3220 supports all cables, receptacles, and plugs. The HD3SS3220 device does not support any USB feature which requires USB Power Delivery (PD) communications over CC lines, such as e-marking or alternate mode.

7.1.1.1 USB Type-C receptacles and Plugs

The following is alist of Type-C receptacles and plugs supported by the HD3SS3220 device:

- USB Type-C receptacle for USB2.0 and USB3.1 and full-featured platforms and devices
- USB Full-Featured Type-C plug
- USB2.0 Type-C Plug

7.1.1.2 USB Type-C Cables

The following is a list of Type-C cables supported by the HD3SS3220 device:

- USB Full-featured Type-C cable with USB3.1 full featured plug
- USB2.0 Type-C cable with USB2.0 plug
- Captive cable with either a USB Full featured plug or USB2.0 plug

7.1.1.3 Legacy Cables and Adapters

The HD3SS3220 supports legacy cable adapters as defined by the Type-C specifications. The cable adapter must correspond to the mode configuration of the HD3SS3220 device.

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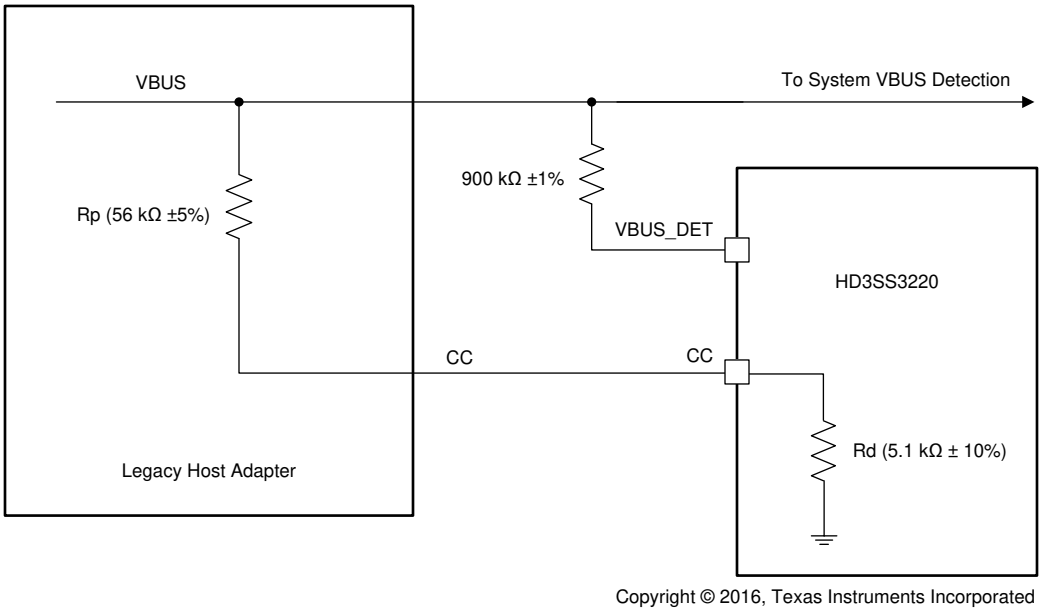

Figure 7-1. Legacy Adapter Implementation Circuit

7.1.1.4 Direct Connect Device

HD3SS3220 supports the attaching and detaching of a direct connect device such as cradle dock.

7.1.1.5 Audio Adapters

Additionally, HD3SS3220 supports audio adapters for audio accessory mode, including:

- Passive Audio Adapte
- Charge Through Audio Adapter

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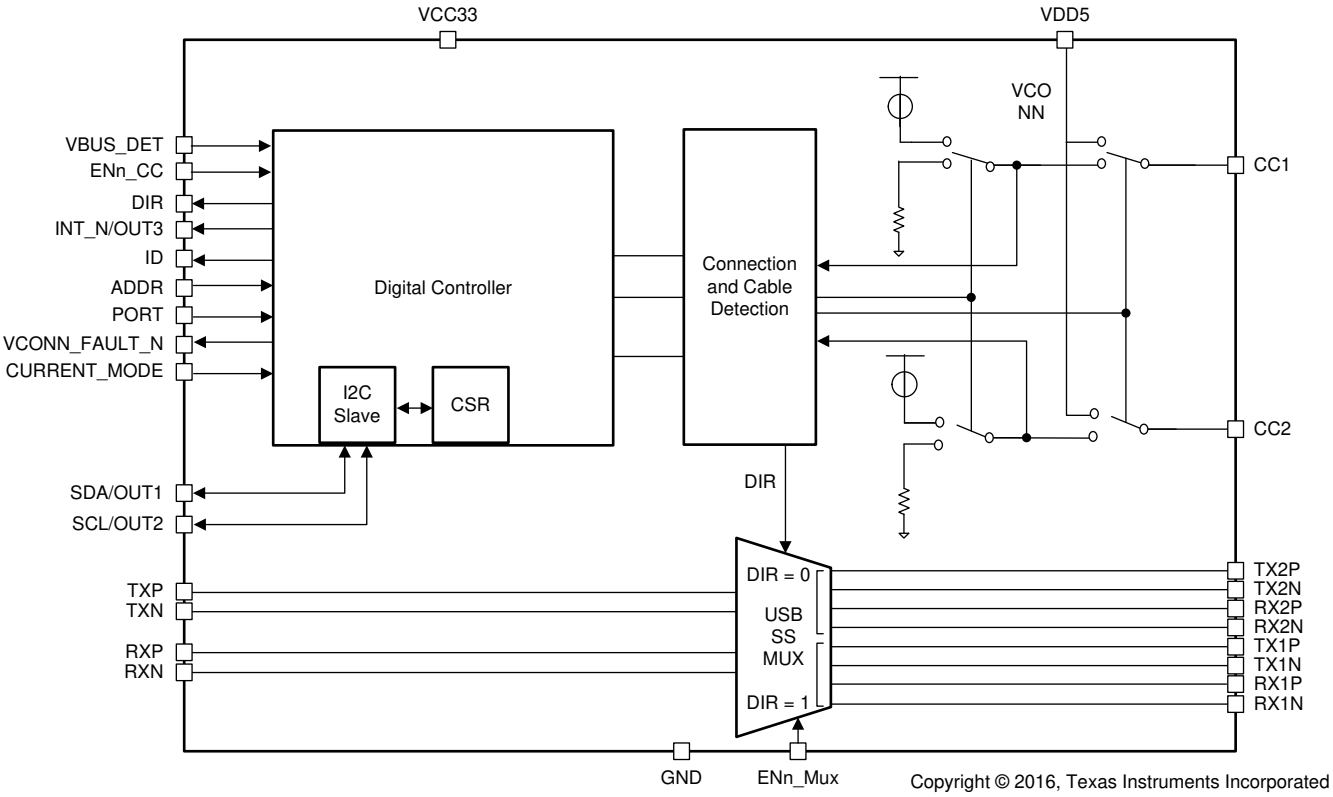
7.2 Functional Block Diagram



7.3 Feature Description

The HD3SS3220 can be configured as a DFP, UFP, or DRP using the 3-level PORT pin. The PORT pin should be strapped high to VDD5 using a pull-up resistance to achieve DFP mode, low to GND for UFP mode or left floating for DRP mode on the PCB. This flexibility allows the HD3SS3220 to be used in a variety of applications. The HD3SS3220 samples the PORT pin after reset and maintains the desired mode until the HD3SS3220 is reset again. It shall be static. Table 7-1 shows the supported features in each mode.

Table 7-1. Supported Features for HD3SS3220 by Mode

PORT PIN	High	Low	NC
Supported Features	**DFP Only**	**UFP Only**	**DRP**
Port Attach/Detach	√	√	√
Cable Orientation	√	√	√
Current Advertisement	√		√(DFP)
Current Detection		√	√(UFP)
Audio Accessory	√	√	√
Debug Accessory Modes	√	√	√
Active Cable Detection	√		√(DFP)
Try.SRC			√
Try.SNK			√
I2C/GPIO	√	√	√
Legacy Cables	√	√	√
VBUS Detection		√	√(UFP)
VCONN	√		√(DFP)
USB 3.1 G1 and G2 SS mux	√	√	√
Adaptive common mode tracking for SS channels	√	√	√

7.3.1 DFP/Source – Downstream Facing Port

The HD3SS3220 can be configured as a DFP only by pulling the PORT pin high through a resistance to VDD5. The HD3SS3220 device can also be configured as a DFP-only device by changing the MODE_SELECT register default setting with PORT pin left floating. In DFP mode, the HD3SS3220 constantly presents $R_{(p)}$ on both CC lines. In this mode, the HD3SS3220 will initially advertise default USB Type-C current. The Type-C current can be adjusted through CURRENT_MODE pin or I^2C if the system wishes to increase the current advertisement. The HD3SS3220 will adjust the $R_{(p)}$ resistors to match the desired advertisement.

A DFP monitors the voltage level on the CC pins looking for the $R_{(d)}$ termination of a UFP. When a UFP is detected and HD3SS3220 is in the attached. SRC state, the HD3SS3220 pulls the ID pin low to indicate to the system the port is attached to a device (UFP). Additionally, when a UFP is detected, the HD3SS3220 supplies VCONN on the unconnected CC pin if $R_{(a)}$ is also detected.

The following list describes the steps for enabling DFP through I^2C:

1. Write a 1'b1 to DISABLE_TERM register (address 0x0A bit 0)
2. Write a 2'b10 to MODE_SELECT register (address 0x0A bits 5:4)
3. Write a 1'b0 to DISABLE_TERM register (address 0x0A bit 0)

When configured as a DFP, the HD3SS3220 can operate with older USB Type-C 1.0 devices except for a USB Type-C 1.0 DRP device. The HD3SS3220 cannot operate with a USB Type-C 1.0 DRP device. This limitation is a result of a backwards compatibility problem between USB Type-C 1.1 DFP and a USB Type-C 1.0 DRP.

Note

Upon detecting a UFP device, HD3SS3220 will keep ID pin high if VBUS is not at VSafe0V. Once VBUS is at VSafe0V, the HD3SS3220 will assert ID pin low. This is done to enforce Type-C requirement that VBUS must be at VSafe0V before re-enabling VBUS.

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7.3.2 UFP/Sink – Upstream Facing Port

The HD3SS3220 can be configured as a UFP only by pulling the PORT pin low to GND. In UFP mode, the HD3SS3220 constantly presents Rd (pull-down resistors) on both CC pins.

In UFP mode, the HD3SS3220 monitors the voltage level at the CC pins for attachment of a DFP and also to determine Type-C current advertisement by the connected DFP. The HD3SS3220 will debounce the CC pins and wait for VBUS detection before successful attachment. As a UFP, the HD3SS3220 will detect and communicate the DFP's advertised current level to the system through the OUT1 and OUT2 pins if in GPIO mode or through the I2C CURRENT_MODE_DETECT register once in the Attached.SNK state.

The following list describes the steps for enabling DFP through I^2C:

1. Write a 1'b1 to DISABLE_TERM register (address 0x0A bit 0)
2. Write a 2'b10 to MODE_SELECT register (address 0x0A bits 5:4)
3. Write a 1'b0 to DISABLE_TERM register (address 0x0A bit 0)

7.3.3 DRP – Dual Role Port

The HD3SS3220 can be configured to operate as DRP when the PORT pin is left floating on the PCB. In DRP mode, the HD3SS3220 toggles between presenting as a DFP (Rp on both CC pins) and presenting as a UFP (Rd on both CC pins according to USB Type-C specification.

When presenting as a DFP, the HD3SS3220 monitors the voltage level on the CC pins looking for the $R_{(d)}$ termination of a UFP. When a UFP is detected and HD3SS3220 is in the attached. SRC state, the HD3SS3220 pulls the ID pin low to indicate to the system the port is attached to a sink (UFP). Additionally, when a UFP is detected, the HD3SS3220 supplies VCONN on the unconnected CC pin if Ra is also detected. In DFP mode, the HD3SS3220 will initially advertise default USB Type-C current. The Type-C current can be adjusted through I^2C if the system wishes to increase the amount advertised. HD3SS3220 will adjust the $R_{(p)}$ resistors to match the desired Type-C current advertisement.

When presenting as a UFP, the HD3SS3220 monitors the CC pins for the voltage level corresponding to the Type-C current advertisement by the connected DFP. The HD3SS3220 will debounce the CC pins and wait for VBUS detection before successfully attaching. As a UFP, the HD3SS3220 detects and communicate the DFP advertised current level to the system through the OUT1 and OUT2 pins if in GPIO mode or through the I2C CURRENT_MODE_DETECT register once in the attached.SNK state.

The HD3SS3220 supports two optional Type-C DRP features called Try.SRC and Try.SNK. Products supporting dual-role functionality may have a requirement to be a source (DFP) or a sink (UFP) when connected to another dual-role capable product. For example, a dual-role capable notebook can be used as a source when connected to a tablet, or a cell phone could be a sink when connected to a notebook or tablet. When standard DRP products (products which don't support either Try.SRC or Try.SNK) are connected together, the role (UFP or DFP) outcome is not predetermined. These two optional DRP features provide a means for dual-role capable products to connect to another dual-role capable product in the role desired. Try.SRC and Try.SNK are only available when HD3SS3220 is configured in I^2C mode. When operating in GPIO mode, the HD3SS3220 will always operate as a standard DRP.

The Try.SRC feature of the HD3SS3220 device provides a means for a DRP product to connect as a DFP when connected to another DRP product that doesn't implement Try.SRC. When two products which implement Try.SRC are connected together, the role outcome of either UFP or DFP is the same as a standard DRP. Try.SRC is enabled by changing I^2C register SOURCE_PREF to 2'b11. Once the register is changed to 2'b11, the HD3SS3220 will always attempt to connect as a DFP when attached to another DRP capable device.

7.3.4 Cable Orientation and Mux Control

The HD3SS3220 detects the cable orientation by monitoring the voltage on the CC pins. When a voltage level within the proper threshold is detected on CC1, the DIR pin is high. When a voltage level within the proper threshold is detected on CC2, the DIR is pulled low. The DIR pin is an open drain output and a pull-up resistor must be installed. The cable orientation status is also be communicated by I^2C for HD3SS3220. The device also controls the integrated SS mux to switch appropriate SS signals pairs (RX1/TX1 or RX2/TX2).

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7.3.5 Type-C Current Mode

Once a valid cable detection and attach have been completed, the DFP has the option to advertise the level of Type-C current a UFP can sink. The default current advertisement for HD3SS3220 can be configured using CURRENT_MODE pin or I2C CURRENT_MODE_ADVERTISE register. When a different than default current is chosen, the device adjusts the $R_{(p)}$ resistors for the specified current level.

Table 7-2. Type-C Current Advertisement for GPIO and I²C Modes

Type-C Current	GPIO Mode (ADDR pin NC)		I²C Mode (ADDR pin H, L)	
	UFP (PORT pin L)	DFP (PORT pin H)	UFP	DFP
Default – 500mA for (USB2.0) 900 mA for (USB3.1)	Detected current mode provided through OUT1/ OUT2	CURRENT_MODE=L	Detected current mode provided through I²C register	Advertisement selected through writing I²C register
Mid – 1.5 A		CURRENT_MODE=M		
High – 3 A		CURRENT_MODE=H		

7.3.6 Accessory Support

HD3SS3220 supports audio and debug accessories in UFP, DFP and DRP mode by default. Audio and debug accessory support is provided through reading of I2C registers. Audio accessory is also support through GPIO mode with INT_N/OUT3 pin (audio accessory has been detected when INT_N/OUT3 is low).

Note

If UFP accessory support is not needed in your application, UFP accessory support can be disabled by setting the DISABLE_UFP_ACCESSORY register.

7.3.7 Audio Accessory

Audio accessory mode is supported through two types of adapters. First, the passive audio adapter can be used to convert the Type-C connector into an audio port. In order to effectively detect the passive audio adapter, the HD3SS3220 must detect a resistance < $R_{(a)}$ on both the CC pins.

Secondly, a charge through audio adapter can be used. The primary difference between a passive and charge through adapter is that the charge through adapter supports supplying 500 mA of current over VBUS. The charge through adapter contains a receptacle and a plug. The plug shall act as a DFP and supply VBUS when it sees it's connected.

When HD3SS3220 is configured in GPIO mode, OUT3 pin shall be used to determine if an Audio Accessory is connected. When an Audio Accessory is detected, the OUT3 pin is pulled low.

7.3.8 Debug Accessory

Debug is an additional state supported by USB Type-C. The specification does not define a specific user scenario for this state, but the end user could use debug accessory mode to enter a test state for production specific to the application. Charge through debug accessory is not supported by HD3SS3220 when in DRP or UFP mode. The HD3SS3220 when configured as a DFP-only or as a DRP acting as a DFP detects a debug accessory which presents $R_{(d)}$ on both CC1 and CC2 pins. The HD3SS3220 sets ACCESSORY_CONNECTED register to 3'b110 to indicate a UFP debug accessory. The HD3SS3220 when configured as a UFP-only or as a DRP acting as a UFP detects a debug accessory which presents $R_{(p)}$ on both CC1 and CC2 pins. The HD3SS3220 sets ACCESSORY_CONNECTED register to 3b'111 to indicate a DFP debug accessory.

7.3.9 VCONN support for Active Cables

The HD3SS3220 supplies VCONN to active cables when configured in DFP mode or DRP acting as a DFP. VCONN is provided only when it is determined that the unconnected CC pin is terminated to a resistance, $R_{(a)}$, and after a UFP is detected and the attached. SRC state is entered. VCONN is supplied from VDD5 through a low resistance power FET out to the unconnected CC pin. VCONN is removed when a detach event is detected and the active cable is removed.

HD3SS3220 provides a current limiting function which will disconnect VCONN when the current being drawn from a device is above the max allowed for VCONN. When a VCONN fault has occurred, the VCONN flag in the

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I²C register is set and HD3SS3220 stops supplying VCONN (switch turns off), until the register flag has been cleared. If HD3SS3220 is in GPIO mode when a fault occurs, the VCONN switch is turned off and HD3SS3220 will not supply VCONN until a port detach and re-attach occurs.

7.3.10 I²C and GPIO Control

The HD3SS3220 can be configured for I²C or GPIO using the ADDR pin. The ADDR pin is a 3-level control pin. When the ADDR pin is left floating (NC), the HD3SS3220 is in GPIO mode. When the ADDR pin is pulled High, the HD3SS3220 is in I²C mode with address bit 6 equal to 1. When the ADDR pin is pulled low, the HD3SS3220 is in I²C mode with address bit 6 equal to 0.

All outputs for HD3SS3220 are open drain configuration.

The OUT1 and OUT2 pins are used to output the Type-C current mode when in GPIO mode. Additionally, the OUT3 pin is used to communicate the Audio Accessory mode in GPIO mode. The specifics of the output pins can be found in Table 7-3.

Table 7-3. Simplified Operation for OUT1 and OUT2

OUT1	OUT2	ADVERTISEMENT
H	H	Default
H	L	Default
L	H	Medium
L	L	High

When operating in I²C mode, HD3SS3220 uses the SCL and SDA lines for clock and data and the INT pin. The INT pin communicates an interrupt, or a change in I²C registers, to the system. The INT pin will be pulled low when the HD3SS3220 updates the registers with new information. The INT_N pin is open drain. The INTERRUPT_STATUS register should be set when the INT pin is pulled low. The customer shall write to I²C to clear the INTERRUPT_STATUS register.

When operating in GPIO mode, the OUT3 pin is used in place of INT pin to determine if an Audio Accessory has been detected and attached. The OUT3 pin is pulled low when an Audio Accessory is detected.

Note

When using the 3.3-V supply for I²C pull-up, the customer must ensure that the VDD5 is 3 V and above. Otherwise, the I²C may back power the device.

7.3.11 HD3SS3220 $V_{(BUS)}$ Detection

The HD3SS3220 device supports VBUS detection according to the Type-C Specification. VBUS detection is used to determine the attachment and detachment of a UFP and to determine the entering and exiting of accessary modes. VBUS detection is also used to successfully resolve the role in DRP mode. The system VBUS voltage must be routed through a 900-kΩ resistor to the VBUS_DET pin on the HD3SS3220 device.

7.3.12 VDD5 and VCC33 Power-On Requirements

The HD3SS3220 has two power supplies: VDD5 and VCC33. The VDD5 supply powers the internal CC controller and also provides VCONN to either CC1 or CC2. The VCC33 powers the 2:1 MUX.

The HD3SS3220 non-failsafe pins are the following: PORT, ADDR, SDA/OUT1, SCL/OUT2, INT_IN/OUT3, VCONN_FAULT_N, and DIR. If any of these non-failsafe pins are pulled-up to a supply other than VDD5, then VDD5 supply must be powered up before the VCC33 supply as depicted in Figure 7-2. If it is not possible to power up VDD5 before VCC33, then the ENn_CC pin must be held high while both supplies are ramping and then asserted low after both supplies are stable as depicted in Figure 7-3.

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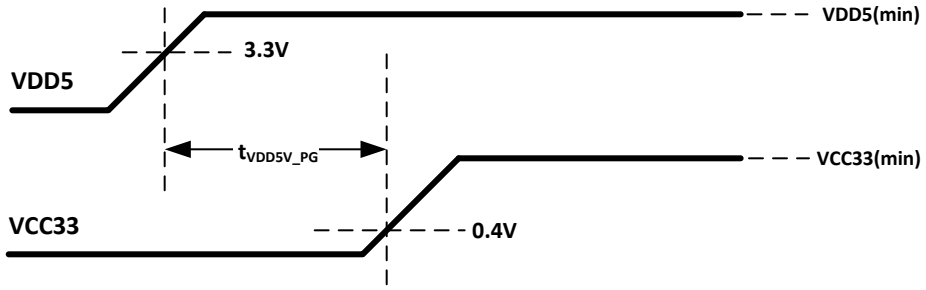

Figure 7-2. PowerOn Timings with ENn_CC always low

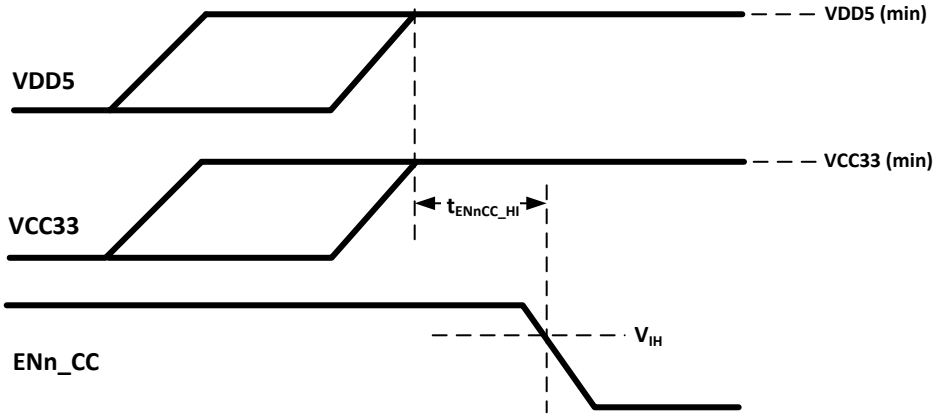

Figure 7-3. PowerOn Timings with ENn_CC Controlled

7.4 Device Functional Modes

The HD3SS3220 has four functional modes. Table 7-4 lists these modes:

Table 7-4. USB Type-C States according to HD3SS3220 Functional Modes

MODES	GENERAL BEHAVIOR	MODE	STATES[1]
Unattached	USB port unattached. ID, PORT operational. I^2C on.	UFP-Only	Unattached.SNK
			AttachWait.SNK
		DFP	Toggle Unattached.SNK → Unattached.SRC
			AttachedWait.SRC or AttachedWait.SNK
		DFP-Only	Unattached.SRC
			AttachWait.SRC
Active	USB port attached. All GPIOs operational. I^2C on.	UFP-Only	Attached.SNK
			Audio Accessory
			Debug Accessory
		DRP	Attached.SNK
			Attached.SRC
			Audio accessory
			Debug accessory
		DFP-Only	Attached.SRC
			Audio accessory
			Debug accessory
Dead battery	No operation. VDD5 not available.	DRP	Default device state to UFP/SNK with $R_{(d)}$.

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Table 7-4. USB Type-C States according to HD3SS3220 Functional Modes (continued)

MODES	GENERAL BEHAVIOR	MODE	STATES[(1)]
Shutdown	No operation. VDD5 available and ENn_CC pin is high	DRP	Default device state to UFP/SNK with $R_{(d)}$.

(1) (1) Required; not in sequential order

7.4.1 Unattached Mode

Unattached mode isthe primary mode of operation for the HD3SS3220 since a USB port can be unattached for a lengthy period of time. In Unattached mode, VDD5 is available, and all IOs and I^2C are operational. VCONN is disabled.

After HD3SS3220 are powered up, the part enters unattached mode until a successful attach has been determined. Initially, right after power up, the HD3SS3220 comes up as an unattached.SNK. The HD3SS3220 checks the PORT pin and operate according to the mode configuration. This means that the HD3SS3220 toggle between UFP and DFP if configured as a DRP

7.4.2 Active Mode

Active mode is defined as the port being attached. In active mode, all GPIOs are operational, and I^2C is read / write (R/W). When in active mode, the HD3SS3220 device communicates to the AP that the USB port is attached. This communication happens through the ID pin if HD3SS3220 is configured as a DFP or DRP connect as source. If HD3SS3220 is configured as a UFP or a DRP connected as a sink, the OUT1/OUT2 and INT_N/OUT3 pins are used. The HD3SS3220 device exits active mode under the following conditions:

- Cable unplug
- VBUS removal if attached as a UFP
- Dead battery; system battery or supply is removed
- EN_N is floated or pulled high

7.4.3 Dead Battery

During Dead battery mode VDD5 is not available. CC pins always default to pull down resistors in dead battery mode. Dead battery mode to means:

- HD3SS3220 in UFP with 5.1 kΩ ±20% $R_{(d)}$; cable connected and providing charge.
- HD3SS3220 in UFP with 5.1 kΩ ±20% $R_{(d)}$; nothing connected (application could be off or have a discharged battery)

7.4.4 Shutdown Mode

Shutdown mode for HD3SS3220 is defined as follows:

- Supply voltage available and EN_N pin is high or floating.
- EN_N pin has internal pullup resistor
- The HD3SS3220 device is off, but still maintains the $R_{(d)}$ on the CC pins.

7.5 Programming

For further programmability, the HD3SS3220 can be controlled using I^{2}C. The HD3SS3220 local I^{2}C interface is available for reading/writing after x clock cycles when the device is powered up. The SCL and SDA terminals are used for I^{2}C clock and I^{2}C data respectively. If I^{2}C is the preferred method of control, the ADDR pin must be set accordingly.

Table 7-5. HD3SS3220 I^{2}C Target Address

ADDR pin	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (W/R)
H	1	1	0	0	1	1	1	0/1
L	1	0	0	0	1	1	1	0/1

The following procedure should be followed to write to HD3SS3220 I^{2}C registers:

1. The master initiates a write operation by generating a start condition (S), followed by the HD3SS3220 7-bit address and a zero-value R/W bit to indicate a write cycle.
2. The HD3SS3220 device acknowledges the address cycle.
3. The master presents the sub-address (I^{2}C register within the HD3SS3220 device) to be written, consisting of one byte of data, MSB-first.
4. The HD3SS3220 device acknowledges the sub-address cycle.
5. The master presents the first byte of data to be written to the I^{2}C register.
6. The HD3SS3220 device acknowledges the byte transfer.
7. The master can continue presenting additional bytes of data to be written, with each byte transfer completing with an acknowledge from the HD3SS3220 device.
8. The master terminates the write operation by generating a stop condition (P).

The following procedure should be followed to read the HD3SS3220 I^{2}C registers:

1. The master initiates a read operation by generating a start condition (S), followed by the HD3SS3220 7-bit address and a one-value R/W bit to indicate a read cycle.
2. The HD3SS3220 device acknowledges the address cycle.
3. The HD3SS3220 device transmits the contents of the memory registers MSB-first starting at register 00h or last read sub-address+1. If a write to the I^{2}C register occurred prior to the read, then the HD3SS3220 device starts at the sub-address specified in the write.
4. The HD3SS3220 device waits for either an acknowledge (ACK) or a not-acknowledge (NACK) from the master after each byte transfer; the I^{2}C master acknowledges reception of each data byte transfer.
5. If an ACK is received, the HD3SS3220 device transmits the next byte of data.
6. The master terminates the read operation by generating a stop condition (P).

The following procedure should be followed for setting a starting sub-address for I^{2}C reads:

1. The master initiates a write operation by generating a start condition (S), followed by the HD3SS3220 7-bit address and a zero-value R/W bit to indicate a read cycle.
2. The HD3SS3220 device acknowledges the address cycle.
3. The master presents the sub-address (I^{2}C register within the HD3SS3220 device) to be read, consisting of one byte of data, MSB-first.
4. The HD3SS3220 device acknowledges the sub-address cycle.
5. The master terminates the read operation by generating a stop condition (P).

Note

If no sub-addressing is included for the read procedure, then the reads start at register offset 00h and continue byte-by-byte through the registers until the I^{2}C master terminates the read operation. If a I^{2}C address write occurred prior to the read, then the reads start at the sub-address specified by the address write.

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7.6 Register Maps

Table 7-6. CSR Registers

OFFSET	RESET	REGISTER NAME	SECTION
0x07 through 0x00	[0x00, 0x54, 0x55, 0x53, 0x42, 0x33, 0x32, 0x32]	Device Identification	Device Identification Register
0x08	0x00	Connection Status	Connection Status Register
0x09	0x20	Connection Status and Control	Connection Status and Control Register
0x0A	0x00	General Control	General Control Register
0xA0	0x02	Device Revision	Device Revision Register

7.6.1 Device Identification Register (offset = 0x07 through 0x00) [reset = 0x00, 0x54, 0x55, 0x53, 0x42, 0x33, 0x32, 0x32]

Figure 7-4. Device Identification Register

7	6	5	4	3	2	1	0
DEVICE_ID							
R							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-7. Device Identification Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DEVICE_ID	R	0x00	For the HD3SS3220 device these fields return a string of ASCII characters returning HD3SS3220 addresses: 0x07 - 0x00 = {0x00, 0x54, 0x55, 0x53, 0x42, 0x33, 0x32, 0x32}

7.6.2 Connection Status Register (offset = 0x08) [reset = 0x00]

Figure 7-5. Connection Status Register

7	6	5	4	3	2	1	0
CURRENT_MODE_ADVERTISE		CURRENT_MODE_DETECT		ACCESSORY_CONNECTED			ACTIVE_CABL E_DETECTION
R/W		R/U		R/U			R/U

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset, R/U = Read/Update

Table 7-8. Connection Status Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	CURRENT_MODE_ADVERTISE	R/W	2'b00	These bits are programmed by the application to raise the current advertisement from Default. 00 – Default (500mA/900mA) Initial value at startup 01 – Mid (1.5A) 10 – High (3A) 11 – Reserved
5:4	CURRENT_MODE_DETECT	R/U	2'b00	These bits are set when a UFP determines the Type-C current mode. 00 – Default (value at start up) 01 – Medium 10 –Charge Through Accessory – 500mA 11 – High
3:1	ACCESSORY_CONNECTED	R/U	3'b000	These bits are read by the application to determine if an accessory was attached. 000 –No Accessory attached (Default) 001 - Reserved 010 – Reserved 011 – Reserved 100 – Audio Accessory 101 – Charged Thru Audio Accessory 110 - Debug Accessory when HD3SS3220 is connected as a DFP 111 – Debug accessory when HD3SS3220 is connected as a UFP
0	ACTIVE_CABL E_DETECTION	R/U	1'b0	This flag indicates that an active cable has been plugged into the Type-C connector 0 - No active cable 1 – Active Cable Attach

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7.6.3 Connection Status and Control Register (offset = 0x09) [reset = 0x20]

Figure 7-6. Connection Status and Control Register

7	6	5	4	3	2	1	0
ATTACHED_STATE		CABLE_DIR	INTERRUPT _STATUS	VCONN _FAULT	DRP_DUTY_CYCLE		DISABLE _UFP_ ACCESSORY
R/U		R/U	R/U	R/U	R/W		R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset, R/U = Read/Update

Table 7-9. Connection Status Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	ATTACHED_STATE	R/U	2'b00	This is an additional method to communicate attach other than the ID pin. These bits can be read by the application to determine what was attached. 00 – Not Attached (Default) 01 – Attached.SRC (DFP) 10 – Attached.SNK (UFP) 11 – Attached to an Accessory
5	CABLE_DIR	R/U	1'b0	Cable orientation. The application can read these bits for cable orientation information. 0 – CC2 1 – CC1 (Default)
4	INTERRUPT _STATUS	R/U	1'b0	The INT pin will be pulled low whenever a CSR changes. When a CSR change has occurred this bit should be held at 1 until the application clears teh bit. 0 – Clear 1 – Interrupt (When INT pulled low, this bit must be 1. This bit will be 1 whenever any CSR have been changed)
3	VCONN _FAULT	R/U	1'b0	Bit is set whenever VCONN overcurrent limit is triggered. 0 – Clear 1 – VCONN fault is detected
2:1	DRP_DUTY_CYCLE	R/W	2'b00	Percentage of time that a DRP shall advertise DFP during t_{DRP} 00 – 30% default 01 – 40% 10 – 50% 11 – 60%
0	DISABLE _UFP_ ACCESSORY	R/W	1'b0	Setting this field will disable UFP accessory support 0 – UFP accessory support enabled (Default) 1 – UFP accessory support disabled

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7.6.4 General Control Register (offset = 0x0A) [reset = 0x00]

Figure 7-7. General Control Register

7	6	5	4	3	2	1	0
DEBOUNCE		MODE_SELECT		I2C_SOFT _RESET	SOURCE_PREF		DISABLE _TERM
R/W		R/W		R/U	R/W		R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-10. General Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	DEBOUNCE	R/W	2'b00	The nominal amount of time the HD3SS3220 debounces the voltages on the CC pins. 00 – 168 ms (Default) 01 – 118 ms 10 – 134 ms 11 – 152 ms
5:4	MODE_SELECT	R/W	2'b00	This register can be written to set the HD3SS3220 mode operation. The ADDR pin must be set to I^2C mode. If the default is maintained, HD3SS3220 shall operate according to the PORT pin levels and modes. The MODE_SELECT can only be changed when in the unattached state. 00 – DRP mode (start from unattached.SNK) (default) 01 – UFP mode (unattached.SNK) 10 – DFP mode (unattached.SRC) 11 – DRP mode (start from unattached.SNK)
3	I2C_SOFT _RESET	R/U	1'b0	This register resets the digital logic. The bit is self-clearing. A write of 1 starts the reset. The following registers can be affected after setting this bit: CURRENT_MODE_DETECT ACTIVE_CABLE_DETECTION ACCESSORY_CONNECTED ATTACHED_STATE CABLE_DIR
2:1	SOURCE_PREF	R/W	2'b00	This field controls the TUSB322I behavior when configured as a DRP. 00 – Standard DRP (default) 01 – DRP performs Try.SNK 10 – Reserved 11 – DRP performs Try.SRC
0	DISABLE _TERM	R/W	1'b0	This field disables the termination on CC pins and transition the CC state machine to the disabled state. 0 – Termination enabled according TUSB322I mode of operation (default) 1 – Termination disabled and state machine held in disable state

7.6.5 Device Revision Register (offset = 0xA0) [reset = 0x02]

Figure 7-8. Device Revision Register

7	6	5	4	3	2	1	0
REVISION							
R							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-11. Device Revision Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REVISION	R	'h02	Revision of HD3SS3220. Defaults to 0x02

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

HD3SS3220 can be used to design USB Type-C systems implementing DRP, DFP and UFP port for applications requiring USB SupeSpeed or SuperSpeedPlus. The device supports native USB-C power handshake for power negotiation up to 15 W. HD3SS3220 can advertise 900 mA, 1.5 A and 3 A current capability as DFP (provider) and detect these settings as UFP (consumer).

Use of I^2C is optional but strongly encouraged and provides additional control of the device and status of the USB-C interface resulting robust and flexible system implementation. A constant I^2C polling is not required and device provides an interrupt signal for servicing microprocessor.

HD3SS3220 mux channels have independent adaptive common mode tracking allowing RX and TX paths to have different common mode voltage simplifying system implementation and avoiding inter-op issues.

Layout for SS signals to USB-C connector needs to be adjusted based on receptacle type.

Note

HD3SS3220 mux does not provide common mode biasing for the channel. Therefore it is required that the device is biased from either side for all active channels. Also note that mux channels are for differential SS signals only.

If power support larger than 15W is required USBPD function is needed and not supported by this device. If split data/power role is desired such as USB host but power consumer or USB device but power provider, an USBPD function is needed as well.

8.2 Typical Application, DRP Port

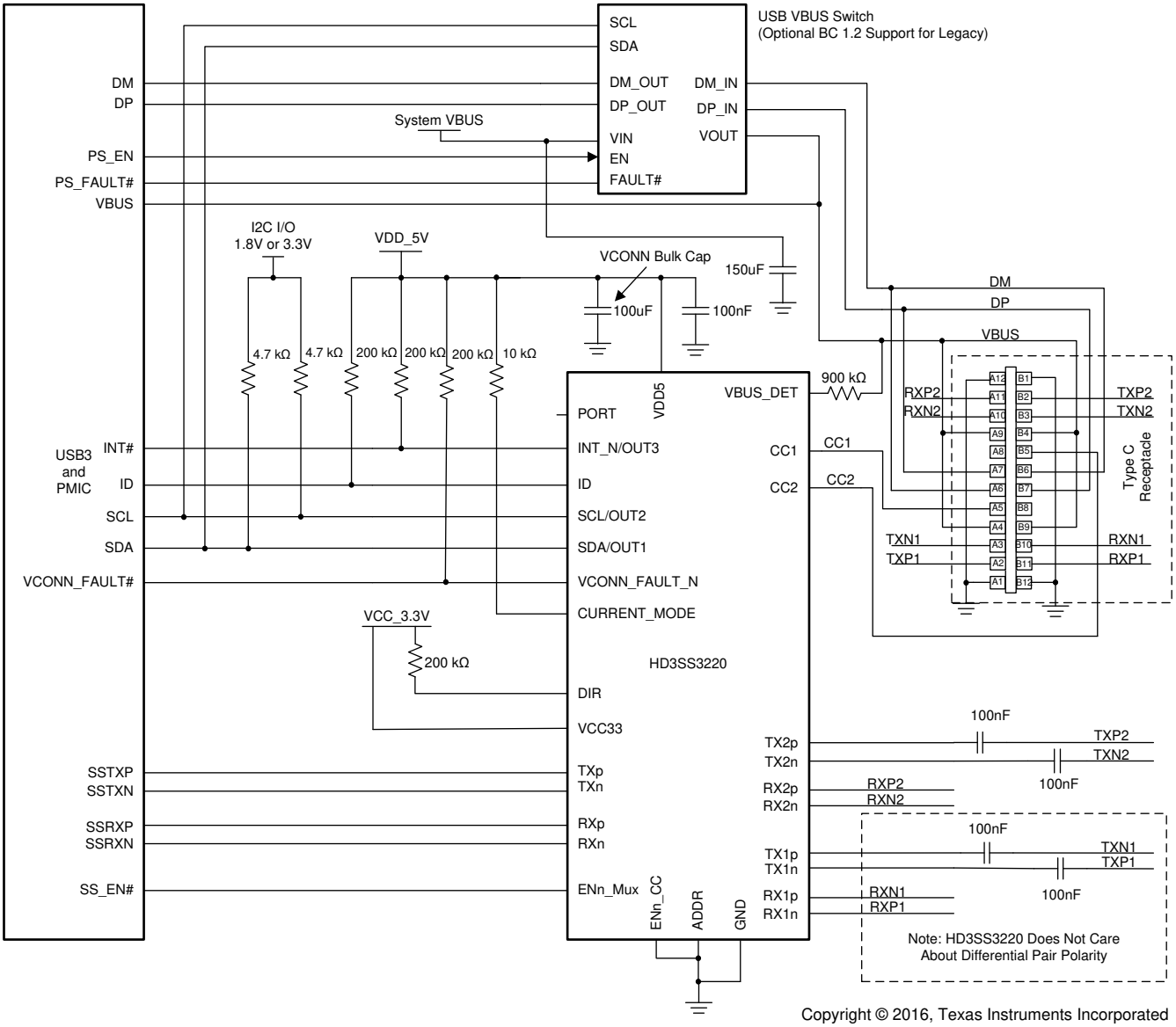

Figure 8-1. DRP Application Using HD3SS3220DRP

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8.2.1 Design Requirements

For this design example, use the parameters shown in Table 8-1.

Table 8-1. Design Parameters, DRP Port

PARAMETER	EXAMPLE	COMMENTS
VDD5	5.25 V	VDD5 is used to provide VCONN power to CC pins. Value of this supply should be ≥ 5 V to keep VCONN ≥ 4.75 V.
System_VBUS	5.25 V	VDD5 and System_VBUS can be shorted together; however careful consideration is needed to maintain desired VBUS and VCONN for the Type-C port.
I^2C I/O Supply	3.3 V	1.8 V is also an option. When using the 3.3-V supply, the customer must ensure that the VDD5 is 3 V and above. Otherwise the I^2C may back power the device
VCC33	3.3 V	3-3.6 V range allowed.
AC Coupling Capacitors for SS signals	100 nF	75-200 nF range allowed. For TX pairs only, RX pairs will be biased by host Receiver. Note that HD3SS3220 requires a common mode biasing of 0-2 V. If host receiver has bias voltage outside this range, appropriate additional ac coupling caps and biasing of HD3SS3220 RX pairs needed.
Pull-up Resistors: DIR, ID, INT_N, VCONN_FAULT_N	200 K	Smaller values can be used, but leakage needs to be considered for device power budget calculations.
Pull-up Resistors: I^2C	4.7 K	
Pull-up Resistors: CURRENT_MODE	10 K	Example here is for 3 A. If 1.5 A or 900 mA needed different values are required.
Series resistor: VBUS_DET	900 K	
Decoupling Capacitors: VCONN Bulk	100 µF	
Decoupling Capacitors: VBUS Bulk	150 µF	As indicated in schematic needs to be switched out when in UFP.

8.2.2 Detailed Design Procedure

HD3SS3220 can be used to design a USB Type-C DRP Port. In DRP mode the device alternate itself as DFP and UFP according to USB-C specifications. An example schematic for DRP implementation is illustrated in Figure 8-1.

8.2.3 Typical Application, DFP Port

HD3SS3220 can be used to design a USB Type-C DFP Port. An example schematic for DFP implementation is illustrated in Figure 8-2.

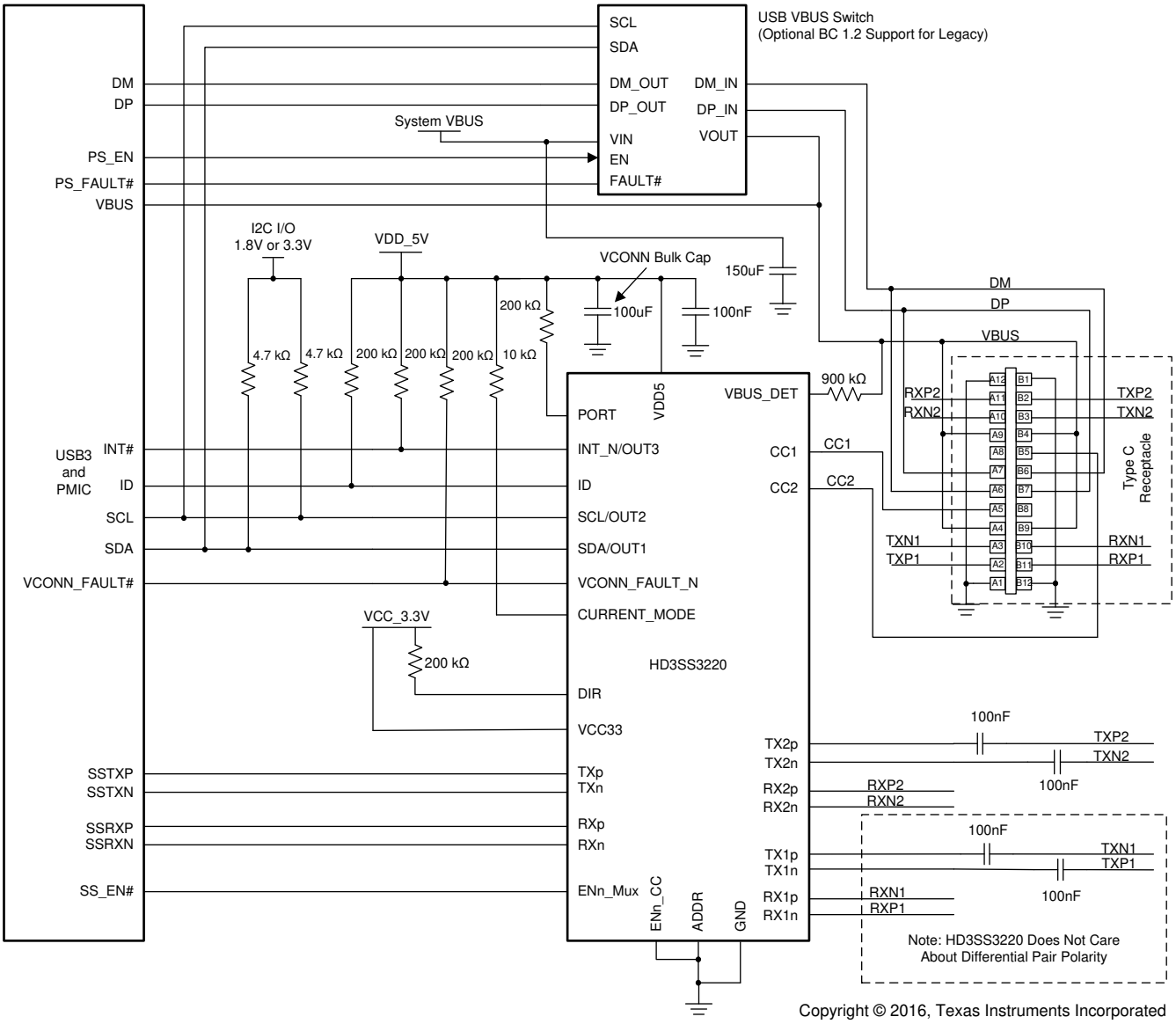

Figure 8-2. DFP Application Using HD3SS3220DFP

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8.2.3.1 Design Requirements

For this design example, use the parameters shown in Table 8-2.

Table 8-2. Design Parameters, DFP Port

PARAMETER	EXAMPLE	COMMENTS
VDD5	5.25 V	VDD5 is used to provide VCONN power to CC pins. Value of this supply should be ≥ 5 V to keep VCONN ≥ 4.75 V.
System_VBUS	5.25 V	VDD5 and System_VBUS can be shorted together; however careful consideration is needed to maintain desired VBUS and VCONN for the Type-C port.
I^2C I/O Supply	3.3 V	1.8 V is also an option. When using the 3.3-V supply, the customer must ensure that the VDD5 is 3 V and above. Otherwise the I^2C may back power the device
VCC33	3.3 V	3-3.6 V range allowed.
AC Coupling Capacitors for SS signals	100 nF	75-200 nF range allowed. For TX pairs only, RX pairs will be biased by host Receiver. Note that HD3SS3220 requires a common mode biasing of 0-2 V. If host receiver has bias voltage outside this range, appropriate additional ac coupling caps and biasing of HD3SS3220 RX pairs needed.
Pull-up Resistors: DIR, ID, INT_N, VCONN_FAULT_N	200 K	Smaller values can be used, but leakage needs to be considered for device power budget calculations.
Pull-up Resistors: I^2C	4.7 K	
Pull-up Resistors: CURRENT_MODE	10 K	Example here is for 3 A. If 1.5 A or 900 mA needed different values are required.
Decoupling Capacitors: VCONN Bulk	100 µF	
Decoupling Capacitors: VBUS Bulk	150 µF	

8.2.3.2 Detailed Design Procedure

HD3SS3220 can be used to design a USB Type-C DFP Port. An example schematic for DFP implementation is illustrated in Figure 8-2.

8.2.4 Typical Application, UFP Port

HD3SS3220 can be used to design a USB Type-C UFP Port. An example schematic for UFP implementation is illustrated in Figure 8-3.

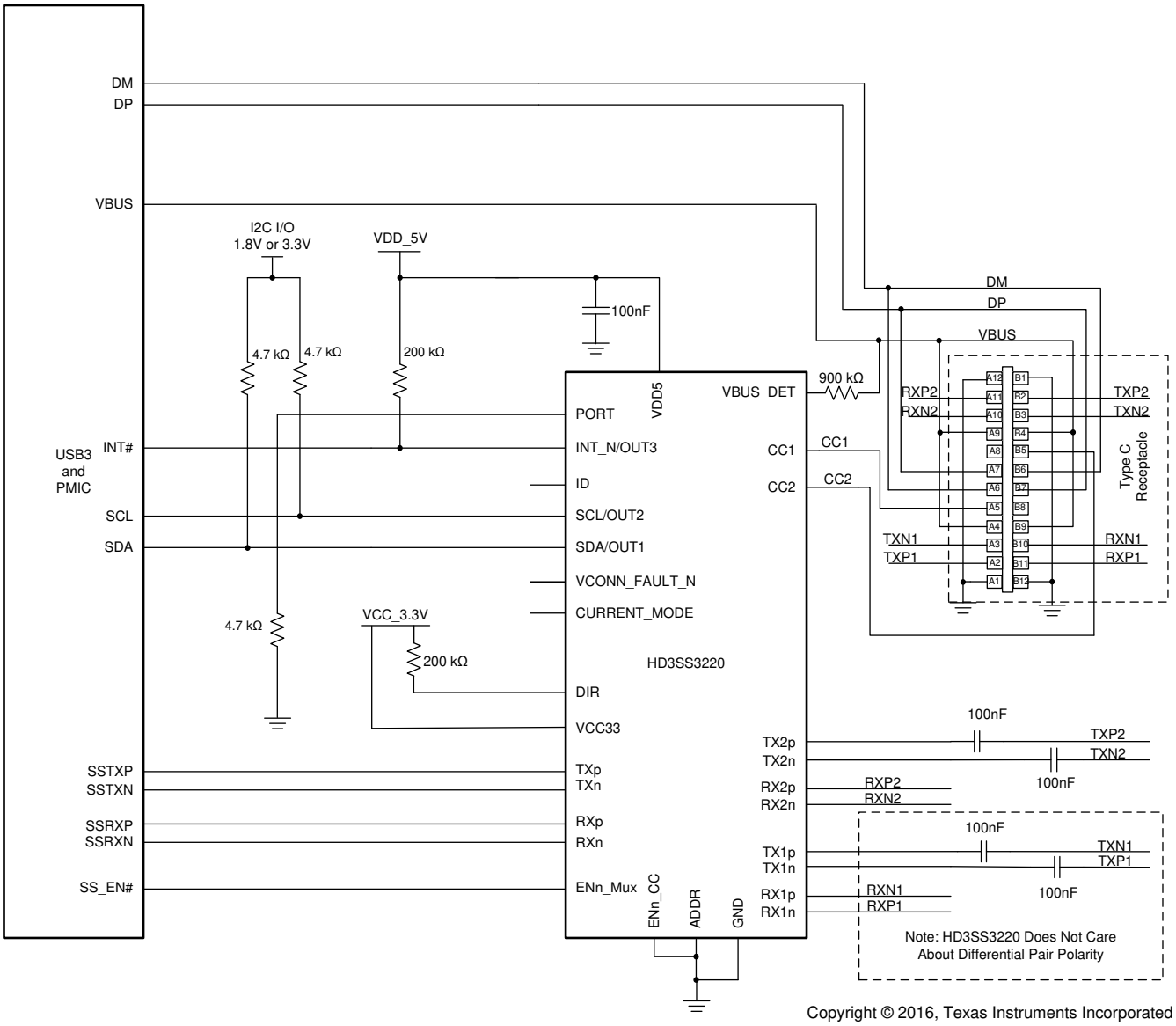

Figure 8-3. UFP Application Using HD3SS3220DFP

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8.2.4.1 Design Requirements

For this design example, use the parameters shown in Table 8-3.

Table 8-3. Design Parameters, UFP Port

PARAMETER	EXAMPLE	COMMENTS
VDD5	5 V	VBUS from Type-C port can be used.
I^2C I/O Supply	3.3 V	1.8 V is also an option. When using the 3.3-V supply, the customer must ensure that the VDD5 is 3 V and above. Otherwise the I^2C may back power the device
VCC33	3.3 V	3-3.6 V range allowed.
AC Coupling Capacitors for SS signals	100 nF	75-200 nF range allowed. For TX pairs only, RX pairs will be biased by host Receiver. Note that HD3SS3220 requires a common mode biasing of 0-2 V. If host receiver has bias voltage outside this range, appropriate additional ac coupling caps and biasing of HD3SS3220 RX pairs needed.
Pull-up Resistors: DIR, INT_N	200 K	Smaller values can be used, but leakage needs to be considered for device power budget calculations.
Pull-up Resistors: I^2C	4.7 K	
Series resistor: VBUS_DET	900 K	

8.2.4.2 Detailed Design Procedure

HD3SS3220 can be used to design a USB Type-C DFP Port. An example schematic for UFP implementation is illustrated in Figure 8-3.

Power Supply Recommendations

HD3SS3220 has 4.5 to 5.5-V supply voltage requirement. The device can be powered from the same rail that provides power for $V_{(BUS)}$.

9 Layout

9.1 Layout Guidelines

9.1.1 Suggested PCB Stackups

TI recommends a PCB of at least six layers. Table 9-1 provides example PCB stackups.

Table 9-1. Example PCB Stackups

6-LAYER	8-LAYER	10-LAYER
SIGNAL	SIGNAL	SIGNAL
GROUND	GROUND	GROUND
SIGNAL(1)	SIGNAL	SIGNAL(1)
SIGNAL(1)	SIGNAL	SIGNAL(1)
POWER/GROUND(2)	POWER/GROUND(2)	POWER
SIGNAL	SIGNAL	POWER/GROUND(2)
	GROUND	SIGNAL(1)
	SIGNAL	SIGNAL(1)
		GROUND
		SIGNAL

(1) Route directly adjacent signal layers at a 90° offset to each other
(2) Plane may be split depending on specific board considerations. Ensure that traces on adjacent planes do not cross splits.

9.1.2 High-Speed Signal Trace Length Matching

Match the etch lengths of the relevant differential pair traces of each interface. The etch length of the differential pair groups do not need to match (that is, the length of the transmit pair does not need to match the length of the receive pair). When matching the intrapair length of the high-speed signals, add serpentine routing to match the lengths as close to the mismatched ends as possible. See Figure 9-1 for more details.

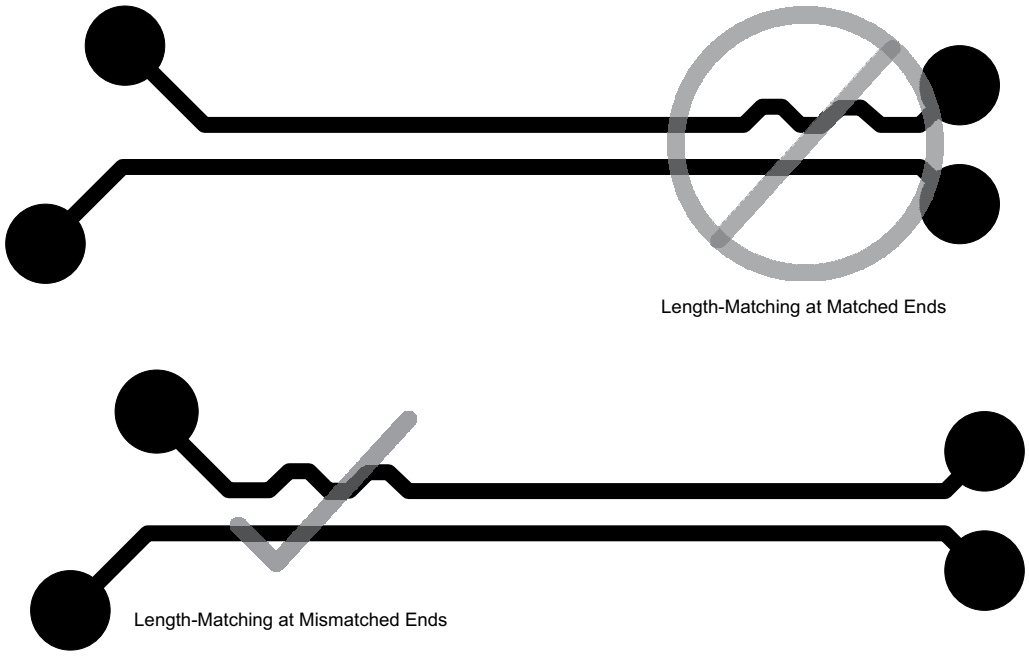

Figure 9-1. Length Matching

9.1.3 Differential Signal Spacing

To minimize crosstalk in high-speed interface implementations, the spacing between the signal pairs must be a minimum of 5 times the width of the trace. This spacing is referred to as the 5W rule. A PCB design with a

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calculated trace width of 6 mils requires a minimum of 30 mils spacing between high-speed differential pairs. Also, maintain a minimum keep-out area of 30 mils to any other signal throughout the length of the trace. Where the high-speed differential pairs abut a clock or a periodic signal, increase this keep-out to a minimum of 50 mils to ensure proper isolation. For examples of high-speed differential signal spacing, see Figure 9-2 and Figure 9-3.

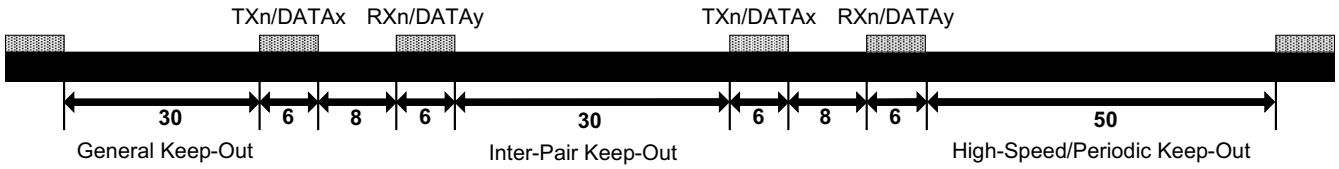

Figure 9-2. USB3/SATA/PCIe Differential Signal Spacing (mils)

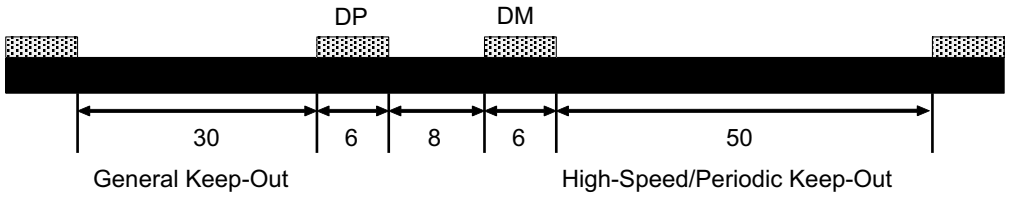

Figure 9-3. USB2 Differential Signal Spacing (mils)

9.1.4 High-Speed Differential Signal Rules

- Do not place probe or test points on any high-speed differential signal.
- Do not route high-speed traces under or near crystals, oscillators, clock signal generators, switching power regulators, mounting holes, magnetic devices, or ICs that use or duplicate clock signals.
- After BGA breakout, keep high-speed differential signals clear of the SoC because high current transients produced during internal state transitions can be difficult to filter out.
- When possible, route high-speed differential pair signals on the top or bottom layer of the PCB with an adjacent GND layer. TI does not recommend stripline routing of the high-speed differential signals.
- Ensure that high-speed differential signals are routed ≥ 90 mils from the edge of the reference plane.
- Ensure that high-speed differential signals are routed at least 1.5 W (calculated trace-width × 1.5) away from voids in the reference plane. This rule does not apply where SMD pads on high-speed differential signals are voided.
- Maintain constant trace width after the SoC BGA escape to avoid impedance mismatches in the transmission lines.
- Maximize differential pair-to-pair spacing when possible.

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9.1.5 Symmetry in the Differential Pairs

Route all high-speed differential pairs together symmetrically and parallel to each other. Deviating from this requirement occurs naturally during package escape and when routing to connector pins. These deviations must be as short as possible and package break-out must occur within 0.25 inches of the package.

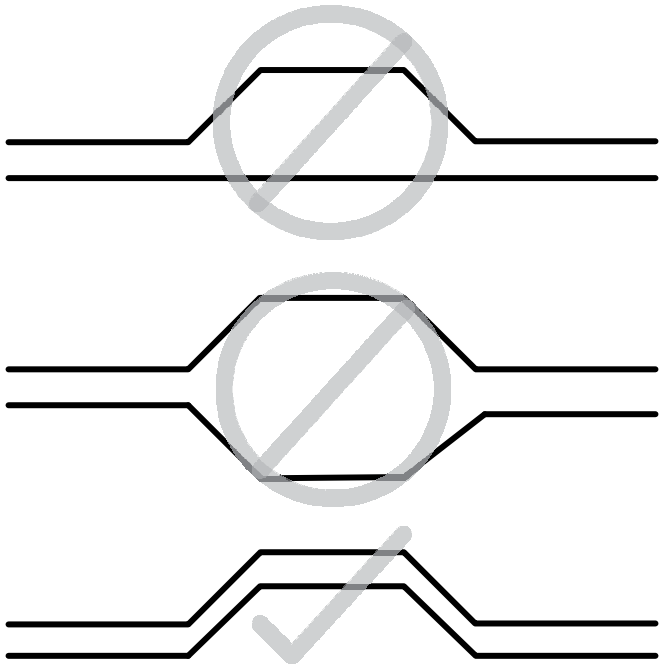

Figure 9-4. Differential Pair Symmetry

9.1.6 Via Discontinuity Mitigation

A via presents a short section of change in geometry to a trace and can appear as a capacitive and/or an inductive discontinuity. These discontinuities result in reflections and some degradation of a signal as it travels through the via. Reduce the overall via stub length to minimize the negative impacts of vias (and associated via stubs).

Because longer via stubs resonate at lower frequencies and increase insertion loss, keep these stubs as short as possible. In most cases, the stub portion of the via present significantly more signal degradation than the signal portion of the via. TI recommends keeping via stubs to less than 15 mils. Longer stubs must be back-drilled. For examples of short and long via lengths, see Figure 9-5 and Figure 9-6.

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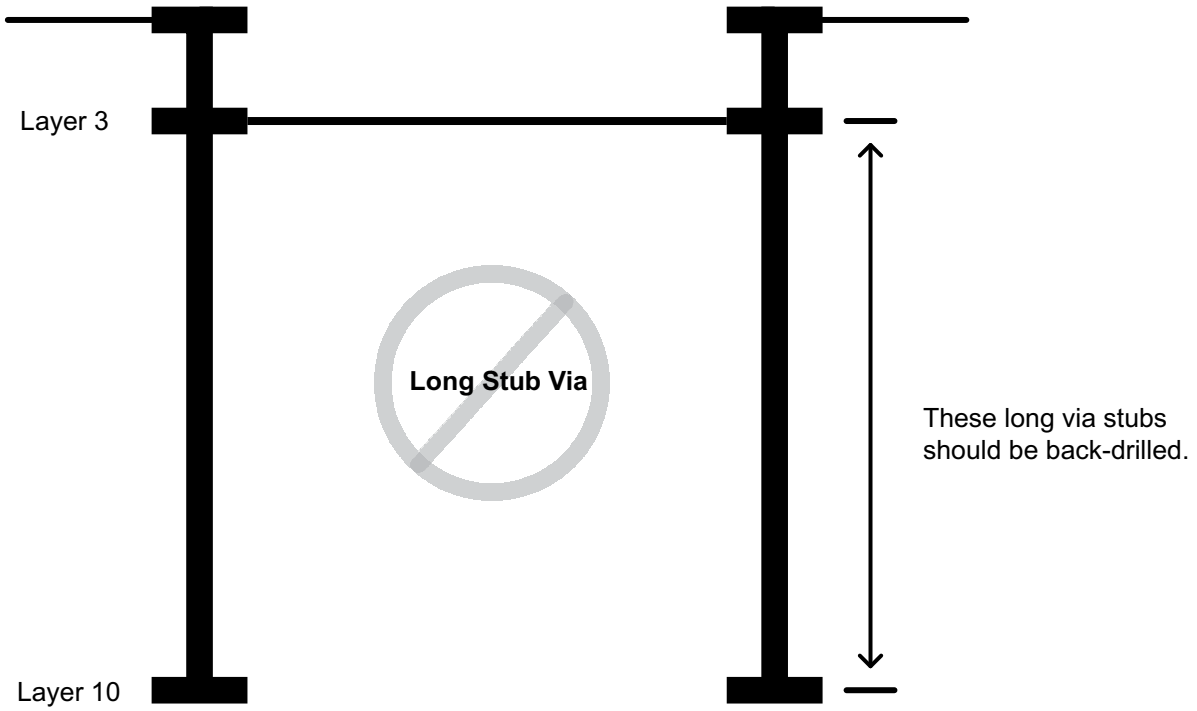

Figure 9-5. Via Length (Long Stub)

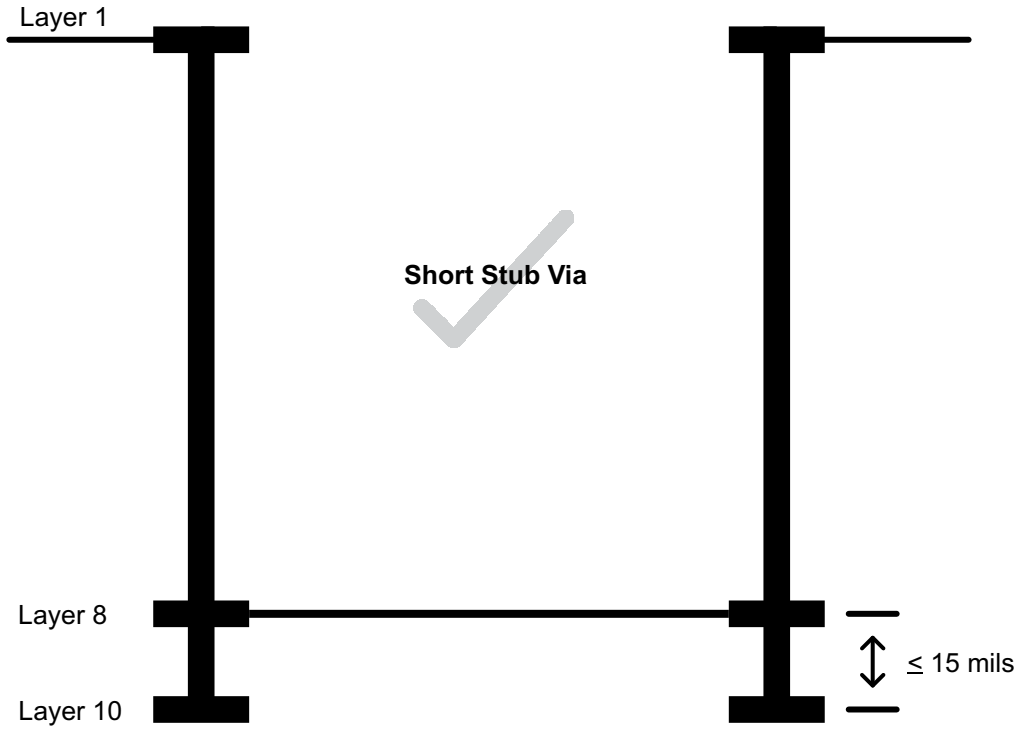

Figure 9-6. Via Length (Short Stub)

9.1.7 Surface-Mount Device Pad Discontinuity Mitigation

Avoid including surface-mount devices (SMDs) on high-speed signal traces because these devices introduce discontinuities that can negatively affect signal quality. When SMDs are required on the signal traces (for example, the USB SuperSpeed transmit AC coupling capacitors) the maximum permitted component size is 0603. TI strongly recommends using 0402 or smaller. Place these components symmetrically during the layout process to ensure optimum signal quality and to minimize reflection. For examples of correct and incorrect AC coupling capacitor placement, see Figure 9-7.

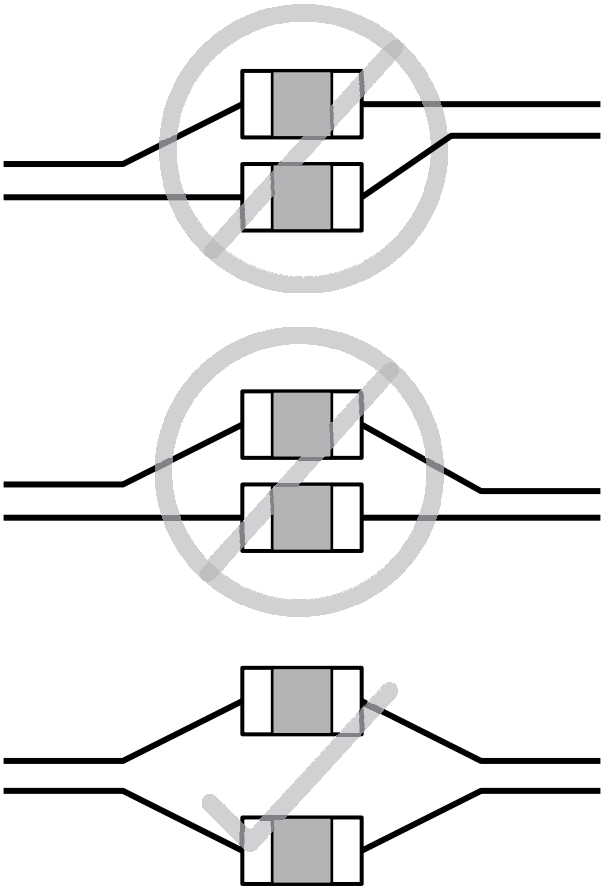

Figure 9-7. AC-Coupling Placement

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To minimize the discontinuities associated with the placement of these components on the differential signal traces, TI recommends partially voiding the SMD mounting pads of the reference plane by approximately 60% because this value strikes a balance between the capacitive effects of a 0% reference void and the inductive effects of a 100% reference void. This void should be at least two PCB layers deep. For an example of a reference plane voiding of surface mount devices, see Figure 9-8.

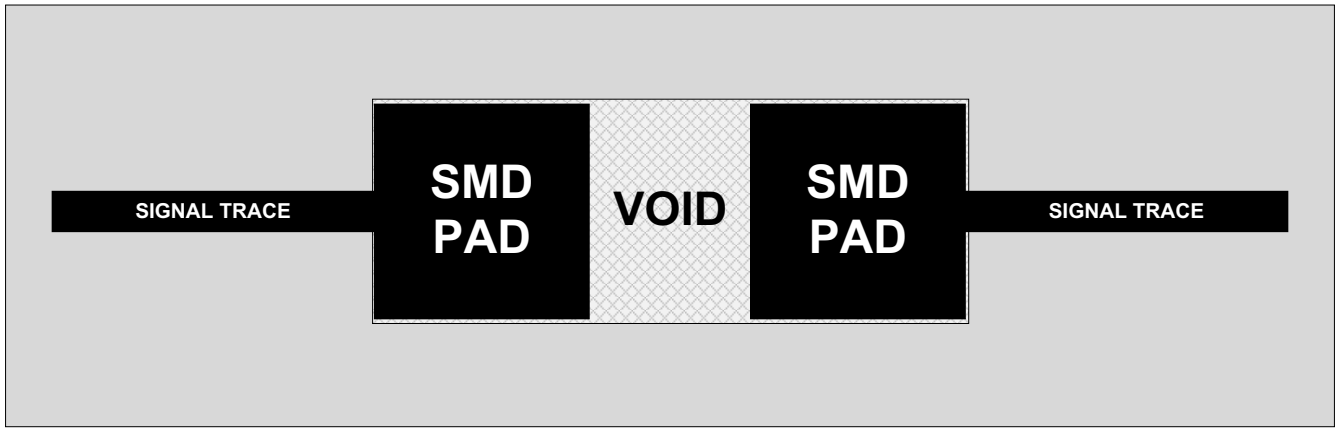

Figure 9-8. Reference Plane Voiding of Surface-Mount Devices

9.1.8 ESD/EMI Considerations

When choosing ESD/EMI components, TI recommends selecting devices that permit flow-through routing of the USB differential signal pair because they provide the cleanest routing. For example, the TI TPD4EUSB30 can be combined with the TI TPD2EUSB30 to provide flow-through ESD protection for both USB2 and USB3 differential signals without the need for bends in the signal pairs. For an example of flow-through routing, see Figure 9-9.

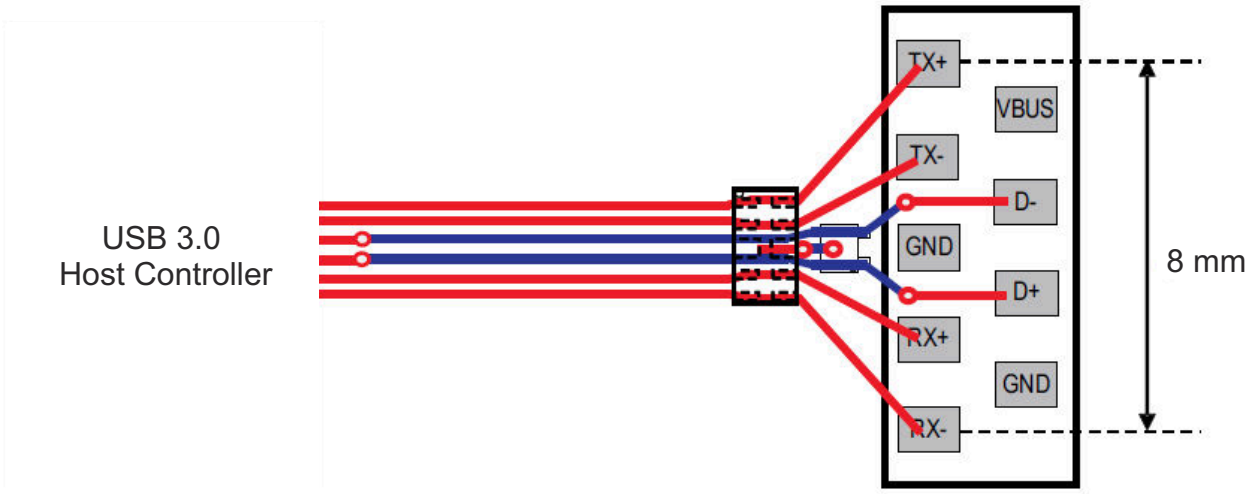

Figure 9-9. Flow-Through Routing

9.2 Layout

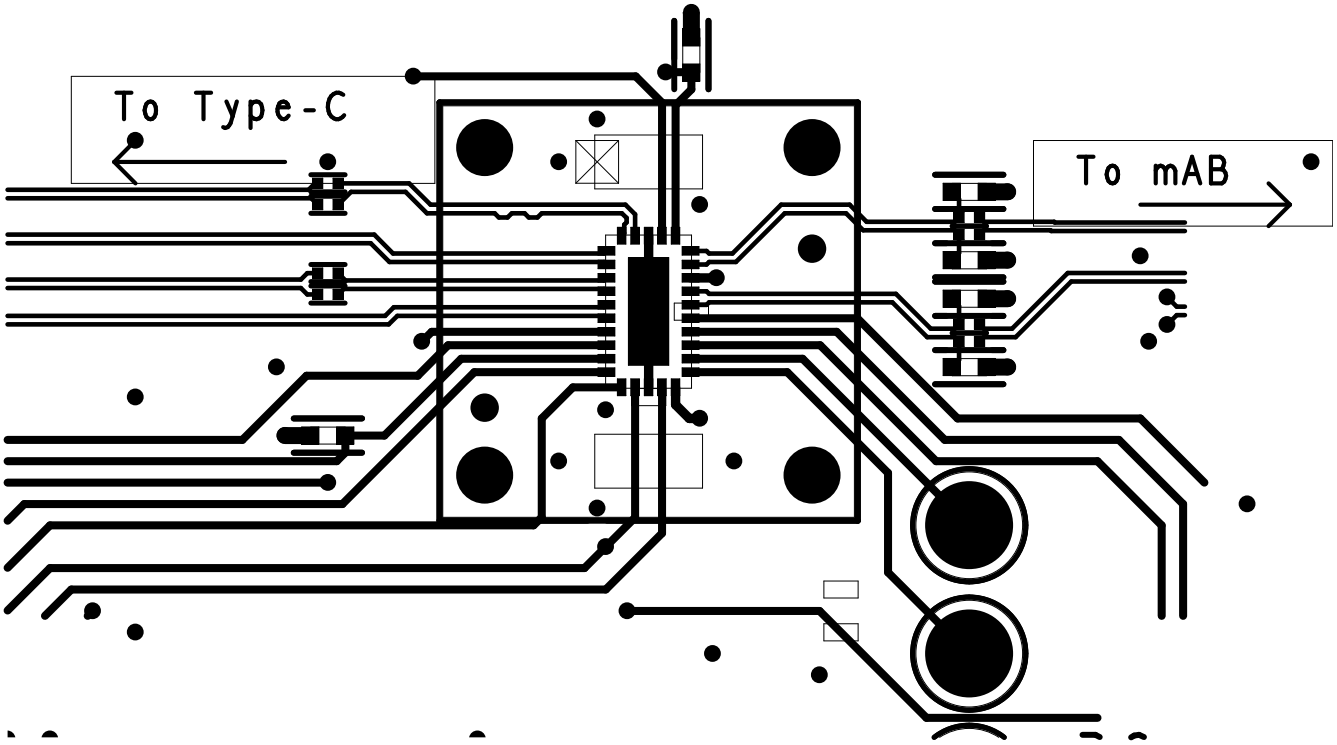

Figure 9-10. Layout Example

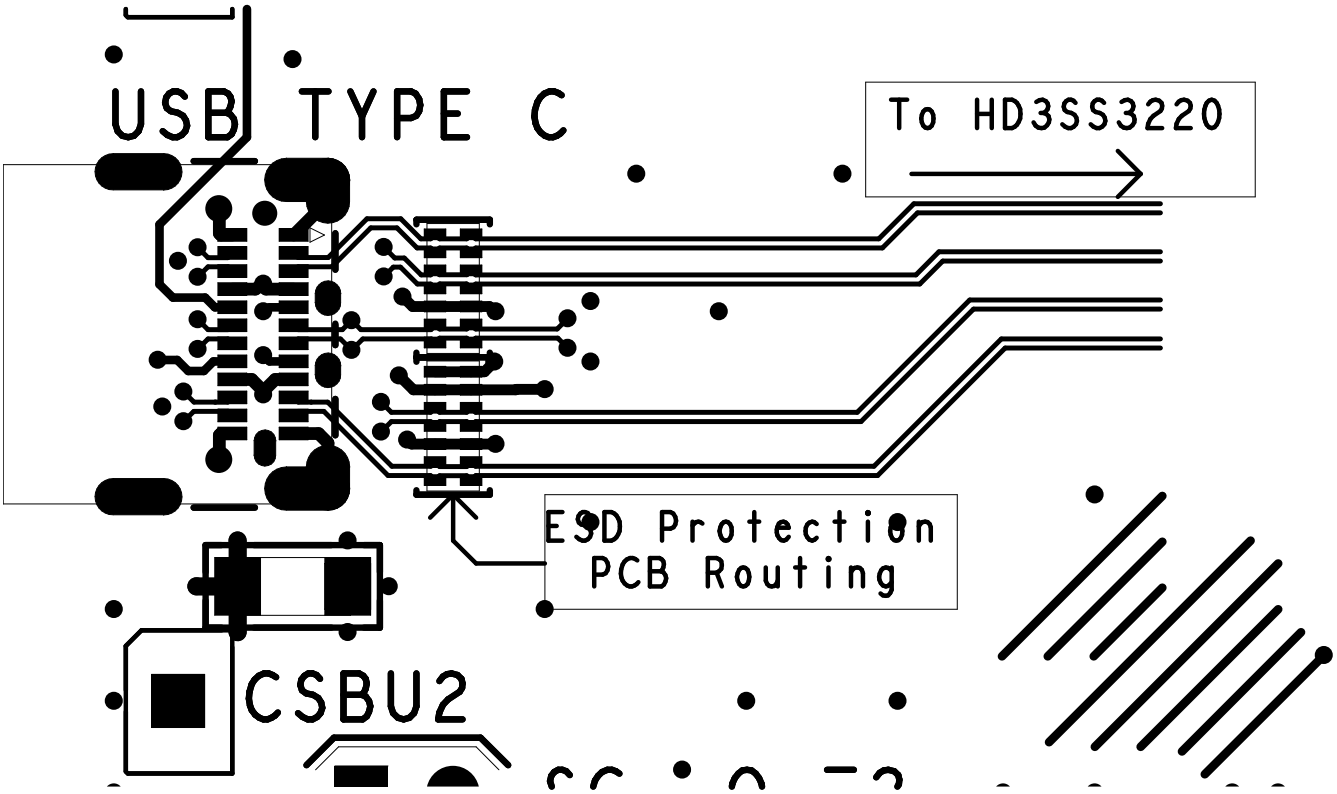

Figure 9-11. Layout Example 2

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10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Community Resources

10.3 Trademarks

All other trademarks are the property of their respective owners.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
HD3SS3220IRNHR	Active	Production	WQFN (RNH) | 30	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HD3220
HD3SS3220IRNHR.A	Active	Production	WQFN (RNH) | 30	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HD3220
HD3SS3220IRNHR.B	Active	Production	WQFN (RNH) | 30	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HD3220
HD3SS3220IRNHT	Active	Production	WQFN (RNH) | 30	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HD3220
HD3SS3220IRNHT.A	Active	Production	WQFN (RNH) | 30	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HD3220
HD3SS3220IRNHT.B	Active	Production	WQFN (RNH) | 30	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HD3220
HD3SS3220IRNHTG4	Active	Production	WQFN (RNH) | 30	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HD3220
HD3SS3220IRNHTG4.A	Active	Production	WQFN (RNH) | 30	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HD3220
HD3SS3220IRNHTG4.B	Active	Production	WQFN (RNH) | 30	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HD3220
HD3SS3220RNHR	Active	Production	WQFN (RNH) | 30	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	HD3220
HD3SS3220RNHR.A	Active	Production	WQFN (RNH) | 30	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	HD3220
HD3SS3220RNHR.B	Active	Production	WQFN (RNH) | 30	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	HD3220
HD3SS3220RNHT	Active	Production	WQFN (RNH) | 30	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	HD3220
HD3SS3220RNHT.A	Active	Production	WQFN (RNH) | 30	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	HD3220
HD3SS3220RNHT.B	Active	Production	WQFN (RNH) | 30	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	HD3220
HD3SS3220RNHTG4	Active	Production	WQFN (RNH) | 30	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HD3220
HD3SS3220RNHTG4.A	Active	Production	WQFN (RNH) | 30	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HD3220
HD3SS3220RNHTG4.B	Active	Production	WQFN (RNH) | 30	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HD3220

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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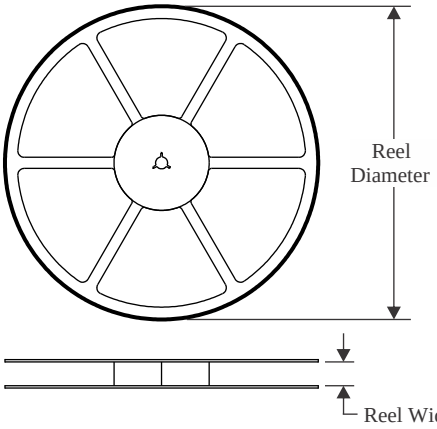
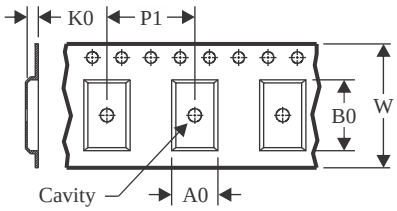
TAPE AND REEL INFORMATION

REEL DIMENSIONS

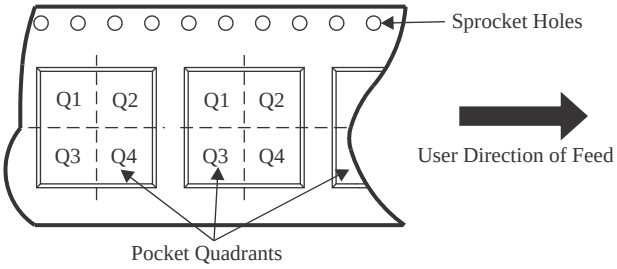


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

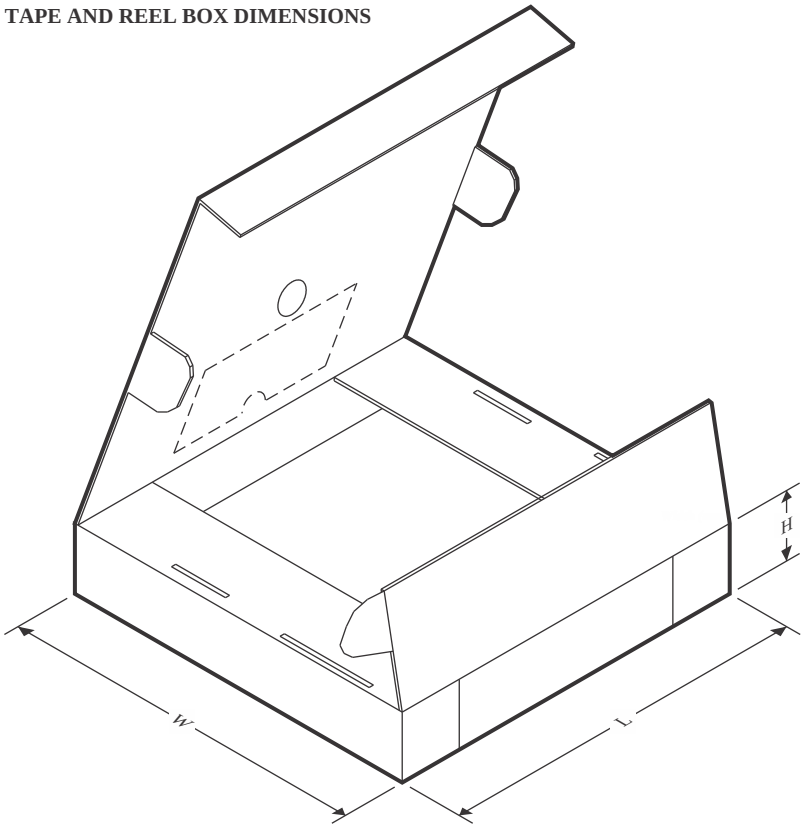
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
HD3SS3220IRNHR	WQFN	RNH	30	3000	330.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1
HD3SS3220IRNHR	WQFN	RNH	30	3000	330.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1
HD3SS3220IRNHT	WQFN	RNH	30	250	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1
HD3SS3220IRNHT	WQFN	RNH	30	250	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1
HD3SS3220IRNHTG4	WQFN	RNH	30	250	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1
HD3SS3220RNHR	WQFN	RNH	30	3000	330.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1
HD3SS3220RNHR	WQFN	RNH	30	3000	330.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1
HD3SS3220RNHT	WQFN	RNH	30	250	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1
HD3SS3220RNHT	WQFN	RNH	30	250	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1
HD3SS3220RNHTG4	WQFN	RNH	30	250	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

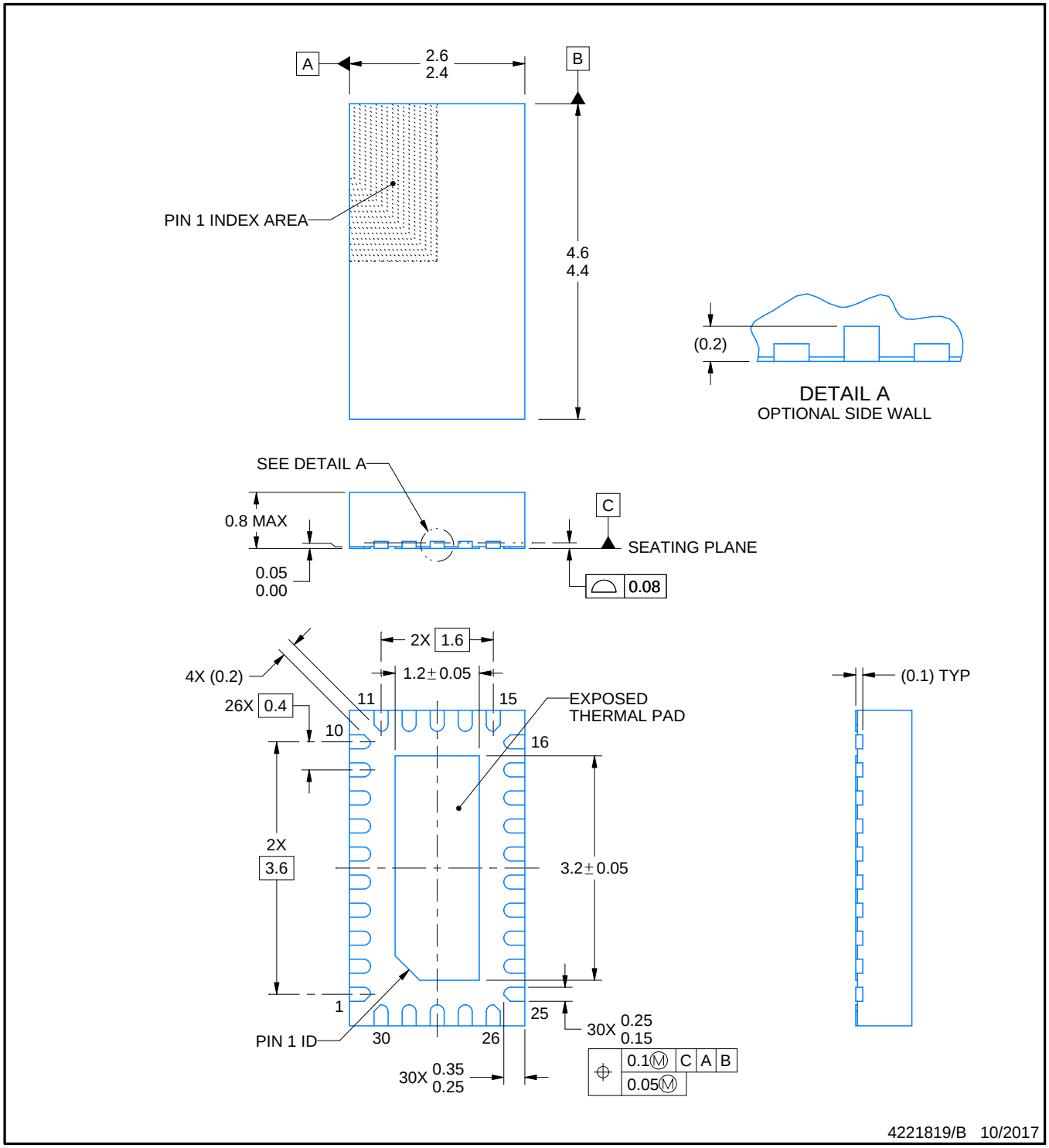
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
HD3SS3220IRNHR	WQFN	RNH	30	3000	367.0	367.0	35.0
HD3SS3220IRNHR	WQFN	RNH	30	3000	346.0	346.0	33.0
HD3SS3220IRNHT	WQFN	RNH	30	250	182.0	182.0	20.0
HD3SS3220IRNHT	WQFN	RNH	30	250	210.0	185.0	35.0
HD3SS3220IRNHTG4	WQFN	RNH	30	250	182.0	182.0	20.0
HD3SS3220RNHR	WQFN	RNH	30	3000	360.0	360.0	36.0
HD3SS3220RNHR	WQFN	RNH	30	3000	346.0	346.0	33.0
HD3SS3220RNHT	WQFN	RNH	30	250	182.0	182.0	20.0
HD3SS3220RNHT	WQFN	RNH	30	250	210.0	185.0	35.0
HD3SS3220RNHTG4	WQFN	RNH	30	250	182.0	182.0	20.0

PACKAGE OUTLINE

RNH0030A

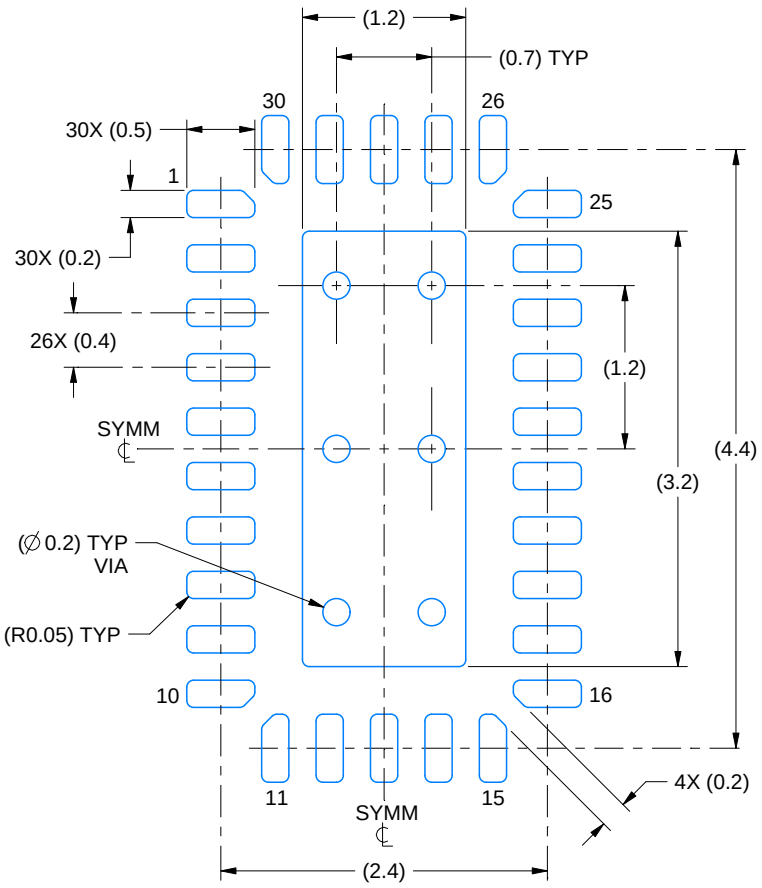
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

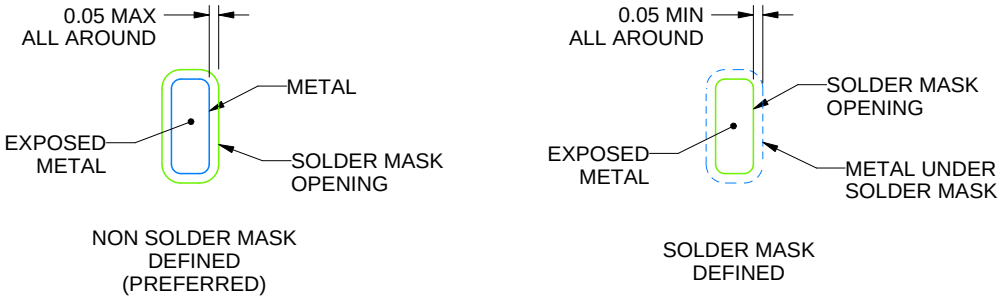


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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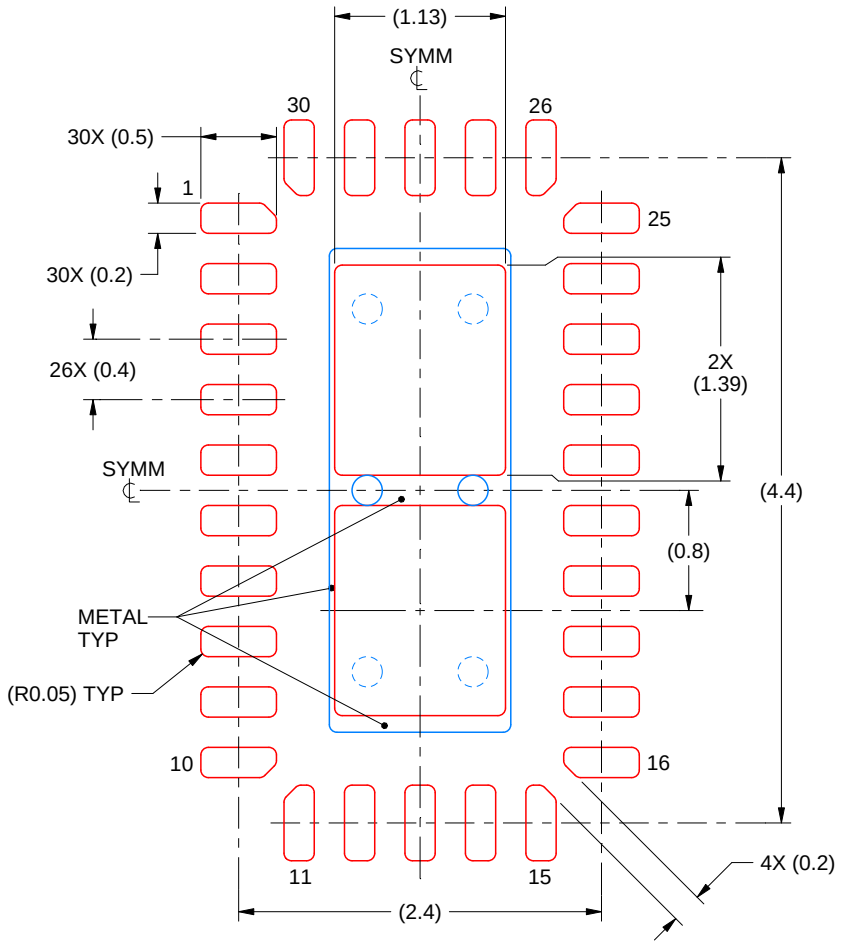
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
82% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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