

Single channel high-side switch



Product status link

[IPS1270H](#)

Product label



Features

- $R_{ON(max)}$ (@ $T_J = 25\text{ }^{\circ}\text{C}$) = $135\text{ m}\Omega$
- Very low standby current
- CMOS compatible input
- Thermal shutdown protection and diagnosis
- Undervoltage shutdown
- Overvoltage clamp
- Output voltage clamp
- Load current limitation
- Reverse polarity protection
- Electrostatic discharge protection
- Designed to drive DC-13 loads according to EN 60947-5-1
- Designed to meet IEC 61131-2, IEC 61000-4-2, IEC 61000-4-4, IEC 61000-4-5
- ECOPACK[®]: lead free and RoHS compliant
- SO8 Package

Application

- Programmable logic control
- Industrial PC peripheral input/output
- Numerical control machines

Description

The **IPS1270H** is monolithic device made by using STMicroelectronics[™] VIPower[™] M0-3 technology, intended for driving any kind of load with one side connected to ground.

Active VCC pin voltage clamp protects the device against low energy spikes.

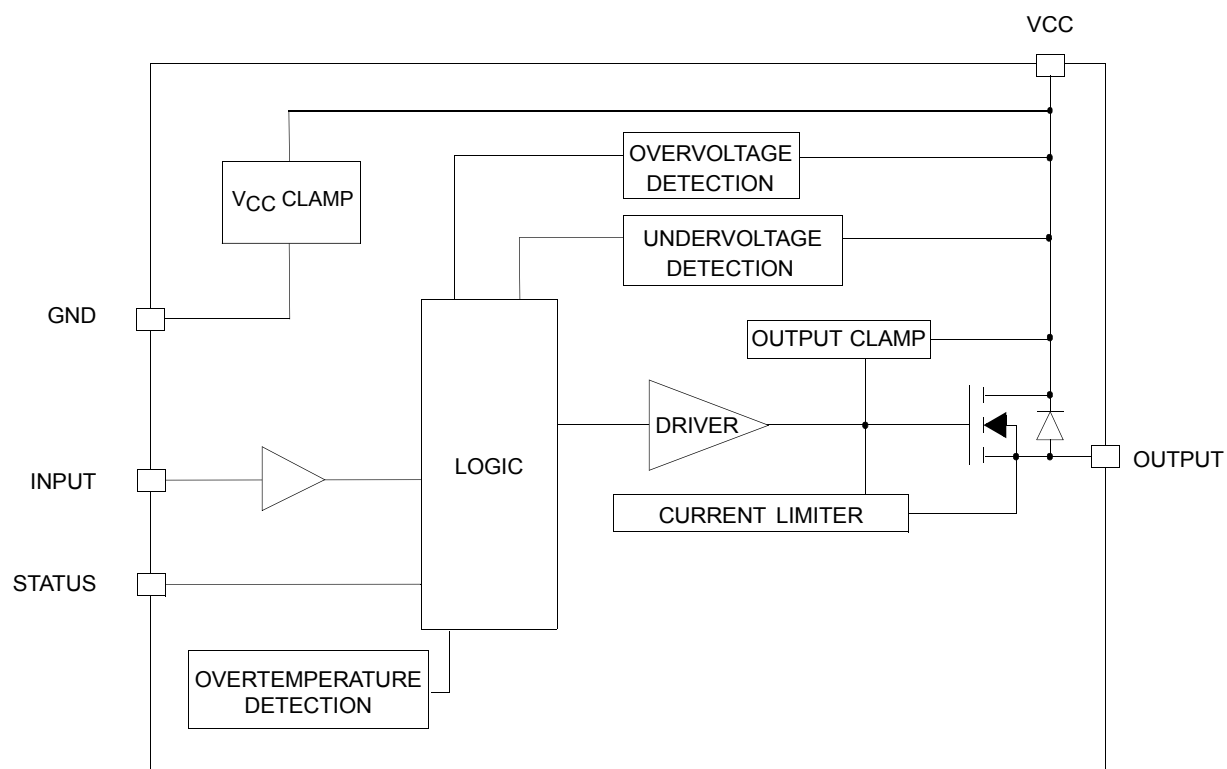
Active current limitation combined with thermal shutdown and automatic restart protect the device against overload.

Active output clamp protects the device against negative voltage at switch-off of inductive loads.

Device automatically turns off in case of ground pin disconnection.

1 Block diagram

Figure 1. Block diagram



2 Pin connection

Figure 2. Pin connection (top view)

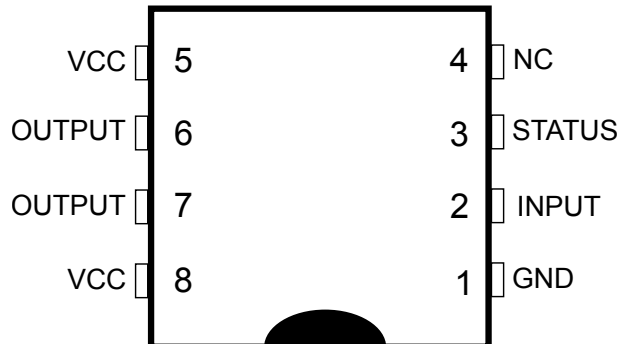


Table 1. Pin function

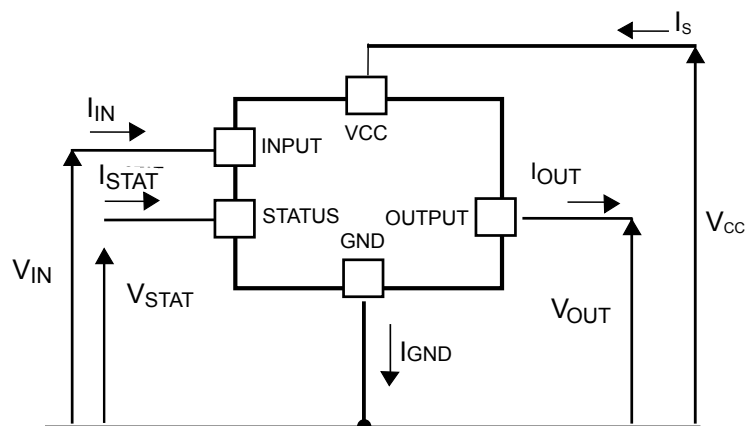
Pin	Name	Type	Function
1	GND	Supply	Ground connection
2	INPUT	Logic input	Voltage controlled input pin with hysteresis. CMOS compatible. It controls embedded output switch state
3	STATUS	Output	Embedded channel overtemperature status (active low)
4	NC	Not connected	
5, 8	VCC	Supply	Power supply
6, 7	OUTPUT	Analog output	Power output

Table 2. Suggested connections for unused and not connected pins

Connection/pin	Status	N.C.	Output	Input
Floating	X	X	X	X
To ground	Not recommended	X	Not recommended	Through 10 KΩ resistor

Note: X = don't care

Figure 3. Current and voltage conventions



3 Maximum rating

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	0.3	V
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	6	A
I_{IN}	DC input current	± 10	mA
V_{IN}	Input voltage range	$-3 / V_{CC}$	V
V_{STAT}	DC status voltage	V_{CC}	V
V_{ESD}	Electrostatic discharge (R = 1.5 k Ω ; C = 100 pF)		
	Input	4000	V
	Status	4000	V
	Output	5000	V
	V_{CC}	5000	V
P_{TOT}	Power dissipation @ $T_{CASE} = 25\text{ }^{\circ}\text{C}$	4.2	W
E_{MAX}	Maximum switching energy L = 77.5 mH; $R_L = 0\text{ }\Omega$; $V_{CC} = 13.5\text{ V}$; $T_{jstart} = 150\text{ }^{\circ}\text{C}$; $I_L = 1.5\text{ A}$	121	mJ
T_J	Junction operating temperature	Internally limited	$^{\circ}\text{C}$
T_{CASE}	Case operating temperature	- 40 to 150	$^{\circ}\text{C}$
T_{STG}	Storage temperature	- 55 to 150	$^{\circ}\text{C}$

Table 4. Thermal data

Symbol	Parameter		Value	Unit
$R_{th(j-lead)}$	Thermal resistance junction-lead	Max.	30	$^{\circ}\text{C/W}$
$R_{th(j-amb)}$	Thermal resistance junction-ambient	Max.	93 ⁽¹⁾	$^{\circ}\text{C/W}$
			82 ⁽²⁾	

1. When mounted on FR4 printed circuit board with 0.5 cm² of copper area (at least 35 μm thick) connected to all VCC pins.
2. When mounted on FR4 printed circuit board with 2 cm² of copper area (at least 35 μm thick).

4 Electrical characteristics

8 V < V_{CC} < 36 V; -40 °C < T_J < 150 °C; unless otherwise specified

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{CC}	Operating supply voltage		5.5		36	V
V _{CC CLAMP}	Clamp on V _{CC}		47	52	57	V
V _{USD}	Undervoltage shutdown		3	4	5.5	V
V _{OV}	Overvoltage shutdown		36	42		V
R _{ON}	On-state resistance	I _{OUT} = 0.5 A @ T _J = 25 °C			135	mΩ
		I _{OUT} = 0.5 A			270	mΩ
I _S	Supply current	Off-state, V _{CC} = 24 V, T _{CASE} = 25 °C		10	20	μA
		On-state, V _{CC} = 24 V, T _{CASE} = 25 °C		1.5		mA
		On-state, V _{CC} = 24 V			2.6	mA
I _{LGND}	Output current at turn-off	V _{CC} = V _{STAT} = V _{IN} = V _{GND} = 24 V; V _{OUT} = 0 V			0.5	mA
I _{L(off1)}	Off-state output current	V _{IN} = V _{OUT} = 0 V	0		50	μA
I _{L(off2)}	Off-state output current	V _{IN} = V _{OUT} = 0 V; V _{CC} = 13 V; T _J = 125 °C			5	μA
I _{L(off3)}	Off-state output current	V _{IN} = V _{OUT} = 0 V; V _{CC} = 13 V; T _J = 25 °C			3	μA

Table 6. Switching (V_{CC} = 24 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(ON)}	Turn-on delay time	R _L = 48 Ω from V _{IN} rising edge to V _{OUT} = 2.4 V		10		μs
t _{d(OFF)}	Turn-off delay time	R _L = 48 Ω from V _{IN} falling edge to V _{OUT} = 21.6 V		40		μs
dV _{OUT} /dt _(on)	Turn-on voltage slope	R _L = 48 Ω from V _{OUT} = 2.4 V to V _{OUT} = 19.2 V (see also Figure 17)		810		V/ms
dV _{OUT} /dt _(off)	Turn-off voltage slope	R _L = 48 Ω from V _{OUT} = 21.6 V to V _{OUT} = 2.4 V (see also Figure 20)		330		

Figure 4. Switching time waveforms

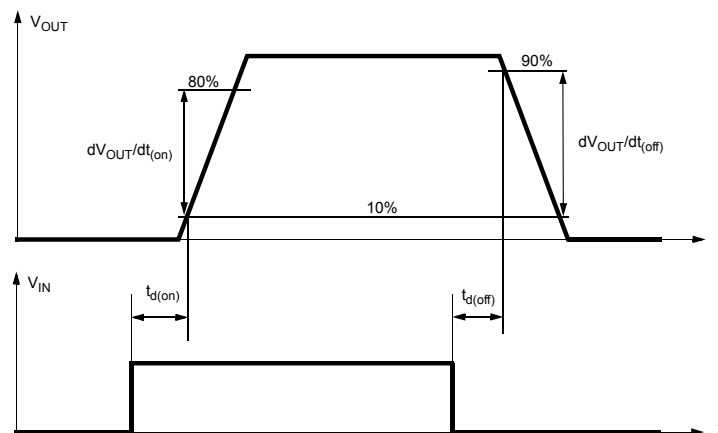


Table 7. INPUT pin

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{INL}	INPUT pin low level				1.25	V
I_{INL}	Low level INPUT pin current	$V_{IN} = 1.25\text{ V}$	1			μA
V_{INH}	INPUT pin high level		3.25			V
I_{INH}	High level INPUT pin current	$V_{IN} = 3.25\text{ V}$			10	μA
V_{INHYS}	INPUT pin hysteresis voltage		0.5			V
I_{IN}	INPUT pin current	$V_{IN} = V_{CC} = 36\text{ V}$			200	μA

Table 8. VCC - OUTPUT diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_F	Forward on voltage	$-I_{OUT} = 0.6\text{ A}$; $T_j = 150\text{ }^\circ\text{C}$			0.6	V

Table 9. STATUS pin

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{STAT}	STATUS pin low output voltage	$I_{STAT} = 1.6\text{ mA}$			0.5	V
I_{LSTAT}	STATUS pin leakage current	Normal operation; $V_{STAT} = V_{CC} = 36\text{ V}$			10	μA
C_{STAT}	STATUS pin input capacitance	Normal operation; $V_{STAT} = 5\text{ V}$			30	pF

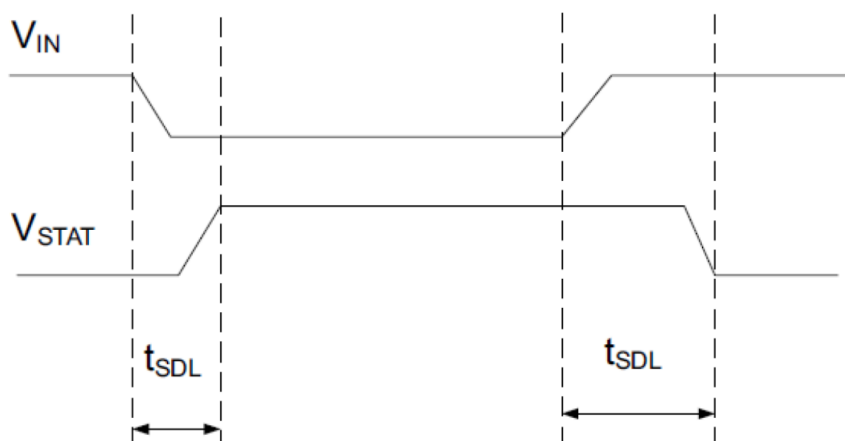
Figure 5. Overtemperature status timing ($T_j > T_{TSD}$)


Table 10. Protections⁽¹⁾

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		135			°C
T_{hyst}	Thermal hysteresis		7	15		°C
t_{SDL}	Status delay in overload condition	$T_J > T_{TSD}$			20	μs
I_{lim}	DC short circuit current	$V_{CC} = 24\text{ V}$; $R_{LOAD} = 10\text{ m}\Omega$	0.7		2	A
V_{DEMAG}	Turn-off output clamp voltage	$I_{OUT} = 24\text{ V}$; $L = 6\text{ mH}$	$V_{CC} - 47$	$V_{CC} - 52$	$V_{CC} - 57$	V

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

5 Protections

5.1 Current limitation

The device is equipped with an output current limiter in order to protect the silicon from excessive current flow. Consequently, in case of short-circuit or overload, the output current is clamped to a safety level, I_{lim} .

5.2 Thermal shutdown

In case the junction temperature of the device exceeds the thermal shutdown threshold T_{TSD} , it automatically switches off and the STATUS pin goes low.

The embedded channel turns OFF and back ON automatically in order to maintain its junction temperature between T_{TSD} and T_R .

The STATUS pin moves consistently with the embedded channel state.

5.3 Negative output voltage clamp

In case the device drives inductive load, the output voltage reaches a negative value during turn off. A negative voltage clamp structure limits the maximum negative voltage to V_{DEMAG} , allowing the inductor energy to be dissipated without damaging the device (see also [Section 10](#)).

6 Signals waveform and functional table

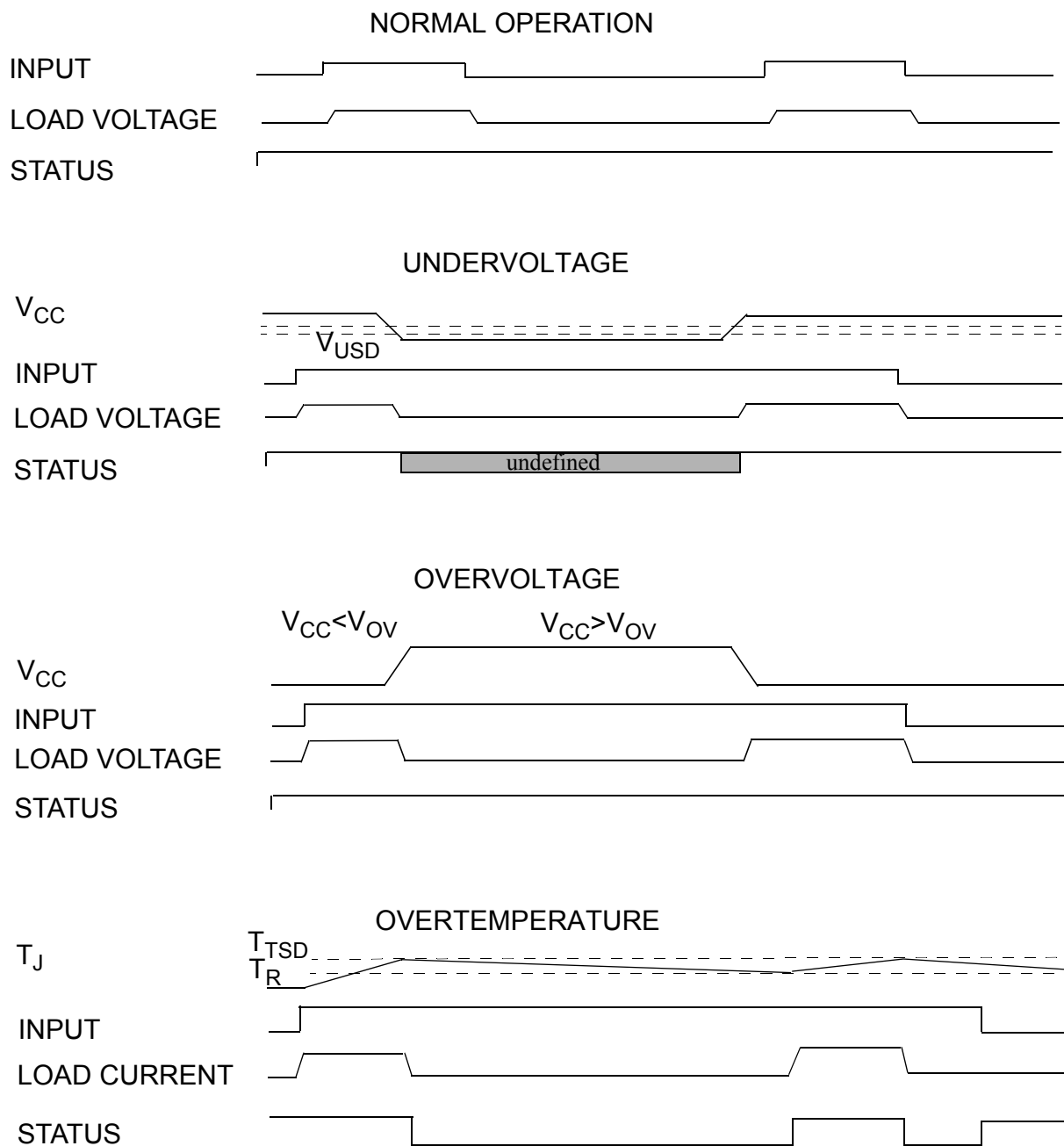
Figure 6. Waveforms


Table 11. Functional table

Device status	Input	Output	Status
Normal operation	L	L	H
	H	H	H
Current limitation	L	L	H
	H	X ⁽¹⁾	(T _J < T _{TSD}) H
	H	X	(T _J > T _{TSD}) L
Overtemperature	L	L	H
	H	L	L
Undervoltage	L	L	X
	H	L	X
Overvoltage	L	L	H
	H	L	H

1. X = don't care

7 Test circuits

Figure 7. I_{lim} short-circuit current

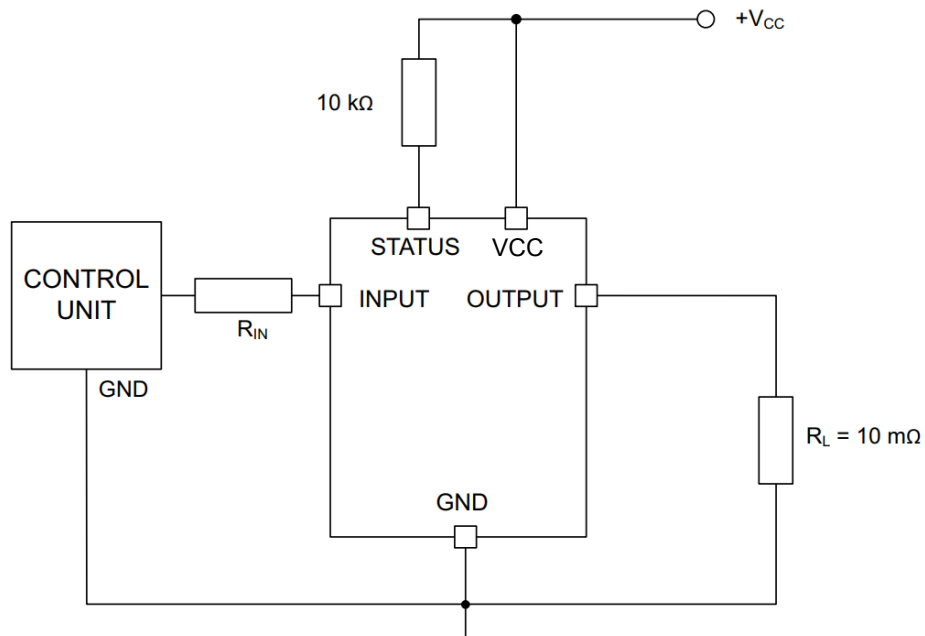
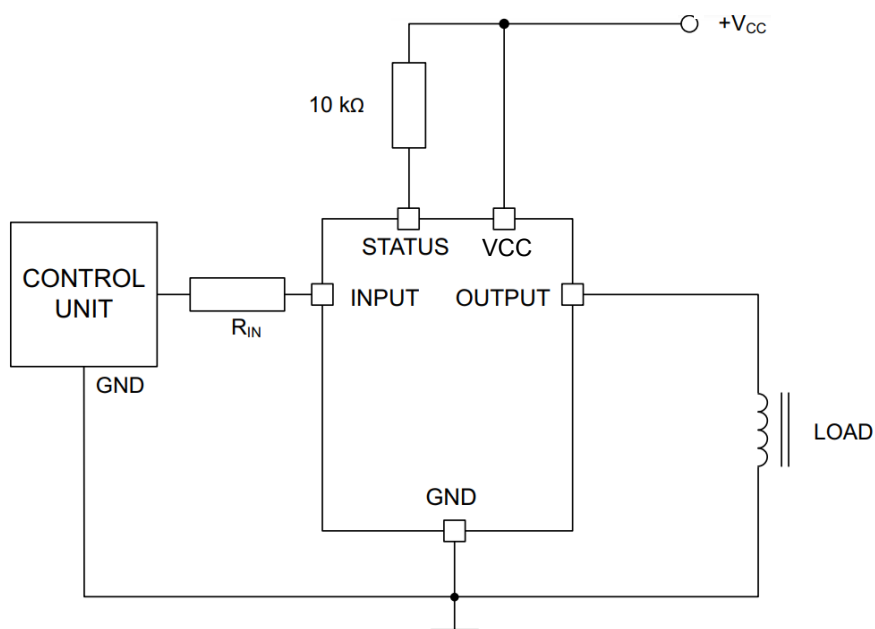
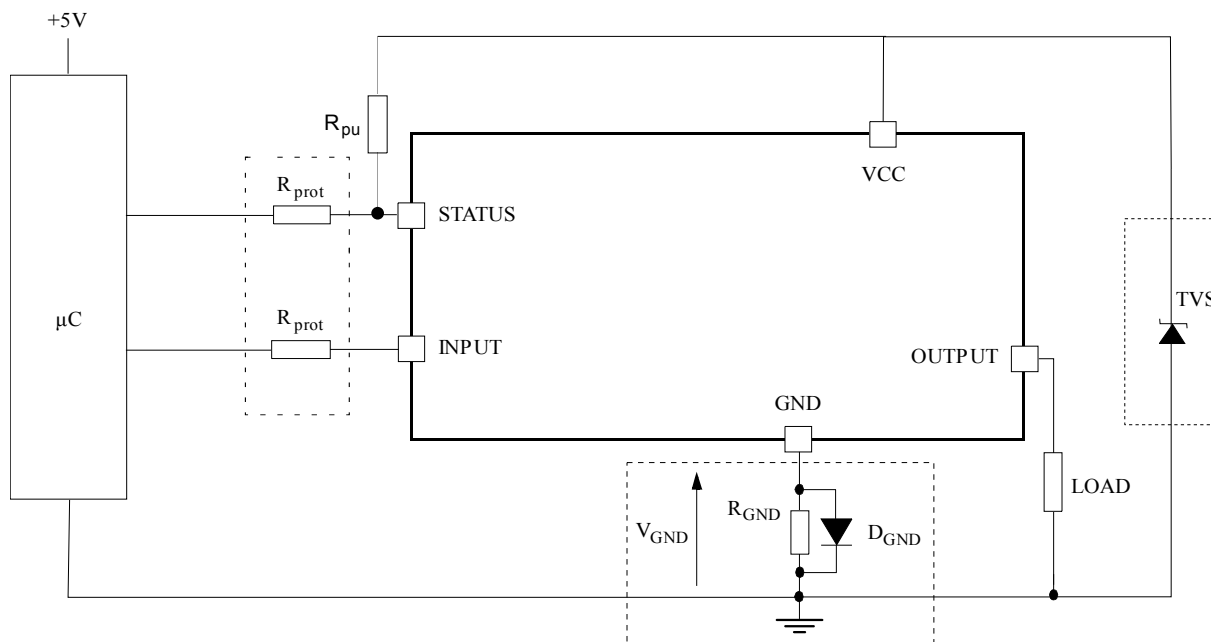


Figure 8. Avalanche energy



8 Application schematics

Figure 9. Application schematic



8.1 Reverse polarity protection

Reverse polarity protection can be implemented on the board using two different solutions:

1. Placing a resistor (R_{GND}) between the IC GND pin and load GND
2. Placing a diode between the IC GND pin and load GND

If option 1 is selected, the minimum resistance value has to be selected according to the following equation:

Equation 1:

$$R_{GND} \geq V_{CC} / I_{GND}$$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power dissipated by R_{GND} (when $V_{CC} < 0$: during reverse polarity situations) is:

Equation 2:

$$P_D = (V_{CC})^2 / R_{GND}$$

If option 2 is selected, the diode has to be chosen by taking into account $V_{RRM} > |V_{CC}|$ and its power dissipation capability:

Equation 3:

$$P_D \geq I_S * V_F$$

A resistor ($R_{GND} = 1 \text{ k}\Omega$) should be inserted in parallel to D_{GND} if the device is driving an inductive load.

Note: In normal conditions (no reverse polarity), due to the diode there is a voltage drop between GND of the device and GND of the system.

8.2 Microcontroller I/Os protection

If a ground protection network is used and negative transients are present on the VCC line, the control pins are pulled negative.

ST suggests to insert a resistor (R_{prot}) in line to prevent the microcontroller I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

For $V_{CCpeak} = -100\text{ V}$ and $I_{latchup} \geq 20\text{ mA}$; $V_{OH\mu C} \geq 4.5\text{ V}$:

$$5\text{ k}\Omega \leq R_{prot} \leq 65\text{ k}\Omega$$

Recommended R_{prot} value is 10 k Ω .

8.3 Vcc overshoot protection

To protect the device from supply rail overshoot, a TVS is inserted between VCC and GND.

It will be chosen to protect the circuit but not interferes with its normal operations.

For this reason, the TVS must be selected with appropriate V_{BR} and V_{CL} values for the maximum operating voltage of the application.

9 Electrical characteristics curves

Figure 10. Off-state OUTPUT pin current

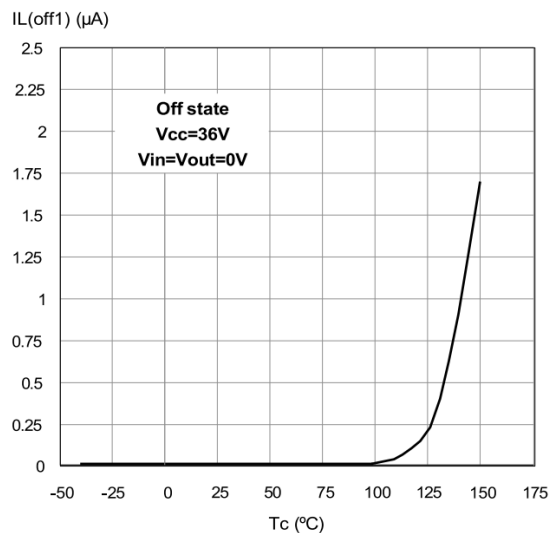


Figure 11. High level INPUT pin current

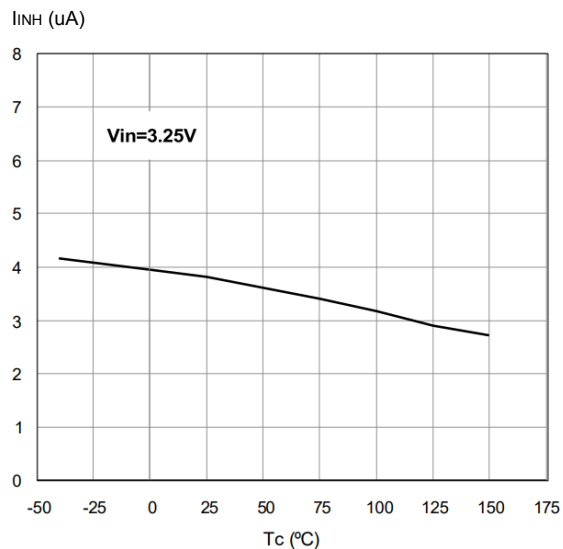


Figure 12. STATUS pin leakage current

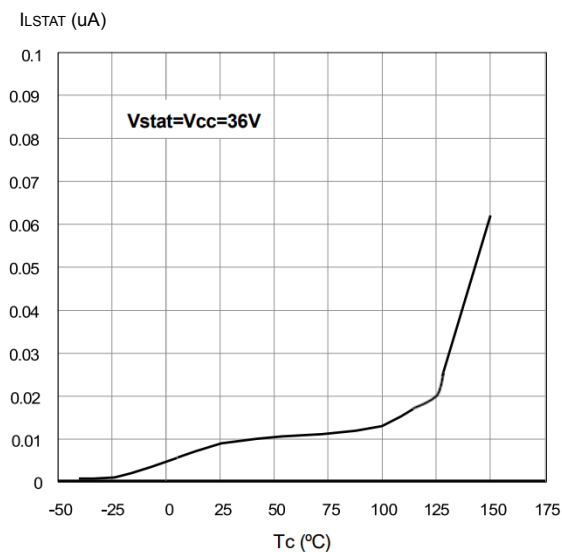


Figure 13. On-state resistance vs T_{CASE}

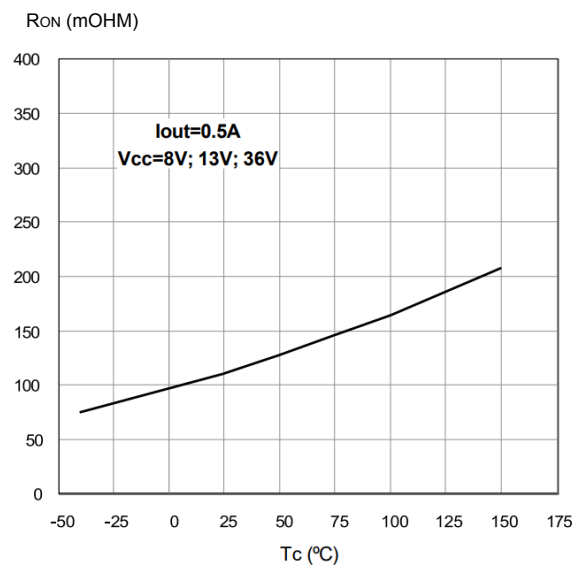


Figure 14. On-state resistance vs V_{CC}

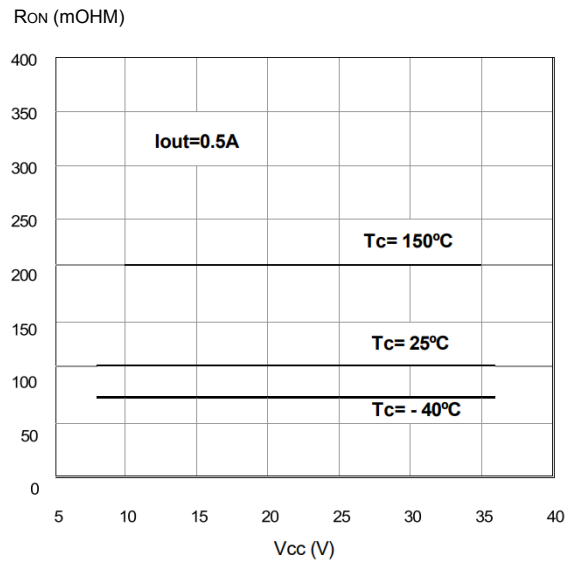


Figure 15. INPUT pin high level

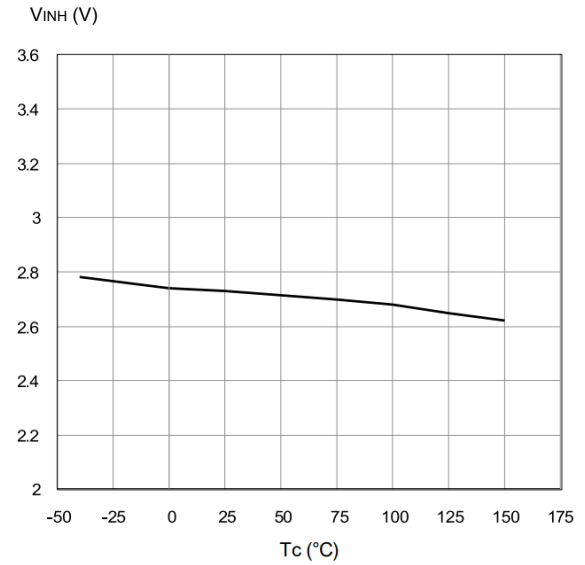


Figure 16. INPUT pin low level

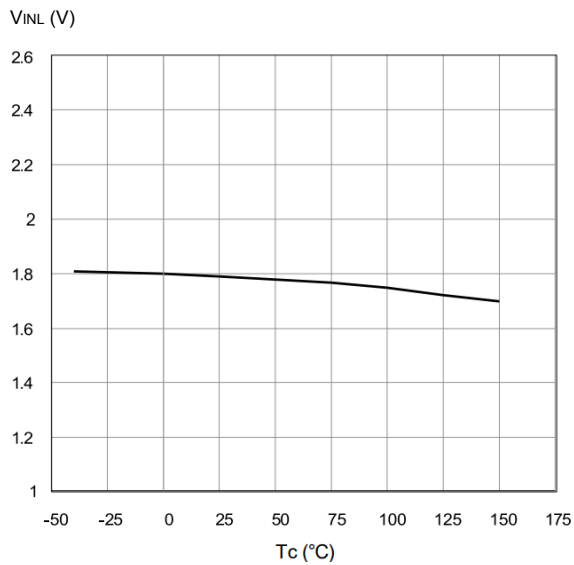


Figure 17. Turn-on output voltage slope

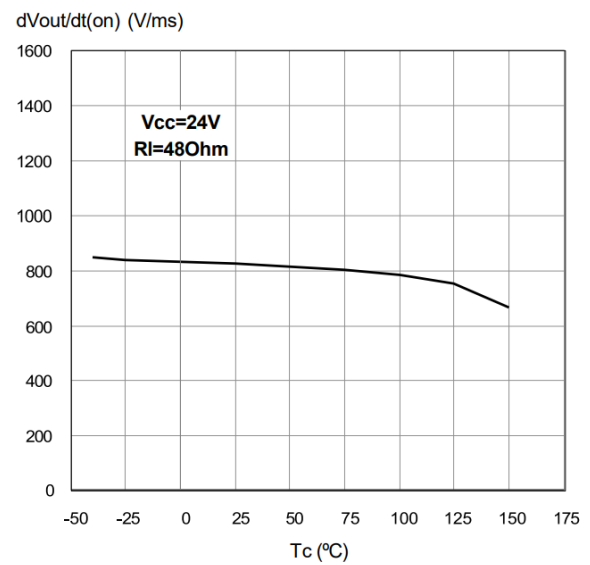


Figure 18. Output overvoltage shutdown

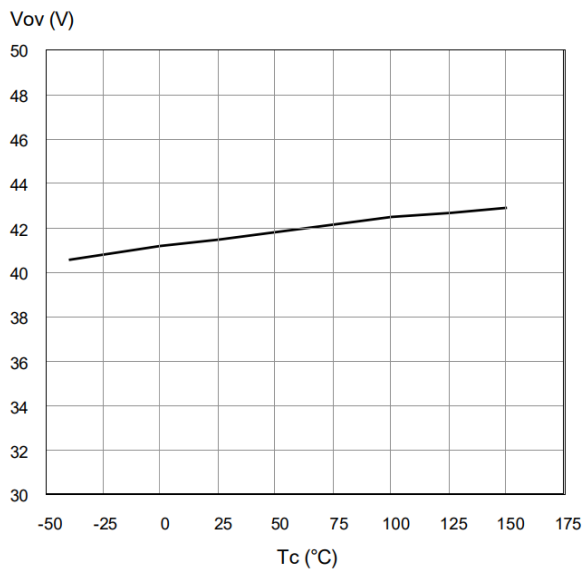


Figure 19. INPUT pin hysteresis voltage

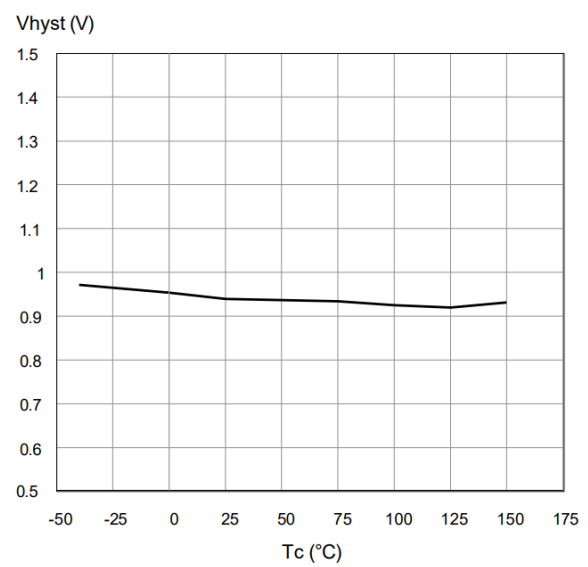


Figure 20. Turn-off output voltage slope

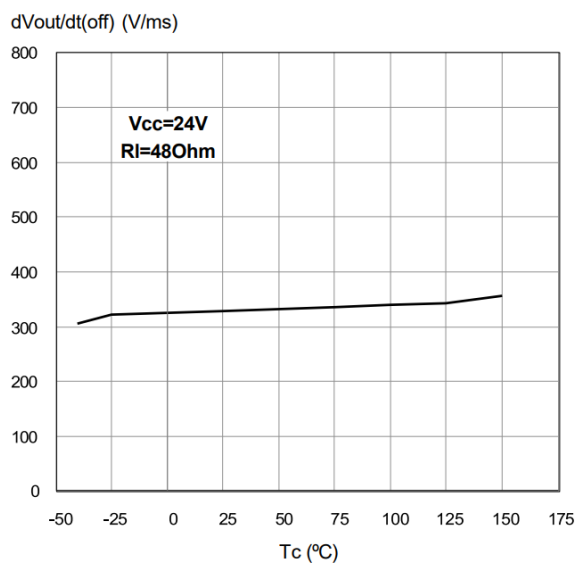
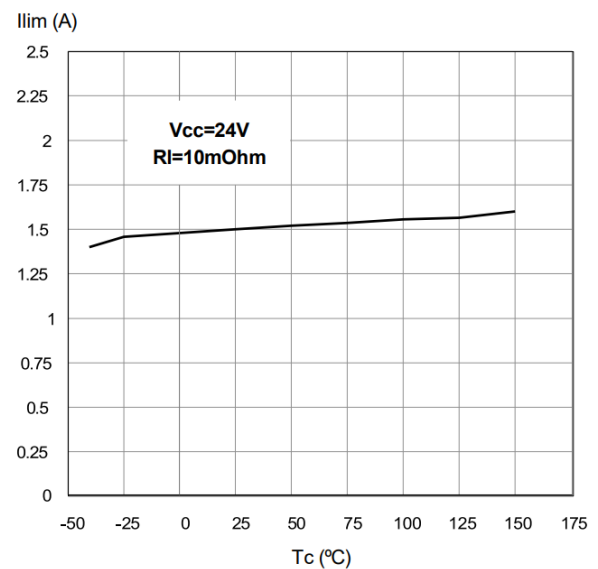


Figure 21. I_{lim} vs T_{CASE}



10 Active clamp

Active clamp is also known as **Fast Demagnetization of inductive loads** or **Fast Current Decay**. When a high-side driver turns off an inductance, an undervoltage on the output is detected (see Figure 22).

The OUTPUT pin is pulled down to V_{DEMAG} . The conduction state is modulated by an internal circuitry in order to keep the OUTPUT pin voltage at $\sim V_{\text{DEMAG}}$ until the load energy has been dissipated. The energy is dissipated in both IC internal switch and load resistance.

Figure 22. Active OUTPUT clamp typical waveforms

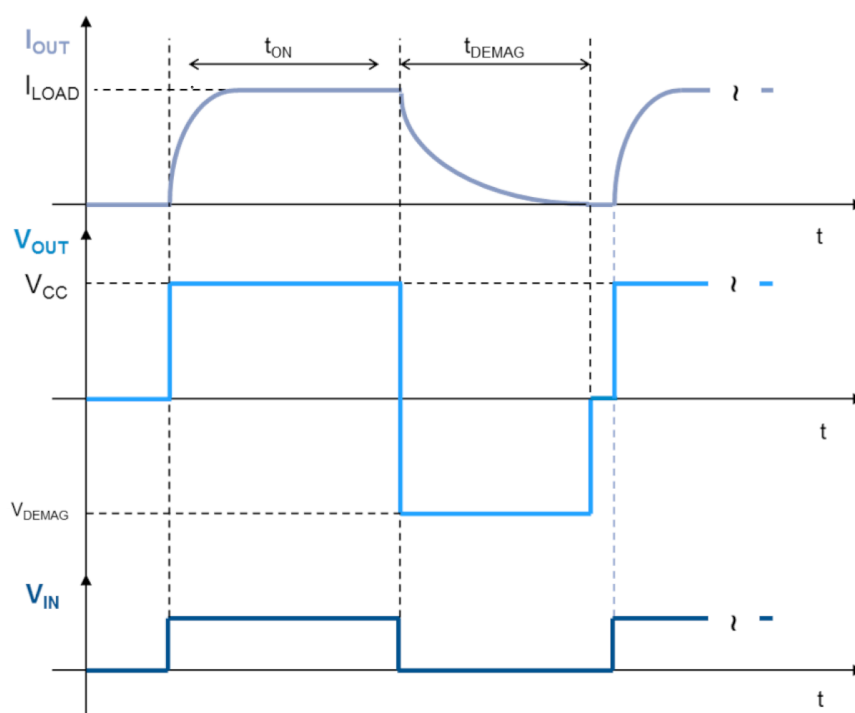
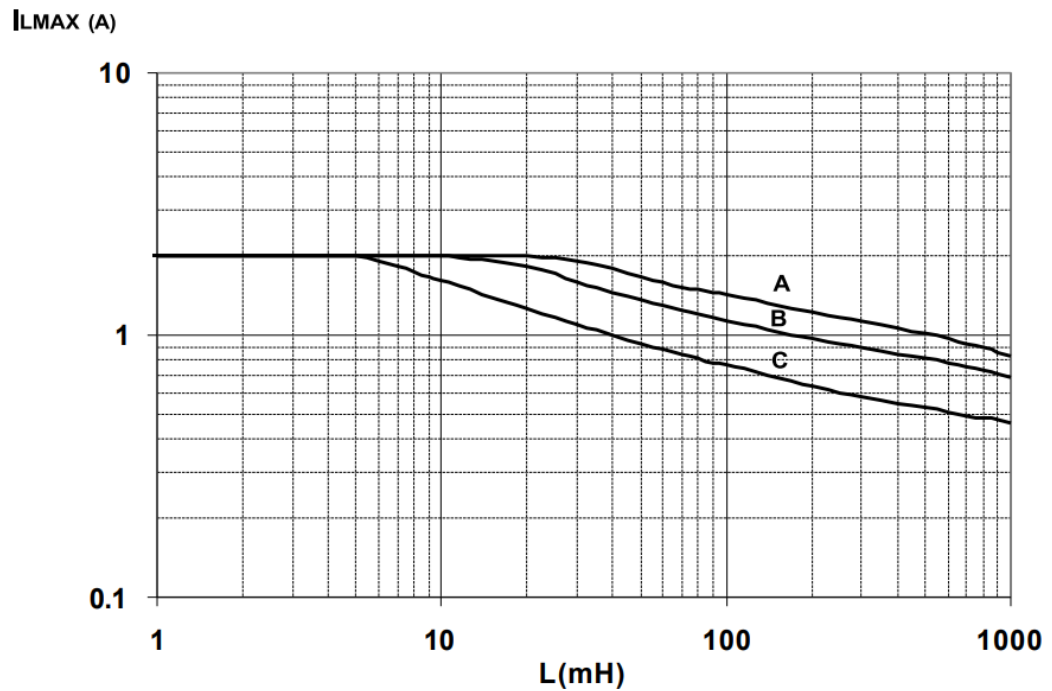


Figure 23. Maximum turn off current versus inductance



Note:

Legenda

A = Single pulse at $T_{jstart} = 150\text{ °C}$

B = Repetitive pulse at $T_{jstart} = 100\text{ °C}$

C = Repetitive Pulse at $T_{jstart} = 125\text{ °C}$

Conditions:

$V_{CC} = 13.5\text{ V}$

Values are generated with $R_L = 0\text{ }\Omega$

In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

11 Package and PCB thermal data

Figure 24. SO-8 PC board



Figure 25. SO-8 $R_{thj-amb}$ vs PCB copper area in open box free air condition

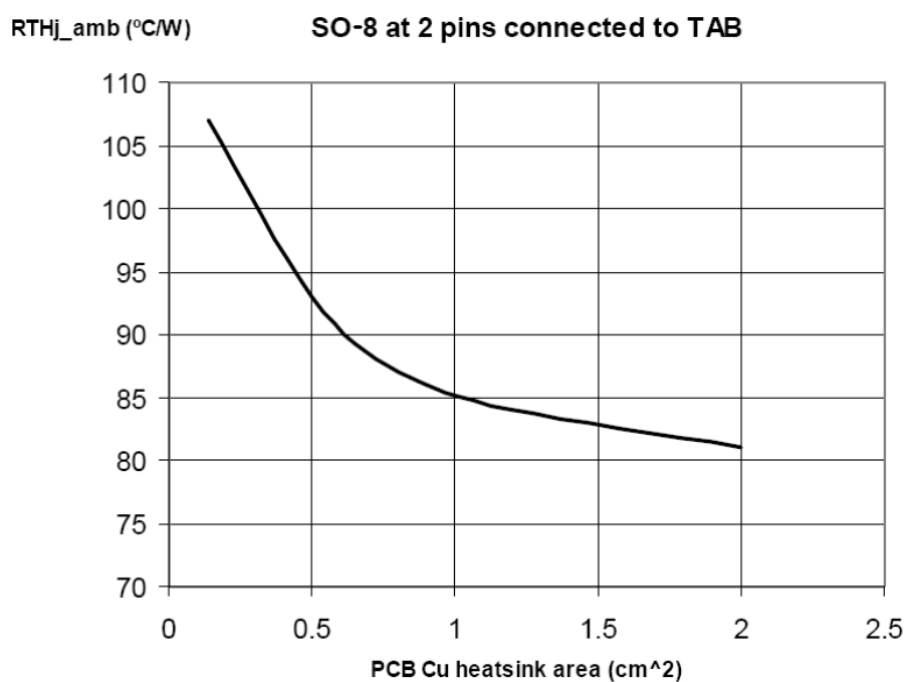


Figure 26. SO-8 thermal impedance junction ambient single pulse

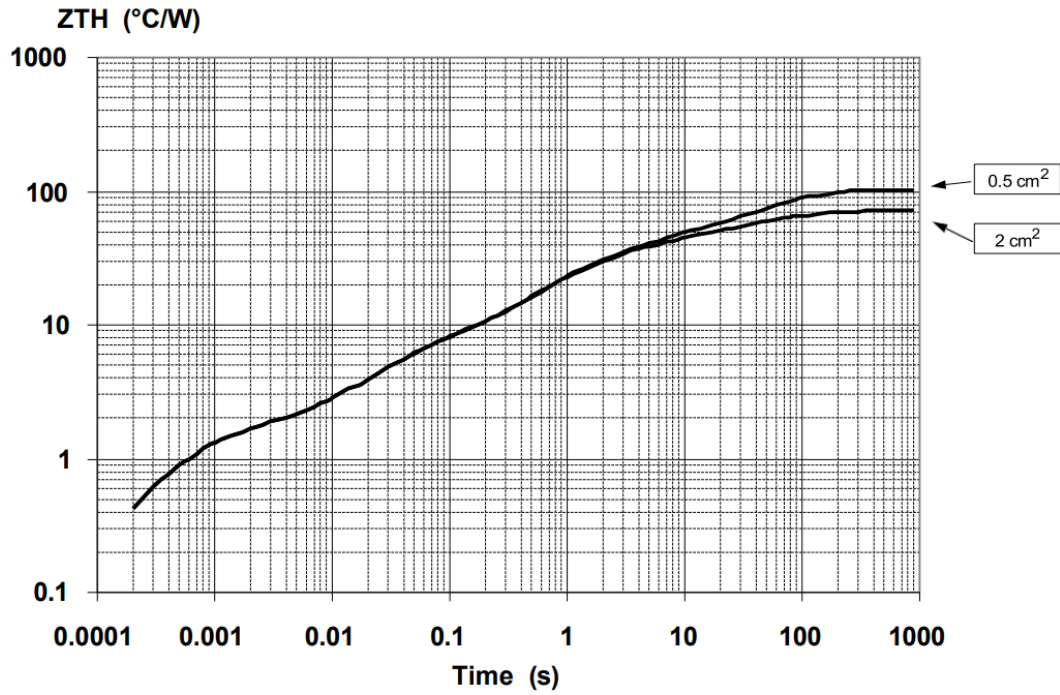
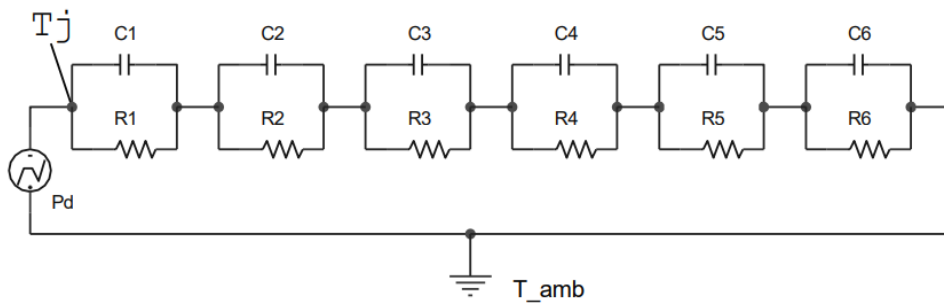


Figure 27. Thermal fitting model of a single channel HSD in SO-8



Pulse calculation formula:

$$Z_{TH\delta} = R_{TH} * \delta + Z_{THtp} (1 - \delta)$$

where:

$$\delta = t_p / T$$

Table 12. Thermal parameter

Area/island (cm ²)	0.14	2
R1 (°C/W)	0.24	
R2 (°C/W)	1.2	
R3 (°C/W)	4.5	
R4 (°C/W)	21	
R5 (°C/W)	16	
R6 (°C/W)	58	28
C1 (W.s/°C)	0.00015	
C2 (W.s/°C)	0.0005	
C3 (W.s/°C)	7.50E-03	
C4 (W.s/°C)	0.045	
C5 (W.s/°C)	0.35	
C6 (W.s/°C)	1.05	2

12 Package information

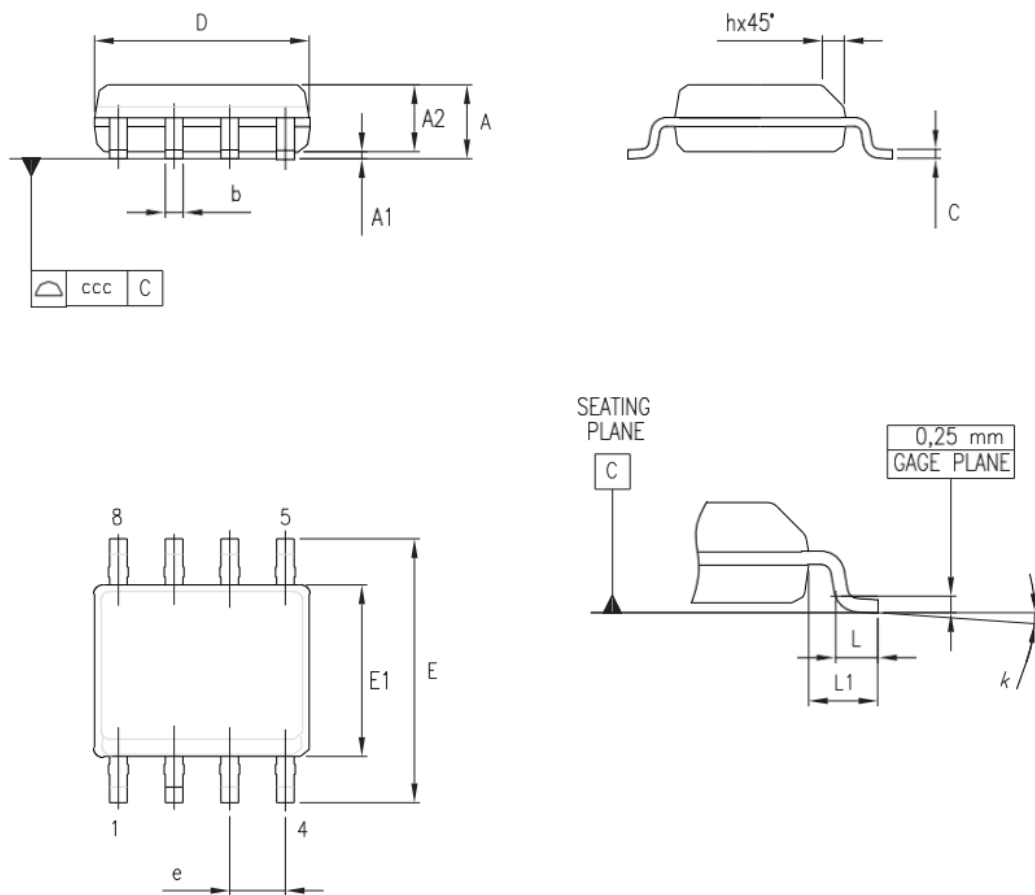
To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

12.1 SO8 package information

Table 13. SO-8 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
a1	0.1		0.25
a2			1.65
a3	0.65		0.85
b	0.35		0.48
b1	0.19		0.25
C	0.25		0.5
c1		45	
D	4.8		5
E	5.8		6.2
e		1.27	
e3		3.81	
F	3.8		4
L	0.4		1.27
M			0.6
S			8
L1	0.8		1.2

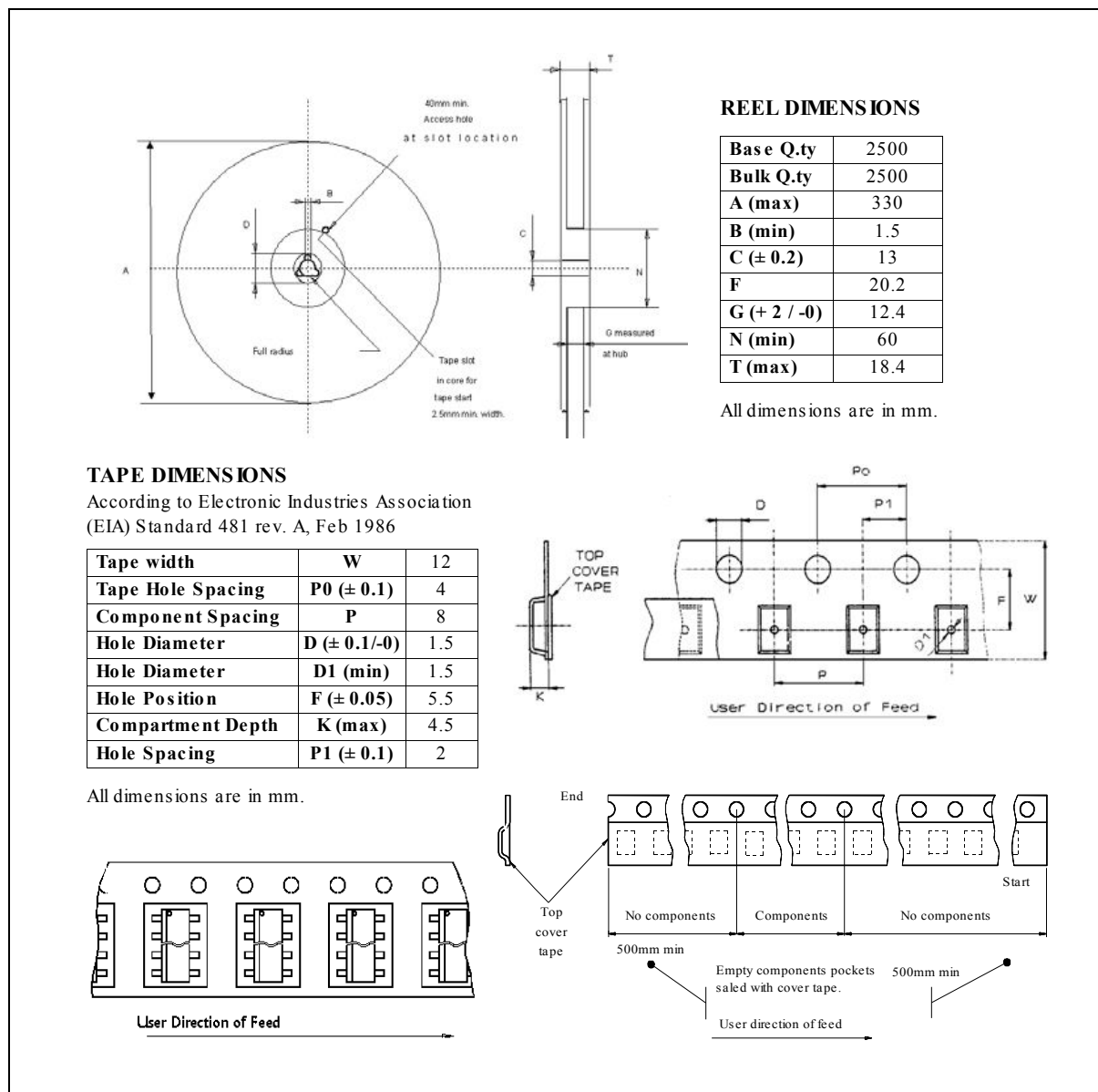
Figure 28. SO-8 package dimensions



0016023 D

12.2 SO8 packing information

Figure 29. SO-8 tape and reel shipment



13 Ordering information

Table 14. Ordering information

Part number	Package	Packing
IPS1270HS	SO8	Tape and reel

Revision history

Table 15. Document revision history

Date	Revision	Changes
08-May-2026	1	Initial release.
04-Aug-2026	2	Added -I _{OUT} parameter in Table 3 ; corrected typo in Section 10 and in Figure 22 ; updated Table 2 ; some minor changes. Figure 9 : added pull-up resistor on STATUS pin.

Contents

1	Block diagram	2
2	Pin connection	3
3	Maximum rating	4
4	Electrical characteristics	5
5	Protections	8
5.1	Current limitation	8
5.2	Thermal shutdown	8
5.3	Negative output voltage clamp	8
6	Signals waveform and functional table	9
7	Test circuits	11
8	Application schematics	12
8.1	Reverse polarity protection	12
8.2	Microcontroller I/Os protection	13
8.3	Vcc overshoot protection	13
9	Electrical characteristics curves	14
10	Active clamp	17
11	Package and PCB thermal data	19
12	Package information	22
12.1	SO8 package information	22
12.2	SO8 packing information	24
13	Ordering information	25
	Revision history	26
	List of tables	28
	List of figures	29

List of tables

Table 1.	Pin function	3
Table 2.	Suggested connections for unused and not connected pins	3
Table 3.	Absolute maximum ratings	4
Table 4.	Thermal data	4
Table 5.	Power section	5
Table 6.	Switching ($V_{CC} = 24\text{ V}$)	5
Table 7.	INPUT pin	6
Table 8.	VCC - OUTPUT diode	6
Table 9.	STATUS pin	6
Table 10.	Protections	7
Table 11.	Functional table	10
Table 12.	Thermal parameter	21
Table 13.	SO-8 mechanical data	22
Table 14.	Ordering information	25
Table 15.	Document revision history	26

List of figures

Figure 1.	Block diagram	2
Figure 2.	Pin connection (top view)	3
Figure 3.	Current and voltage conventions	3
Figure 4.	Switching time waveforms	5
Figure 5.	Overtemperature status timing ($T_j > T_{TSD}$)	6
Figure 6.	Waveforms	9
Figure 7.	I_{lim} short-circuit current	11
Figure 8.	Avalanche energy	11
Figure 9.	Application schematic	12
Figure 10.	Off-state OUTPUT pin current	14
Figure 11.	High level INPUT pin current	14
Figure 12.	STATUS pin leakage current	14
Figure 13.	On-state resistance vs T_{CASE}	14
Figure 14.	On-state resistance vs V_{CC}	15
Figure 15.	INPUT pin high level	15
Figure 16.	INPUT pin low level	15
Figure 17.	Turn-on output voltage slope	15
Figure 18.	Output overvoltage shutdown	16
Figure 19.	INPUT pin hysteresis voltage	16
Figure 20.	Turn-off output voltage slope	16
Figure 21.	I_{lim} vs T_{CASE}	16
Figure 22.	Active OUTPUT clamp typical waveforms	17
Figure 23.	Maximum turn off current versus inductance	18
Figure 24.	SO-8 PC board	19
Figure 25.	SO-8 $R_{thj-amb}$ vs PCB copper area in open box free air condition	19
Figure 26.	SO-8 thermal impedance junction ambient single pulse	20
Figure 27.	Thermal fitting model of a single channel HSD in SO-8	20
Figure 28.	SO-8 package dimensions	23
Figure 29.	SO-8 tape and reel shipment	24

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice.

In the event of any conflict between the provisions of this document and the provisions of any contractual arrangement in force between the purchasers and ST, the provisions of such contractual arrangement shall prevail.

The purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgment.

The purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of the purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

If the purchasers identify an ST product that meets their functional and performance requirements but that is not designated for the purchasers' market segment, the purchasers shall contact ST for more information.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2026 STMicroelectronics – All rights reserved