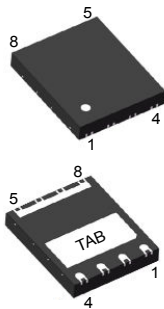
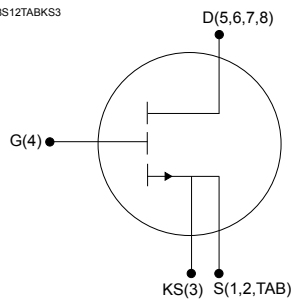


700 V, 74 mΩ typ., 21 A, e-mode PowerGaN transistor



**PowerFLAT 5x6 HV
for PowerGaN**

G4D5678S12TABKS3



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	Series
SGT100R70FDC	700 V	100 mΩ	21 A	G-HEMT

- Enhancement mode normally off transistor
- Very high switching speed
- High power management capability
- Extremely low capacitances
- Zero reverse recovery charge
- ESD safeguard

Applications

- AC-DC converters
- DC-DC converters
- USB type-C PD adapters and quick chargers
- Wireless charging

Description

The **SGT100R70FDC** is a 700 V V, 21 A A e-mode PowerGaN transistor. The resulting device provides extremely low conduction losses, high current capability and ultra-fast switching operation to enable high power density and unbeatable efficiency performances.

Product status link

[SGT100R70FDC](#)

Product summary

Order code	SGT100R70FDC
Marking	100R70F
Package	PowerFLAT 5x6 HV for PowerGaN
Packing	Tape and reel

1 Electrical ratings

$T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	700 ⁽¹⁾	V
	Drain-source voltage (transient, $t_p < 200\text{ }\mu\text{s}$)	800	
V_{GS}	Gate-source voltage	-6 to 7 ⁽²⁾	V
I_D	Drain current (continuous)	21	A
I_{DM}	Pulse drain current ($t_p = 10\text{ }\mu\text{s}$)	41	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	107	W
T_{stg}	Storage temperature range	-55 to 150	$^{\circ}\text{C}$
T_J	Operating junction temperature range		$^{\circ}\text{C}$

1. Recommended continuous maximum bus voltage during switching operations should not exceed 450 V.
2. Refer to AN6268: GaN transistors gate driving solutions.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	1.16	$^{\circ}\text{C/W}$
R_{thJA} ⁽¹⁾	Thermal resistance, junction-to-ambient	69.94	$^{\circ}\text{C/W}$

1. When mounted on a standard 1 inch² area of FR-4 PCB with 2-oz copper.

Related links

[AN6268: GaN transistors gate driving solutions.](#)

2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Table 3. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{DSS}	Drain-source leakage current	$V_{GS} = 0\text{ V}, V_{DS} = 700\text{ V}$		0.8		μA
		$V_{GS} = 0\text{ V}, V_{DS} = 700\text{ V}, T_J = 125\text{ }^{\circ}\text{C}$		9		
I_{GSS}	Gate-source leakage current	$V_{DS} = 0\text{ V}, V_{GS} = 6\text{ V}$		90		μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 18.3\text{ mA}$	1.1	1.7	2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 6\text{ V}, I_D = 0.5\text{ A}$		74	100	$\text{m}\Omega$
		$V_{GS} = 6\text{ V}, I_D = 6\text{ A}, T_J = 125\text{ }^{\circ}\text{C}$		148		

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 400\text{ V}, f = 100\text{ kHz}$	-	133	-	pF
C_{oss}	Output capacitance		-	45	-	pF
C_{rss}	Reverse transfer capacitance		-	1	-	pF
$C_{o(er)}^{(1)}$	Equivalent output capacitance energy related	$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ to }400\text{ V}$	-	67	-	pF
$C_{o(tr)}^{(2)}$	Equivalent output capacitance time related		-	81	-	pF
R_g	Intrinsic gate resistance	$f = 5\text{ MHz}, I_D = 0\text{ A}$	-	6	-	Ω
V_{plat}	Gate plateau voltage	$V_{DS} = 400\text{ V}, I_D = 6\text{ A}$	-	2.7	-	V
Q_g	Total gate charge	$V_{GS} = 0\text{ to }6\text{ V}, V_{DS} = 400\text{ V}, I_D = 6\text{ A}$	-	2.8	-	nC
Q_{gs}	Gate-source charge		-	0.85	-	nC
Q_{gd}	Gate-drain charge		-	0.85	-	nC
Q_{rr}	Reverse recovery charge	$V_{GS} = 0\text{ V}, V_{DS} = 400\text{ V}$	-	0	-	nC
Q_{oss}	Output charge		-	35.9	-	nC

- $C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to the stated value.
- $C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to the stated value.

Table 5. Reverse conduction

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}	Source-drain reverse voltage	$V_{GS} = 0\text{ V}, I_{SD} = 6\text{ A}$	-	2.4	-	V

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DS} = 400\text{ V}$, $I_D = 6\text{ A}$, $V_{GS} = 6\text{ V}$, $R_{G(on)} = 10\text{ }\Omega$, $R_{G(off)} = 2\text{ }\Omega$, $L = 170\text{ }\mu\text{H}$	-	6.5	-	ns
t_r	Rise time		-	4.7	-	ns
$t_{d(off)}$	Turn-off delay time		-	5.3	-	ns
t_f	Fall time		-	6.2	-	ns

2.1 Electrical characteristics (curves)

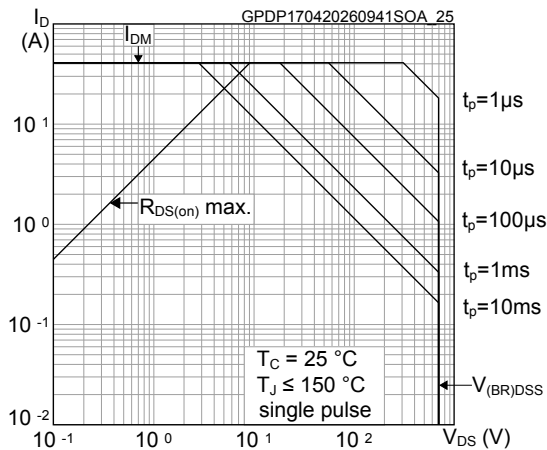
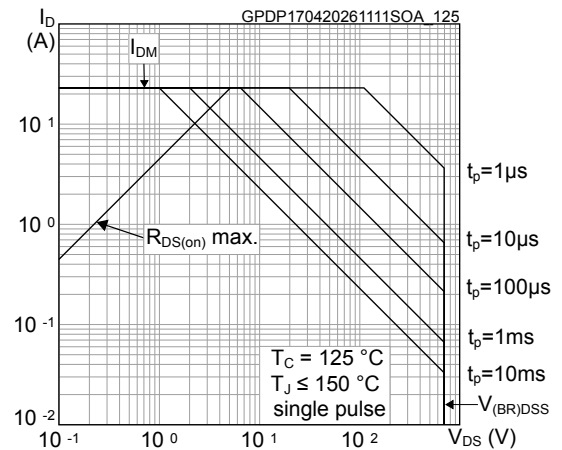
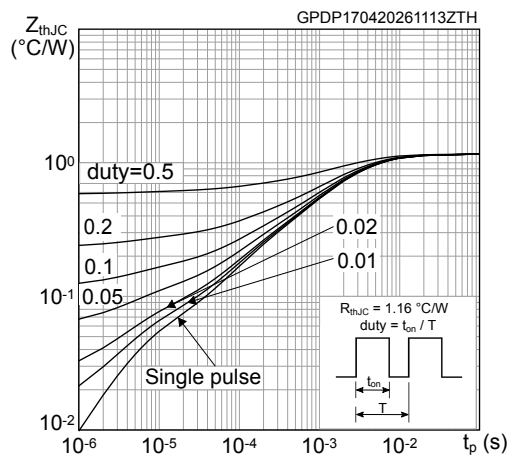
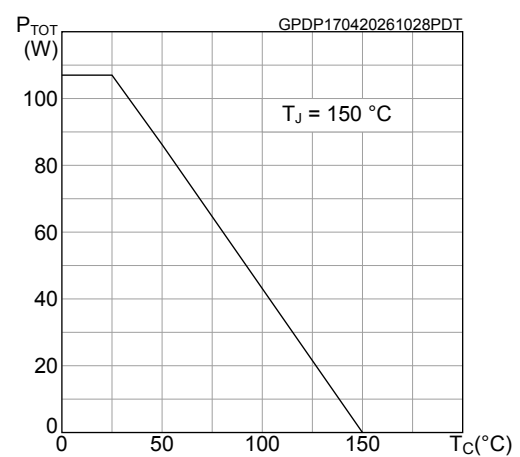
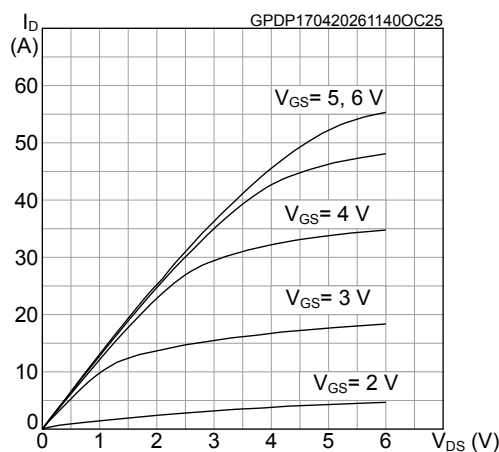
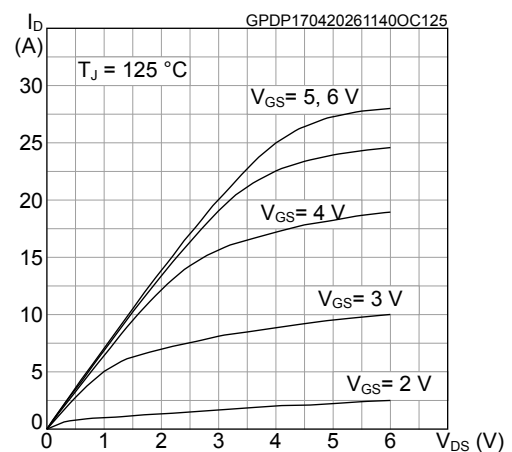
Figure 1. Safe operating area ($T_C = 25\text{ }^{\circ}\text{C}$)

Figure 2. Safe operating area ($T_C = 125\text{ }^{\circ}\text{C}$)

Figure 3. Maximum transient thermal impedance

Figure 4. Total power dissipation

Figure 5. Typical output characteristics ($T_J = 25\text{ }^{\circ}\text{C}$)

Figure 6. Typical output characteristics ($T_J = 125\text{ }^{\circ}\text{C}$)


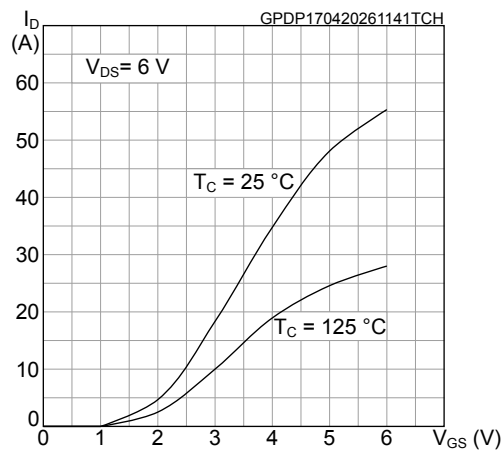
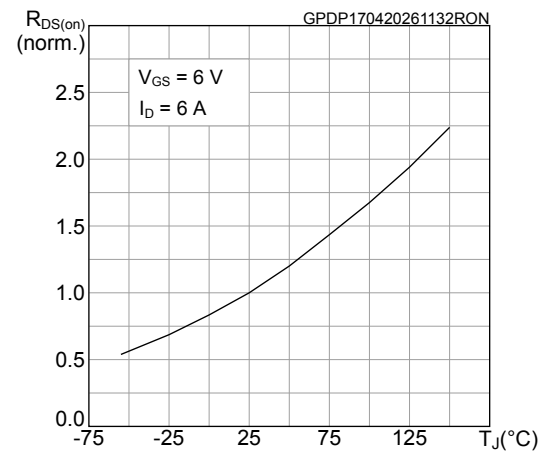
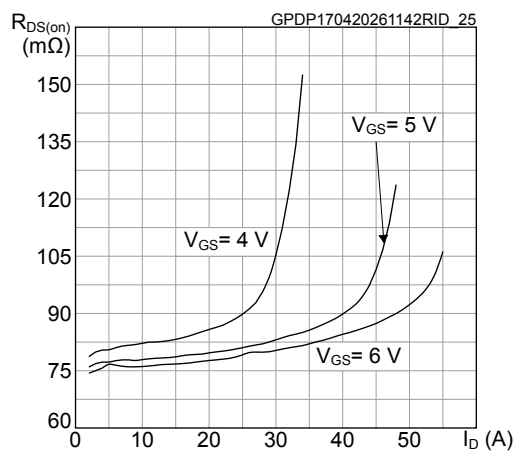
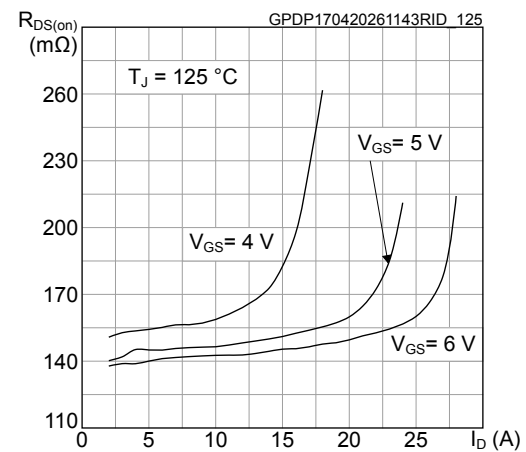
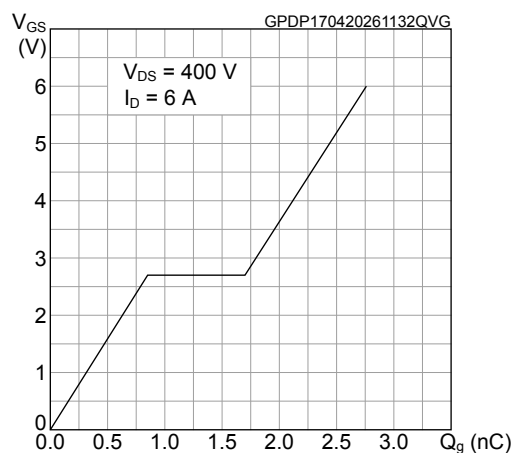
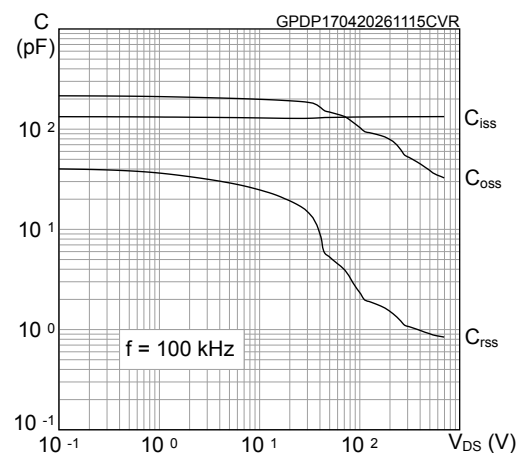
Figure 7. Typical transfer characteristics

Figure 8. Normalized on-resistance vs temperature

Figure 9. Typical drain-source on-resistance ($T_J = 25 \text{ }^{\circ}\text{C}$)

Figure 10. Typical drain-source on-resistance ($T_J = 125 \text{ }^{\circ}\text{C}$)

Figure 11. Typical gate charge characteristics

Figure 12. Typical capacitance characteristics


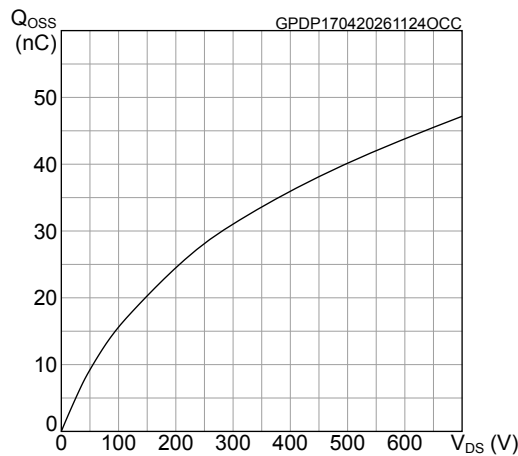
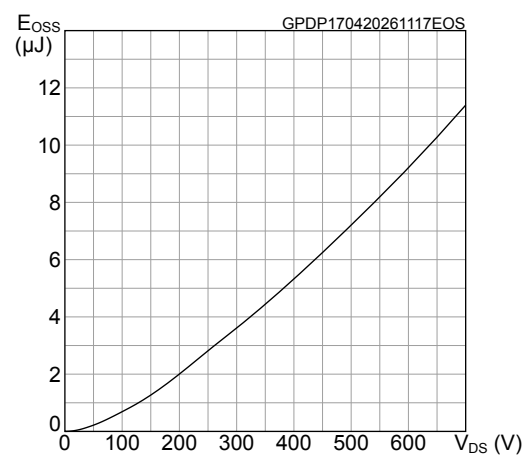
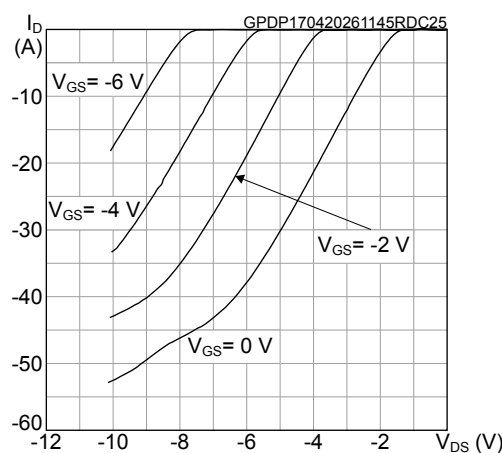
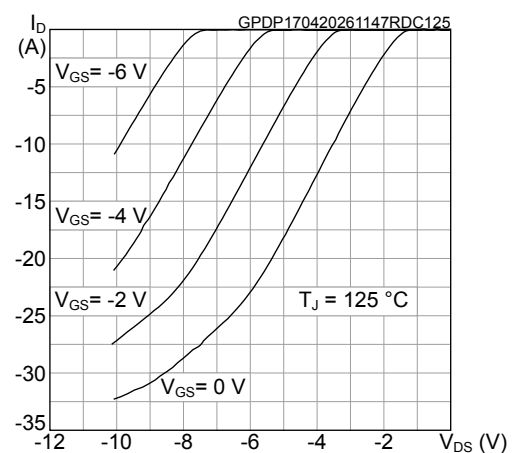
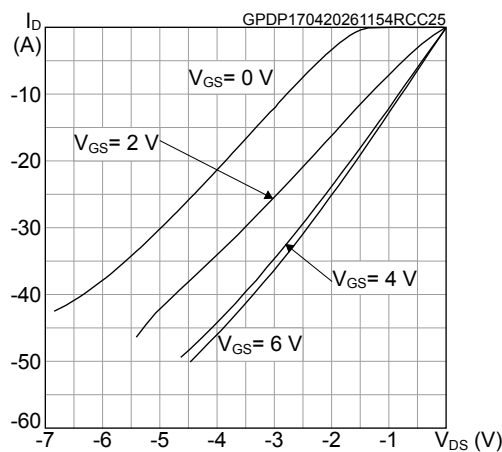
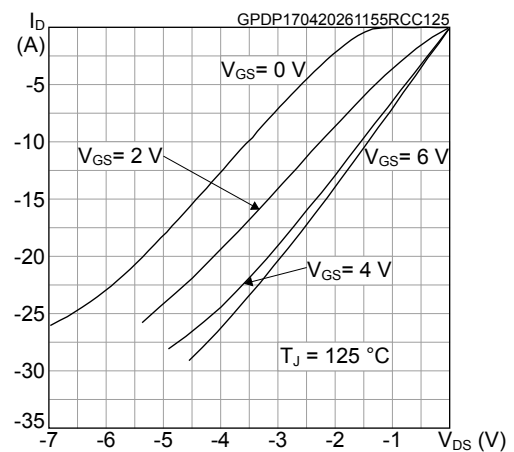
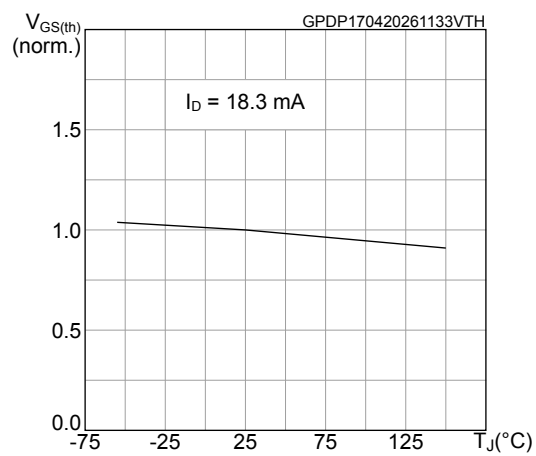
Figure 13. Typical output capacitance charge

Figure 14. Typical output capacitance stored energy

Figure 15. Typical diode reverse conduction characteristics ($T_J = 25^\circ\text{C}$)

Figure 16. Typical diode reverse conduction characteristics ($T_J = 125^\circ\text{C}$)

Figure 17. Typical reverse conduction characteristics ($T_J = 25^\circ\text{C}$)

Figure 18. Typical reverse conduction characteristics ($T_J = 125^\circ\text{C}$)


Figure 19. Normalized gate threshold vs temperature



3 Test circuits

Figure 20. Test circuit for inductive load switching times

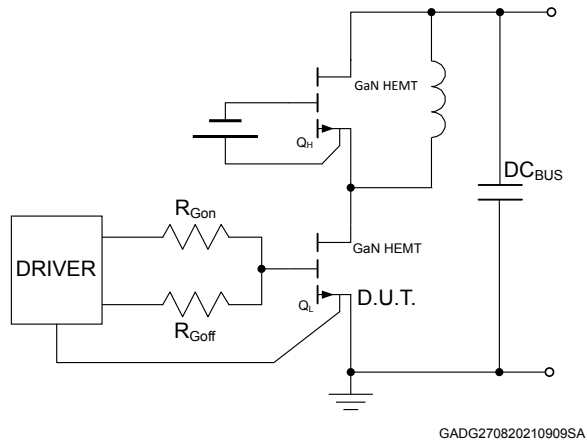
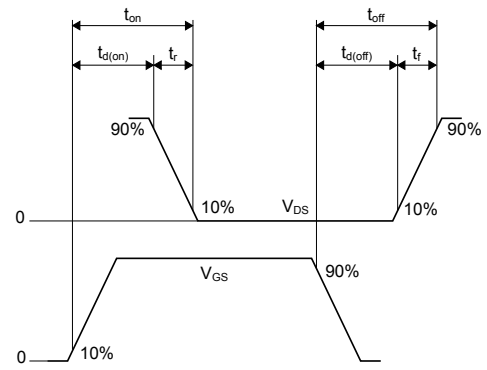


Figure 21. Switching time waveforms



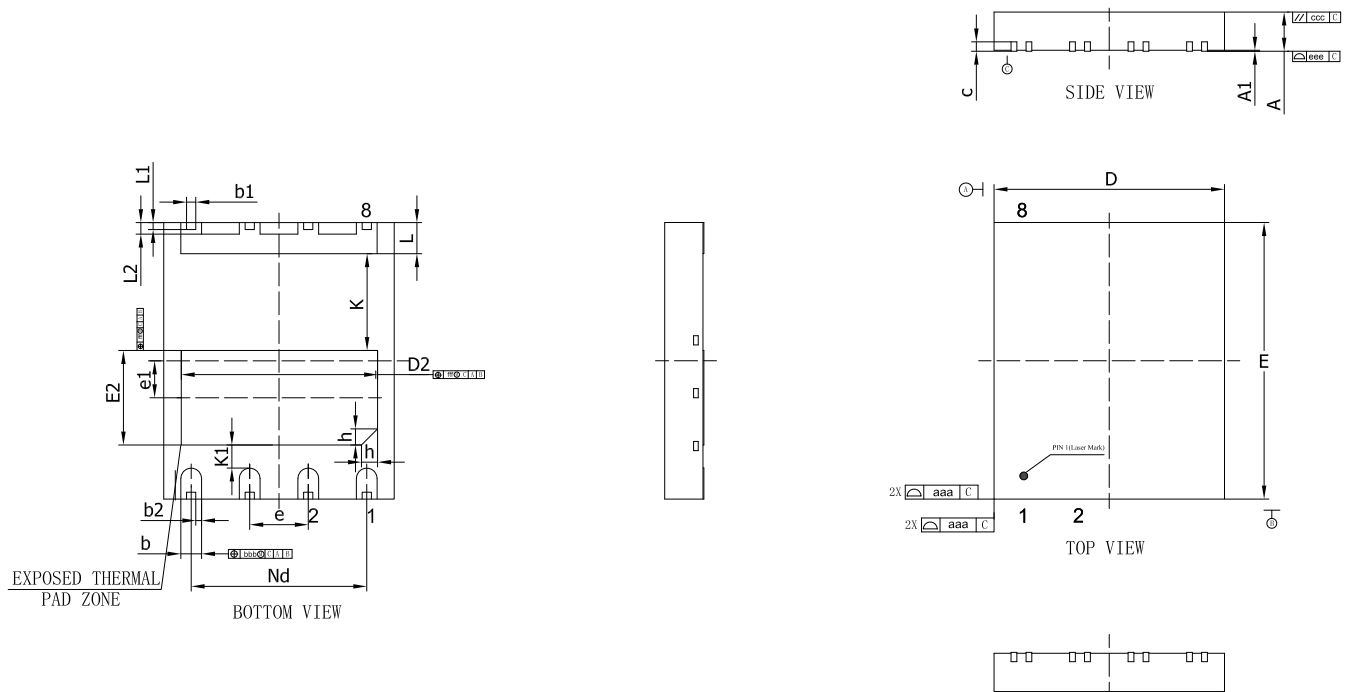
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4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 PowerFLAT 5x6 HV for PowerGaN package information

Figure 22. PowerFLAT 5x6 HV for PowerGaN package outline

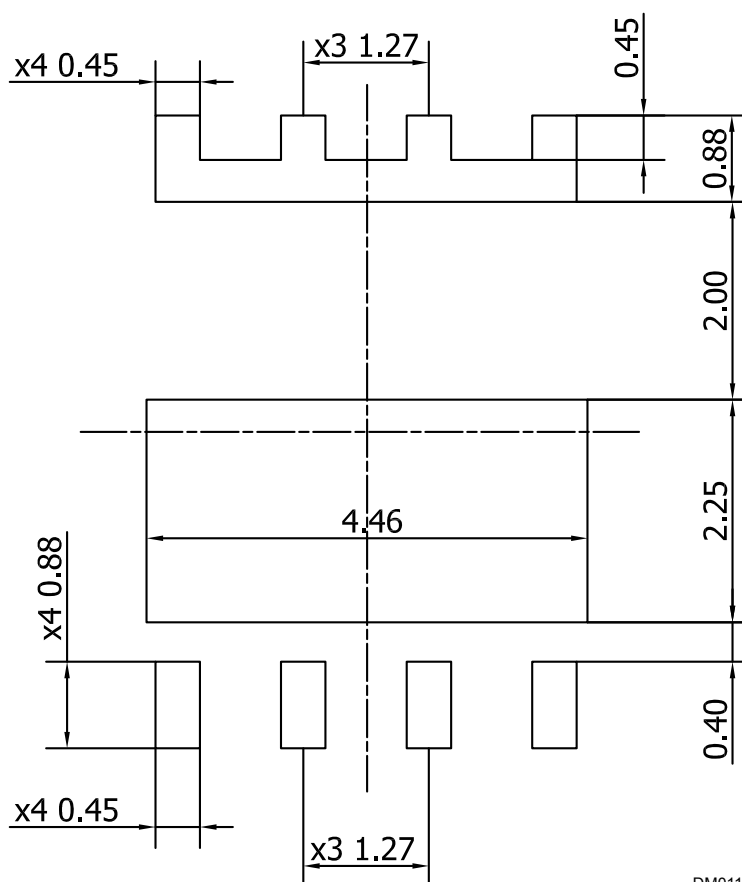


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Table 7. PowerFLAT 5x6 HV for PowerGaN mechanical data

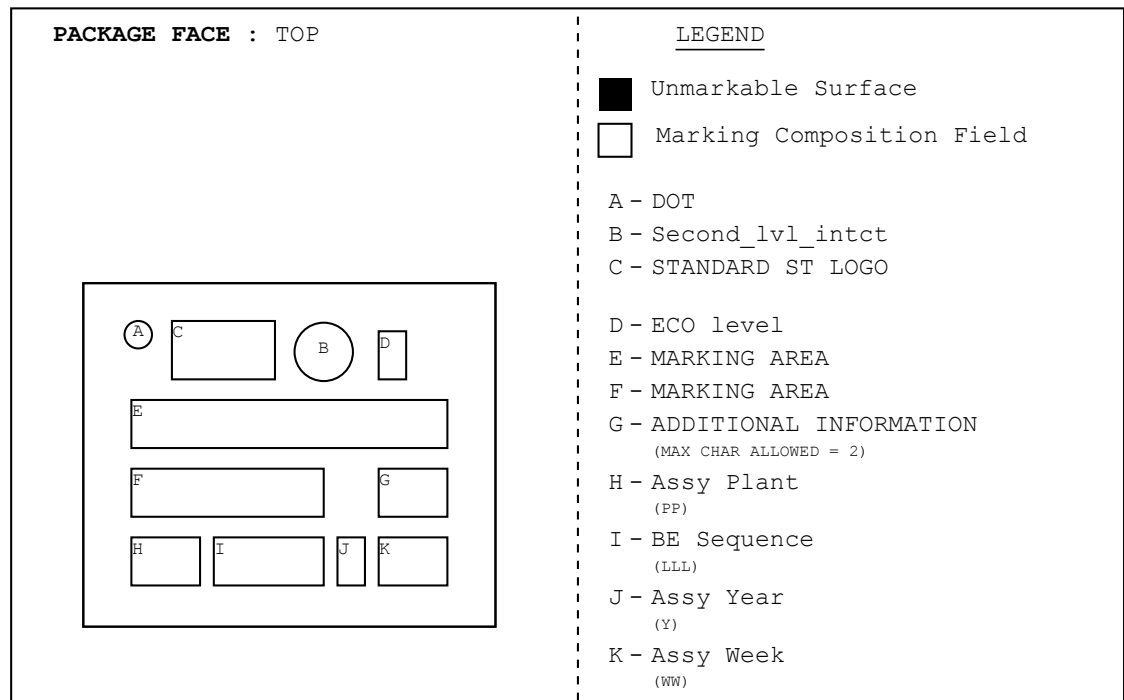
Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.40	0.45	0.50
b1	0.20REF		
b2	0.125REF		
c	0.203REF		
D	4.90	5.00	5.10
D2	4.16	4.26	4.36
e	1.27BSC		
e1	0.80BSC		
Nd	3.81BSC		
E	5.90	6.00	6.10
E2	1.95	2.05	2.15
L	0.625	0.675	0.725
L1	0.15REF		
L2	0.25REF		
h	0.30	0.35	0.40
K	2.10REF		
K1	0.50REF		
aaa	0.10		
bbb	0.07		
ccc	0.10		
eee	0.08		
fff	0.10		

Figure 23. PowerFLAT 5x6 HV for PowerGaN recommended footprint (dimensions are in mm)



DM01190469_Rev_2_footprint_for_GaN

Figure 24. Marking composition for PowerFLAT 5x6 HV for PowerGaN



DM01207361_rev.3

Engineering samples

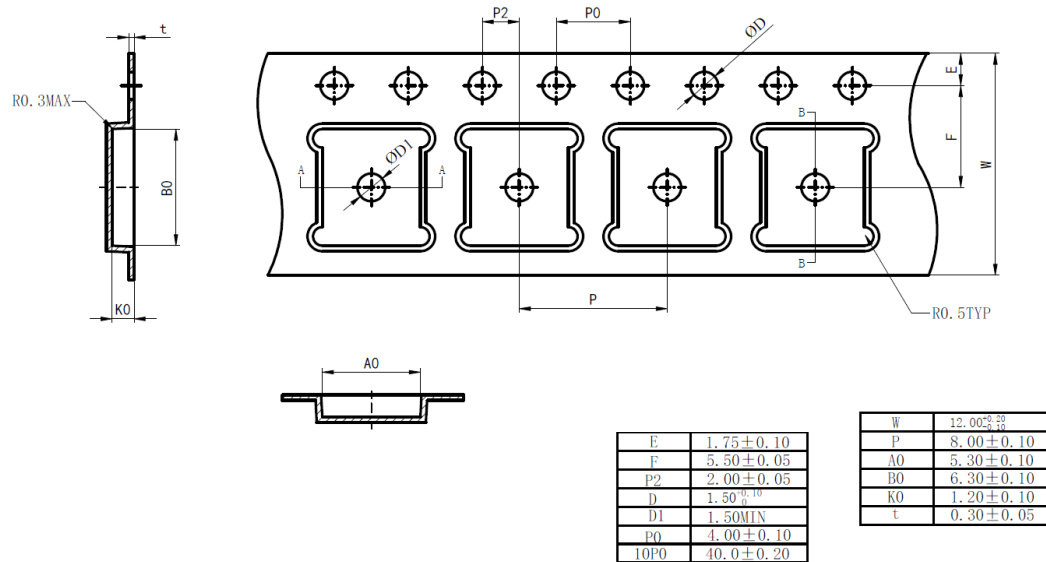
These samples are clearly identified by "ES" digits in the marking additional information field of each unit. These samples are intended to be used for electrical compatibility evaluation only; usage for any other purpose may be agreed only upon written authorization by ST. ST is not liable for any customer usage in production and/or in reliability qualification trials.

Commercial samples

Fully qualified parts from ST standard production with no limitations of use or special identification marking.

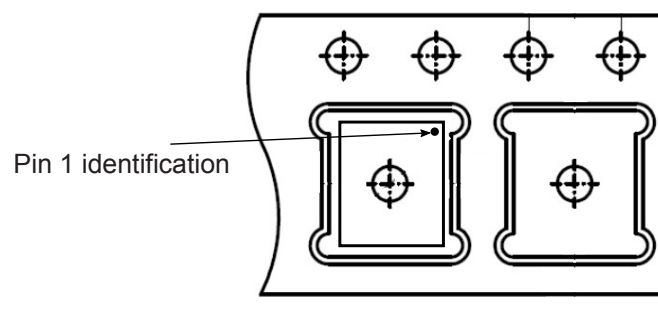
4.2 PowerFLAT 5x6 HV for PowerGaN packing information

Figure 25. PowerFLAT 5x6 HV for PowerGaN tape (dimensions are in mm)



Tape_PowerFLAT5x6_HV_GaN

Figure 26. PowerFLAT 5x6 HV for PowerGaN package orientation in carrier tape



Revision history

Table 8. Document revision history

Date	Revision	Changes
06-May-2026	1	First release.
16-Jul-2026	2	Added footnote in Table 1. Absolute maximum ratings and updated Table 3. Static.

Contents

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4	Package information.....	10
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