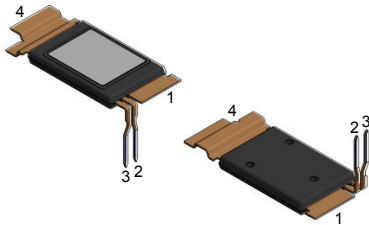
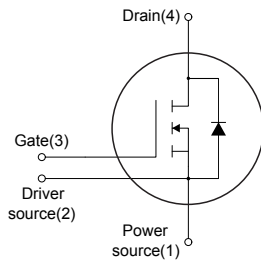


Automotive-grade silicon carbide Power MOSFET 750 V, 6.5 mΩ typ., 300 A in a STPAK package



STPAK



NG3DS2PS1D4



Features

Order code	V _{DS}	R _{DS(on)} typ.	I _D
SCTHS300N75G3AG	750 V	6.5 mΩ	300 A

- AEC-Q101 qualified 
- Very low R_{DS(on)} over the entire temperature range
- High speed switching performances
- Very fast and robust intrinsic body diode
- Source sensing pin for increased efficiency

Application

- Main inverter (electric traction)

Description

This silicon carbide Power MOSFET device has been developed using ST's advanced and innovative 3rd generation SiC MOSFET technology. The device features a very low R_{DS(on)} over the entire temperature range combined with low capacitances and very high switching operations, which improve application performance in frequency, energy efficiency, system size and weight reduction.

Product status link

[SCTHS300N75G3AG](#)

Product summary

Order code	SCTHS300N75G3AG
Marking	SC300N75G3AG
Package	STPAK
Packing	Tray

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	750	V
V_{GS}	Gate-source voltage	-10 to 22	V
	Gate-source voltage (recommended operating values)	-5 to 18	
I_D	Drain current (continuous) at $T_C = 25\text{ °C}$	300	A
	Drain current (continuous) at $T_C = 100\text{ °C}$	230	
$I_{DM}^{(1)}$	Drain current (pulsed)	935	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ °C}$	972	W
V_{ISO}	Insulation withstand voltage applied between each pin and the heat sink plate (DC voltage, $t = 1\text{ s}$)	4.3	kV
T_{stg}	Storage temperature range	-55 to 200	°C
T_J	Operating junction temperature range		°C

1. Pulse width is limited by safe operating area.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.18	°C/W

2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	750			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 750\text{ V}$			40	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = -10\text{ to }22\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 5.4\text{ mA}$	1.8	3	4.2	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 18\text{ V}$, $I_D = 150\text{ A}$		6.5	8.8	m Ω
		$V_{GS} = 18\text{ V}$, $I_D = 150\text{ A}$, $T_J = 175\text{ }^{\circ}\text{C}$		8.3		
		$V_{GS} = 18\text{ V}$, $I_D = 150\text{ A}$, $T_J = 200\text{ }^{\circ}\text{C}$		8.8		

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 400\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	6903	-	pF
C_{oss}	Output capacitance		-	632	-	pF
C_{rss}	Reverse transfer capacitance		-	67	-	pF
R_g	Gate input resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	0.64	-	Ω
Q_g	Total gate charge	$V_{DD} = 400\text{ V}$, $V_{GS} = 0\text{ to }18\text{ V}$, $I_D = 150\text{ A}$	-	303	-	nC
Q_{gs}	Gate-source charge		-	105	-	nC
Q_{gd}	Gate-drain charge		-	97	-	nC

Table 5. Switching energy (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
E_{on}	Turn-on switching energy	$V_{DD} = 400\text{ V}$, $I_D = 150\text{ A}$, $R_G = 5.6\text{ }\Omega$, $V_{GS} = -5\text{ V to }18\text{ V}$	-	1426	-	μJ
E_{off}	Turn-off switching energy		-	1980	-	μJ

Table 6. Switching times (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400\text{ V}$, $I_D = 150\text{ A}$, $R_G = 5.6\text{ }\Omega$, $V_{GS} = -5\text{ to }18\text{ V}$	-	43	-	ns
t_f	Fall time		-	42	-	ns
$t_{d(off)}$	Turn-off delay time		-	85	-	ns
t_r	Rise time		-	30	-	ns

Table 7. Reverse SiC diode characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}	Diode forward voltage	$I_{SD} = 150\text{ A}$, $V_{GS} = -5\text{ V}$	-	4.6	-	V
t_{rr}	Reverse recovery time	$I_{SD} = 150\text{ A}$, $di/dt = 1\text{ kA}/\mu\text{s}$, $V_{GS} = -5\text{ V}$, $V_{DD} = 400\text{ V}$	-	46	-	ns
Q_{rr}	Reverse recovery charge		-	778	-	nC
I_{RRM}	Reverse recovery current		-	30	-	A

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

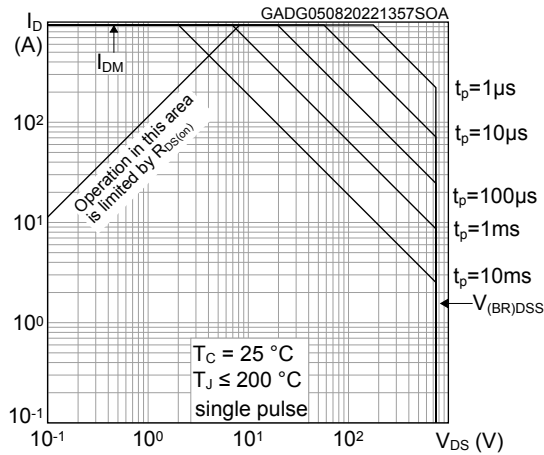


Figure 2. Maximum transient thermal impedance

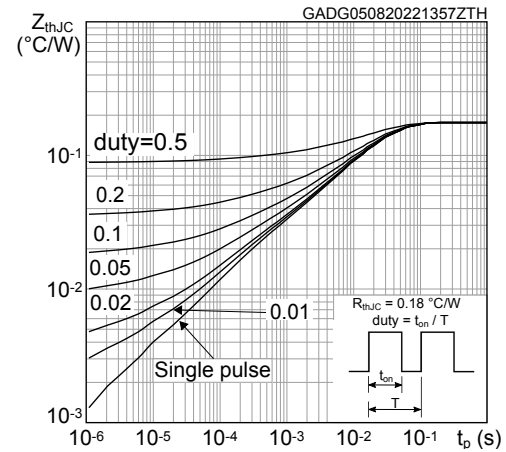


Figure 3. Typical output characteristics ($T_J = 25\text{ °C}$)

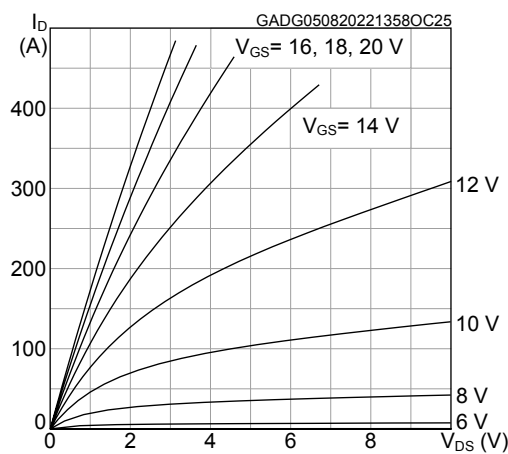


Figure 4. Typical output characteristics ($T_J = 200\text{ °C}$)

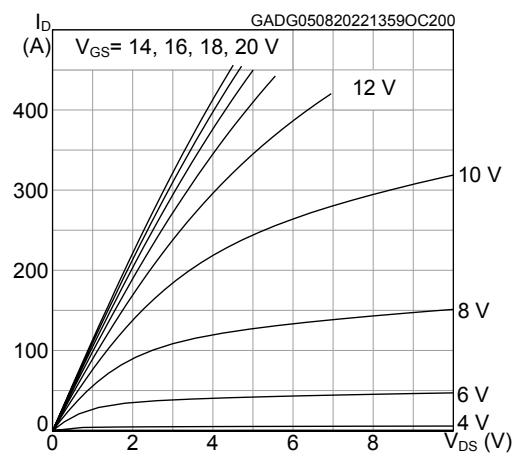


Figure 5. Typical transfer characteristics

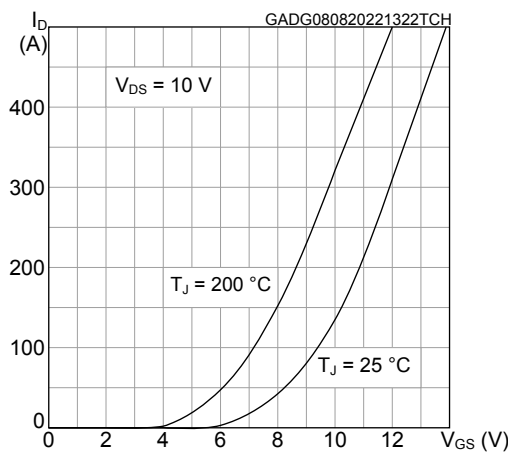


Figure 6. Total power dissipation

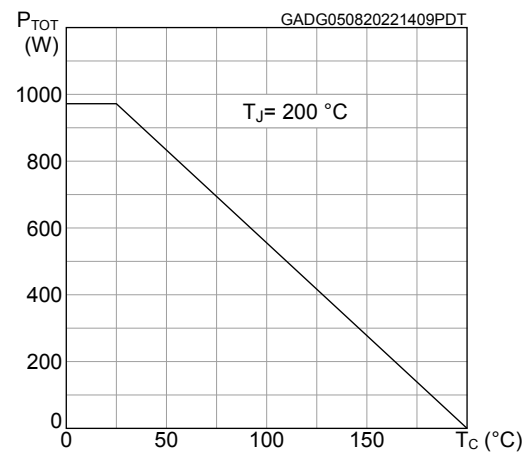


Figure 7. Typical gate charge characteristics

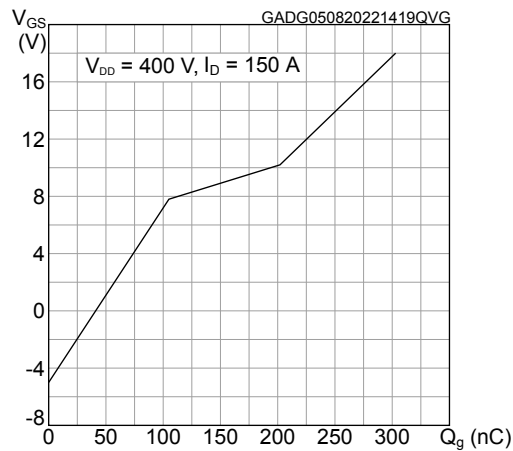


Figure 8. Typical capacitance characteristics

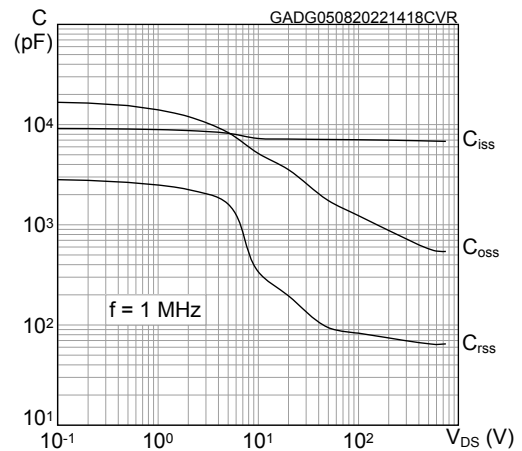


Figure 9. Typical switching energy vs drain current

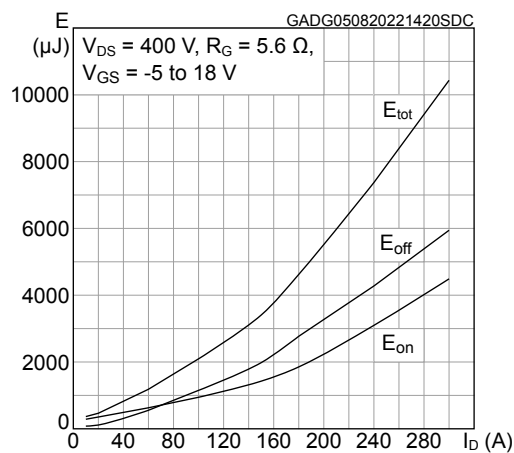


Figure 10. Typical switching energy vs supply voltage

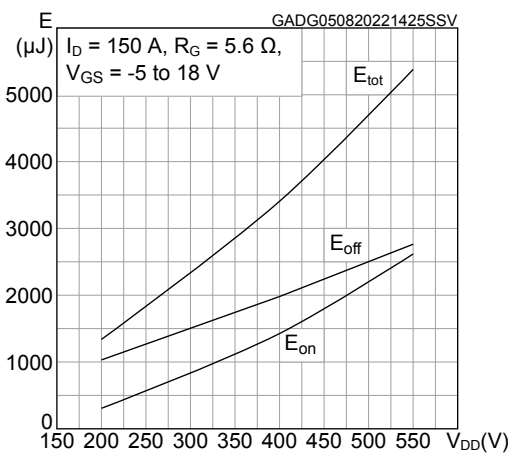


Figure 11. Typical switching energy vs gate resistance

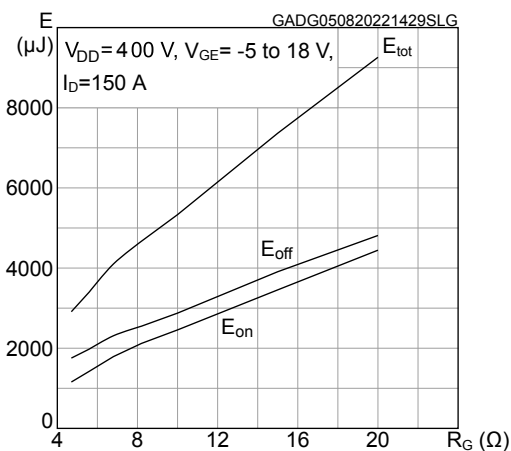


Figure 12. Normalized breakdown voltage vs temperature

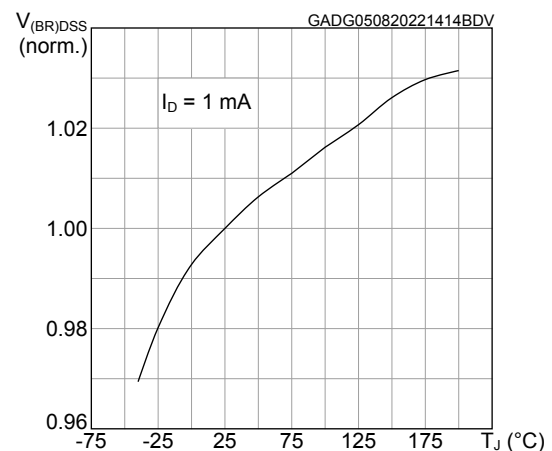


Figure 13. Normalized gate threshold vs temperature

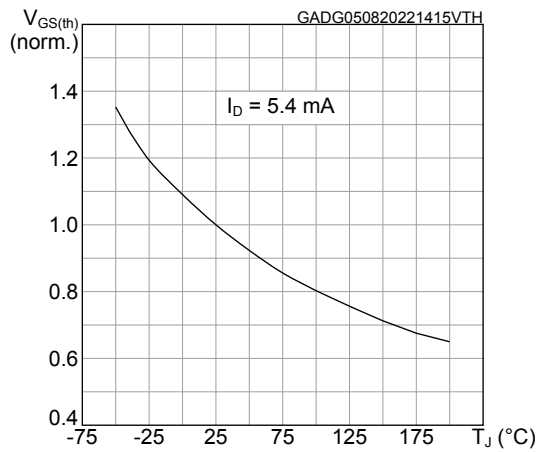


Figure 14. Normalized on-resistance vs temperature

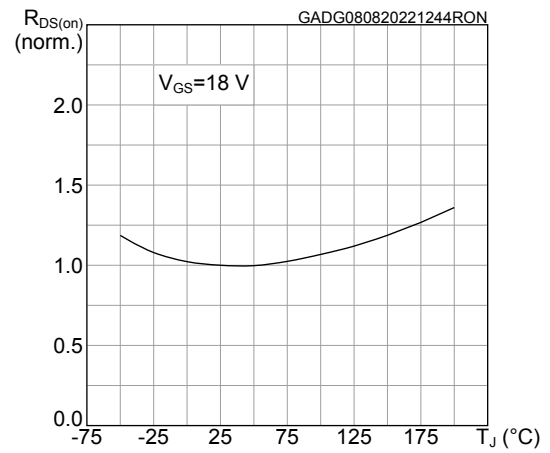


Figure 15. Typical reverse conduction characteristics (T_J = 25 °C)

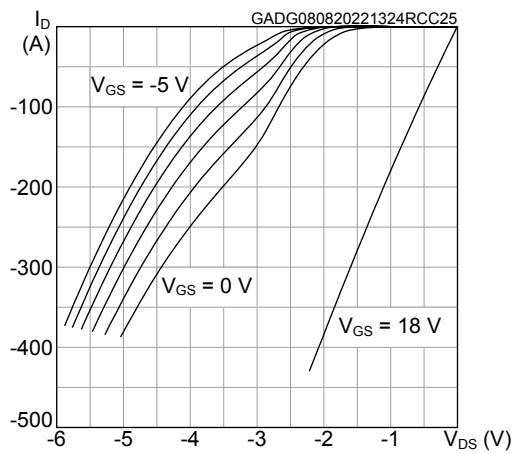
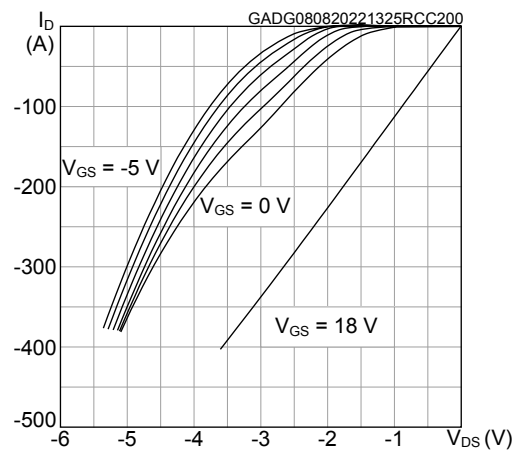


Figure 16. Typical reverse conduction characteristics (T_J = 200 °C)

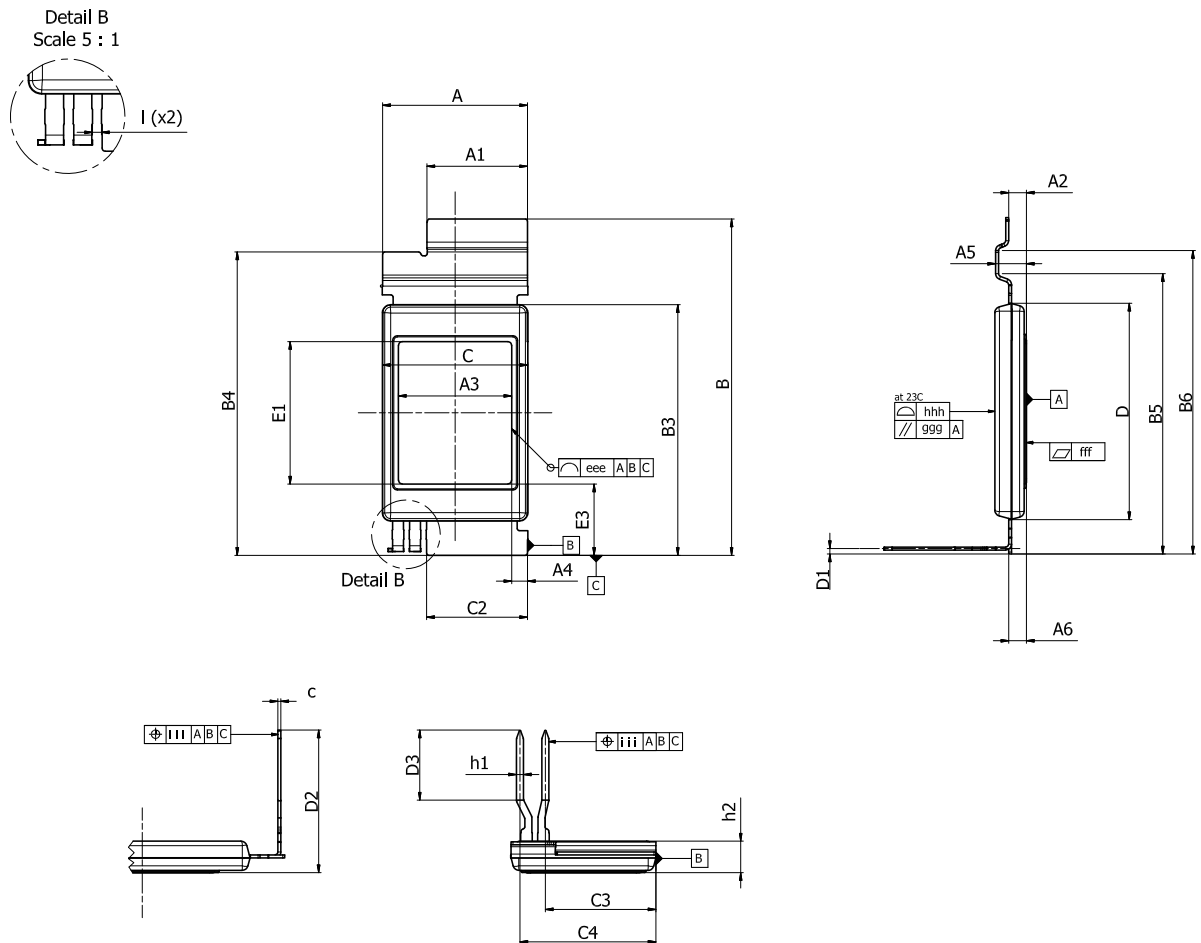


3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

3.1 STPAK package information

Figure 17. STPAK package outline



DM00305987_10

Table 8. STPAK package mechanical data

Ref.	Dimensions			Notes
	mm			
	Min.	Typ.	Max.	
A	18.60	18.80	19.00	
A1	12.85	13.05	13.25	
A2	2.00	2.30	2.60	
A3	13.40	13.90	14.40	Exposed Pad
A4	1.95	2.45	2.95	
A5	3.80	4.00	4.20	
A6	2.10	2.30	2.50	
B	43.40	43.70	44.00	
B3	32.20	32.50	32.80	
B4	39.10	39.40	39.70	
B5	36.07	36.37	36.67	
B6	39.07	39.37	39.67	
c	0.34	0.39	0.44	
C		18.55	19.10	Encompass both large and small cav.
C2	12.90	13.10	13.30	
C3		14.35		
C4		17.65		
D	27.90	28.10	28.30	
D1		0.69		
D2	18.50	19.00	19.50	
D3	9.10	9.60	10.10	
E1	17.20	17.70	18.20	Exposed pad
E3	9.15	9.65	10.15	
h1	0.85	0.90	0.95	x2 - Pins width
h2	4.00	4.10	4.20	
I	0.60	0.70	0.80	
eee	0.50			
fff	0.10 at 23 °C – 0.05 at 220 °C			Convex with center higher than edges
ggg	0.05			
hhh	0.10			
iii	0.60			

Revision history

Table 9. Document revision history

Date	Revision	Changes
14-Sep-2022	1	First release.
05-Oct-2022	2	Updated <i>Internal schematic</i> on cover page.
20-Feb-2024	3	Updated <i>Figure 3. Typical output characteristics (T_J = 25 °C)</i> , <i>Figure 4. Typical output characteristics (T_J = 200 °C)</i> , <i>Figure 5. Typical transfer characteristics</i> , <i>Figure 7. Typical gate charge characteristics</i> , <i>Figure 8. Typical capacitance characteristics</i> , <i>Figure 14. Normalized on-resistance vs temperature</i> , <i>Figure 15. Typical reverse conduction characteristics (T_J = 25 °C)</i> and <i>Figure 16. Typical reverse conduction characteristics (T_J = 200 °C)</i> . Updated <i>Section 3.1: STPAK package information</i> .
15-Jul-2024	4	Updated <i>Table 7. Reverse SiC diode characteristics</i> . Updated <i>Table 8. STPAK package mechanical data</i> .



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