

SERIAL PRESENCE DETECT

M391A1G43DB0-CPB/CRC

Organization : 1G x 72
 Composition : 512M x8 *18ea
 Used component part # : K4A4G085WD-BCPB/BCRC
 # of rows in module : 2Rows
 # of banks in component : 4Banks 4BG
 Feature : 31.25mm height & Double sided component
 Refresh : 8K/64ms
 Bin Sort : PB(DDR4 2133@CL=15),RC(DDR4 2400@CL=17)
 RCD Vendor and Revision : N/A

Byte #	Function Described	Function Supported		Hex Value		Note
		CPB	CRC	CPB	CRC	
0	Number of Bytes Used / Number of Bytes in SPD Device / CRC Coverage	512B Total, 384B Used		23h		
1	SPD Revision	Ver 1.0		10h		
2	Key Byte / DRAM Device Type	DDR4 SDRAM		0Ch		
3	Key Byte / Module Type	UDIMM		02h		
4	SDRAM Density and Banks	4Gb, 4BG&4Banks		84h		
5	SDRAM Addressing	Row bits 15, Column bits 10		19h		
6	SDRAM Device Type	Monolithic Device		00h		
7	SDRAM Optional Features	Unlimited MAC		08h		
8	SDRAM Thermal and Refresh Option	Reserved		00h		
9	Other SDRAM Optional Features	PPR supported		40h		
10	Reserved	Reserved		00h		
11	Module Nominal Voltage, VDD	1.2V		03h		
12	Module Organization	2Rx8		09h		
13	Module Memory Bus Width	64bit,ECC		0Bh		
14	Module Thermal Sensor	With TS		80h		
15~16	Reserved	Reserved		00h		
17	Timebases	MTB 125ps, FTB 1ps		00h		
18	SDRAM Minimum Cycle Time(tckavg min)	0.938ns	0.833ns	08h	07h	
19	SDRAM Minimum Cycle Time(tckavg max)	1.5ns		0Ch		
20	Cas Latency Supported, First Byte	10,11,12,13,14,15,16	10,11,12,13,14,15,16,17,18	F8h		
21	Cas Latency Supported, Second Byte	10,11,12,13,14,15,16	10,11,12,13,14,15,16,17,18	03h	0Fh	
22	Cas Latency Supported, Third Byte	10,11,12,13,14,15,16	10,11,12,13,14,15,16,17,18	00h		
23	Cas Latency Supported, Fourth Byte	10,11,12,13,14,15,16	10,11,12,13,14,15,16,17,18	00h		
24	Minimum Cas Latency Time (tAAmin)	13.75ns		6Eh		
25	Minimum RAS to CAS Delay Time(tRCD min)	13.75ns		6Eh		
26	Minimum Raw Precharge Delay Time(trp min)	13.75ns		6Eh		
27	Upper Nibbles for tRASmin and tRCmin	tRAS=33ns, tRC=46.75ns	tRAS=32ns, tRC=45.75ns	11h		
28	Minimum Active to Precharge Delay Time (tRASmin), Least Significant Byte	tRAS=33ns	tRAS=32ns	08h	00h	
29	Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Byte	tRC=46.75ns	tRC=45.75ns	76h	6Eh	
30	Minimum Refresh Recovery Delay Time (tRFC1min), LSB	260ns		20h		
31	Minimum Refresh Recovery Delay Time (tRFC1min), MSB	260ns		08h		
32	Minimum Refresh Recovery Delay Time (tRFC2min), LSB	160ns		00h		
33	Minimum Refresh Recovery Delay Time (tRFC2min), MSB	160ns		05h		
34	Minimum Refresh Recovery Delay Time (tRFC4min), LSB	110ns		70h		
35	Minimum Refresh Recovery Delay Time (tRFC4min), MSB	110ns		03h		
36	Minimum Four Active Window Time (tFAWmin), Most Significant Nibble	21ns		00h		
37	Minimum Four Activate Window Time (tFAWmin), Least Significant Byte	21ns		A8h		
38	Minimum Active to Active Delay Time (tRRD_smin), different Bank Group	3.7ns	3.3ns	1Eh	1Bh	
39	Minimum Active to Active Delay Time (tRRD_Lmin), Same Bank Group	5.3ns	4.9ns	2Bh	28h	

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		CPB	CRC	CPB	CRC	
40	Minimum CAS to CAS Delay Time(tCCD_Lmin), same bank group	5.625ns	5ns	2Eh	28h	
41-59	Reserved	reserved		00h		
60	Connector to SDRAM Bit Mapping	DQ0-3 (ECC U E)		0Ch		
61	Connector to SDRAM Bit Mapping	DQ4-7 (ECC U E)		2Ch		
62	Connector to SDRAM Bit Mapping	DQ8-11 (ECC U E)		15h		
63	Connector to SDRAM Bit Mapping	DQ12-15(ECC U E)		35h		
64	Connector to SDRAM Bit Mapping	DQ16-19(ECC U E)		15h		
65	Connector to SDRAM Bit Mapping	DQ20-23(ECC U E)		35h		
66	Connector to SDRAM Bit Mapping	DQ24-27(ECC U E)		0Bh		
67	Connector to SDRAM Bit Mapping	DQ28-31(ECC U E)		2Ch		
68	Connector to SDRAM Bit Mapping	CB0-3DQ20-23(ECC U E)		15h		
69	Connector to SDRAM Bit Mapping	CB4-7DQ20-23(ECC U E)		35h		
70	Connector to SDRAM Bit Mapping	DQ32-35(ECC U E)		0Bh		
71	Connector to SDRAM Bit Mapping	DQ36-39(ECC U E)		35h		
72	Connector to SDRAM Bit Mapping	DQ40-43(ECC U E)		0Bh		
73	Connector to SDRAM Bit Mapping	DQ44-47(ECC U E)		2Ch		
74	Connector to SDRAM Bit Mapping	DQ48-51(ECC U E)		0Bh		
75	Connector to SDRAM Bit Mapping	DQ52-55(ECC U E)		35h		
76	Connector to SDRAM Bit Mapping	DQ56-59(ECC U E)		15h		
77	Connector to SDRAM Bit Mapping	DQ60-63(ECC U E)		36h		
78-116	Reserved	reserved		00h		
117	Fine Offset for Minimum CAS to CAS Delay Time(tCCD_Lmin), same bank group	5.625ns	5ns	83h	00h	
118	Fine Offset for Minimum Activate to Acticate Delay Time(tRRD_L_min), Same Bank Group	5.3ns	4.9ns	B5h	9Ch	
119	Fine Offset for Minimum Activate to Acticate Delay Time(tRRD_Smin), Different Bank Group	3.7ns	3.3ns	CEh	B5h	
120	Fine Offset for Minimum Activate to Acticate/Refresh Delay Time(tRCmin)	46.75ns	45.75ns	00h		
121	Fine Offset for Minimum Row Precharge Delay Time(tRPmin)	13.75ns		00h		
122	Fine Offset for Minimum RAS to CAS Delay Time(tRCD_min)	13.75ns		00h		
123	Fine Offset for Minimum CAS Latency Delay Time(tAA_min)	13.75ns		00h		
124	Fine Offset for DRAM Maximum Cycle Time(tCKAVG_max)	1.5ns		00h		
125	Fine Offset for DRAM Minimum Cycle Time(tCKAVG_min)	0.938ns	0.833ns	C2h	D6h	
126	Cyclical Redundancy Code	-		ADh	17h	
127	Cyclical Redundancy Code	-		91h	08h	
128	Raw Card Extension, Module Nominal Height	R/C E 0.0 , 31.25mm		11h		
129	Module Maximum Thickness	(Each side)1<thickness<2mm		11h		
130	Reference Raw Card Used	R/C E 0.0		04h		
131	Address Mapping from Edge Connector to DRAM	Mirrored		01h		
132	Reserved	Reserved		00h		
133	Reserved	Reserved		00h		
134	Reserved	Reserved		00h		
135	Reserved	Reserved		00h		
136	Reserved	Reserved		00h		
137	Reserved	Reserved		00h		
138	Reserved	Reserved		00h		
139-253	Reserved	Reserved		00h		
254	Cyclical Redundancy Code	-		0Ch		

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		CPB	CRC	CPB	CRC	
255	Cyclical Redundancy Code	-		2Eh		
256-319	Reserved	Reserved		00h		
320	Module Manufacturer's ID Code, Least Significant Byte	Samsung		80h		
321	Module Manufacturer's ID Code, Most Significant Byte	Samsung		CEh		
322	Module Manufacturing Location	Samsung		00h		
323	Module Manufacturing Date	Year		00h		
324	Module Manufacturing Date	Week		00h		
325	Module Serial Number	-		00h		
326	Module Serial Number	-		00h		
327	Module Serial Number	-		00h		
328	Module Serial Number	-		00h		
329	Module Part Number	M		4Dh		
330	Module Part Number	3		33h		
331	Module Part Number	9		39h		
332	Module Part Number	1		31h		
333	Module Part Number	A		41h		
334	Module Part Number	1		31h		
335	Module Part Number	G		47h		
336	Module Part Number	4		34h		
337	Module Part Number	3		33h		
338	Module Part Number	D-die		44h		
339	Module Part Number	B		42h		
340	Module Part Number	0		30h		
341	Module Part Number	-		2Dh		
342	Module Part Number	C		43h		
343	Module Part Number	P	R	50h	52h	
344	Module Part Number	B	C	42h	43h	
345	Module Part Number	Blank		20h		
346	Module Part Number	Blank		20h		
347	Module Part Number	Blank		20h		
348	Module Part Number	Blank		20h		
349	Module Revision Code	0.0		00h		
350	DRAM Manufacturer's ID Code, Least Significant Byte	SAMSUNG		80h		
351	DRAM Manufacturer's ID Code, Most Significant Byte	SAMSUNG		CEh		
352	DRAM Stepping	Ver 0.0		00h		
353-381	Module Manufacturer's Specific Data	Reserved		00h		
382-383	Reserved	Reserved		00h		
384-511	End User Programmable	Reserved		00h		

Note : 1. ### #####.
2. ### #####.
3. ### #####.