

# R1LV1616HSA-I Series

Wide Temperature Range Version

16 M SRAM (1-Mword  $\times$  16-bit / 2-Mword  $\times$  8-bit)

REJ03C0195-0103

Rev. 1.03

Feb.20.2020

## Description

The R1LV1616HSA-I Series is 16-Mbit static RAM organized 1-Mword  $\times$  16-bit / 2-Mword  $\times$  8-bit with embedded ECC. R1LV1616HSA-I Series has realized higher density, higher performance and low power consumption by employing CMOS process technology (6-transistor memory cell). It offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It is packaged in 48-pin plastic TSOP for high density surface mounting.

## Features

- Single 3.0 V supply: 2.7 V to 3.6 V
- Fast access time: 45/55 ns (max)
- Power dissipation:
  - Active: 9 mW/MHz (typ)
  - Standby: 1.5  $\mu$ W (typ)
- Completely static memory.
  - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output.
  - Three state output
- Battery backup operation.
  - 2 chip selection for battery backup
- Temperature range:  $-40$  to  $+85^{\circ}\text{C}$
- Byte function (x8 mode) available by BYTE# & A-1
- Embedded ECC (error checking and correction) for single-bit error correction

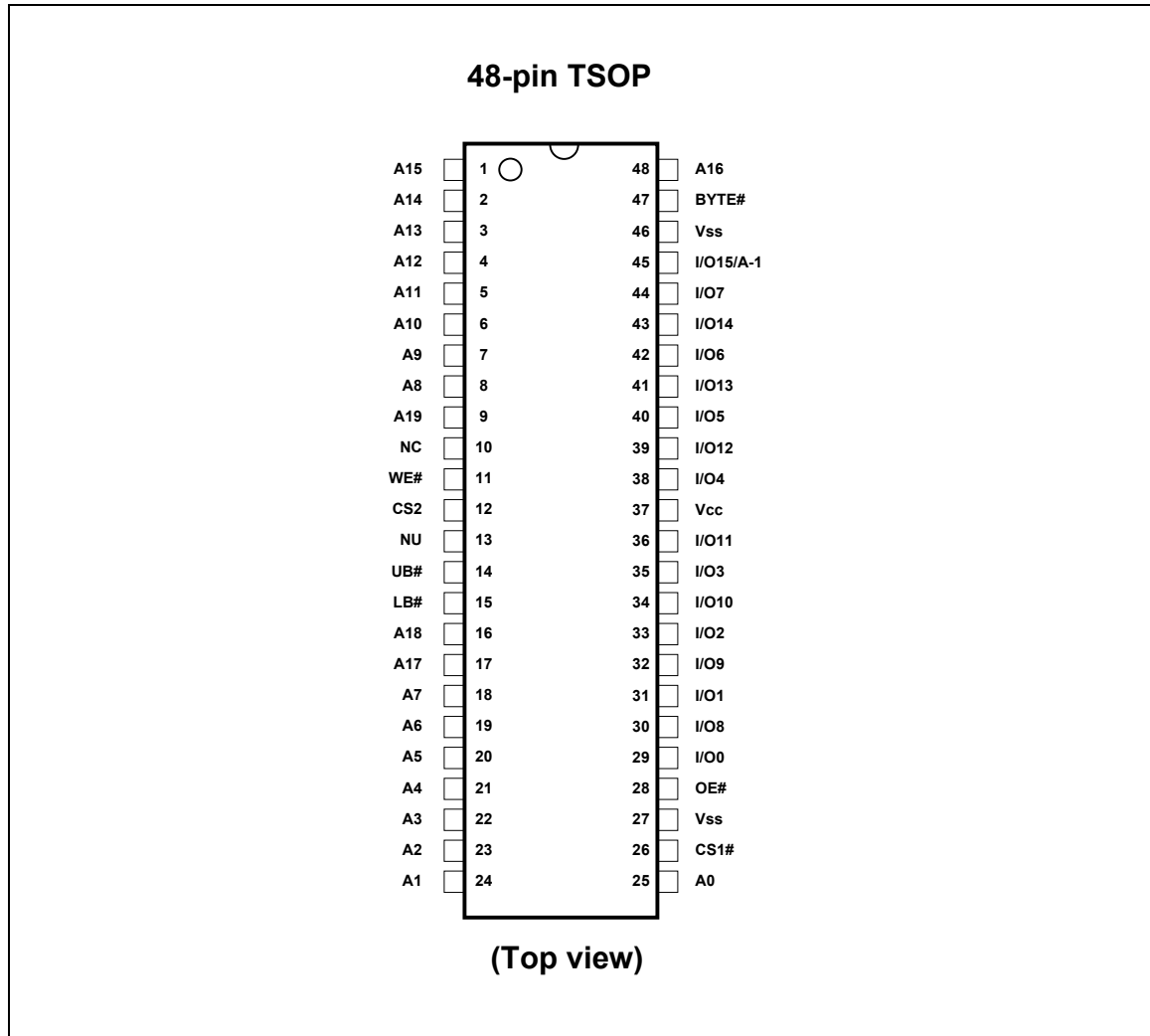
## R1LV1616HSA-I Series

---

### Ordering Information

| Type No.        | Access time | Package              |
|-----------------|-------------|----------------------|
| R1LV1616HSA-4SI | 45 ns       | 48-pin plastic TSOP1 |
| R1LV1616HSA-5SI | 55 ns       |                      |

## Pin Arrangement

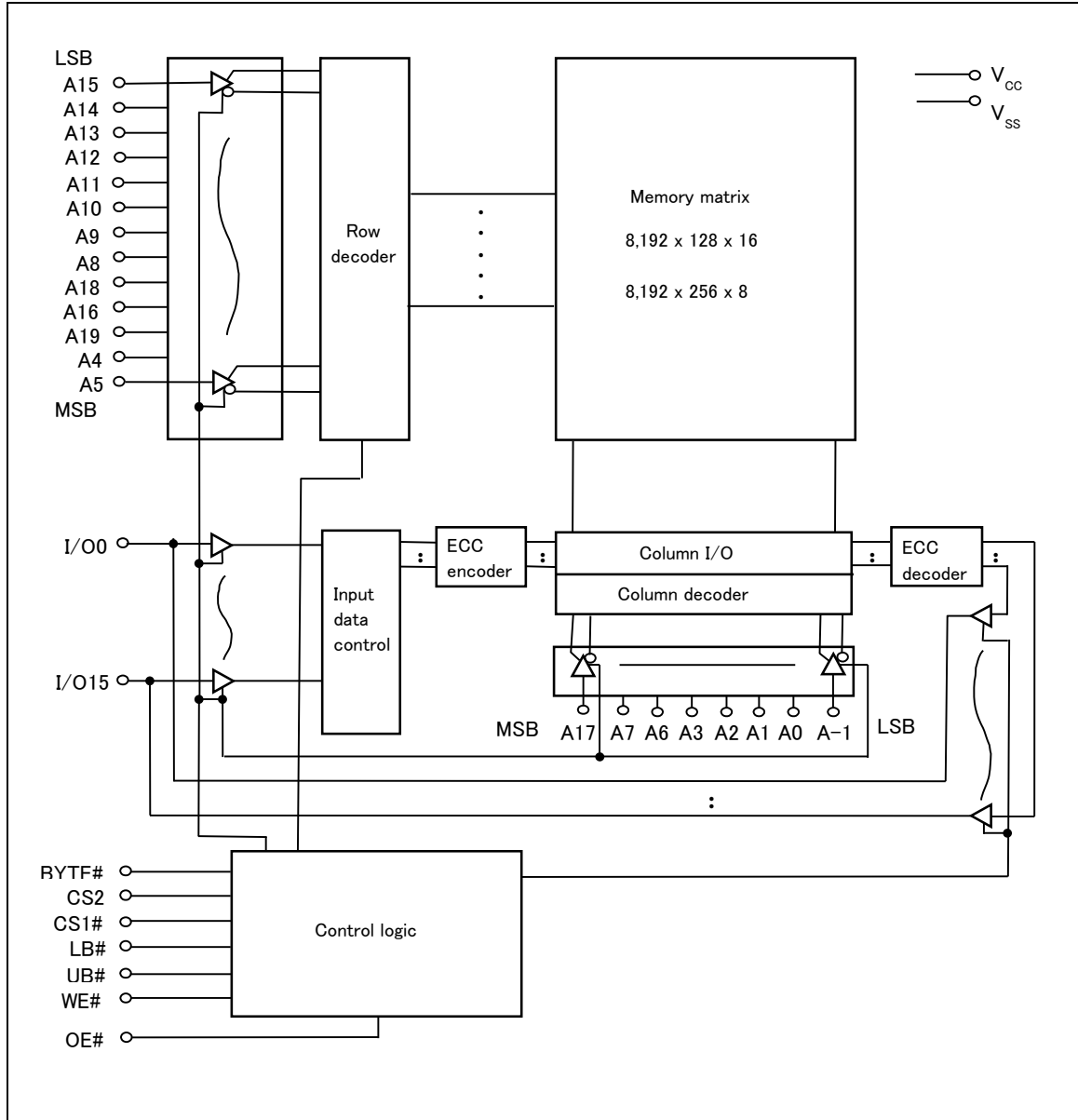


**Pin Description (TSOP)**

| Pin name                           | Function                  |
|------------------------------------|---------------------------|
| A0 to A19                          | Address input (word mode) |
| A-1 to A19                         | Address input (byte mode) |
| I/O0 to I/O15                      | Data input/output         |
| CS1# ( $\overline{\text{CS1}}$ )   | Chip select 1             |
| CS2                                | Chip select 2             |
| WE# ( $\overline{\text{WE}}$ )     | Write enable              |
| OE# ( $\overline{\text{OE}}$ )     | Output enable             |
| LB# ( $\overline{\text{LB}}$ )     | Lower byte select         |
| UB# ( $\overline{\text{UB}}$ )     | Upper byte select         |
| BYTE# ( $\overline{\text{BYTE}}$ ) | Byte enable               |
| V <sub>CC</sub>                    | Power supply              |
| V <sub>SS</sub>                    | Ground                    |
| NC                                 | No connection             |
| NU*1                               | Not used (test mode pin)  |

Note: 1. This pin should be connected to a ground (V<sub>SS</sub>), or not be connected (open).

# Block Diagram (TSOP)



## Operation Table (TSOP)

### Byte mode

| CS1# | CS2 | WE# | OE# | UB# | LB# | BYTE# | I/O0 to I/O7 | I/O8 to I/O14 | I/O15  | Operation      |
|------|-----|-----|-----|-----|-----|-------|--------------|---------------|--------|----------------|
| H    | ×   | ×   | ×   | ×   | ×   | L     | High-Z       | High-Z        | High-Z | Standby        |
| ×    | L   | ×   | ×   | ×   | ×   | L     | High-Z       | High-Z        | High-Z | Standby        |
| L    | H   | H   | L   | ×   | ×   | L     | Dout         | High-Z        | A-1    | Read           |
| L    | H   | L   | ×   | ×   | ×   | L     | Din          | High-Z        | A-1    | Write          |
| L    | H   | H   | H   | ×   | ×   | L     | High-Z       | High-Z        | High-Z | Output disable |

Note: H:  $V_{IH}$ , L:  $V_{IL}$ , ×:  $V_{IH}$  or  $V_{IL}$

### Word mode

| CS1# | CS2 | WE# | OE# | UB# | LB# | BYTE# | I/O0 to I/O7 | I/O8 to I/O14 | I/O15  | Operation        |
|------|-----|-----|-----|-----|-----|-------|--------------|---------------|--------|------------------|
| H    | ×   | ×   | ×   | ×   | ×   | H     | High-Z       | High-Z        | High-Z | Standby          |
| ×    | L   | ×   | ×   | ×   | ×   | H     | High-Z       | High-Z        | High-Z | Standby          |
| ×    | ×   | ×   | ×   | H   | H   | H     | High-Z       | High-Z        | High-Z | Standby          |
| L    | H   | H   | L   | L   | L   | H     | Dout         | Dout          | Dout   | Read             |
| L    | H   | H   | L   | H   | L   | H     | Dout         | High-Z        | High-Z | Lower byte read  |
| L    | H   | H   | L   | L   | H   | H     | High-Z       | Dout          | Dout   | Upper byte read  |
| L    | H   | L   | ×   | L   | L   | H     | Din          | Din           | Din    | Write            |
| L    | H   | L   | ×   | H   | L   | H     | Din          | High-Z        | High-Z | Lower byte write |
| L    | H   | L   | ×   | L   | H   | H     | High-Z       | Din           | Din    | Upper byte write |
| L    | H   | H   | H   | ×   | ×   | H     | High-Z       | High-Z        | High-Z | Output disable   |

Note: H:  $V_{IH}$ , L:  $V_{IL}$ , ×:  $V_{IH}$  or  $V_{IL}$

**Absolute Maximum Ratings**

| Parameter                                               | Symbol            | Value                             | Unit |
|---------------------------------------------------------|-------------------|-----------------------------------|------|
| Power supply voltage relative to V <sub>SS</sub>        | V <sub>CC</sub>   | −0.5 to +4.6                      | V    |
| Terminal voltage on any pin relative to V <sub>SS</sub> | V <sub>T</sub>    | −0.5*1 to V <sub>CC</sub> + 0.3*2 | V    |
| Power dissipation                                       | P <sub>T</sub>    | 1.0                               | W    |
| Storage temperature range                               | T <sub>stg</sub>  | −55 to +125                       | °C   |
| Storage temperature range under bias                    | T <sub>bias</sub> | −40 to +85                        | °C   |

Notes: 1. V<sub>T</sub> min: −2.0 V for pulse half-width ≤ 10 ns.  
2. Maximum voltage is +4.6 V.

**DC Operating Conditions**

| Parameter                 | Symbol          | Min  | Typ | Max                   | Unit | Note |
|---------------------------|-----------------|------|-----|-----------------------|------|------|
| Supply voltage            | V <sub>CC</sub> | 2.7  | 3.0 | 3.6                   | V    |      |
|                           | V <sub>SS</sub> | 0    | 0   | 0                     | V    |      |
| Input high voltage        | V <sub>IH</sub> | 2.2  | —   | V <sub>CC</sub> + 0.3 | V    |      |
| Input low voltage         | V <sub>IL</sub> | −0.3 | —   | 0.6                   | V    | 1    |
| Ambient temperature range | T <sub>a</sub>  | −40  | —   | +85                   | °C   |      |

Note: 1. V<sub>IL</sub> min: −2.0 V for pulse half-width ≤ 10 ns.

## DC Characteristics

| Parameter                 | Symbol                   | Min            | Typ   | Max | Unit          | Test conditions*2                                                                                                                                                                                                                                                                                              |
|---------------------------|--------------------------|----------------|-------|-----|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Input leakage current     | $ I_{LI} $               | —              | —     | 1   | $\mu\text{A}$ | $V_{in} = V_{SS} \text{ to } V_{CC}$                                                                                                                                                                                                                                                                           |
| Output leakage current    | $ I_{LO} $               | —              | —     | 1   | $\mu\text{A}$ | CS1# = $V_{IH}$ or CS2 = $V_{IL}$ or<br>OE# = $V_{IH}$ or WE# = $V_{IL}$ or<br>LB# = UB# = $V_{IH}$ , $V_{I/O} = V_{SS} \text{ to } V_{CC}$                                                                                                                                                                    |
| Operating current         | $I_{CC}$                 | —              | —     | 20  | mA            | CS1# = $V_{IL}$ , CS2 = $V_{IH}$ ,<br>Others = $V_{IH}/V_{IL}$ , $I_{I/O} = 0 \text{ mA}$                                                                                                                                                                                                                      |
| Average operating current | $I_{CC1}$<br>(READ)      | —              | 22*1  | 35  | mA            | Min. cycle, duty = 100%,<br>$I_{I/O} = 0 \text{ mA}$ , CS1# = $V_{IL}$ , CS2 = $V_{IH}$ ,<br>WE# = $V_{IH}$ , Others = $V_{IH}/V_{IL}$                                                                                                                                                                         |
|                           | $I_{CC1}$                | —              | 30*1  | 50  | mA            | Min. cycle, duty = 100%,<br>$I_{I/O} = 0 \text{ mA}$ , CS1# = $V_{IL}$ , CS2 = $V_{IH}$ ,<br>Others = $V_{IH}/V_{IL}$                                                                                                                                                                                          |
|                           | $I_{CC2}^{*3}$<br>(READ) | —              | 3*1   | 8   | mA            | Cycle time = 70 ns, duty = 100%,<br>$I_{I/O} = 0 \text{ mA}$ , CS1# = $V_{IL}$ , CS2 = $V_{IH}$ ,<br>WE# = $V_{IH}$ , Others = $V_{IH}/V_{IL}$<br>Address increment scan or<br>decrement scan                                                                                                                  |
|                           | $I_{CC2}^{*3}$           | —              | 20*1  | 30  | mA            | Cycle time = 70 ns, duty = 100%,<br>$I_{I/O} = 0 \text{ mA}$ , CS1# = $V_{IL}$ , CS2 = $V_{IH}$ ,<br>Others = $V_{IH}/V_{IL}$<br>Address increment scan or<br>decrement scan                                                                                                                                   |
|                           | $I_{CC3}$                | —              | 3*1   | 8   | mA            | Cycle time = 1 $\mu\text{s}$ , duty = 100%,<br>$I_{I/O} = 0 \text{ mA}$ , CS1# $\leq 0.2 \text{ V}$ ,<br>CS2 $\geq V_{CC} - 0.2 \text{ V}$ ,<br>$V_{IH} \geq V_{CC} - 0.2 \text{ V}$ , $V_{IL} \leq 0.2 \text{ V}$                                                                                             |
| Standby current           | $I_{SB}$                 | —              | 0.1*1 | 0.5 | mA            | CS2 = $V_{IL}$                                                                                                                                                                                                                                                                                                 |
| Standby current           | $I_{SB1}$                | —              | 0.5*1 | 8   | $\mu\text{A}$ | $0 \text{ V} \leq V_{in}$<br>(1) $0 \text{ V} \leq \text{CS2} \leq 0.2 \text{ V}$ or<br>(2) CS1# $\geq V_{CC} - 0.2 \text{ V}$ ,<br>CS2 $\geq V_{CC} - 0.2 \text{ V}$ or<br>(3) LB# = UB# $\geq V_{CC} - 0.2 \text{ V}$ ,<br>CS2 $\geq V_{CC} - 0.2 \text{ V}$ ,<br>CS1# $\leq 0.2 \text{ V}$<br>Average value |
| Output high voltage       | $V_{OH}$                 | 2.4            | —     | —   | V             | $I_{OH} = -1 \text{ mA}$                                                                                                                                                                                                                                                                                       |
|                           | $V_{OH}$                 | $V_{CC} - 0.2$ | —     | —   | V             | $I_{OH} = -100 \mu\text{A}$                                                                                                                                                                                                                                                                                    |
| Output low voltage        | $V_{OL}$                 | —              | —     | 0.4 | V             | $I_{OL} = 2 \text{ mA}$                                                                                                                                                                                                                                                                                        |
|                           | $V_{OL}$                 | —              | —     | 0.2 | V             | $I_{OL} = 100 \mu\text{A}$                                                                                                                                                                                                                                                                                     |

## R1LV1616HSA-I Series

---

Notes: 1. Typical values are at  $V_{CC} = 3.0\text{ V}$ ,  $T_a = +25^\circ\text{C}$  and not guaranteed.  
2.  $\text{BYTE\#} \geq V_{CC} - 0.2\text{ V}$  or  $\text{BYTE\#} \leq 0.2\text{ V}$   
3.  $I_{CC2}$  is the value measured while the valid address is increasing or decreasing by one bit.  
Word mode: LSB (least significant bit) is A0.  
Byte mode: LSB (least significant bit) is A-1.

## Capacitance

( $T_a = +25^\circ\text{C}$ ,  $f = 1.0\text{ MHz}$ )

| Parameter                | Symbol    | Min | Typ | Max | Unit | Test conditions        | Note |
|--------------------------|-----------|-----|-----|-----|------|------------------------|------|
| Input capacitance        | $C_{in}$  | —   | —   | 8   | pF   | $V_{in} = 0\text{ V}$  | 1    |
| Input/output capacitance | $C_{I/O}$ | —   | —   | 10  | pF   | $V_{I/O} = 0\text{ V}$ | 1    |

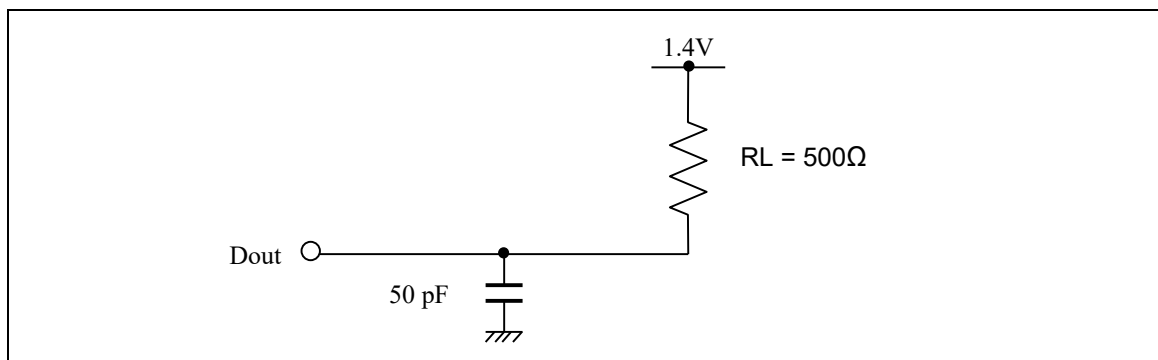
Note: 1. This parameter is sampled and not 100% tested.

## AC Characteristics

( $T_a = -40$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 2.7$  V to  $3.6$  V, unless otherwise noted.)

### Test Conditions

- Input pulse levels:  $V_{IL} = 0.4$  V,  $V_{IH} = 2.4$  V
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.4 V
- Output load: See figures (Including scope and jig)



## R1LV1616HSA-I Series

### Read Cycle

| Parameter                          | Symbol            | R1LV1616HSA-I |     |      |     | Unit | Notes   |
|------------------------------------|-------------------|---------------|-----|------|-----|------|---------|
|                                    |                   | -4SI          |     | -5SI |     |      |         |
|                                    |                   | Min           | Max | Min  | Max |      |         |
| Read cycle time                    | t <sub>RC</sub>   | 45            | —   | 55   | —   | ns   |         |
| Address access time                | t <sub>AA</sub>   | —             | 45  | —    | 55  | ns   |         |
| Chip select access time            | t <sub>ACS1</sub> | —             | 45  | —    | 55  | ns   |         |
|                                    | t <sub>ACS2</sub> | —             | 45  | —    | 55  | ns   |         |
| Output enable to output valid      | t <sub>OE</sub>   | —             | 30  | —    | 35  | ns   |         |
| Output hold from address change    | t <sub>OH</sub>   | 10            | —   | 10   | —   | ns   |         |
| LB#, UB# access time               | t <sub>BA</sub>   | —             | 45  | —    | 55  | ns   |         |
| Chip select to output in low-Z     | t <sub>CLZ1</sub> | 10            | —   | 10   | —   | ns   | 2, 3    |
|                                    | t <sub>CLZ2</sub> | 10            | —   | 10   | —   | ns   | 2, 3    |
| LB#, UB# enable to low-Z           | t <sub>BLZ</sub>  | 5             | —   | 5    | —   | ns   | 2, 3    |
| Output enable to output in low-Z   | t <sub>OLZ</sub>  | 5             | —   | 5    | —   | ns   | 2, 3    |
| Chip deselect to output in high-Z  | t <sub>CHZ1</sub> | 0             | 20  | 0    | 20  | ns   | 1, 2, 3 |
|                                    | t <sub>CHZ2</sub> | 0             | 20  | 0    | 20  | ns   | 1, 2, 3 |
| LB#, UB# disable to high-Z         | t <sub>BHZ</sub>  | 0             | 15  | 0    | 20  | ns   | 1, 2, 3 |
| Output disable to output in high-Z | t <sub>OHZ</sub>  | 0             | 15  | 0    | 20  | ns   | 1, 2, 3 |

### Write Cycle

| Parameter                          | Symbol           | R1LV1616HSA-I |     |      |     | Unit | Notes |
|------------------------------------|------------------|---------------|-----|------|-----|------|-------|
|                                    |                  | -4SI          |     | -5SI |     |      |       |
|                                    |                  | Min           | Max | Min  | Max |      |       |
| Write cycle time                   | t <sub>WC</sub>  | 45            | —   | 55   | —   | ns   |       |
| Address valid to end of write      | t <sub>AW</sub>  | 45            | —   | 50   | —   | ns   |       |
| Chip selection to end of write     | t <sub>CW</sub>  | 45            | —   | 50   | —   | ns   | 5     |
| Write pulse width                  | t <sub>WP</sub>  | 35            | —   | 40   | —   | ns   | 4     |
| LB#, UB# valid to end of write     | t <sub>BW</sub>  | 45            | —   | 50   | —   | ns   |       |
| Address setup time                 | t <sub>AS</sub>  | 0             | —   | 0    | —   | ns   | 6     |
| Write recovery time                | t <sub>WR</sub>  | 0             | —   | 0    | —   | ns   | 7     |
| Data to write time overlap         | t <sub>DW</sub>  | 25            | —   | 25   | —   | ns   |       |
| Data hold from write time          | t <sub>DH</sub>  | 0             | —   | 0    | —   | ns   |       |
| Output active from end of write    | t <sub>OW</sub>  | 5             | —   | 5    | —   | ns   | 2     |
| Output disable to output in high-Z | t <sub>OHZ</sub> | 0             | 15  | 0    | 20  | ns   | 1, 2  |
| Write to output in high-Z          | t <sub>WHZ</sub> | 0             | 15  | 0    | 20  | ns   | 1, 2  |

## R1LV1616HSA-I Series

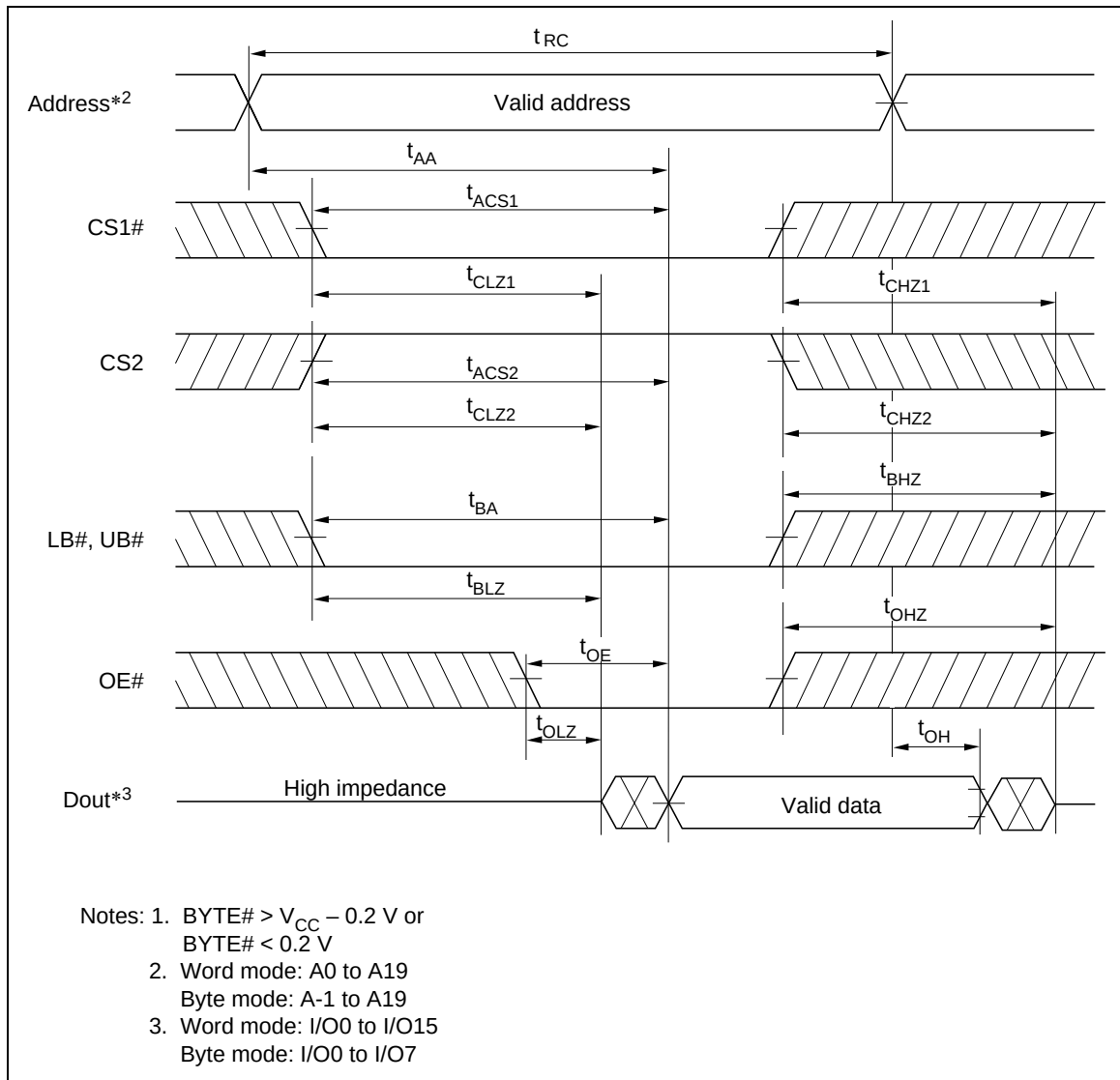
### Byte Control

| Parameter           | Symbol          | R1LV1616HSA-I |     |      |     | Unit | Notes |
|---------------------|-----------------|---------------|-----|------|-----|------|-------|
|                     |                 | -4SI          |     | -5SI |     |      |       |
|                     |                 | Min           | Max | Min  | Max |      |       |
| BYTE# setup time    | t <sub>BS</sub> | 5             | —   | 5    | —   | ms   |       |
| BYTE# recovery time | t <sub>BR</sub> | 5             | —   | 5    | —   | ms   |       |

- Notes:
1.  $t_{CHZ}$ ,  $t_{OHZ}$ ,  $t_{WHZ}$  and  $t_{BHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
  2. This parameter is sampled and not 100% tested.
  3. At any given temperature and voltage condition,  $t_{HZ}$  max is less than  $t_{LZ}$  min both for a given device and from device to device.
  4. A write occurs during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#. A write begins at the latest transition among CS1# going low, CS2 going high, WE# going low and LB# going low or UB# going low. A write ends at the earliest transition among CS1# going high, CS2 going low, WE# going high and LB# going high or UB# going high.  $t_{WP}$  is measured from the beginning of write to the end of write.
  5.  $t_{CW}$  is measured from the later of CS1# going low or CS2 going high to the end of write.
  6.  $t_{AS}$  is measured from the address valid to the beginning of write.
  7.  $t_{WR}$  is measured from the earliest of CS1# or WE# going high or CS2 going low to the end of write cycle.

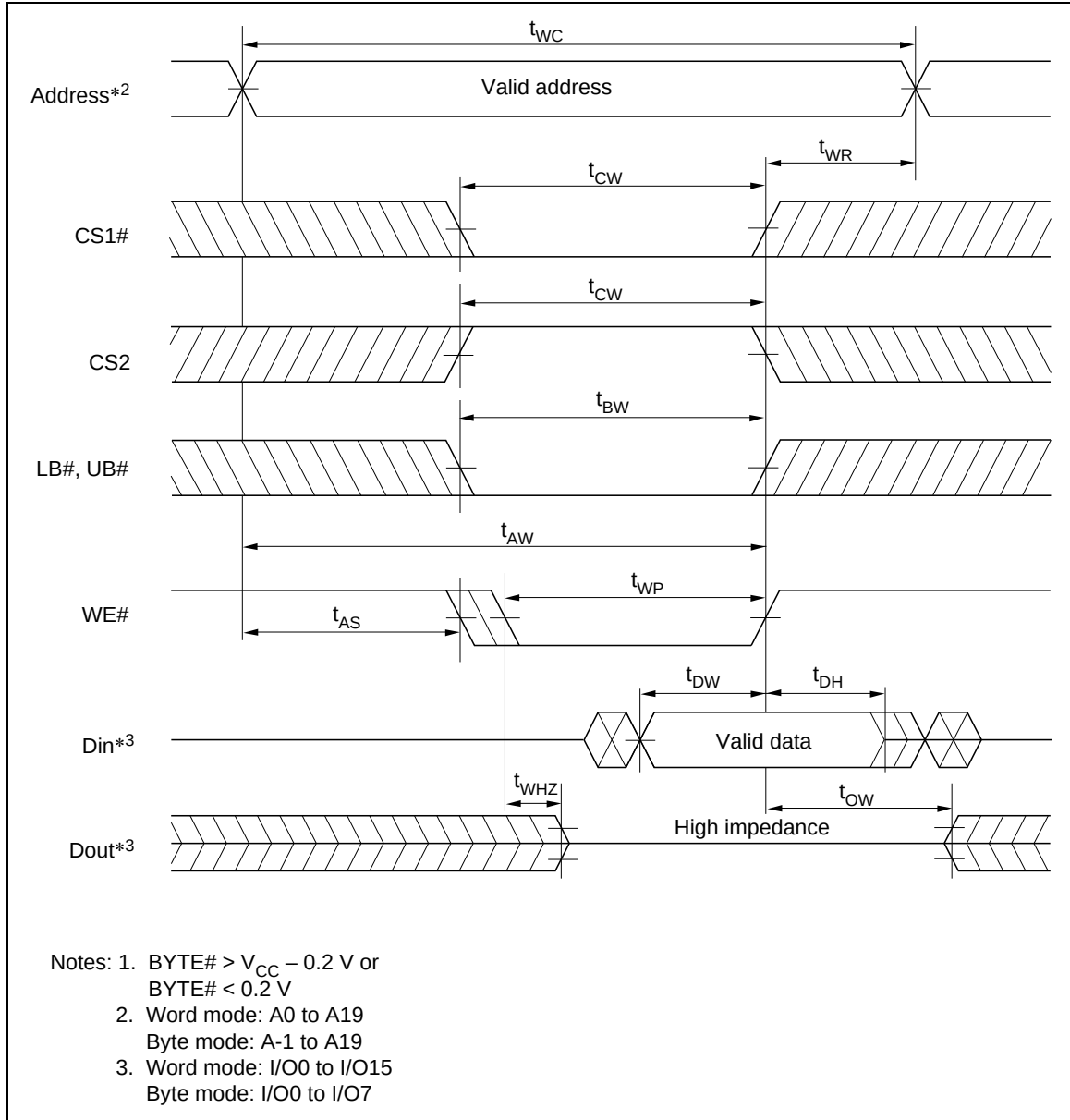
## Timing Waveform

### Read Cycle\*1



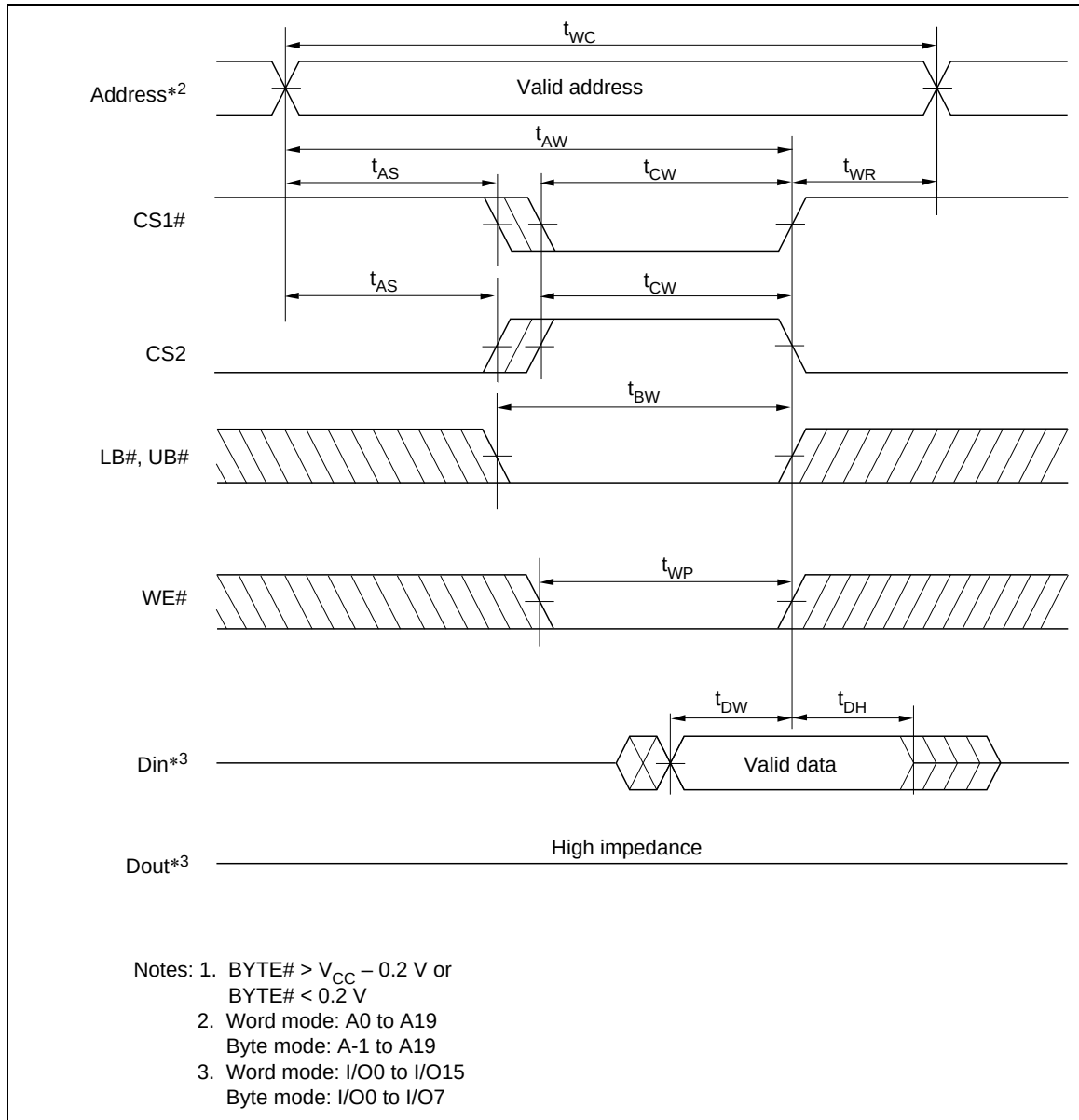
## R1LV1616HSA-I Series

### Write Cycle (1)\*<sup>1</sup> (WE# Clock)



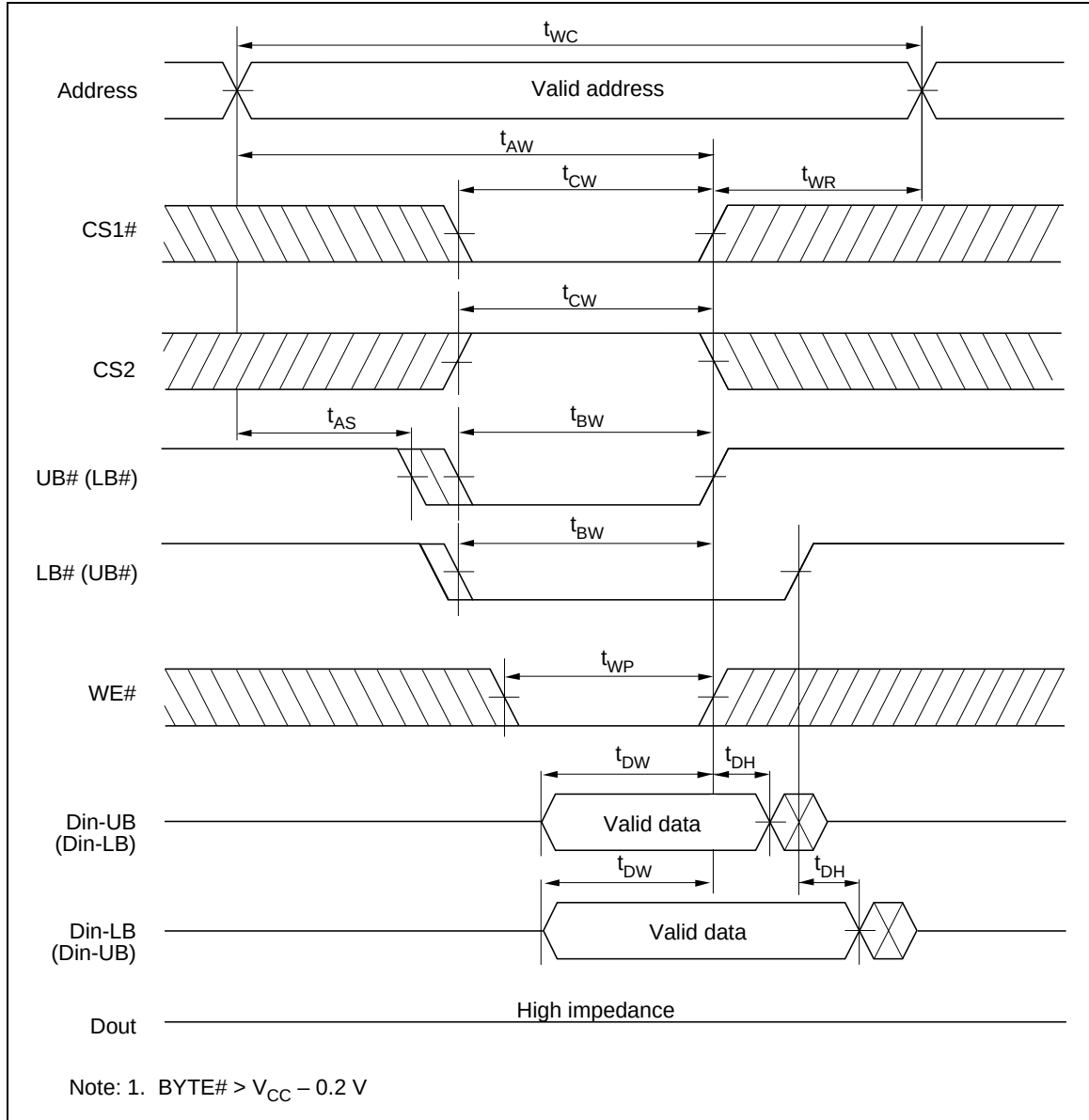
## R1LV1616HSA-I Series

**Write Cycle (2)\*<sup>1</sup>** (CS1#, CS2 Clock, OE# = V<sub>IH</sub>)

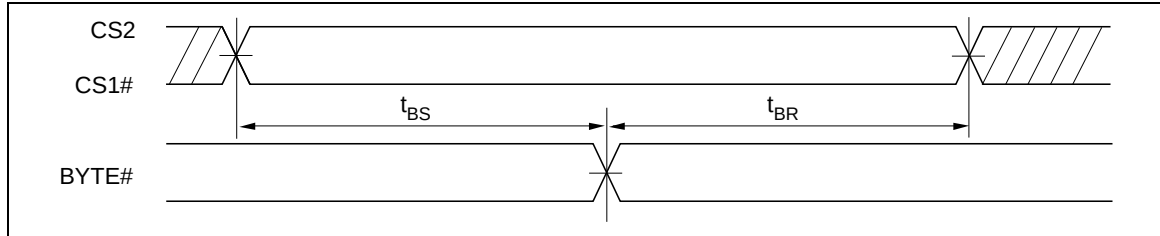


## R1LV1616HSA-I Series

Write Cycle (3)\*<sup>1</sup> (LB#, UB# Clock, OE# = V<sub>IH</sub>)



**Byte Control (TSOP)**



Low  $V_{CC}$  Data Retention Characteristics

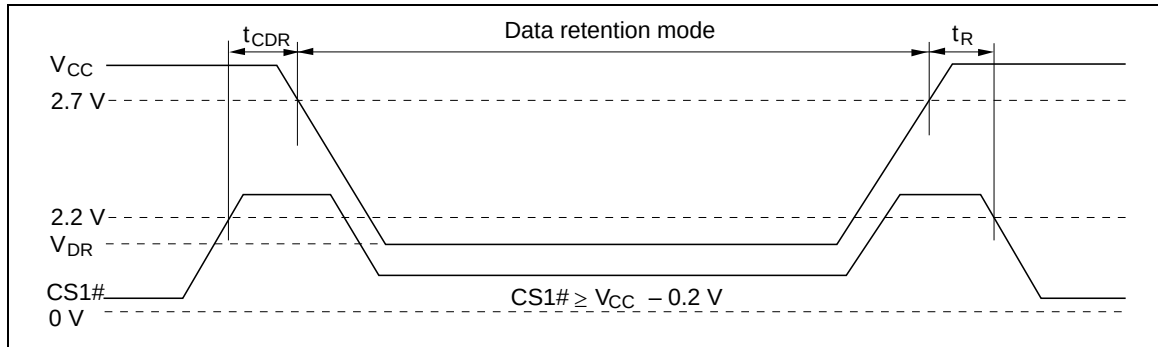
(Ta = -40 to +85°C)

| Parameter                            | Symbol     | Min | Typ   | Max | Unit    | Test conditions*2, 3                                                                                                                                                                                                                                       |
|--------------------------------------|------------|-----|-------|-----|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| $V_{CC}$ for data retention          | $V_{DR}$   | 1.5 | —     | 3.6 | V       | $V_{in} \geq 0$ V<br>(1) $0$ V $\leq$ CS2 $\leq$ 0.2 V or<br>(2) CS2 $\geq V_{CC} - 0.2$ V,<br>CS1# $\geq V_{CC} - 0.2$ V or<br>(3) LB# = UB# $\geq V_{CC} - 0.2$ V,<br>CS2 $\geq V_{CC} - 0.2$ V,<br>CS1# $\leq$ 0.2 V                                    |
| Data retention current               | $I_{CCDR}$ | —   | 0.5*1 | 8   | $\mu$ A | $V_{CC} = 3.0$ V, $V_{in} \geq 0$ V<br>(1) $0$ V $\leq$ CS2 $\leq$ 0.2 V or<br>(2) CS2 $\geq V_{CC} - 0.2$ V,<br>CS1# $\geq V_{CC} - 0.2$ V or<br>(3) LB# = UB# $\geq V_{CC} - 0.2$ V,<br>CS2 $\geq V_{CC} - 0.2$ V,<br>CS1# $\leq$ 0.2 V<br>Average value |
| Chip deselect to data retention time | $t_{CDR}$  | 0   | —     | —   | ns      | See retention waveforms                                                                                                                                                                                                                                    |
| Operation recovery time              | $t_R$      | 5   | —     | —   | ms      |                                                                                                                                                                                                                                                            |

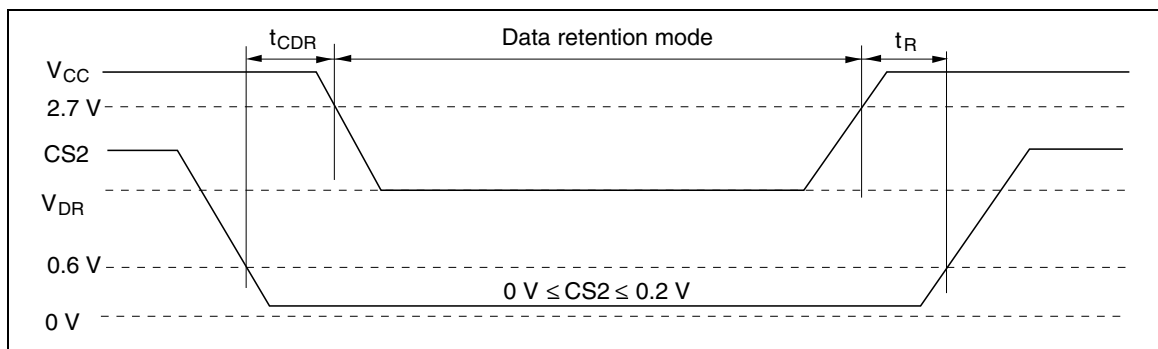
Notes: 1. Typical values are at  $V_{CC} = 3.0$  V, Ta = +25°C and not guaranteed.2. BYTE#  $\geq V_{CC} - 0.2$  V or BYTE#  $\leq 0.2$  V3. CS2 controls address buffer, WE# buffer, CS1# buffer, OE# buffer, LB#, UB# buffer and Din buffer. If CS2 controls data retention mode, Vin levels (address, WE#, OE#, CS1#, LB#, UB#, I/O) can be in the high impedance state. If CS1# controls data retention mode, CS2 must be CS2  $\geq V_{CC} - 0.2$  V or  $0$  V  $\leq$  CS2  $\leq$  0.2 V. The other input levels (address, WE#, OE#, LB#, UB#, I/O) can be in the high impedance state.

## R1LV1616HSA-I Series

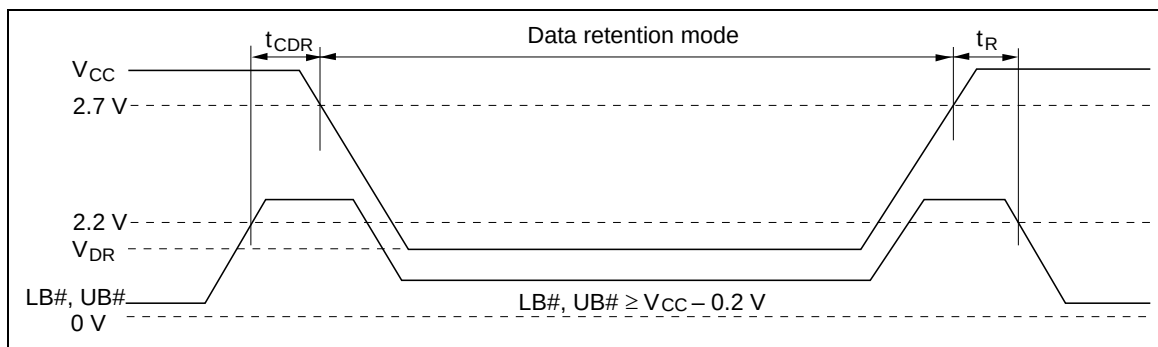
### Low $V_{CC}$ Data Retention Timing Waveform (1) (CS1# Controlled)



### Low $V_{CC}$ Data Retention Timing Waveform (2) (CS2 Controlled)



### Low $V_{CC}$ Data Retention Timing Waveform (3) (LB#, UB# Controlled)



## Revision History

## R1LV1616HSA-I Series Data Sheet

| Rev. | Date        | Contents of Modification |                                          |
|------|-------------|--------------------------|------------------------------------------|
|      |             | Page                     | Description                              |
| 1.00 | Apr.22.2004 | —                        | Initial issue                            |
| 1.01 | Nov.18.2004 | —                        | Addition of 2-Mword x 8-bit function     |
| 1.02 | Feb.23.2017 | p.1,p.5                  | Disclosed embedded ECC features          |
|      |             | p.2                      | Deleted previous package code (48P3R-B)  |
| 1.03 | Feb.20.2020 | Last page                | Updated the Notice to the latest version |

## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:  
[www.renesas.com/contact/](http://www.renesas.com/contact/)

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.