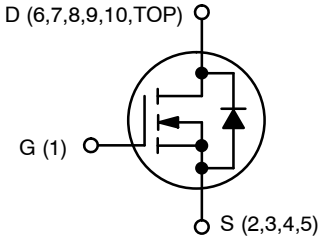
MOSFET - Power, Single N-Channel, STD Gate, TCPAK57

80 V, 2.8 mohm, 157 A

NVMJST2D8N08X

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
80 V	2.8 mΩ @ V_{GS} = 10 V	157 A



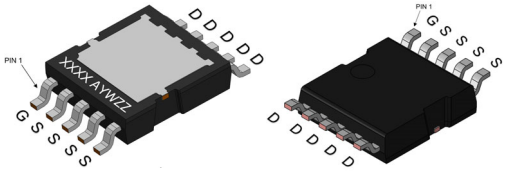
N−CHANNEL MOSFET

Features

- Low Q_{RR}, Soft Recovery Body Diode
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- AECQ101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Synchronous Rectification (SR) in DC-DC and AC-DC
- Primary Switch in Isolated DC-DC Converter
- Motor Drives
- Automotive 48 V System



TCPAK57
CASE 760AG

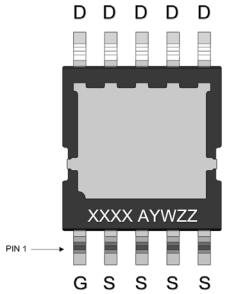
MAXIMUM RATINGS (T_J = 25 °C unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	80	V
Gate-to-Source Voltage		V_{GS}	20	V
Continuous Drain Current	T_C = 25 °C	I_D	157	A
	T_C = 100 °C		111	
Power Dissipation	T_C = 25 °C	P_D	136	W
Pulsed Drain Current	T_C = 25 °C, t_p = 100 μs	I_{DM}	483	A
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to +175	°C
Continuous Source-Drain Current (Body Diode)	T_C = 25 °C, V_{GS} = 0 V	I_S	157	A
Single Pulse Avalanche Energy (I_{PK} = 52 A)		E_{AS}	135	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)		T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using a 1 in^2, 1 oz. Cu pad
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
3. E_{AS} is based on started T_J = 25 °C, rated I_{AS}, V_{DD} = 64 V, V_{GS} = 10 V, 100% avalanche tested.

MARKING DIAGRAM



XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Assembly Lot Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

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THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.1	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	44	

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA, T_J = 25 °C	80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	I_D = 1 mA, Referenced to 25 °C		41.8		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, T_J = 25 °C			1	μA
		V_{DS} = 80 V, T_J = 125 °C (Note 4)			250	
Gate-to-Source Leakage Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
ON CHARACTERISTICS						
Drain-to-Source On Resistance	$R_{DS(ON)}$	V_{GS} = 10 V, I_D = 30 A, T_J = 25 °C		2.4	2.8	mΩ
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 184 μA, T_J = 25 °C	2.4		3.6	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)}/\Delta T_J$	V_{GS} = V_{DS}, I_D = 184 μA		−8.3		mV/°C
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 30 A		101		S
CHARGES, CAPACITANCES & GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{DS} = 40 V, V_{GS} = 0 V, f = 1 MHz		3192		pF
Output Capacitance	C_{OSS}			923		
Reverse Transfer Capacitance	C_{RSS}			14		
Output Charge	Q_{OSS}			66		nC
Total Gate Charge	$Q_{G(TOT)}$	V_{DD} = 40 V, I_D = 30 A, V_{GS} = 10 V		45		
Threshold Gate Charge	$Q_{G(TH)}$			9.8		
Gate-to-Source Charge	Q_{GS}			15		
Gate-to-Drain Charge	Q_{GD}			7.0		
Gate Plateau Voltage	V_{GP}			4.7		V
Gate Resistance	R_G	f = 1 MHz		0.75		Ω
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{d(ON)}$	Resistive Load V_{GS} = 0/10 V, V_{DD} = 64 V, I_D = 37 A, R_G = 2.5 Ω		24		ns
Rise Time	t_r			7.4		
Turn-Off Delay Time	$t_{d(OFF)}$			37		
Fall Time	t_f			5.6		
SOURCE-TO-DRAIN DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 30 A, T_J = 25 °C		0.82	0.93	V
		V_{GS} = 0 V, I_S = 30 A, T_J = 125 °C		0.71		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, I_S = 30 A, dI/dt = 1000 A/μs, V_{DD} = 64 V		23		ns
Charge Time	t_a			13		
Discharge Time	t_b			10		
Reverse Recovery Charge	Q_{RR}			162		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Guaranteed by design and is not production tested

TYPICAL CHARACTERISTICS

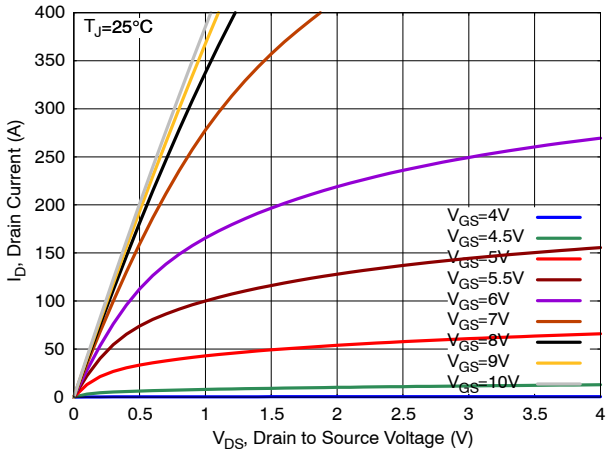


Figure 1. On-Region Characteristics

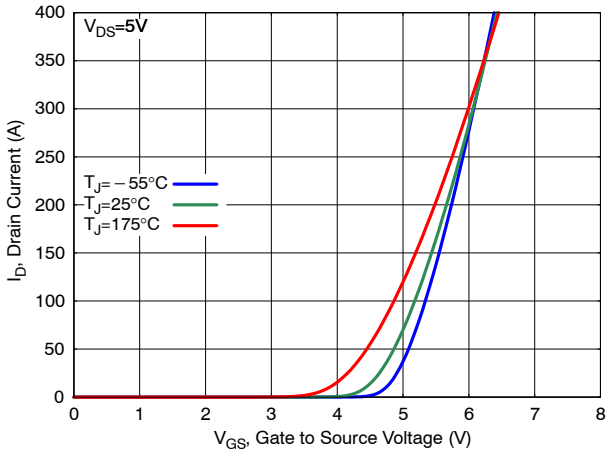


Figure 2. Transfer Characteristics

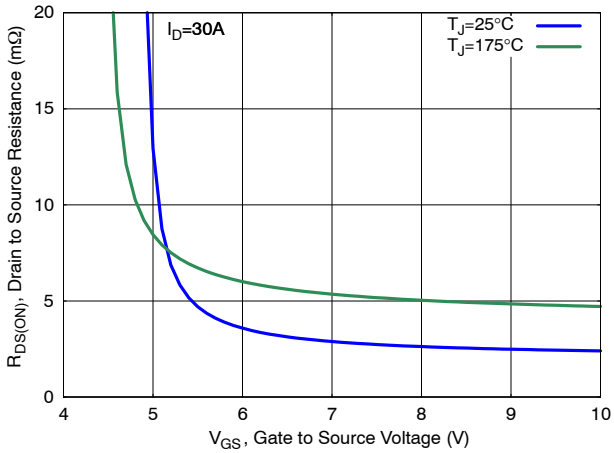


Figure 3. On-Resistance vs. Gate Voltage

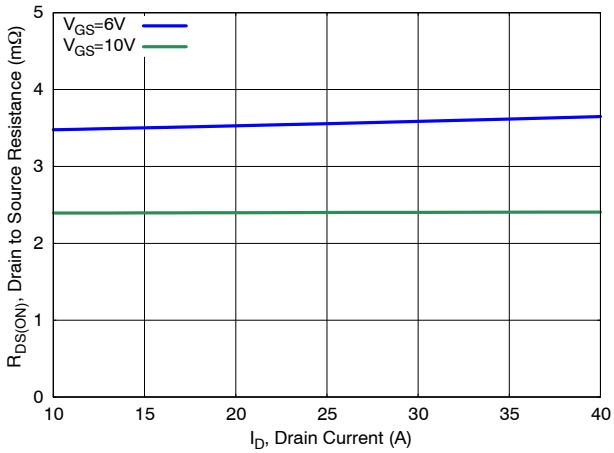


Figure 4. On-Resistance vs. Drain Current

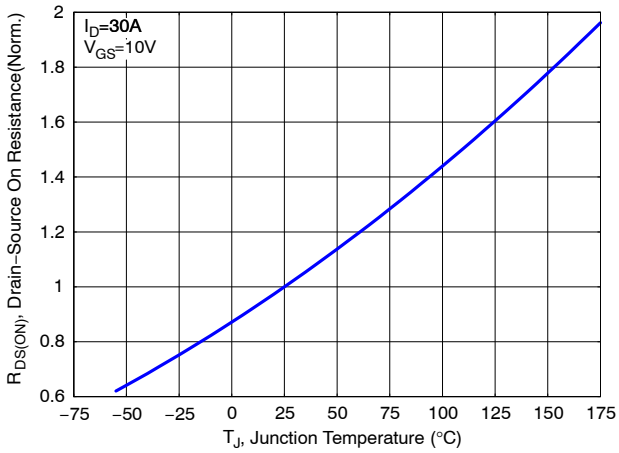


Figure 5. Normalized ON Resistance vs. Junction Temperature

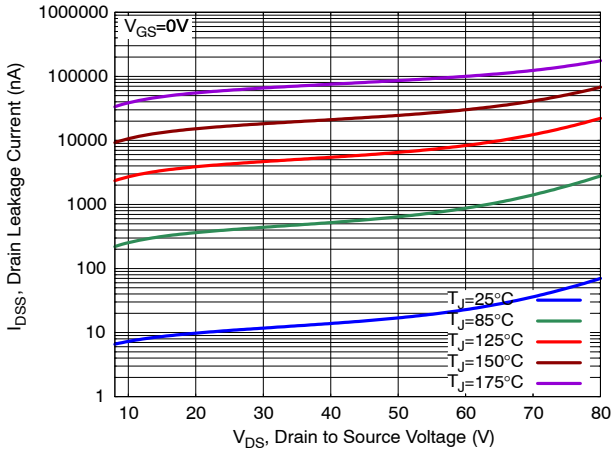


Figure 6. Drain Leakage Current vs. Drain Voltage

TYPICAL CHARACTERISTICS

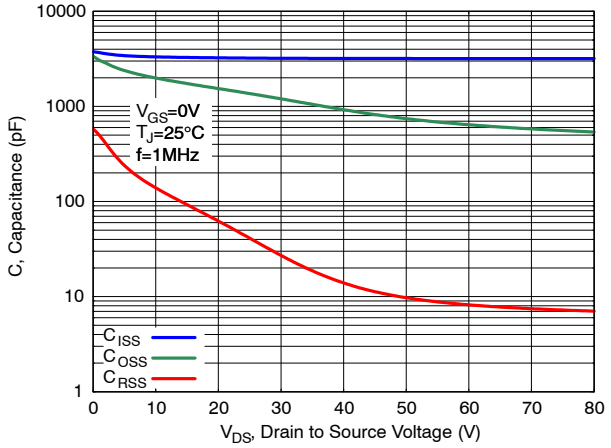


Figure 7. Capacitance Characteristics

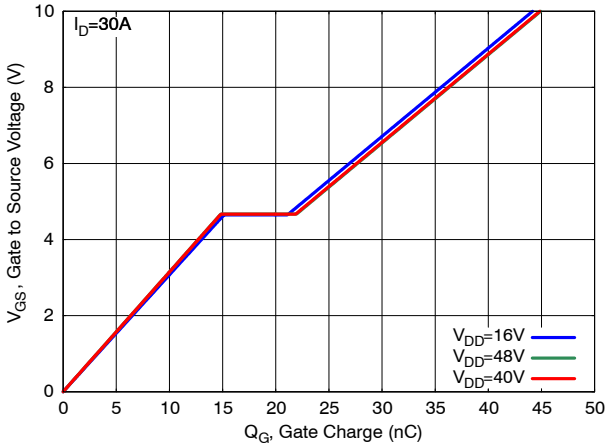


Figure 8. Gate Charge Characteristics

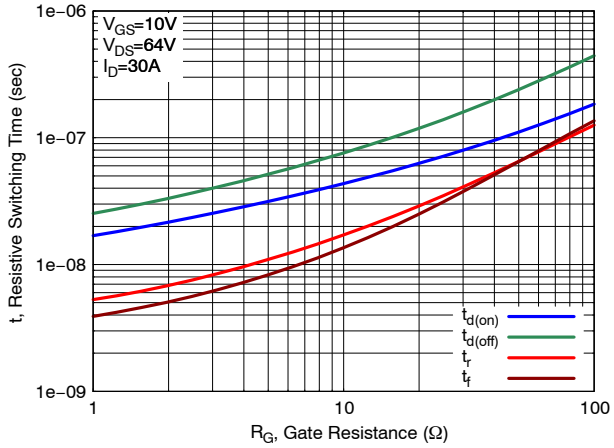


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

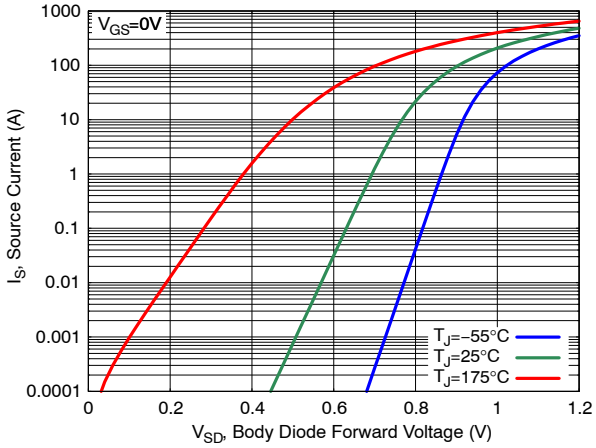


Figure 10. Diode Forward Characteristics

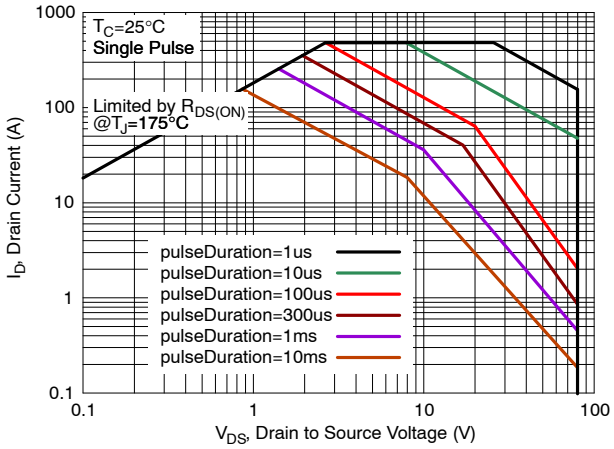


Figure 11. Safe Operating Area (SOA)

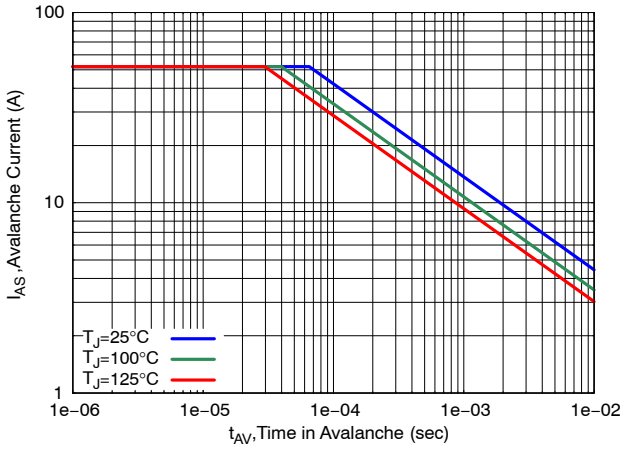


Figure 12. Avalanche Current vs. Pulse Time (UIS)

TYPICAL CHARACTERISTICS

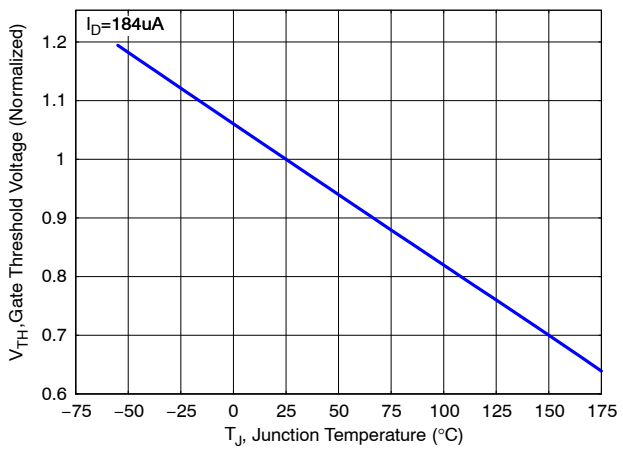


Figure 13. Gate Threshold Voltage vs. Junction Temperature

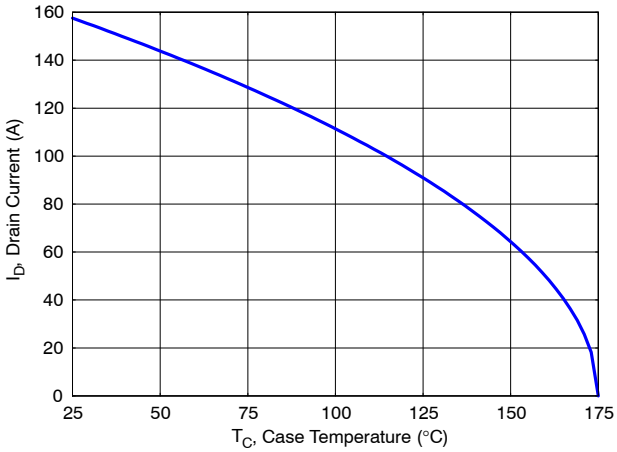


Figure 14. Maximum Current vs. Case Temperature

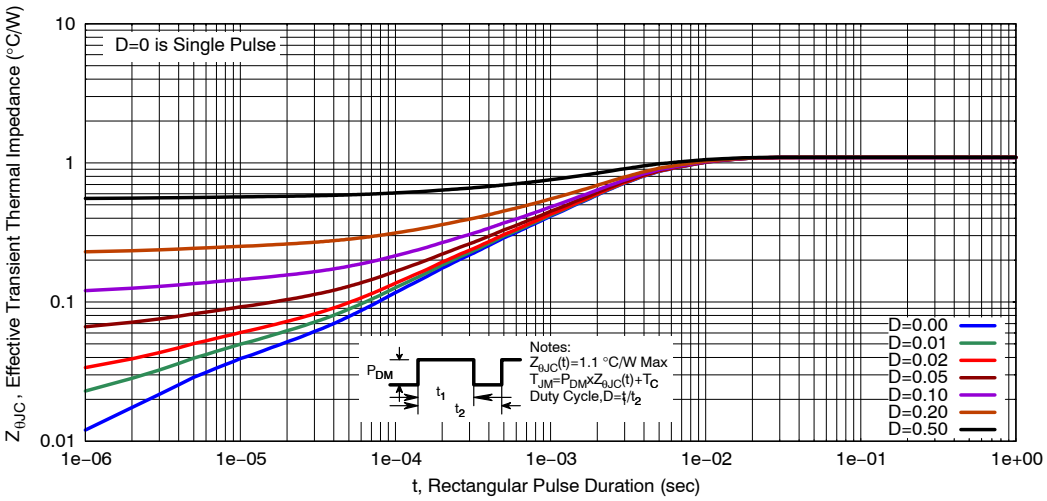


Figure 15. Transient Thermal Response

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NVMJST2D8N08XTXG	2D88	TCPAK57 Top Cool (Pb-Free)	3000 / Tape & Reel

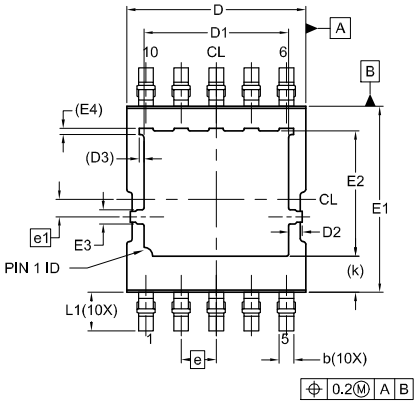
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

REVISION HISTORY

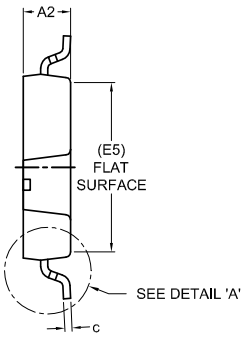
Revision	Description of Changes	Date
0	Initial Document release.	4/24/2026
1	Maximum VSD specification updated from 1.2 V to 0.93 V.	5/1/2026

PACKAGE DIMENSIONS

TCPAK10 5.1x7.5, 1.0P
CASE 760AG
ISSUE D



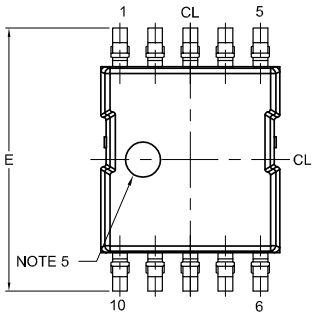
TOP VIEW



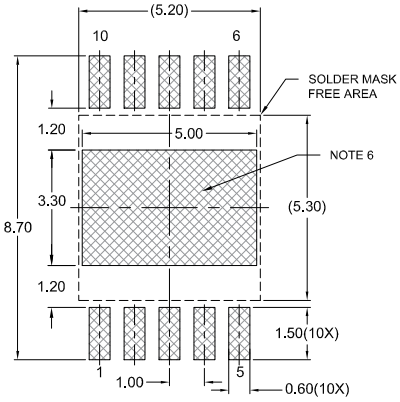
SIDE VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. UNIT DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
4. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. OPTIONAL MOLD FEATURE.
6. LAND PAD UNDER THE PACKAGE BODY IS FOR MECHANICAL SUPPORT ONLY. SOLDER CONNECTION IS NOT REQUIRED.
7. DIMENSION A1 IS THE LEAD STAND-OFF FROM THE BOTTOM SURFACE OF THE PACKAGE BODY.



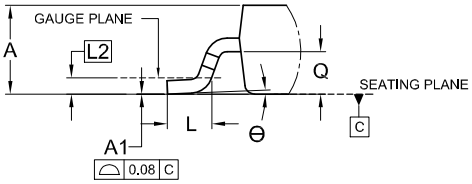
BOTTOM VIEW



LAND PAD RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.30	1.35	1.45
A1	-0.05	0.00	0.05
A2	1.30	1.35	1.40
b	0.36	0.41	0.46
c	0.16	0.21	0.26
D	5.00	5.10	5.20
D1	4.02	4.12	4.22
D2	0.30	0.40	0.50
D3	0.14 REF		
E	7.40	7.50	7.60
E1	5.20	5.30	5.40
E2	3.47	3.57	3.67
E3	0.30	0.40	0.50
E4	0.17 REF		
E5	4.82 REF		
e	1.00 BSC		
e1	0.50 BSC		
k	1.03 REF		
L	0.49	0.69	0.89
L1	0.90	1.10	1.30
L2	0.25 BSC		
Q	0.60	0.65	0.70
ϴ	0°	2.5°	5°



DETAIL 'A'

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