

Enhancement Mode Gallium Nitride (GaN) HEMT

650 V, 39 mΩ, 40 A, PDSO-F9

NTBL050N65GN1

Features

- Low $R_{DS(ON)}$ to Minimize Conduction Losses
- Ultra Low Gate Charge for High Speed Switching
- $FOM-Q_G = 367 \text{ nC} \cdot \text{m}\Omega$
- Small Footprint for High Density PCB Design
- This Device is Halide Free and RoHS Compliant with Exemption 7a, Pb-Free 2LI (on second level interconnection)

Typical Applications

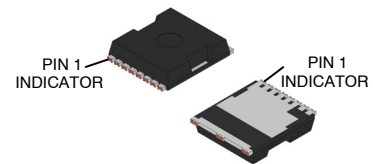
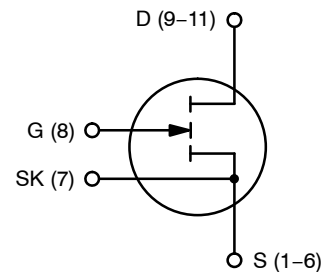
- High Density Power Modules
- High Frequency AC-DC and DC-DC Converters
- High Performance PSU for Datacenter and Industrial
- Resonant Conversion

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	650	V
Drain-to-Source Transient Voltage, $t_p < 200 \mu\text{s}$	$V_{DS(TRAN)}$	800	V
Gate-to-Source Voltage	V_{GS}	-6 to 7	V
Gate-to-Source Transient Voltage, $t_p = 50 \text{ ns}$, $f_p = 100 \text{ kHz}$, open drain	$V_{GS(PULSE)}$	-20 to 10	V
Continuous Drain Current, $T_{CASE} = 25^\circ\text{C}$ $T_{CASE} = 100^\circ\text{C}$	I_{DS}	40 30	A
Pulsed Drain Current, $t_p < 10 \mu\text{s}$, $T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$	$I_{DS(PULSE)}$	77 40	A
Power Dissipation, $V_{GS} = 6 \text{ V}$, $T_{CASE} = 25^\circ\text{C}$	P_{TOT}	250	W
Operating Junction Temperature	T_J	-55 to 150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55 to 150	$^\circ\text{C}$

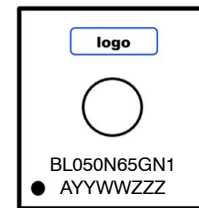
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ TYP}$	$I_{DS} \text{ MAX}$
650 V	39 mΩ	40 A



PDSO-F9 10.38 x 9.90 x 2.30, 1.20P
CASE 207AA

MARKING DIAGRAM



BL050N65GN1 = Specific Device Code
A = Assembly Site
YY = Year of Production
WW = Work Week Number
ZZZ = Assembly Lot Number

ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

NTBL050N65GN1

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Junction-to-Case	$R_{\theta JC}$	0.5	$^{\circ}\text{C/W}$
Junction-to-Ambient (Note 1)	$R_{\theta JA}$	56	$^{\circ}\text{C/W}$
Maximum Soldering Temperature (MSL3)	T_{SLD}	260	$^{\circ}\text{C}$

1. Device on 1 in², 2 oz copper pad on single layer FR-4 PCB

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
-----------	--------	-----------------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}$	650			V
Drain-to-Source Leakage Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 650\text{ V}$		8	100	μA
		$V_{GS} = 0\text{ V}, V_{DS} = 650\text{ V}, T_J = 125^{\circ}\text{C}$ (Note 3)		20		
Gate-to-Source Leakage Current	I_{GSS}	$V_{GS} = 6\text{ V}, V_{DS} = 0\text{ V}$		250		μA
		$V_{GS} = 6\text{ V}, V_{DS} = 0\text{ V}, T_J = 125^{\circ}\text{C}$ (Note 3)		875		μA

ON CHARACTERISTICS (Note 2)

Drain-to-Source On Resistance	$R_{DS(ON)}$	$V_{GS} = 6\text{ V}, I_{DS} = 13\text{ A}$		39	50	m Ω
		$V_{GS} = 6\text{ V}, I_{DS} = 13\text{ A}, T_J = 125^{\circ}\text{C}$ (Note 3)		75		
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}, I_{DS} = 46.8\text{ mA}, T_J = 25^{\circ}\text{C}$	1.2	1.5	2.5	V
		$V_{DS} = V_{GS}, I_{DS} = 46.8\text{ mA}, T_J = 125^{\circ}\text{C}$ (Note 3)		1.4		

DYNAMIC CHARACTERISTICS (Note 3)

Input Capacitance	C_{ISS}	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		338		pF
Output Capacitance	C_{OSS}			118		
Reverse Transfer Capacitance	C_{RSS}			1.5		
Output Capacitance, Energy Related	$C_{OSS(ER)}$	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$		189		pF
Output Capacitance, Time Related	$C_{OSS(TR)}$			255		
Output Charge	Q_{OSS}			102		nC
Output Capacitance Stored Energy	E_{OSS}			15		μJ
Gate Resistance	R_G	$f = 5\text{ MHz}$		1.5		Ω
Gate Charge	Q_G	$V_{DS} = 400\text{ V}, I_{DS} = 13\text{ A}, V_{GS} = 0/6\text{ V}$		10.6		nC
Gate-to-Source Charge	Q_{GS}			4.2		
Gate-to-Drain Charge	Q_{GD}			1.6		
Gate Plateau Voltage	V_{PLAT}			2.8		V

SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	$t_{D(ON)}$	$V_{DS} = 400\text{ V}, I_{DS} = 13\text{ A}, V_{GS} = 0/6\text{ V},$ $R_{G,ON} = 10\text{ }\Omega, R_{G,OFF} = 4\text{ }\Omega$		4.5		ns
Turn-Off Delay Time	$t_{D(OFF)}$			9.2		ns
Turn-On Rise Time	t_R			7.3		ns
Turn-Off Fall Time	t_F			9.9		ns



NTBL050N65GN1

ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
-----------	--------	-----------------	-----	-----	-----	------

REVERSE CONDUCTION CHARACTERISTICS

Source-to-Drain Reverse Voltage	V_{SD}	$V_{GS} = -3\text{ V}, I_{SD} = 13\text{ A}$ (Note 3)		5.4		V
		$V_{GS} = 0\text{ V}, I_{SD} = 13\text{ A}$		2.5		
		$V_{GS} = 6\text{ V}, I_{SD} = 13\text{ A}$ (Note 3)		0.5		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. No prior drain bias or switching stress is applied during the measurement of $V_{GS(TH)}$ and $R_{DS(ON)}$.

3. Defined by design, not subject to production test.



TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

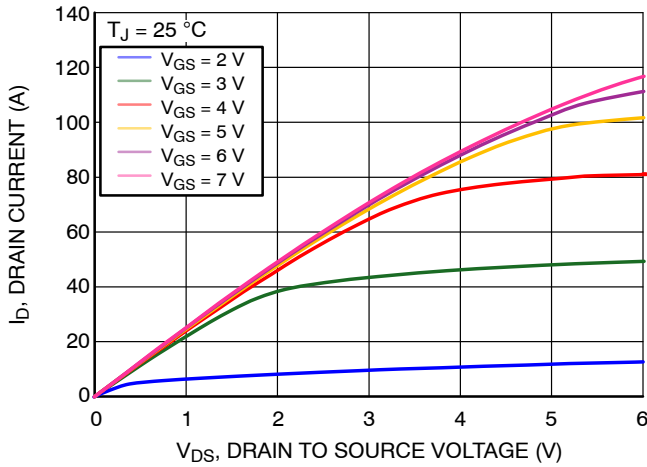


Figure 1. Output Characteristics at $T_J = 25^\circ\text{C}$

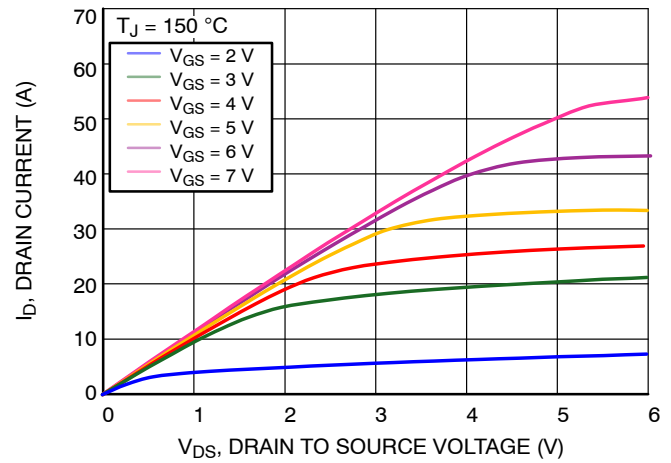


Figure 2. Output Characteristics at $T_J = 125^\circ\text{C}$

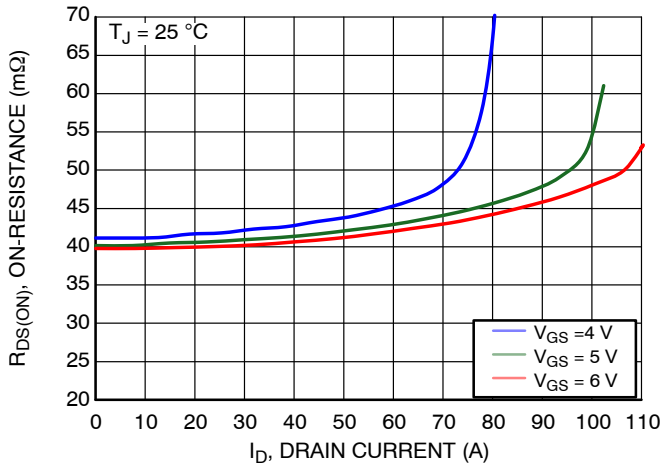


Figure 3. On-Resistance vs. Drain Current at $T_J = 25^\circ\text{C}$

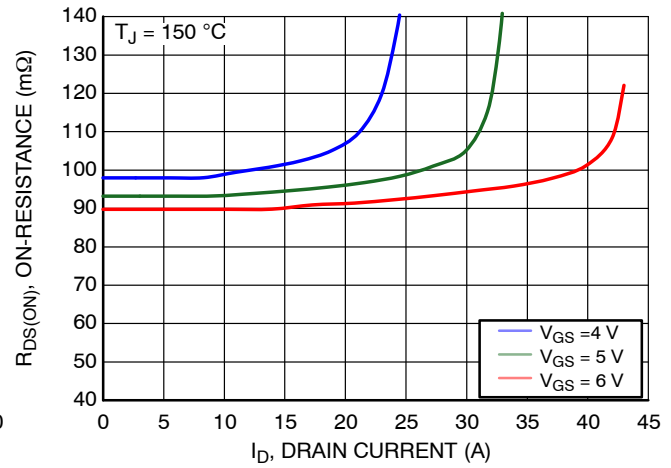


Figure 4. On-Resistance vs. Drain Current at $T_J = 125^\circ\text{C}$

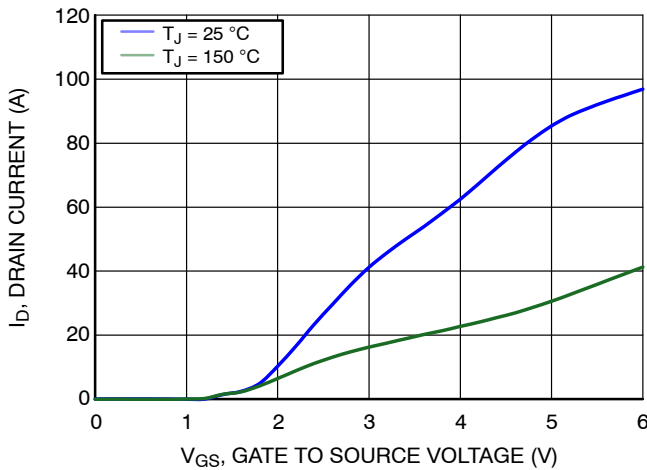


Figure 5. Transfer Characteristics at $V_{DS} = 3\text{V}$

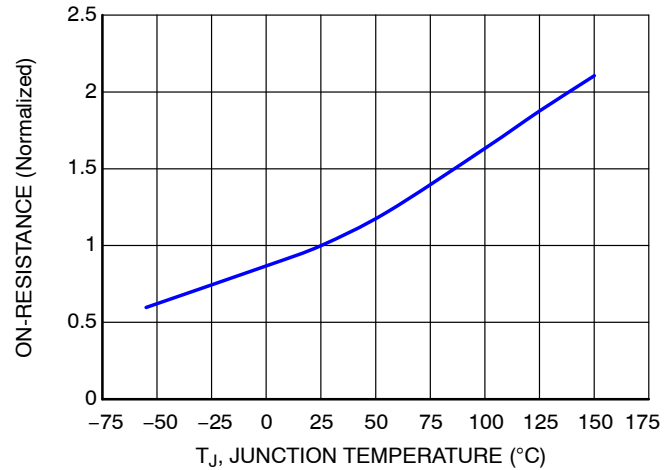


Figure 6. Normalized On-Resistance vs. Temperature at $V_{GS} = 6\text{V}$

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

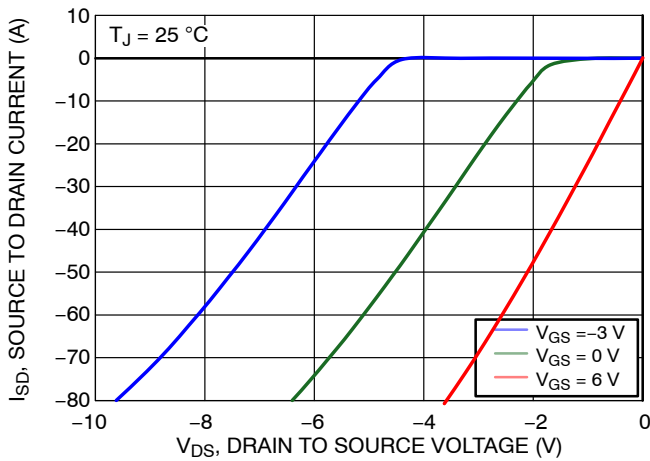


Figure 7. Reverse Conduction Characteristics at $T_J = 25^\circ\text{C}$

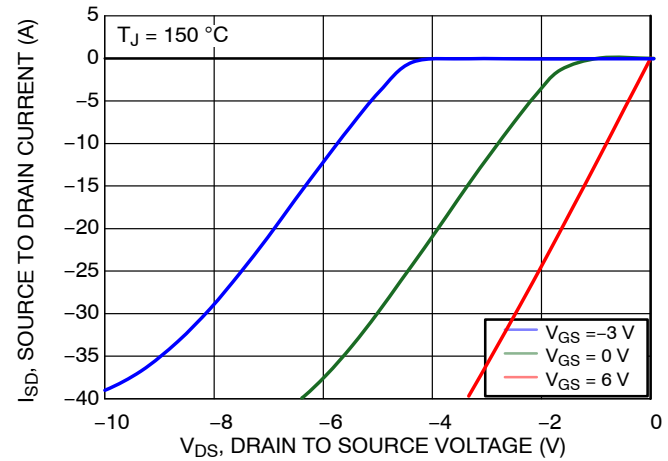


Figure 8. Reverse Conduction Characteristics at $T_J = 125^\circ\text{C}$

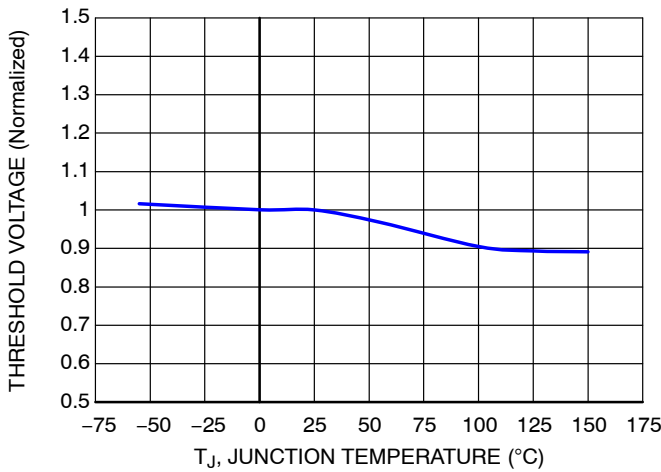


Figure 9. Normalized Threshold Voltage vs. Temperature

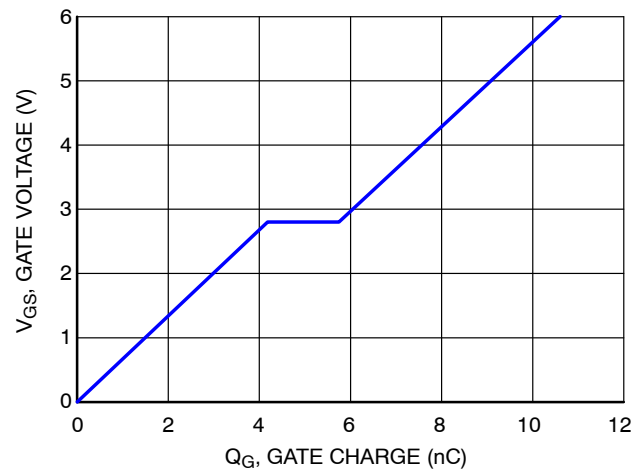


Figure 10. Gate Charge Characteristics at $I_{DS} = 13\text{ A}$

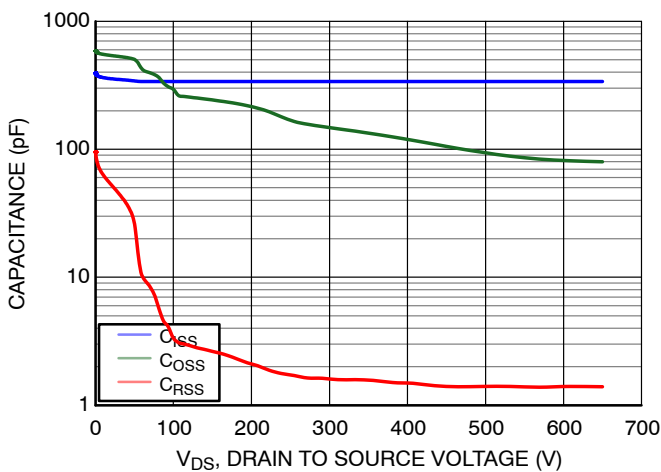


Figure 11. Capacitance Characteristics

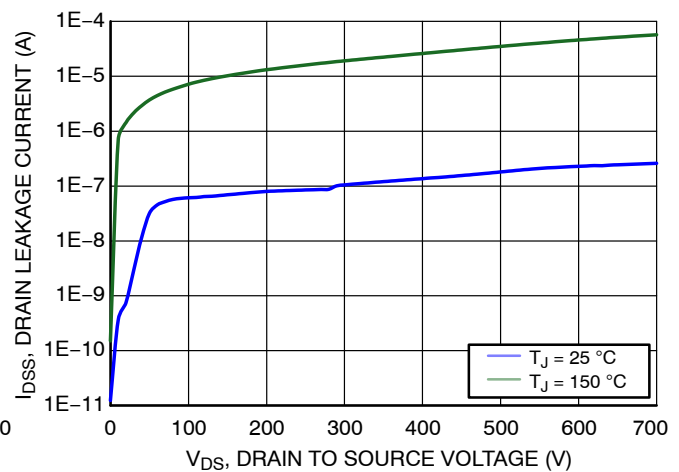


Figure 12. Drain Leakage Characteristics

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

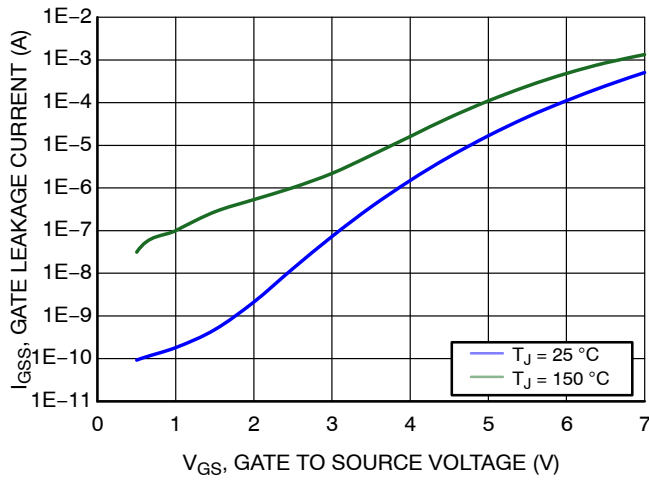


Figure 13. Gate Leakage Characteristics

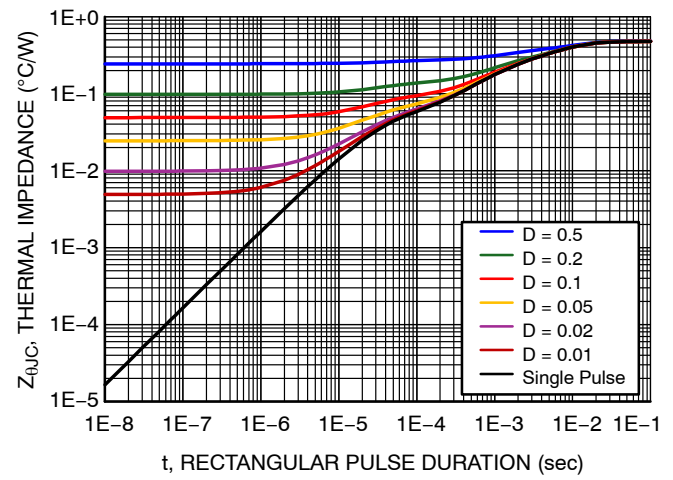


Figure 14. Transient Thermal Impedance

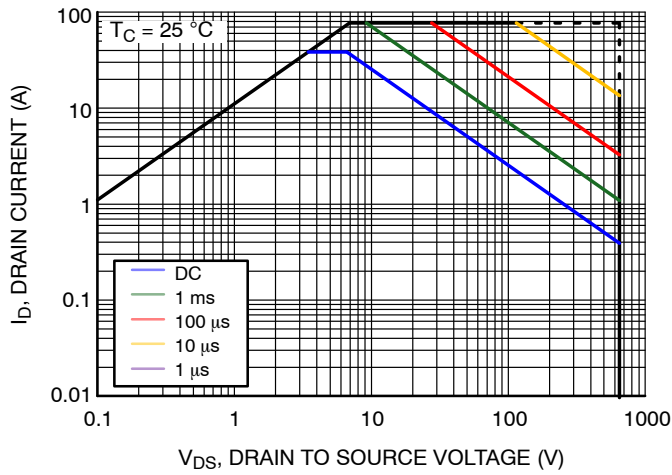


Figure 15. Safe Operating Area at $T_C = 25^\circ\text{C}$

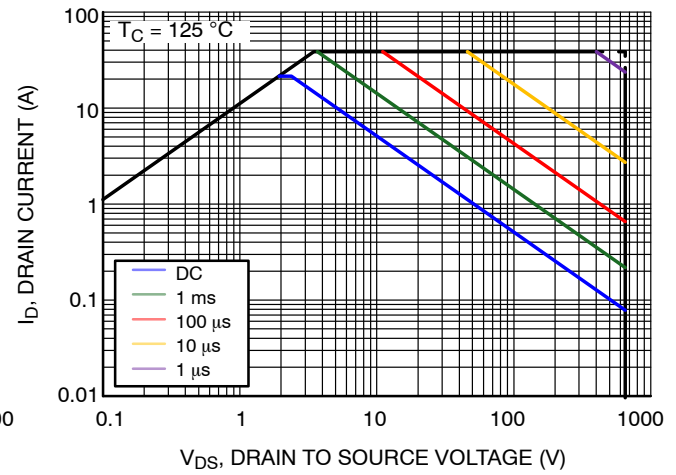


Figure 16. Safe Operating Area at $T_C = 125^\circ\text{C}$

Gate Drive Guidelines

This GaN device utilizes a Schottky gate structure, which behaves similarly to a MOSFET with a purely capacitive input and does not require continuous gate current during the on-state. For optimal performance, apply a low-impedance gate driver with appropriate gate resistance to control switching speed and limit ringing. A typical gate voltage of

6 V is recommended, with optional negative gate bias for hard-switching applications to improve dv/dt immunity and prevent false turn-on. Minimize gate loop inductance (<1 nH) through careful PCB layout and short connections. For additional robustness, Zener clamps may be used to limit gate voltage in both polarities.

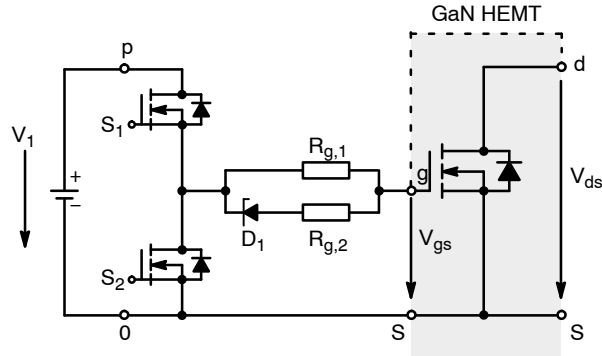


Figure 17. Schottky Gate Conventional Driver Schematic

ORDERING INFORMATION

Device Order Number	Package Type	Shipping [†]
NTBL050N65GN1TXG	PDSO-F9 10.38 x 9.90 x 2.30, 1.20P	1200 / Tape & Reel

[†] For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

NTBL050N65GN1

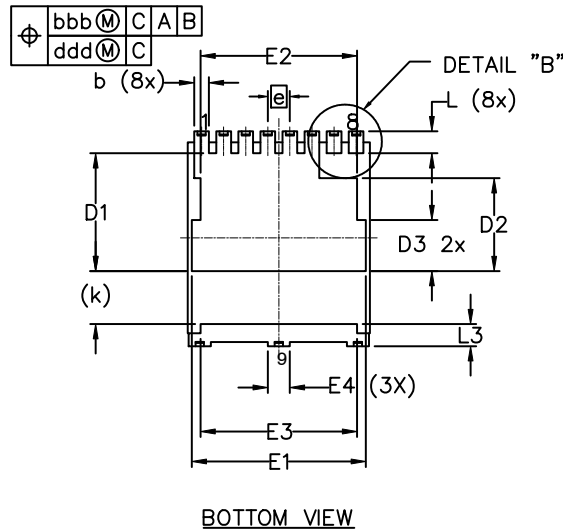
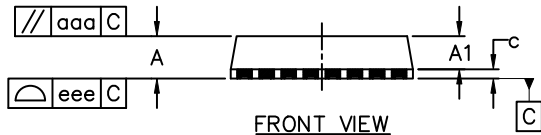
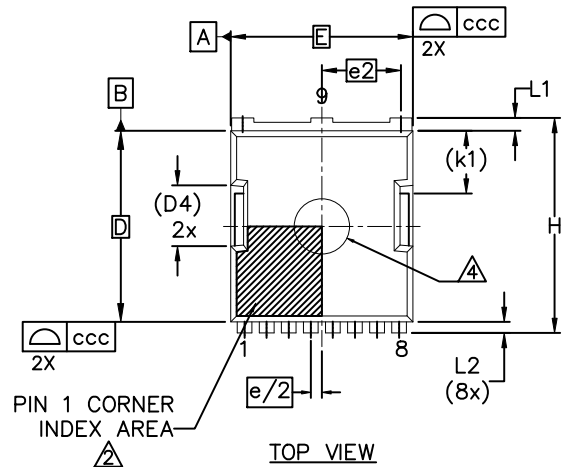
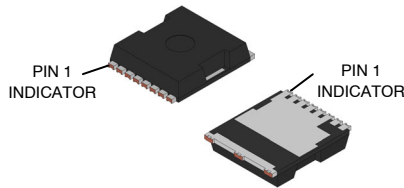
REVISION HISTORY

Revision	Description of Changes	Date
0	Initial document release.	7/29/2026

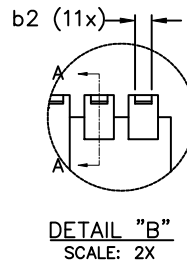
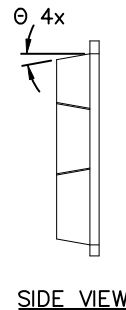


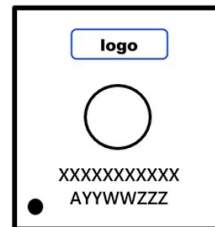
PDSO-F9 10.38x9.90x2.30, 1.20P
CASE 207AA
ISSUE 0

DATE 25 FEB 2026


NOTES:

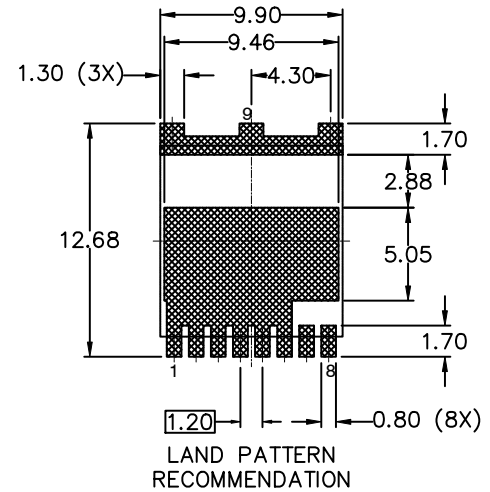
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE HATCHED AREA.
3. DIMENSIONS DO NOT INCLUDE MOLD FLASH AND BURR.
4. THE LOCATION AND SIZE OF EJECTOR MARKS ARE OPTIONAL.


SECTION "A-A"
SCALE: 4X

GENERIC MARKING DIAGRAM*


XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.15	2.30	2.45
A1	1.65	1.80	1.95
b	0.70	0.80	0.90
b2	0.31	0.43	0.55
c	0.40	0.50	0.60
c2	0.10	—	—
D	10.38 BSC		
D1	6.20	6.40	6.60
D2	4.85	5.05	5.25
D3	2.57	2.77	3.97
D4	3.30 REF		
E	9.90 BSC		
E1	9.26	9.46	9.66
E2	8.30	8.50	8.70
E3	8.30	8.50	8.70
E4	1.10	1.20	1.30
e	1.20 BSC		
e/2	0.60 BSC		
e2	4.30 BSC		
H	11.48	11.68	11.88
L	1.00	1.20	1.40
L1	0.50	0.70	0.90
L2	0.50	0.60	0.70
L3	1.00	1.20	1.40
L4	0.23 REF		
k	2.88 REF		
k1	3.41 REF		
θ	10° REF		
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.20		

DOCUMENT NUMBER: 98AON70698H

Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.

DESCRIPTION: PDSO-F9 10.38x9.90x2.30, 1.20P

PAGE 1 OF 1

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales