

ESD Protection Diode Array, Low Capacitance, Four Data Lines

NUP4304MR6T1G, SZNUP4304MR6T1G

NUP4304MR6T1G is a micro-integrated device designed to provide protection for sensitive components from possible harmful electrical transients; for example, ESD (electrostatic discharge).

Features

- Low Capacitance (1.5 pF Maximum Between I/O Lines)
- Single Package Integration Design
- Provides ESD Protection for JEDEC Standards JESD22
Machine Model = Class C
Human Body Model = Class 3B
- Protection for IEC61000-4-2 (Level 4)
8.0 kV (Contact)
15 kV (Air)
- Ensures Data Line Speed and Integrity
- Fewer Components and Less Board Space
- Direct the Transient to Either Positive Side or to the Ground

Applications

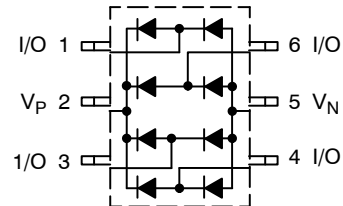
- USB 1.1 and 2.0 Data Line Protection
- T1/E1 Secondary IC Protection
- T3/E3 Secondary IC Protection
- HDLSL, IDSL Secondary IC Protection
- Video Line Protection
- Microcontroller Input Protection
- Base Stations
- I²C Bus Protection
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These are Pb-Free Devices*

* For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, [SOLDERRM/D](#).

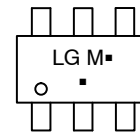


TSOP-6
CASE 318F

PIN CONFIGURATION AND SCHEMATIC



MARKING DIAGRAM



LG = Specific Device Code
M = Date Code
■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NUP4304MR6T1G	TSOP-6 (Pb-Free)	3,000 / Tape & Reel

DISCONTINUED (Note 1)

SZNUP4304MR6T1G	TSOP-6 (Pb-Free)	3,000 / Tape & Reel
-----------------	---------------------	------------------------

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

1. **DISCONTINUED:** This device is not available. Please contact your **onsemi** representative for information. The most current information on this device may be available on [www.onsemi.com](#).

NUP4304MR6T1G, SZNUP4304MR6T1G

MAXIMUM RATINGS (Each Diode) ($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	70	Vdc
Forward Current	I_F	200	mAdc
Peak Forward Surge Current	$I_{FM(surge)}$	500	mAdc
Repetitive Peak Reverse Voltage	V_{RRM}	70	V
Average Rectified Forward Current (Note 1) (averaged over any 20 ms period)	$I_{F(AV)}$	715	mA
Repetitive Peak Forward Current	I_{FRM}	450	mA
Non-Repetitive Peak Forward Current t = 1.0 μ s t = 1.0 ms t = 1.0 S	I_{FSM}	2.0 1.0 0.5	A

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. FR-5 = $1.0 \times 0.75 \times 0.062$ in.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	556	$^{\circ}\text{C/W}$
Lead Solder Temperature Maximum 10 Seconds Duration	T_L	260	$^{\circ}\text{C}$
Junction Temperature	T_J	-40 to +150	$^{\circ}\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted) (Each Diode)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Reverse Breakdown Voltage ($I_{(BR)} = 100\text{ }\mu\text{A}$)	$V_{(BR)}$	70	–	–	Vdc
Reverse Voltage Leakage Current ($V_R = 70\text{ Vdc}$) ($V_R = 25\text{ Vdc}$, $T_J = 150\text{ }^{\circ}\text{C}$) ($V_R = 70\text{ Vdc}$, $T_J = 150\text{ }^{\circ}\text{C}$)	I_R	– – –	– – –	2.5 30 50	μAdc
Capacitance (between I/O pins) ($V_R = 0\text{ V}$, $f = 1.0\text{ MHz}$)	C_D	–	0.8	1.5	pF
Capacitance (between I/O pin and ground) ($V_R = 0\text{ V}$, $f = 1.0\text{ MHz}$)	C_D	–	1.6	3	pF
Forward Voltage ($I_F = 1.0\text{ mAdc}$) ($I_F = 10\text{ mAdc}$) ($I_F = 50\text{ mAdc}$) ($I_F = 150\text{ mAdc}$)	V_F	– – – –	– – – –	715 855 1000 1250	mVdc

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. FR-5 = $1.0 \times 0.75 \times 0.062$ in.
2. Alumina = $0.4 \times 0.3 \times 0.024$ in. 99.5% alumina.
3. Include SZ-prefix devices where applicable.



CURVES APPLICABLE TO EACH CATHODE

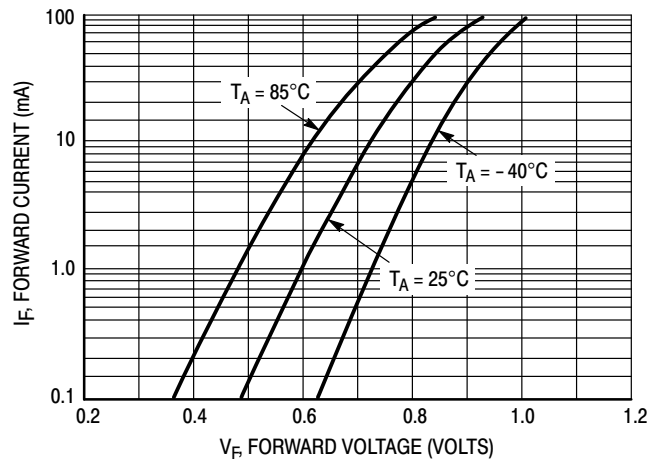


Figure 1. Forward Voltage

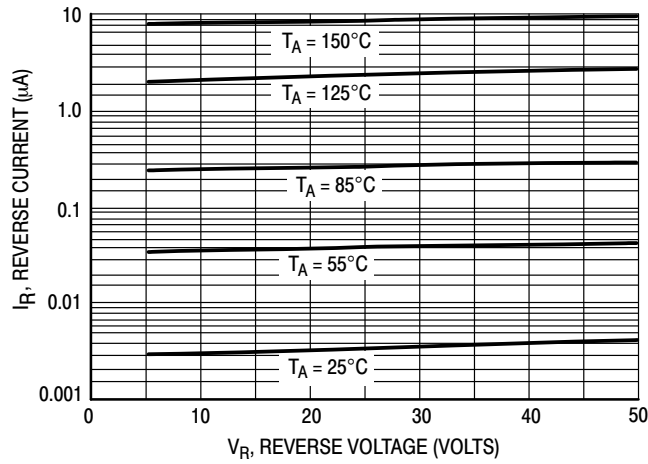


Figure 2. Leakage Current

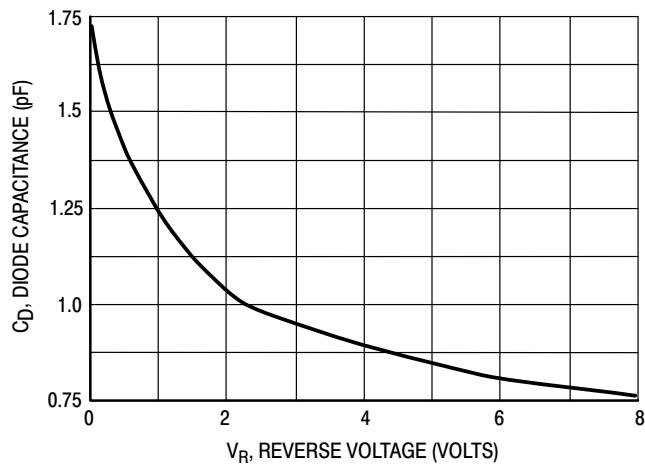


Figure 3. Capacitance

APPLICATIONS INFORMATION

The NUP4304MR6 is a low capacitance diode array designed to protect sensitive electronics such as communications systems, computers, and computer peripherals against damage due to ESD events or transient overvoltage conditions. Because of its low capacitance, it can be used on high speed I/O data lines. The integrated design of the NUP4304MR6 offers surge rated, low capacitance steering diodes integrated in a single package (TSOP-6). If a transient condition occurs, the steering diodes will drive the transient to the positive rail of the power supply or to ground.

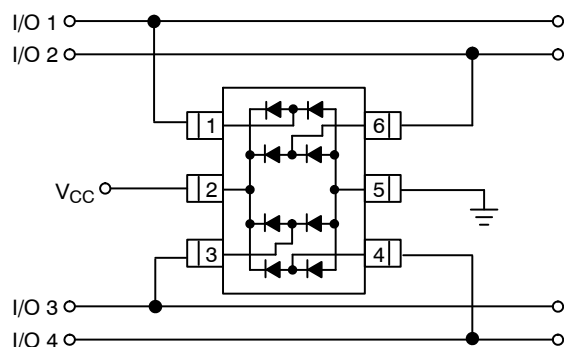
NUP4304MR6 CONFIGURATION OPTIONS

The NUP4304MR6 is able to protect up to four data lines against transient overvoltage conditions by driving them to a fixed reference point for clamping purposes. The steering diodes will be forward biased whenever the voltage on the protected line exceeds the reference voltage (V_f or $V_{CC} + V_f$). The diodes will force the transient current to bypass the sensitive circuit.

Data lines are connected at pins 1, 3, 4 and 6. The negative reference is connected at pin 5. This pin must be connected directly to ground by using a ground plane to minimize the PCB's ground inductance. It is very important to reduce the PCB trace lengths as much as possible to minimize parasitic inductance.

OPTION 1

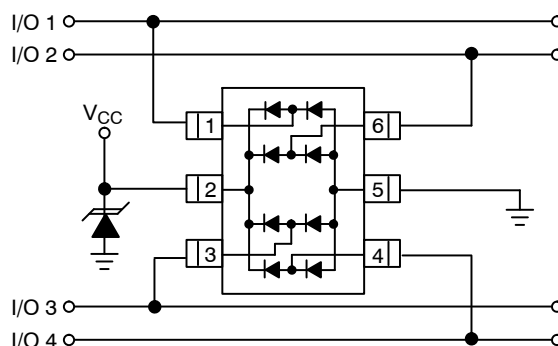
Protection of four data lines using V_{CC} as reference.



For this configuration, connect pin 2 directly to the positive supply rail (V_{CC}), the data lines are referenced to the supply voltage. Biasing of the steering diodes reduces their capacitance.

OPTION 2

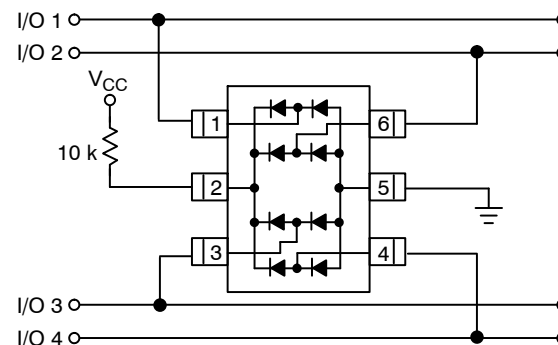
Protection of four data lines and the supply rail using V_{CC} as a reference and an external surge protection diode.



If additional protection of the supply rail is desired, an external surge protection diode may be added across V_{CC} and ground. This will prevent overvoltage conditions on the supply rail protecting the supply and other circuits connected to it.

OPTION 3

Protection of four data lines with bias and power supply isolation resistor.

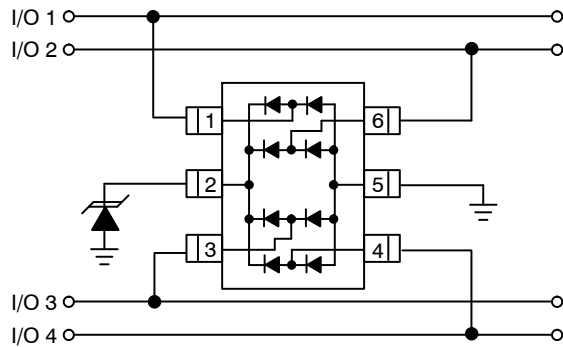


The NUP4304MR6 can be isolated from the power supply by connecting a series resistor between pin 2 and V_{CC} . A 10 kΩ resistor is recommended for this application. This will maintain bias on the internal steering diodes, reducing their capacitance.

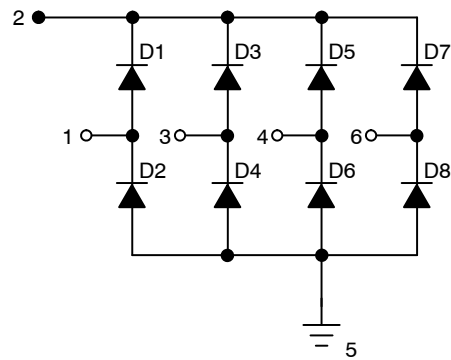
NUP4304MR6T1G, SZNUP4304MR6T1G

OPTION 4

Protection of four data lines without biasing of the internal steering diodes.



In applications lacking a positive supply reference an external surge protection diode may be used as a reference. For these applications, the surge protection is connected between pin 2 and the ground plane. The steering diodes will conduct whenever the voltage on the protected line exceeds their forward voltage plus the working voltage of the surge protection diode ($V_c = V_f + V_{RWM}$). In this case, the effective capacitance of the steering diodes will be higher than if a bias was applied.



NUP4304MR6 Equivalent Circuit

NUP4304MR6T1G, SZNUP4304MR6T1G

REVISION HISTORY

Revision	Description of Changes	Date
7	Rebranded the Data Sheet to onsemi format. SZNUP4304MR6T1G OPN Marked as Discontinued.	2/24/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

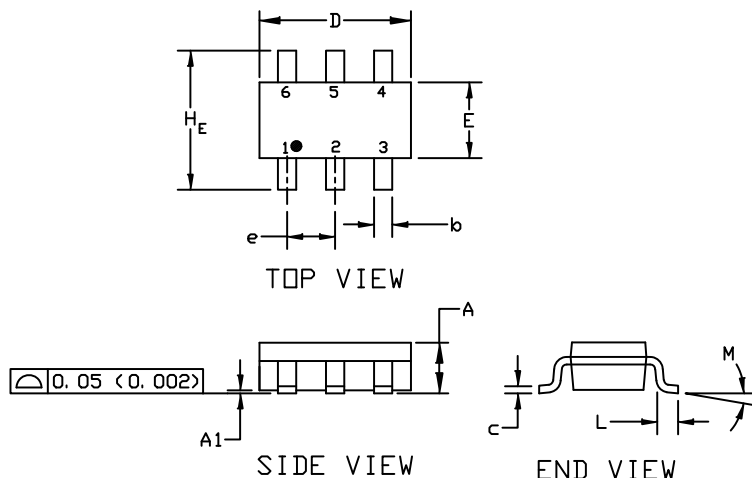
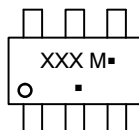




SCALE 2:1

SC-74
CASE 318F
ISSUE P

DATE 07 OCT 2021


GENERIC
MARKING DIAGRAM*


XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

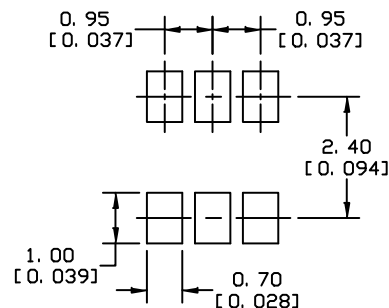
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994
2. CONTROLLING DIMENSION: INCHES
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.

DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.37	0.50	0.010	0.015	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
H _E	2.50	2.75	3.00	0.099	0.108	0.118
L	0.20	0.40	0.60	0.008	0.016	0.024
M	0*	---	10*	0*	---	10*



* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SOLDERING FOOTPRINT

STYLE 1: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. CATHODE 5. ANODE 6. CATHODE	STYLE 2: PIN 1. NO CONNECTION 2. COLLECTOR 3. EMITTER 4. NO CONNECTION 5. COLLECTOR 6. BASE	STYLE 3: PIN 1. EMITTER 1 2. BASE 1 3. COLLECTOR 2 4. EMITTER 2 5. BASE 2 6. COLLECTOR 1	STYLE 4: PIN 1. COLLECTOR 2 2. EMITTER 1/EMITTER 2 3. COLLECTOR 1 4. EMITTER 3 5. BASE 1/BASE 2/COLLECTOR 3 6. BASE 3	STYLE 5: PIN 1. CHANNEL 1 2. ANODE 3. CHANNEL 2 4. CHANNEL 3 5. CATHODE 6. CHANNEL 4	STYLE 6: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE
STYLE 7: PIN 1. SOURCE 1 2. GATE 1 3. DRAIN 2 4. SOURCE 2 5. GATE 2 6. DRAIN 1	STYLE 8: PIN 1. EMITTER 1 2. BASE 2 3. COLLECTOR 2 4. EMITTER 2 5. BASE 1 6. COLLECTOR 1	STYLE 9: PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2	STYLE 10: PIN 1. ANODE/CATHODE 2. BASE 3. EMITTER 4. COLLECTOR 5. ANODE 6. CATHODE	STYLE 11: PIN 1. EMITTER 2. BASE 3. ANODE/CATHODE 4. ANODE 5. CATHODE 6. COLLECTOR	

DOCUMENT NUMBER:	98ASB42973B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SC-74	PAGE 1 OF 1

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marketing.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales