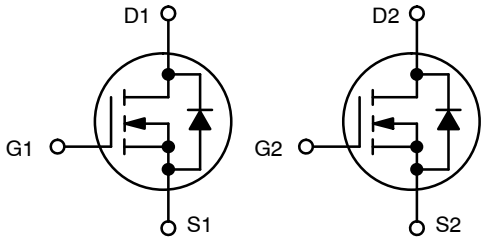
MOSFET – Power, Dual N-Channel, STD Gate

80 V, 21 mΩ, 29 A

NVMJD020N08H

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
80 V	21 mΩ @ V_{GS} = 10 V	29 A



DUAL N-CHANNEL

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- LFPAK8 Package, Industry Standard
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25 °C unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	80	V
Gate-to-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25 °C	I_D	29	A
	T_C = 100 °C		21	
Power Dissipation	T_C = 25 °C	P_D	42	W
Pulsed Drain Current	T_C = 25 °C, t_p = 10 μs	I_{DM}	157	A
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to +175	°C
Continuous Source-Drain Current (Body Diode)	T_C = 25 °C, V_{GS} = 0 V	I_S	29	A
Single Pulse Avalanche Energy (I_{PK} = 27 A)		E_{AS}	36	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)		T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

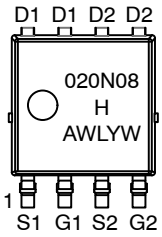
THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	3.6	°C/W
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	48	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

LFPAK8
CASE 760AF

MARKING DIAGRAM



020N08H	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
W	= Work Week

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA	80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	I_D = 1 mA, Referenced to 25 °C		53		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, T_J = 25 °C			10	μA
		V_{DS} = 80 V, T_J = 125 °C			100	
Gate-to-Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
ON CHARACTERISTICS						
Drain-to-Source On Resistance	$R_{DS(ON)}$	V_{GS} = 10 V, I_D = 15 A		18	21	mΩ
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 30 μA	2.0		4.0	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)}/\Delta T_J$	V_{GS} = V_{DS}, I_D = 30 μA		−6		mV/°C
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 15 A		26		S
CHARGES, CAPACITANCES & GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 40 V		540		pF
Output Capacitance	C_{OSS}			125		
Reverse Transfer Capacitance	C_{RSS}			5		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DD} = 64 V, I_D = 15 A		10		nC
Threshold Gate Charge	$Q_{G(TH)}$			1.6		
Gate-to-Source Charge	Q_{GS}			2.8		
Gate-to-Drain Charge	Q_{GD}			3.0		
Gate Plateau Voltage	V_{GP}			5.0		V
Gate Resistance	R_G	f = 1 MHz		1.1		Ω
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{d(ON)}$	Resistive Load, V_{GS} = 0/10 V, V_{DD} = 64 V, I_D = 15 A, R_G = 2.5 Ω		8		ns
Rise Time	t_r			8		
Turn-Off Delay Time	$t_{d(OFF)}$			15		
Fall Time	t_f			3		
DRAIN-SOURCE DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 15 A, T_J = 25 °C		0.83	1.2	V
		V_{GS} = 0 V, I_S = 15 A, T_J = 125 °C		0.70		
Forward Diode Voltage Temperature Coefficient	V_{SDTCR}	V_{GS} = 0 V, I_S = 15 A		−1.3		mV/°C
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, I_S = 15 A, dI/dt = 100 A/μs, V_{DD} = 64 V		27		ns
Charge Time	t_a			16		
Discharge Time	t_b			11		
Reverse Recovery Charge	Q_{RR}			20		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

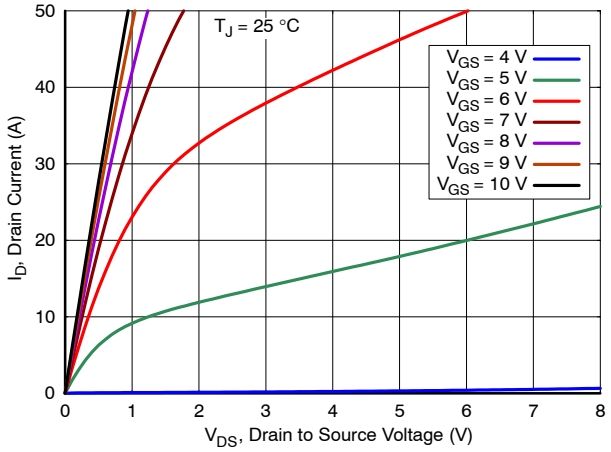


Figure 1. On-Region Characteristics

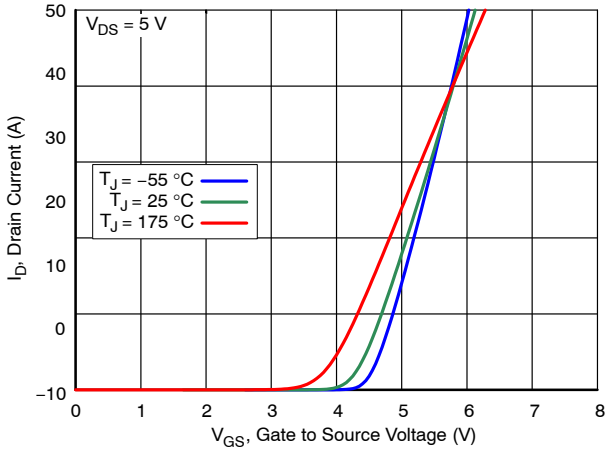


Figure 2. Transfer Characteristics

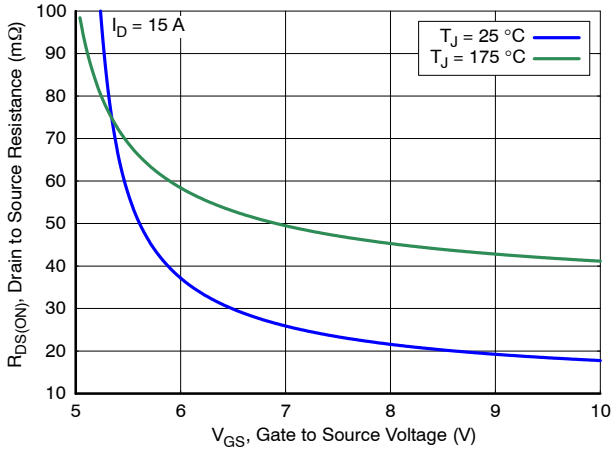


Figure 3. On-Resistance vs. Gate Voltage

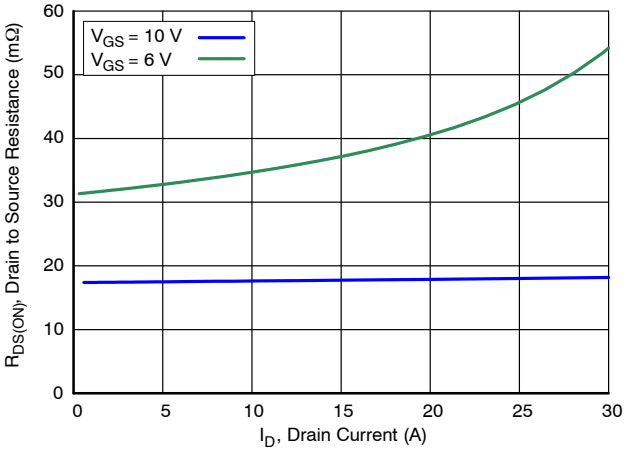


Figure 4. On-Resistance vs. Drain Current

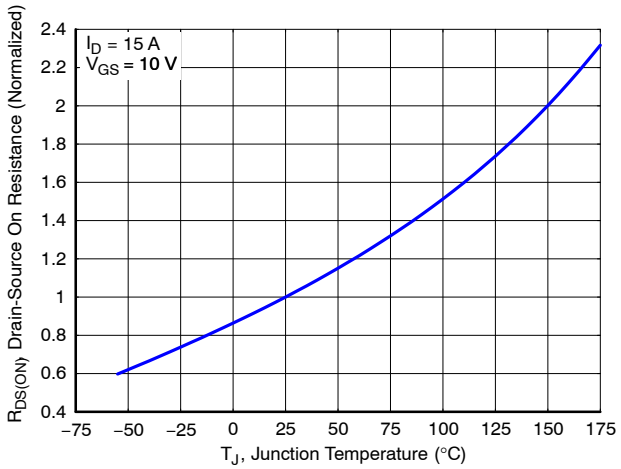


Figure 5. Normalized ON Resistance vs. Junction Temperature

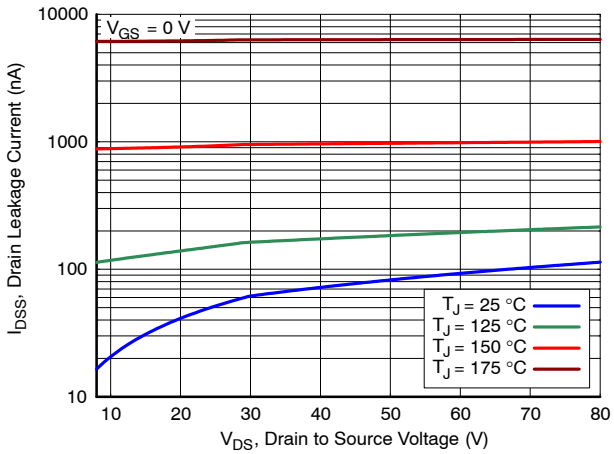


Figure 6. Drain Leakage Current vs. Drain Voltage

TYPICAL CHARACTERISTICS

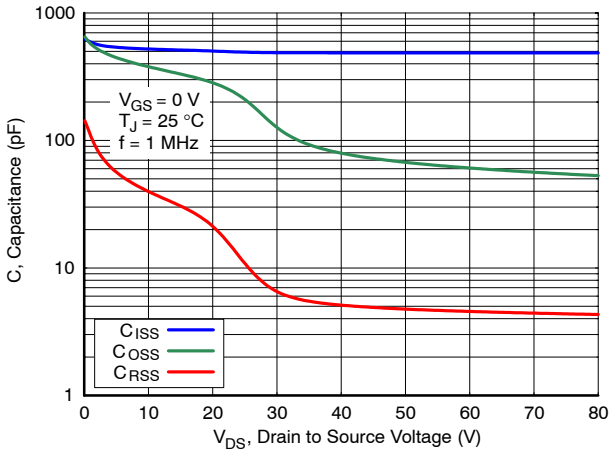


Figure 7. Capacitance Characteristics

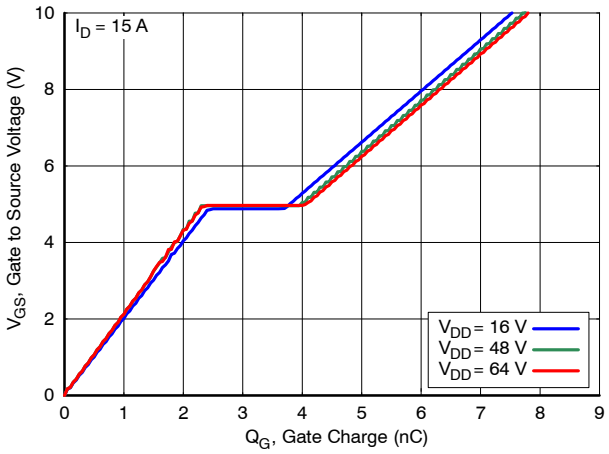


Figure 8. Gate Charge Characteristics

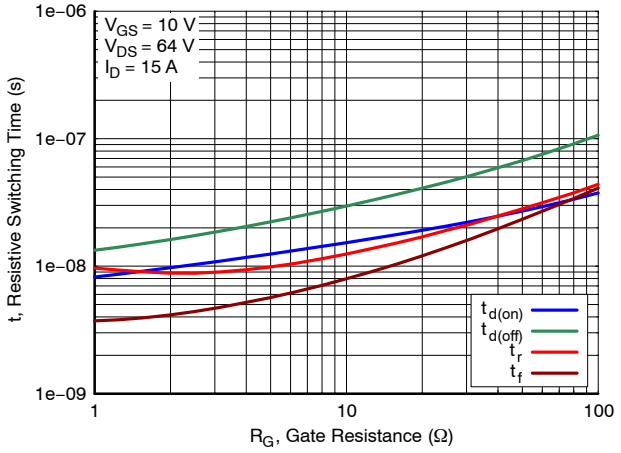


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

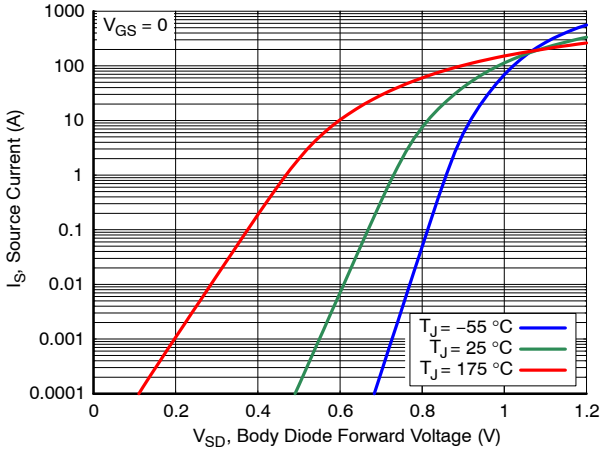


Figure 10. Diode Forward Characteristics

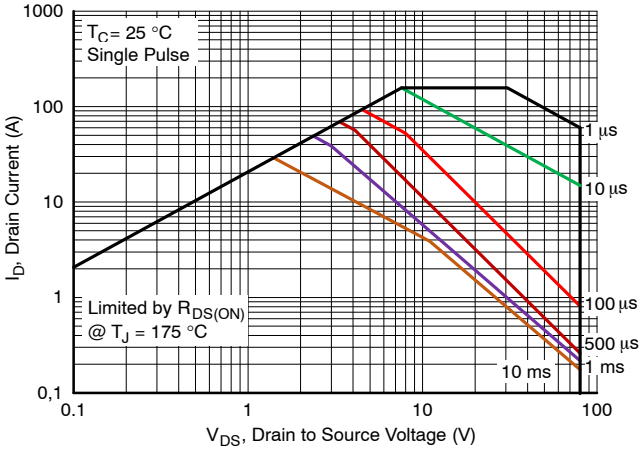


Figure 11. Safe Operating Area (SOA)

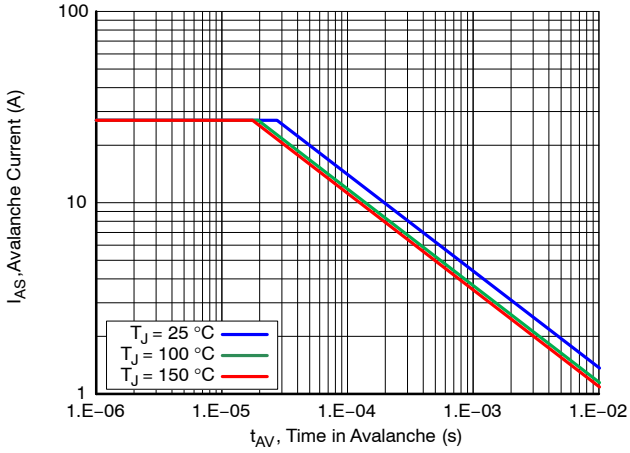


Figure 12. Avalanche Current vs. Pulse Time (UIS)

TYPICAL CHARACTERISTICS

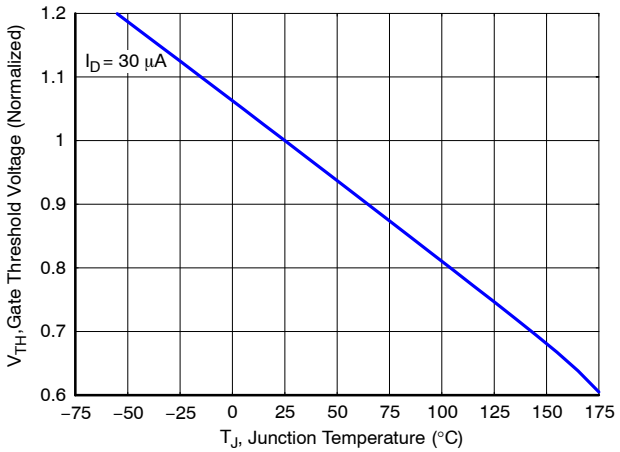


Figure 13. Gate Threshold Voltage vs. Junction Temperature

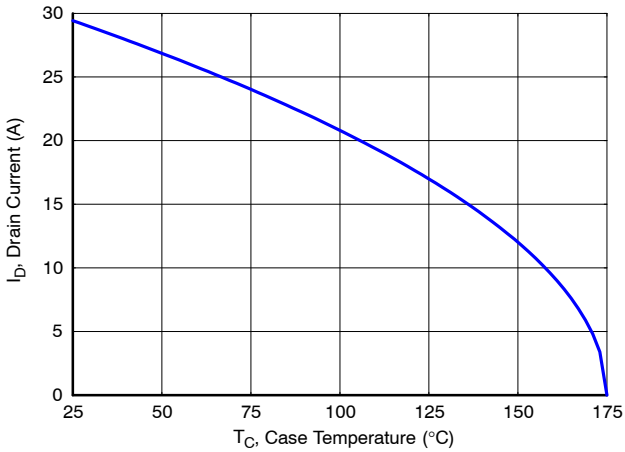


Figure 14. Maximum Current vs. Case Temperature

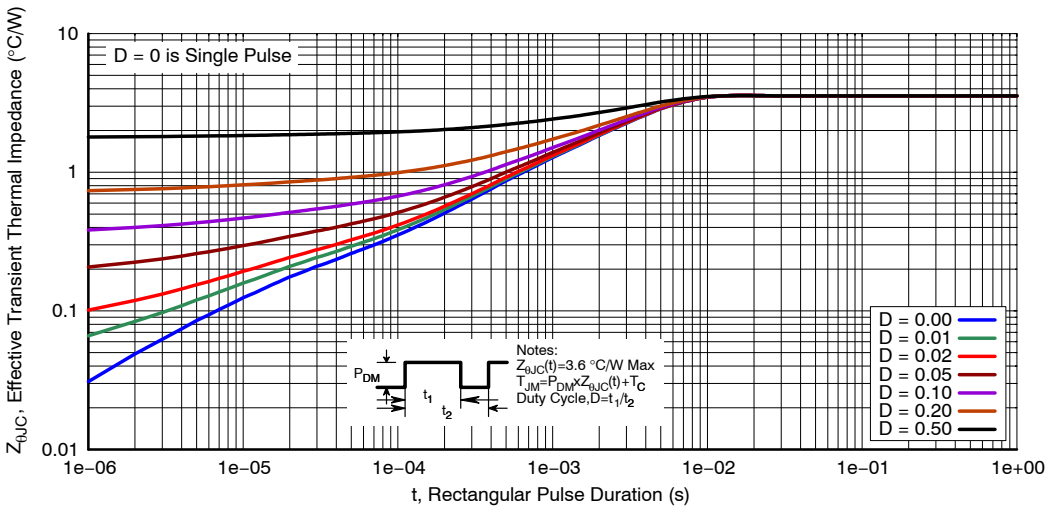


Figure 15. Transient Thermal Response

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NVMJD020N08HTWG	020N08H	LFPAK8 Dual (Pb-Free)	3000 / Tape & Reel

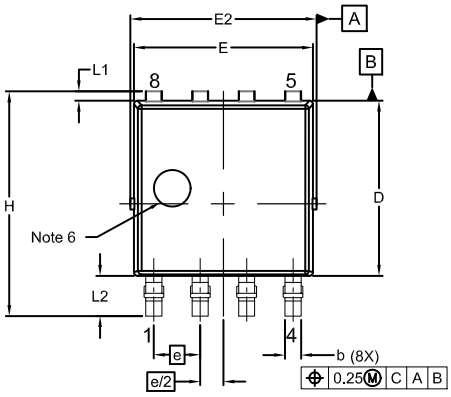
† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

REVISION HISTORY

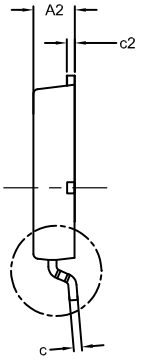
Revision	Description of Changes	Date
0	Initial document release.	7/29/2026

LFPAK8 5.15x6.15
CASE 760AF
ISSUE O

DATE 30 OCT 2019

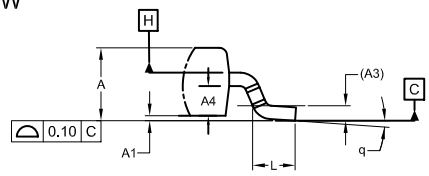


TOP VIEW

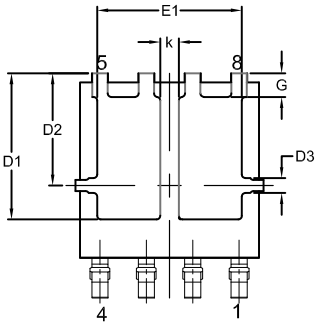


SIDE VIEW

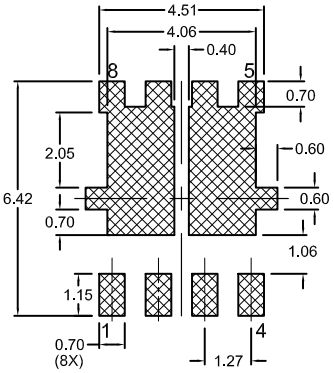
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
4. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
6. OPTIONAL MOLD FEATURE.



DETAIL 'A'



BOTTOM VIEW

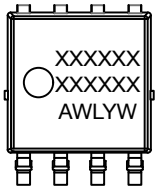


RECOMMENDED LAND PAD

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.10	1.20	1.30
A1	0.00	0.08	0.15
A2	1.10	1.15	1.20
A3		0.25 REF	
A4	0.45	0.50	0.55
b	0.40	0.45	0.50
c	0.19	0.22	0.25
c2	0.19	0.22	0.25
D	4.70	4.80	4.90
D1	3.80	4.00	4.20
D2	3.00	3.10	3.20
D3	0.30	0.40	0.50
E	4.80	4.90	5.00
E1	3.90	4.00	4.10
E2	5.00	5.15	5.30
e		1.270 BSC	
e/2		0.635 BSC	
G	0.55	0.65	0.75
H	6.00	6.15	6.30
k	0.40	0.50	0.60
L	0.45	0.65	0.85
L1	0.15	0.25	0.35
L2	0.90	1.10	1.30
q	0°	4°	8°

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON13533H**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**LFPAK8 5.15x6.15**		**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
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