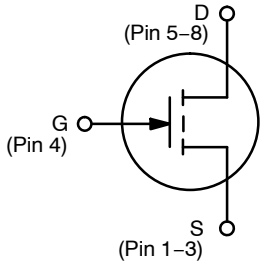
Enhancement Mode Gallium Nitride (GaN) HEMT

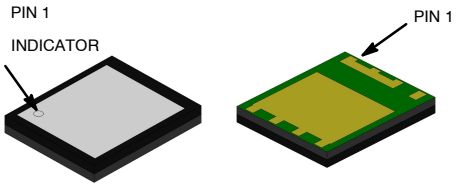
100 V, 0.8 mΩ, TBD A, PDSO-N8 5.0x6.0

Preliminary Document

NTLEF1D0N10GN1

$V_{(BR)DSS}$	$R_{DS(ON)}$ TYP	I_{DS} MAX
100 V	0.8 mΩ	TBD A





PDSO-N8 5.00x6.00x0.87, 1.27P, GEN 2
CASE 144AB

Features

- Low $R_{DS(ON)}$ to Minimize Conduction Losses
- Ultra Low Gate Charge for High Speed Switching
- FOM-Q_G = 20.9 nC*mΩ
- Small Footprint for High Density PCB Design
- Pb-Free, Halide Free and RoHS Compliant

Typical Applications

- High Density Power Modules
- High Frequency DC-DC Converters
- High Power Synchronous Rectifiers
- Motor Drivers

MAXIMUM RATINGS (T_J = 25 °C unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	100	V
Drain-to-Source Transient Voltage, t_P < 100 μs	$V_{DS(TRAN)}$	120	V
Gate-to-Source Voltage	V_{GS}	−4 to 6	V
Gate-to-Source Transient Voltage, t_P = 100 ns, f_P = 100 kHz, open drain	$V_{GS(PULSE)}$	6.5	V
Continuous Drain Current, T_{CASE} = 25 °C T_{CASE} = 100 °C	I_{DS}	TBD TBD	A
Pulsed Drain Current, t_P < 100 μs, T_J = 25 °C T_J = 150 °C	$I_{DS(PULSE)}$	1400 1080	A
Power Dissipation, V_{GS} = 5 V, T_{CASE} = 25 °C	P_{TOT}	TBD	W
Operating Junction Temperature	T_J	−55 to 150	°C
Storage Temperature	T_{STG}	−55 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

MARKING DIAGRAM

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

This Preliminary document is for informational purposes only. **onsemi** may update or withdraw it without notice. Content and referenced products are under development and subject to change.

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THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Junction-to-Cases	$R_{\theta JC}$	TBD	°C/W
Junction-to-Board	$R_{\theta JB}$	TBD	°C/W
Junction-to-Ambient (Note 1)	$R_{\theta JA}$	TBD	°C/W
Maximum Soldering Temperature (MSL3)	T_{SLD}	260	°C

1. Device on 1 in^2, 2 oz copper pad on single layer FR-4 PCB.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V	100			V
Drain-to-Source Leakage Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 100 V		10	400	μA
		V_{GS} = 0 V, V_{DS} = 100 V, T_J = 125 °C		400		
Gate-to-Source Leakage Current	I_{GSS}	V_{GS} = 6 V, V_{DS} = 0 V		4	200	μA
		V_{GS} = 6 V, V_{DS} = 0 V, T_J = 125 °C		100		μA
ON CHARACTERISTICS						
Drain-to-Source On Resistance	$R_{DS(ON)}$	V_{GS} = 5 V, I_{DS} = 70 A		0.8	1.0	mΩ
		V_{GS} = 5 V, I_{DS} = 70 A, T_J = 125 °C		TBD		
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_{DS} = 27 mA, T_J = 25 °C		1.1		V
		V_{DS} = V_{GS}, I_{DS} = 27 mA, T_J = 125 °C		TBD		
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{ISS}	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz		5480		pF
Output Capacitance	C_{OSS}			1570		
Reverse Transfer Capacitance	C_{RSS}			31		
Output Capacitance, Energy Related	$C_{OSS(ER)}$	V_{DS} = 0 V to 50 V, V_{GS} = 0 V		TBD		pF
Output Capacitance, Time Related	$C_{OSS(TR)}$			3120		
Output Charge	Q_{OSS}			156		nC
Output Capacitance Stored Energy	E_{OSS}			TBD		μJ
Gate Resistance	R_G	f = 5 MHz		1.3		Ω
Gate Charge	Q_G	V_{DS} = 50 V, I_{DS} = 70 A, V_{GS} = 0/5 V		39		nC
Gate-to-Source Charge	Q_{GS}			10.2		
Gate-to-Drain Charge	Q_{GD}			4.8		
Gate Plateau Voltage	V_{PLAT}			TBD		V
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{D(ON)}$	V_{DS} = 50 V, I_{DS} = 70 A, V_{GS} = 0/5 V, R_G = 4 Ω		TBD		ns
Turn-Off Delay Time	$t_{D(OFF)}$			TBD		ns
Turn-On Rise Time	t_R			TBD		ns
Turn-Off Fall Time	t_F			TBD		ns

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ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
REVERSE CONDUCTION CHARACTERISTICS						
Source-to-Drain Reverse Voltage	V_{SD}	V_{GS} = −3 V, I_{SD} = 70 A		TBD		V
		V_{GS} = 0 V, I_{SD} = 70 A		TBD		
		V_{GS} = 5 V, I_{SD} = 70 A		TBD		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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GATE DRIVE GUIDELINES

This GaN device utilizes a Schottky gate structure, which behaves similarly to a MOSFET with a purely capacitive input and does not require continuous gate current during the on-state. For optimal performance, apply a low-impedance gate driver with appropriate gate resistance to control switching speed and limit ringing. A typical gate voltage of **5 – 6 V** is recommended, with optional negative gate bias for hard-switching applications to improve dv/dt immunity and prevent false turn-on. Minimize gate loop inductance (<1 nH) through careful PCB layout and short connections. For additional robustness, Zener clamps may be used to limit gate voltage in both polarities.

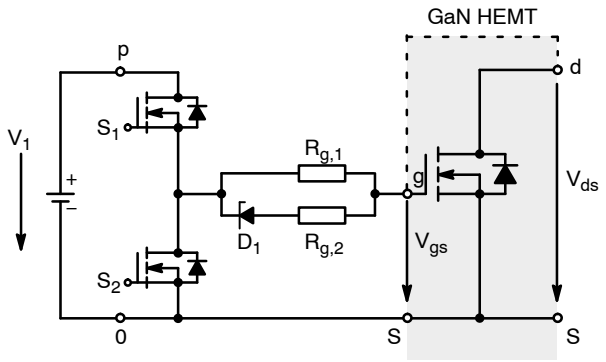

Figure 1. Schottky Gate Conventional Driver Schematic

ORDERING INFORMATION

Device Order Number	Package Type	Shipping†
ENGNTLEF1D0N10GN1TXG	PDSO-N8 5.00x6.00x0.87, 1.27P, GEN 2	2500 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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REVISION HISTORY

Revision	Description of Changes	Date
P0	Initial Preliminary document release.	4/6/2026
P1	Update – Package and Shipping information, Marking Diagram.	6/30/2026

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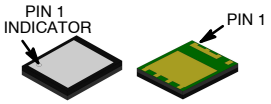

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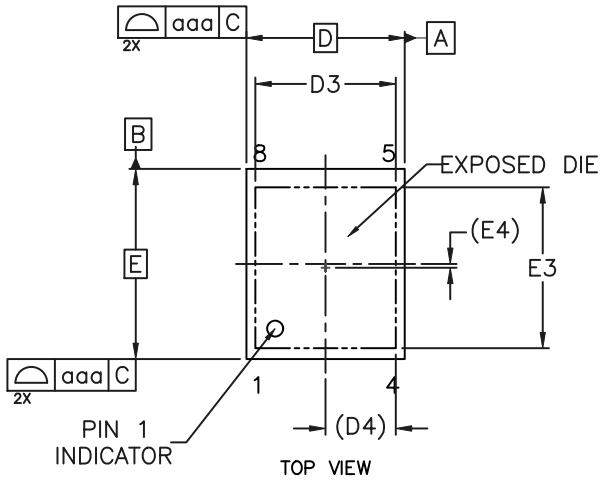
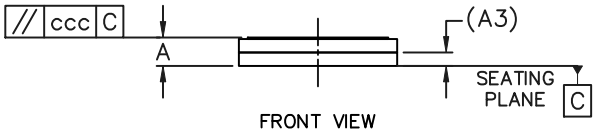
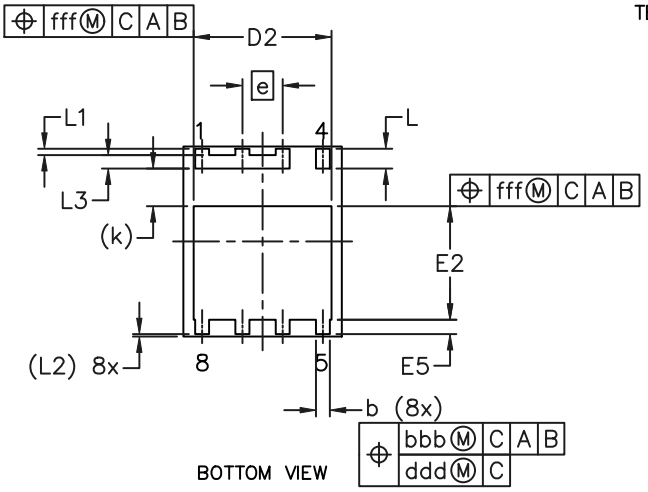
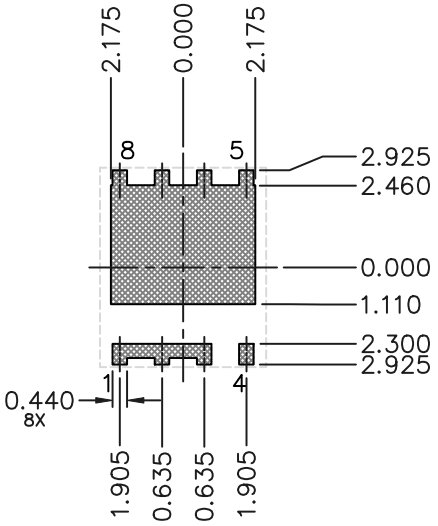
CASE 144AB
ISSUE O

19 MAR 2026









*FOR ADDITIONAL INFORMATION ON OUR PB–FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

UNIT IN MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.77	0.87	0.97
A3	0.425 REF		
b	0.390	0.440	0.490
D	5.00 BSC		
D2	4.300	4.350	4.400
D3	3.600	–	4.400
D4	2.190 REF		
e	1.270 BSC		
E	6.00 BSC		
E2	3.530	3.580	3.630
E3	4.600	–	5.400
E4	0.120 REF		
E5	0.405	0.455	0.505
k	1.190 REF		
L	0.575	0.625	0.675
L1	0.150	0.200	0.250
L2	0.075 REF		
L3	0.375	0.425	0.475
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
fff	0.10		

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
Y = Year
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ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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