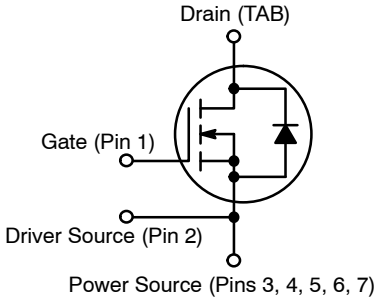
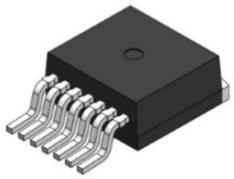
MOSFET - Power, Single N-Channel, D2PAK-7L
650 V, 190 mΩ, 20 A

NVBG190N65S3F

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
650 V	190 mΩ @ 10 V	20 A



N−CHANNEL MOSFET



D2PAK−7L
CASE 418BJ

Description

SUPERFET® III MOSFET is **onsemi**'s brand−new high voltage super−junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on−resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate.

Consequently, SUPERFET III MOSFET is very suitable for the various power system for miniaturization and higher efficiency. SUPERFET III FRFET® MOSFET's optimized reverse recovery performance of body diode can remove additional component and improve system reliability.

In addition, the D2PAK 7 lead package offers Kelvin sense. This allows higher switching speeds and gives designers the ability to reduce the overall application footprint.

Features

- 700 V @ T_J = 150°C
- Typ. $R_{DS(on)}$ = 158 mΩ
- Ultra Low Gate Charge (Typ. Q_g = 36 nC)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)}$ = 339 pF)
- 100% Avalanche Tested
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- Automotive On Board Charger
- Automotive DC/DC Converter for BEV

MARKING DIAGRAM

VBG190N65S3F = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

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Table 1. ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise stated)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain−to−Source Voltage		650	V
V_{GS}	Gate−to−Source Voltage	− DC	±30	V
		− AC (f > 1 Hz)	±30	
I_D	Drain Current	− Continuous (T_C = 25°C)	20	A
		− Continuous (T_C = 100°C)	12.7	
I_{DM}	Drain Current	− Pulsed (Note 1)	50	A
E_{AS}	Single Pulse Avalanche Energy (Note 2)		220	mJ
I_{AS}	Avalanche Current		2.8	A
E_{AR}	Repeated Avalanche Energy (Note 1)		1.62	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		50	
P_D	Power Dissipation	T_C = 25°C	162	W
		− Derate Above 25°C	1.3	W/°C
T_J, T_{stg}	Operating Junction and Storage Temperature Range		−55 to 150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8″ from Case for 5 Seconds		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse − width limited by maximum junction temperature.
2. IAS = 3.2 A, RG = 25 Ω, starting T_J = 25°C.
3. ISD ≤ 12 A, di/dt ≤ 200 A/μs, V_{DD} ≤ 400 V, starting T_C = 25°C.

Table 2. THERMAL RESISTANCE RATINGS

Symbol	Parameter	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction−to−Case, Max.	0.77	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient, Max.	40	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain−to−Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	650	–	–	V
		V_{GS} = 0 V, I_D = 10 mA, T_J = 150°C	700	–	–	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 20 mA, Referenced to 25°C	–	0.61	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650 V, V_{GS} = 0 V	–	–	10	μA
		V_{DS} = 520 V, T_C = 125°C	–	128	–	μA
I_{GSS}	Gate−to−Body Leakage Current	V_{DS} = 0 V, V_{GS} = ±30 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Drain−to−Source Breakdown Voltage	V_{GS} = V_{DS}, I_D = 0.43 mA	3.0	–	5.0	V
$R_{DS(on)}$	Static Drain−to−Source On Resistance	V_{GS} = 10 V, I_D = 10 A	–	158	190	mΩ
g_{FS}	Forward Transconductance	V_{GS} = 20 V, I_D = 10 A	–	11	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 400 V, V_{GS} = 0 V, f = 1 MHz	–	1710	–	pF
C_{oss}	Output Capacitance		–	34	–	pF
$C_{oss(eff.)}$	Effective Output Capacitance	V_{DS} = 0 to 400 V, V_{GS} = 0 V	–	339	–	pF
$C_{oss(er.)}$	Energy Related Output Capacitance	V_{DS} = 0 to 400 V, V_{GS} = 0 V	–	58	–	pF
$Q_{g(total)}$	Total Gate Charge at 10 V	V_{DS} = 400 V, I_D = 10 A, V_{GS} = 10 V (Note 4)	–	36	–	nC
Q_{gs}	Gate−to−Source Gate Charge		–	10.6	–	nC
Q_{gd}	Gate−to−Drain “Miller” Charge		–	14.5	–	nC
ESR	Equivalent Series Resistance	F = 1 MHz	–	1.7	–	Ω
SWITCHING CHARACTERISTICS, V_{GS} = 10 V						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 400 V, I_D = 10 A, V_{GS} = 10 V, R_G = 4.7 Ω (Note 4)	–	24	–	ns
t_r	Rise Time		–	15.7	–	ns
$t_{d(off)}$	Turn-Off Delay Time		–	50	–	ns
t_f	Fall Time		–	4.3	–	ns
SOURCE−DRAIN DIODE CHARACTERISTICS						
I_S	Maximum Continuous Source−to−Drain Diode Forward Current		–	–	20	A
I_{SM}	Maximum Pulsed Source−to−Drain Diode Forward Current		–	–	50	A
V_{SD}	Source−to−Drain Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 10 A	–	–	1.3	V
t_{rr}	Reverse−Recovery Time	V_{GS} = 0 V, I_{SD} = 10 A, dI_F/dt = 100 A/μs	–	73	–	ns
Q_{rr}	Reverse−Recovery Charge		–	224	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL CHARACTERISTICS

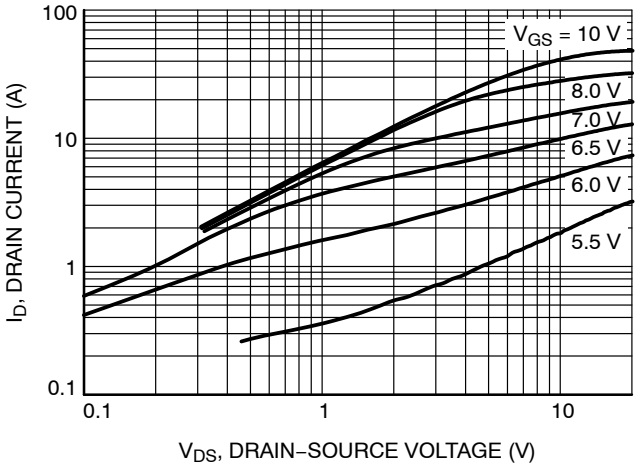

Figure 1. On−Region Characteristics

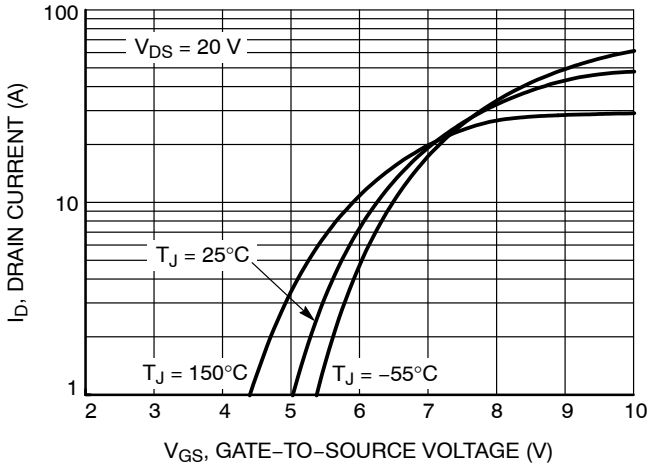

Figure 2. Transfer Characteristics

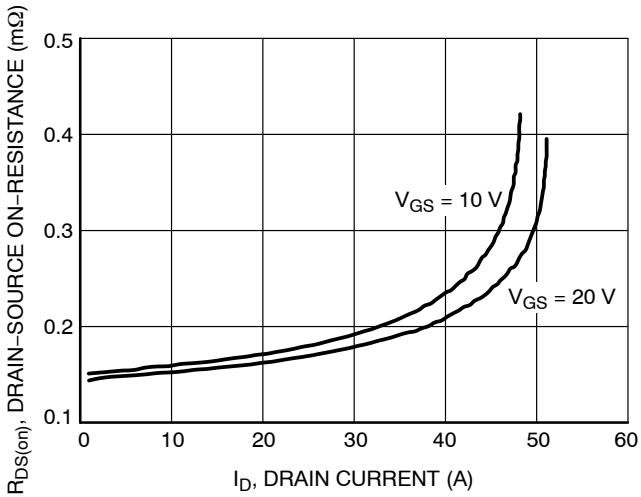

Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

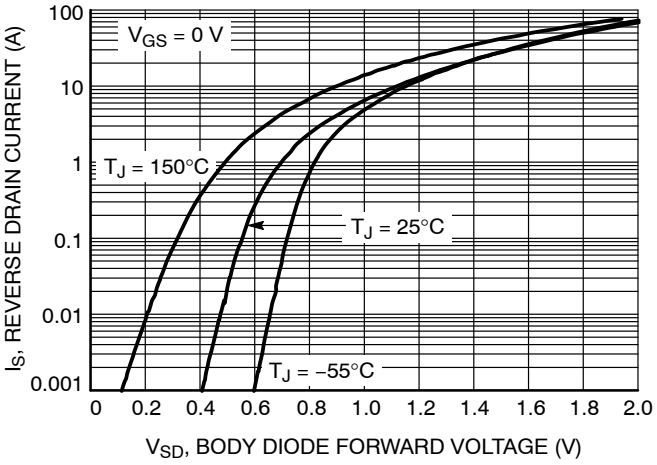

Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

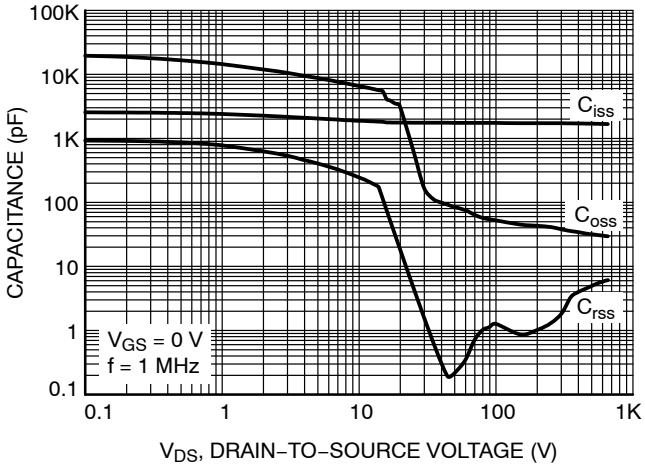

Figure 5. Capacitance Characteristics

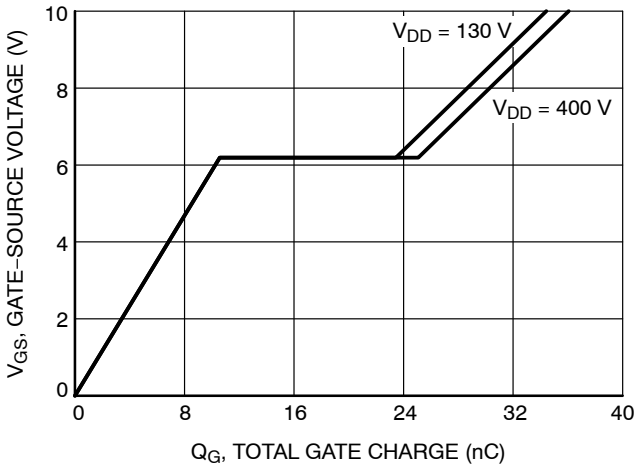

Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS

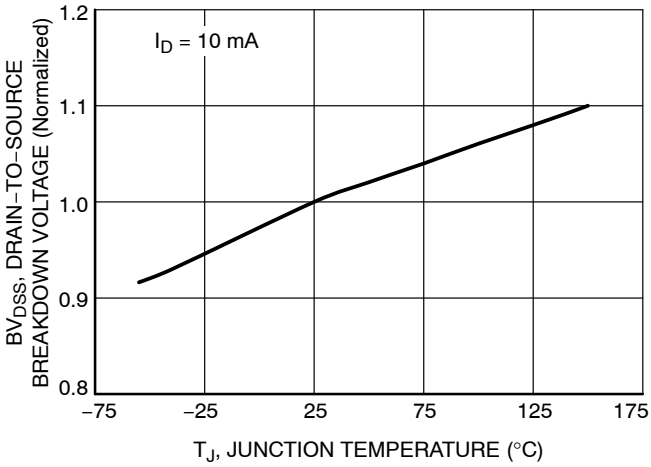

Figure 7. Breakdown Voltage Variation vs. Temperature

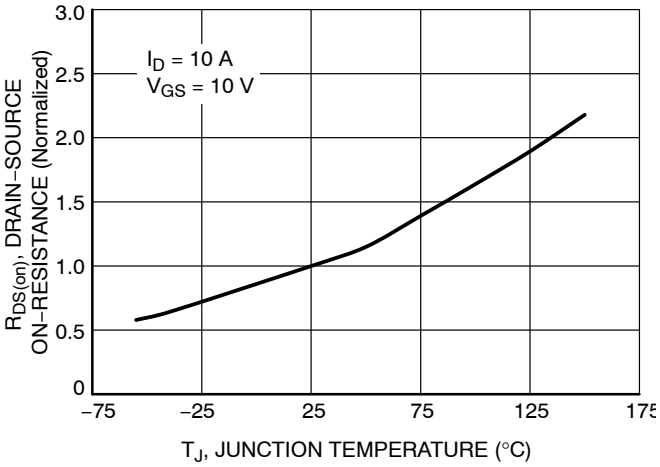

Figure 8. On−Resistance Variation vs. Temperature

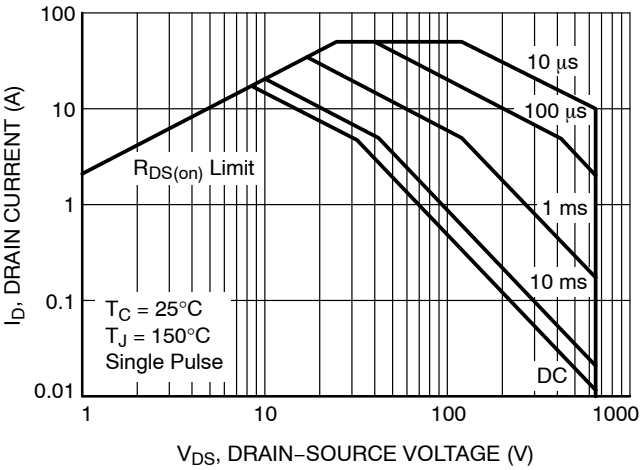

Figure 9. Maximum Safe Operating Area

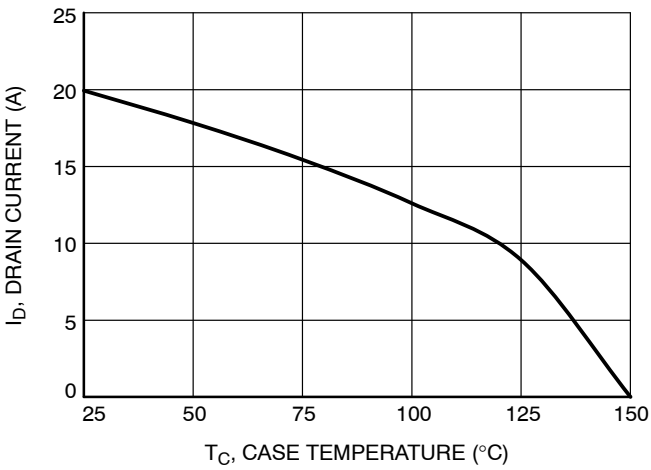

Figure 10. Maximum Drain Current vs. Case Temperature

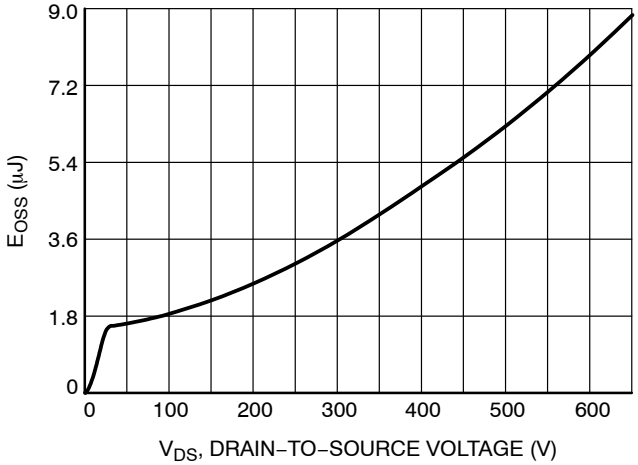

Figure 11. E_{OSS} vs. Drain−to−Source Voltage

TYPICAL CHARACTERISTICS

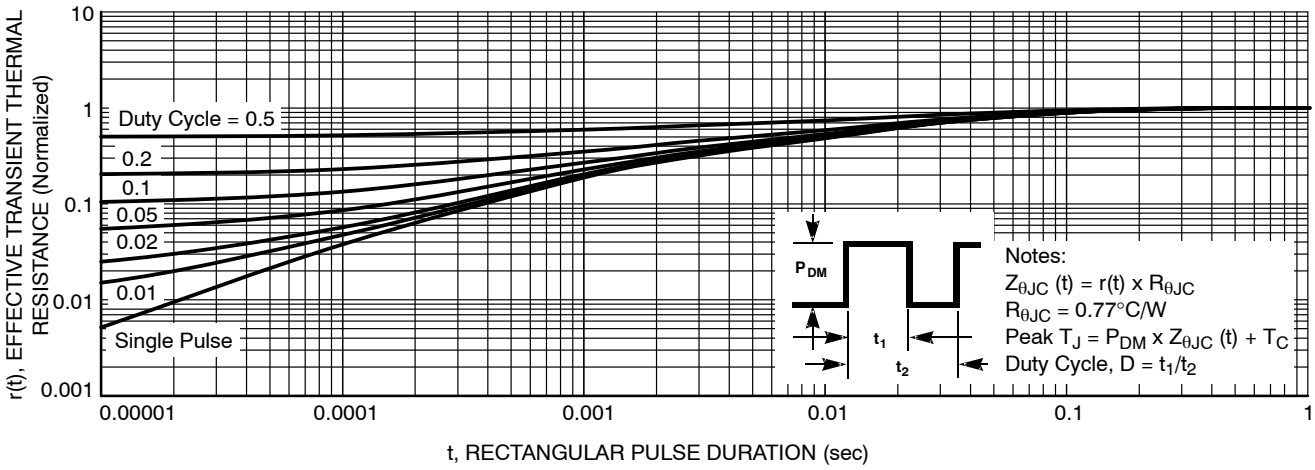

Figure 12. Transient Thermal Response

DEVICE ORDERING INFORMATION

Device	Package	Shipping†
NVBG190N65S3F	D2PAK−7L	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

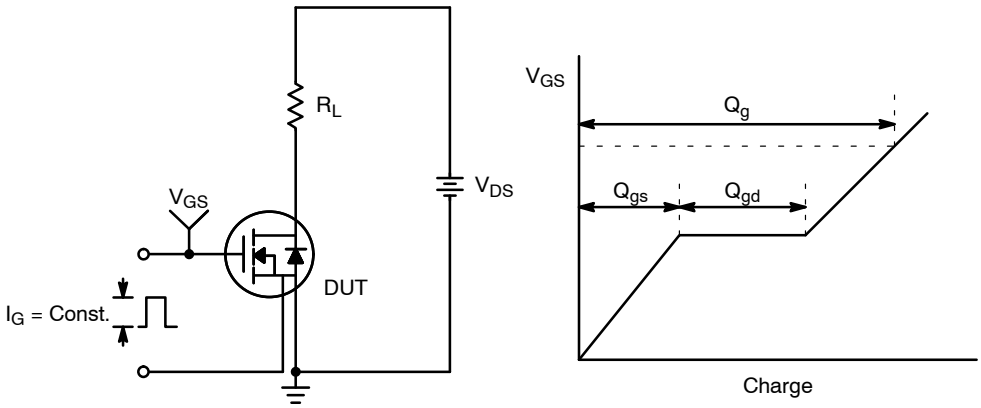

Figure 13. Gate Charge Test Circuit & Waveform

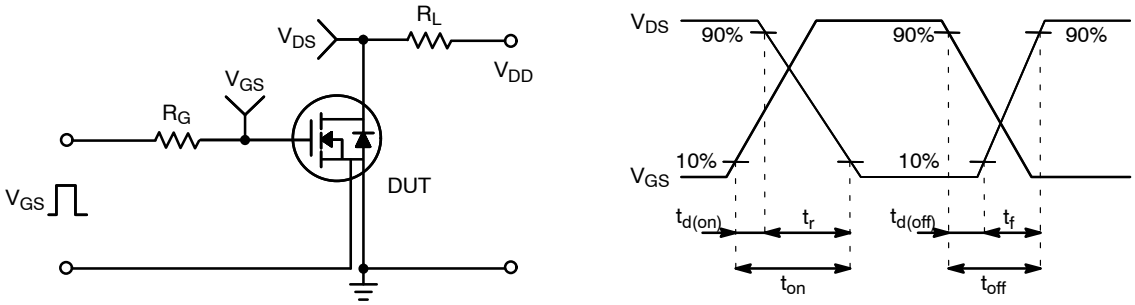

Figure 14. Resistive Switching Test Circuit & Waveforms

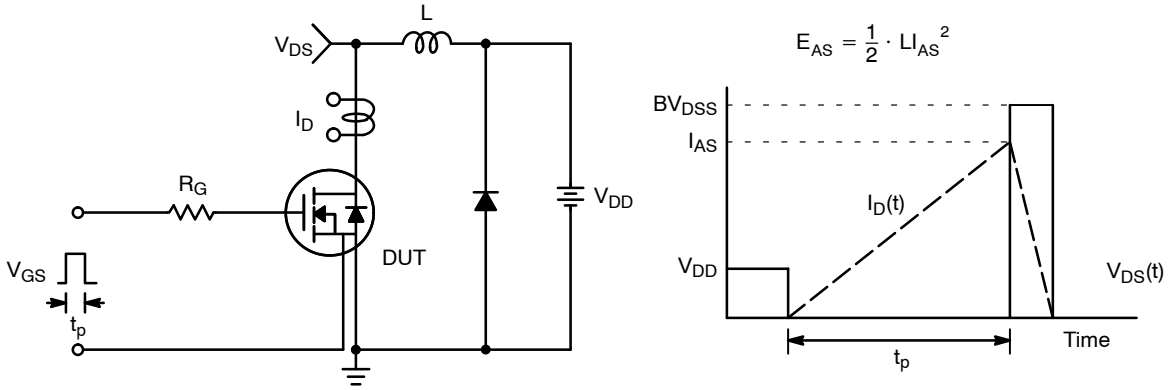

Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

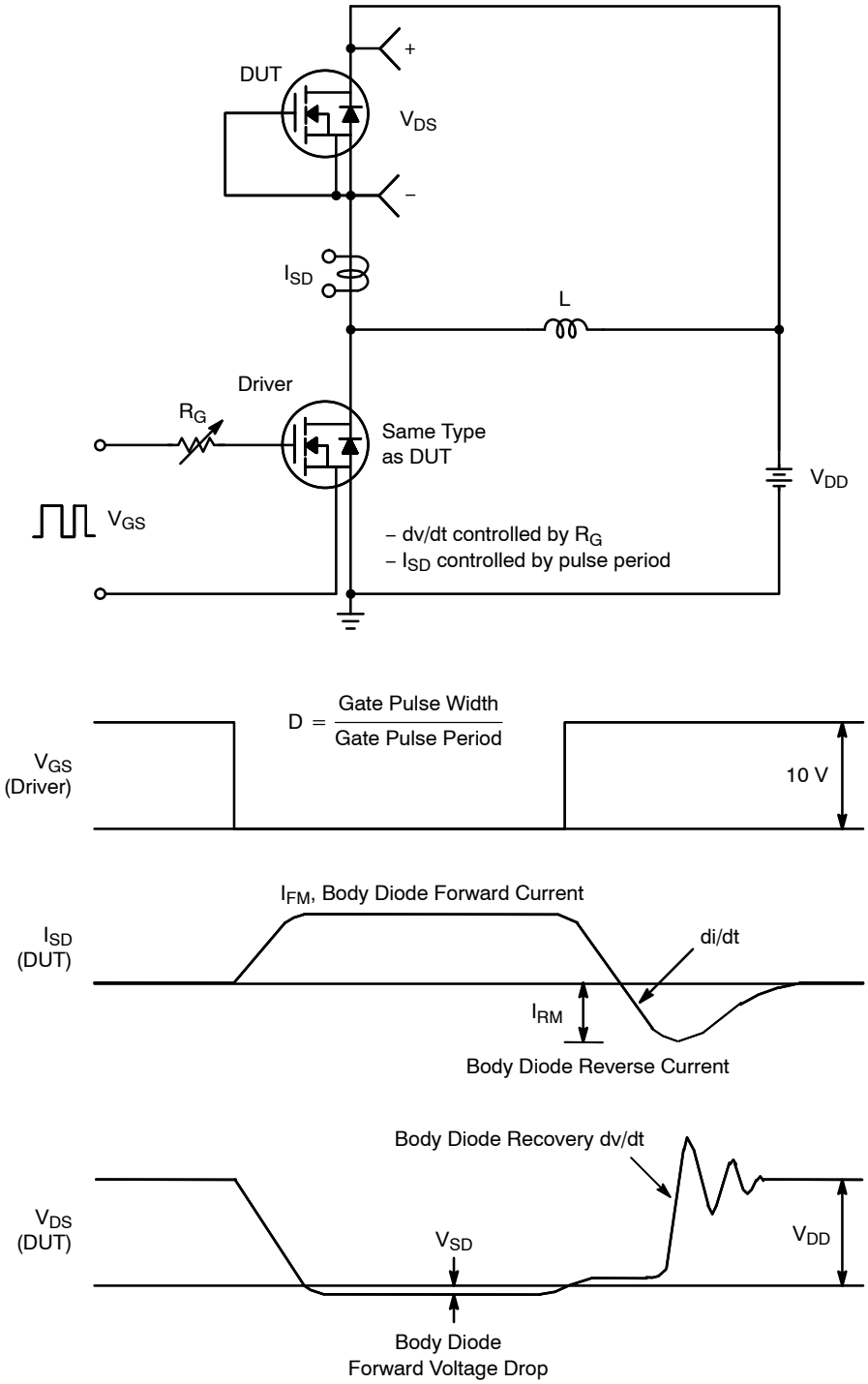

Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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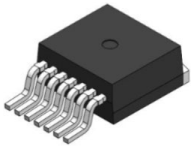
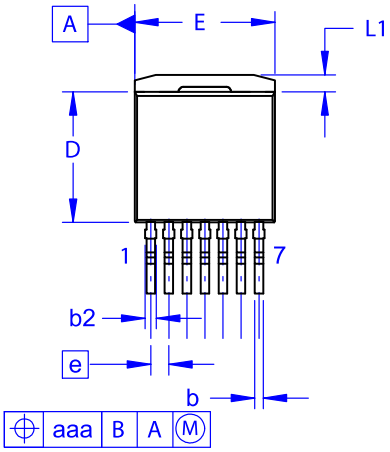
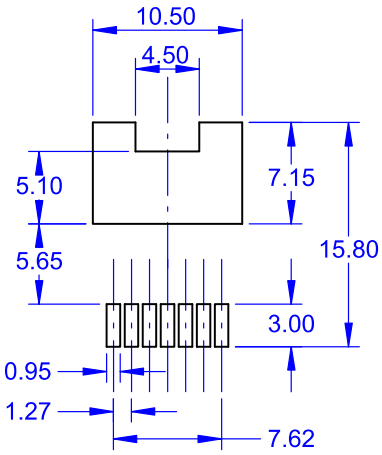


D²PAK7 (TO−263−7L HV)
CASE 418BJ
ISSUE B

DATE 16 AUG 2019



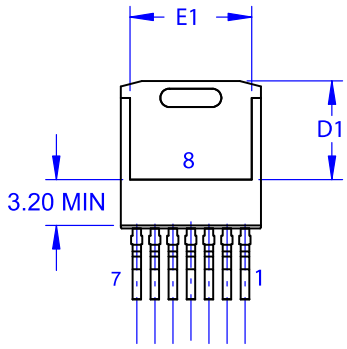


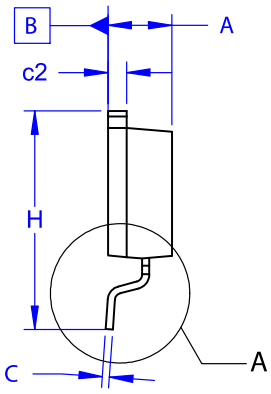
LAND PATTERN RECOMMENDATION

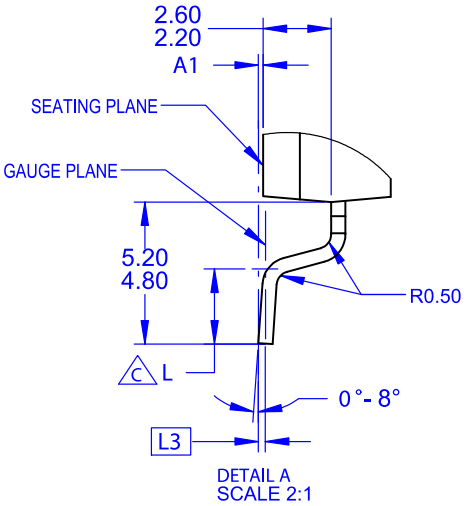
NOTES:

A. PACKAGE CONFORMS TO JEDEC TO-263 VARIATION CB EXCEPT WHERE NOTED.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. OUT OF JEDEC STANDARD VALUE.
D. DIMENSION AND TOLERANCE AS PER ASME Y14.5-2009.
E. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	0.00	0.10	0.20
b2	0.60	0.70	0.80
b	0.51	0.60	0.70
c	0.40	0.50	0.60
c2	1.20	1.30	1.40
D	9.00	9.20	9.40
D1	6.15	6.80	7.15
E	9.70	9.90	10.20
E1	7.15	7.65	8.15
e	~	1.27	~
H	15.10	15.40	15.70
L	2.44	2.64	2.84
L1	1.00	1.20	1.40
L3	~	0.25	~
aaa	~	~	0.25







GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	D²PAK7 (TO−263−7L HV)	PAGE 1 OF 1

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