

MOSFET – Power, Single N-Channel, DFNW8

80 V, 229 A, 2 mΩ

NTMTS002N08MC

Features

- Small Footprint (8x8 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Power Tools, Battery Operated Vacuums
- UAV/Drones, Material Handling
- BMS/Storage, Home Automation

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter			Value	Unit
V_{DS}	Drain-to-Source Voltage			80	V
V_{GS}	Gate-to-Source Voltage			± 20	V
I_D	Continuous Drain Current $R_{\theta JC}$ (Note 2)	Steady State	$T_C = 25^\circ\text{C}$	229	A
P_D	Power Dissipation $R_{\theta JC}$ (Note 2)			208	W
I_D	Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_A = 25^\circ\text{C}$	29	A
P_D	Power Dissipation $R_{\theta JA}$ (Notes 1, 2)			3.3	W
I_{DM}	Pulsed Drain Current	$T_C = 25^\circ\text{C}$, $t_p = 10 \mu\text{s}$		3577	A
T_J , T_{stg}	Operating Junction and Storage Temperature Range			-55 to +150	$^\circ\text{C}$
E_{AS}	Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 29 \text{ A}$, $L = 3 \text{ mH}$)			1261.5	mJ
T_L	Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			260	$^\circ\text{C}$

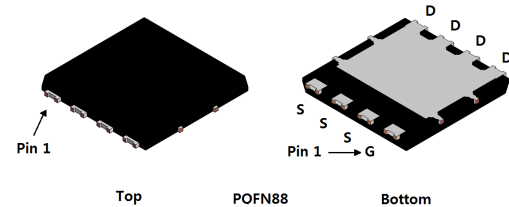
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

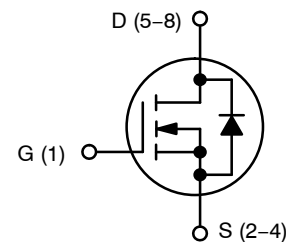
Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Junction-to-Case – Steady State (Note 2)	0.6	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-Ambient – Steady State (Note 2)	38	

1. Surface-mounted on FR4 board using a 1 in² pad size, 1 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
80 V	2 mΩ @ 10 V	229 A
	5.1 mΩ @ 6 V	

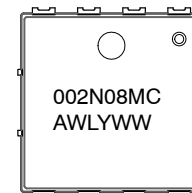


DFNW8
CASE 507AP



N-CHANNEL MOSFET

MARKING DIAGRAM



002N08MC = Device Code
A = Assembly Location
WL = 2-digit Wafer Lot Code
Y = Year Code
WW = Work Week Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NTMTS002N08MC

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	80			V
$V_{(BR)DSS}/T_J$	Drain-to-Source Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, ref to 25°C		68		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{GS} = 0\text{ V}, V_{DS} = 80\text{ V}$	$T_J = 25^\circ\text{C}$		1	μA
			$T_J = 125^\circ\text{C}$		250	
I_{GSS}	Gate-to-Source Leakage Current	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 3)

$V_{GS(TH)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 540\text{ }\mu\text{A}$	2.0	2.7	4.0	V
$V_{GS(TH)}/T_J$	Negative Threshold Temperature Coefficient	$I_D = 540\text{ }\mu\text{A}$, ref to 25°C		-7.9		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 90\text{ A}$		1.3	2.0	m Ω
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 6\text{ V}, I_D = 48\text{ A}$		1.8	5.1	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 90\text{ A}$		214		S
R_G	Gate Resistance	$T_A = 25^\circ\text{C}$		0.8		Ω

CHARGES, CAPACITANCES & GATE RESISTANCE

C_{ISS}	Input Capacitance	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 40\text{ V}$		6350	8900	pF
C_{OSS}	Output Capacitance			2100	3000	
C_{RSS}	Reverse Transfer Capacitance			93	130	
$Q_{G(TOT)}$	Total Gate Charge	$V_{GS} = 10\text{ V}, V_{DS} = 40\text{ V}; I_D = 90\text{ A}$		89	125	nC
$Q_{G(TH)}$	Threshold Gate Charge			16	22	
Q_{GS}	Gate-to-Source Charge			25		
Q_{GD}	Gate-to-Drain Charge			19		
Q_{OSS}	Output Charge			117		
Q_{sync}	Sync Charge			72		
$V_{plateau}$	Plateau Voltage			4		V

SWITCHING CHARACTERISTICS, $V_{GS} = 10\text{ V}$ (Note 3)

$t_{d(ON)}$	Turn-On Delay Time	$V_{GS} = 10\text{ V}, V_{DS} = 40\text{ V}, I_D = 90\text{ A}, R_G = 6\text{ }\Omega$		26		ns
t_r	Rise Time			20		
$t_{d(OFF)}$	Turn-Off Delay Time			65		
t_f	Fall Time			29		

DRAIN-SOURCE DIODE CHARACTERISTICS

V_{SD}	Forward Diode Voltage	$V_{GS} = 0\text{ V}, I_S = 2\text{ A}$		0.7	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 90\text{ A}$		0.8	1.3	
t_{RR}	Reverse Recovery Time	$I_F = 45\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		34	54	ns
Q_{RR}	Reverse Recovery Charge			71	114	
t_{RR}	Reverse Recovery Time	$I_F = 45\text{ A}, di/dt = 1000\text{ A}/\mu\text{s}$		27	43	nC
Q_{RR}	Reverse Recovery Charge			177	283	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

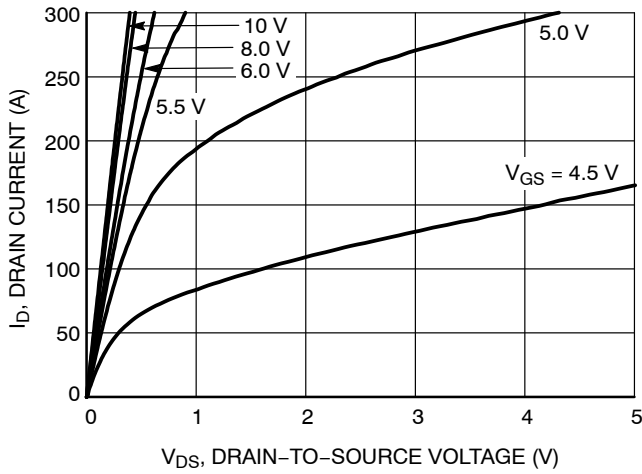


Figure 1. On-Region Characteristics

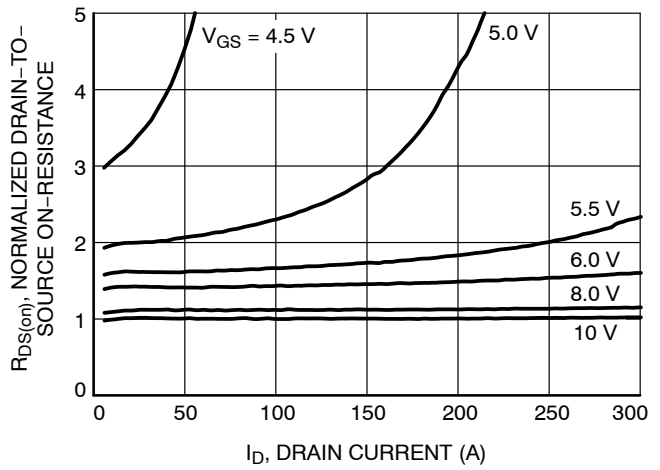


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

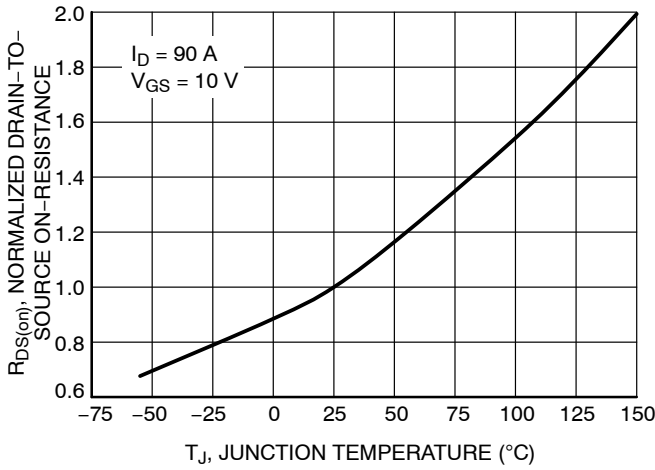


Figure 3. Normalized On Resistance vs. Junction Temperature

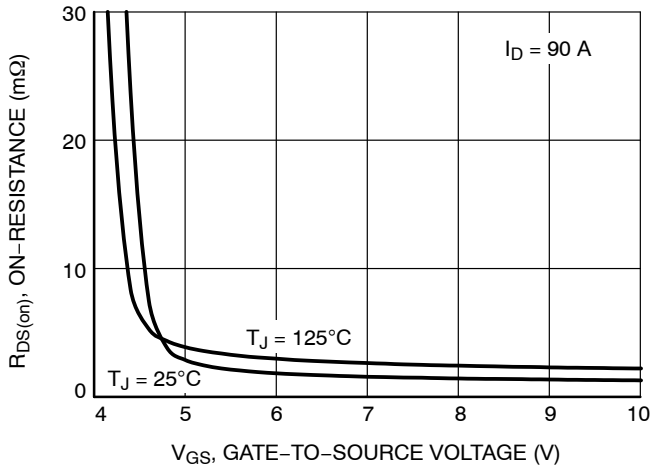


Figure 4. On-Resistance vs. Gate-to-Source Voltage

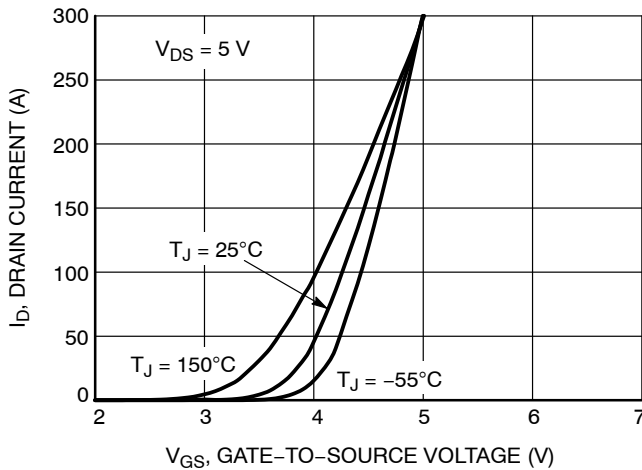


Figure 5. Transfer Characteristics

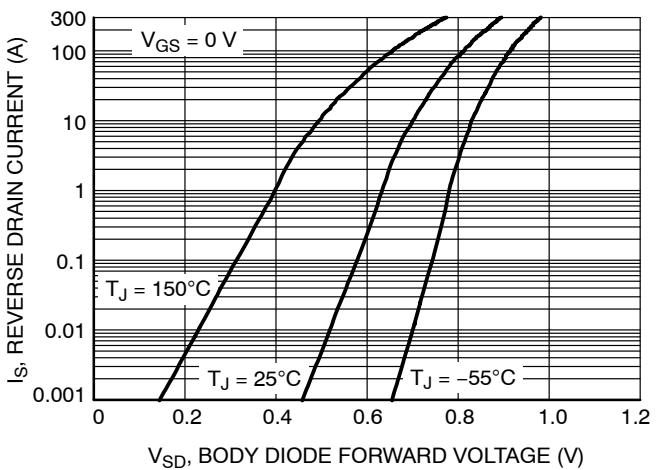


Figure 6. Source-to-Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (continued)

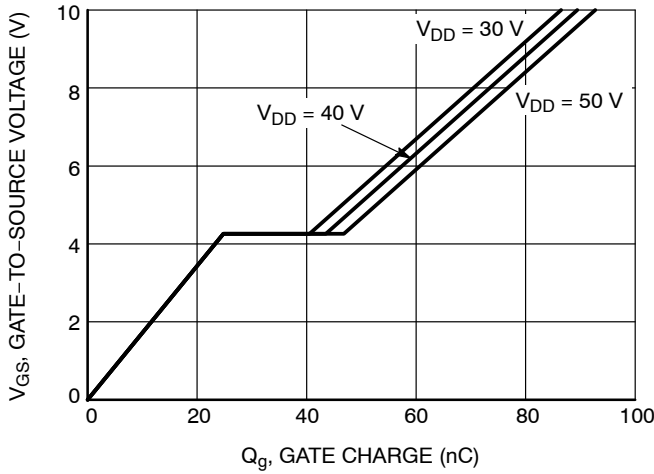


Figure 7. Gate Charge Characteristics

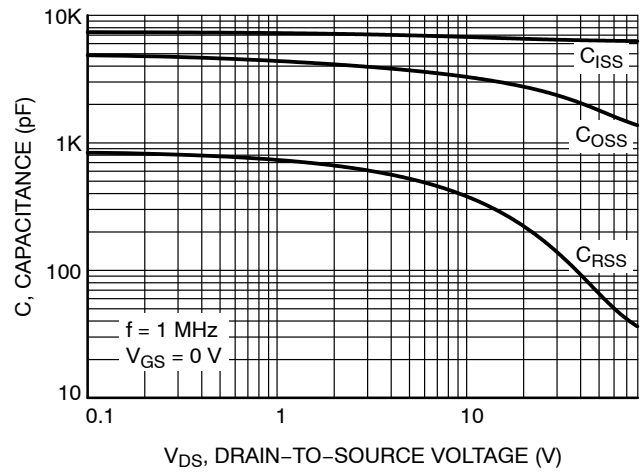


Figure 8. Capacitance vs. Drain-to-Source Voltage

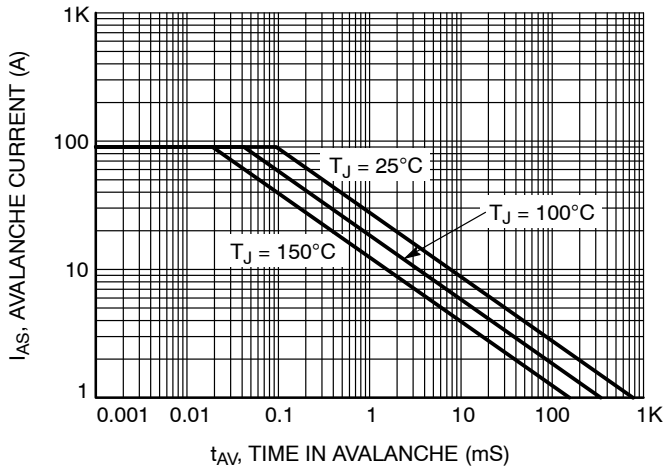


Figure 9. Unclamped Inductive Switching Capability

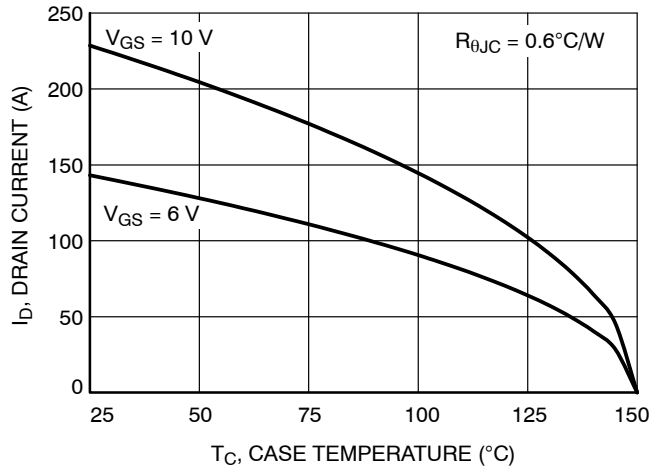


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

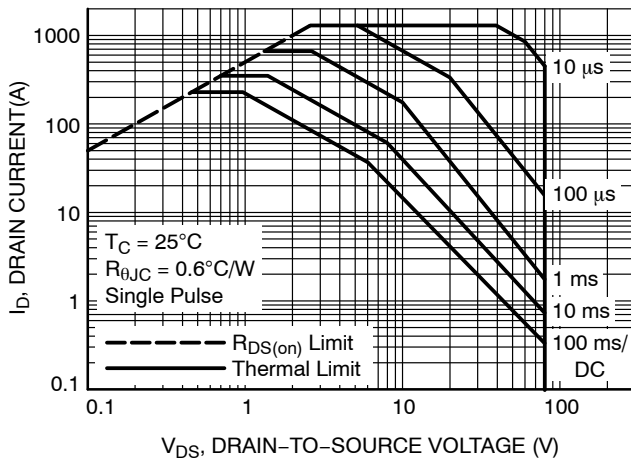


Figure 11. Forward Biased Safe Operating Area

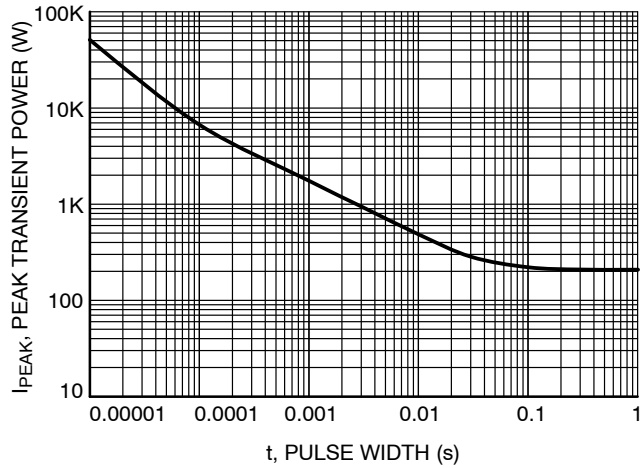


Figure 12. Single Pulse Maximum Power Dissipation

NTMTS002N08MC

TYPICAL CHARACTERISTICS (continued)

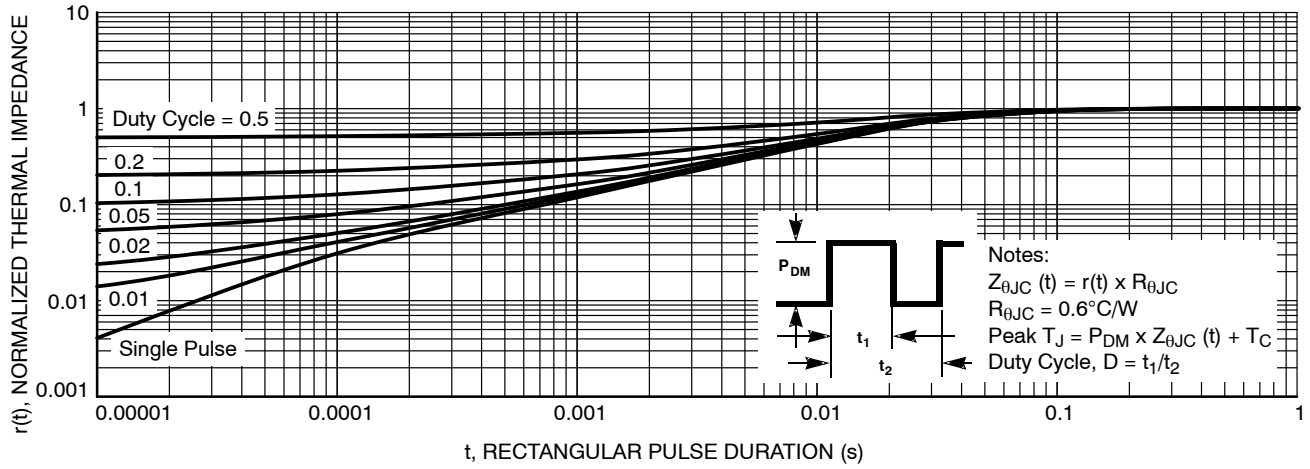
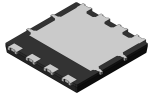


Figure 13. Transient Thermal Impedance

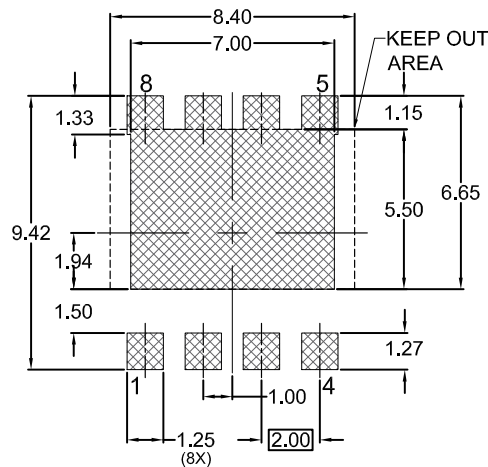
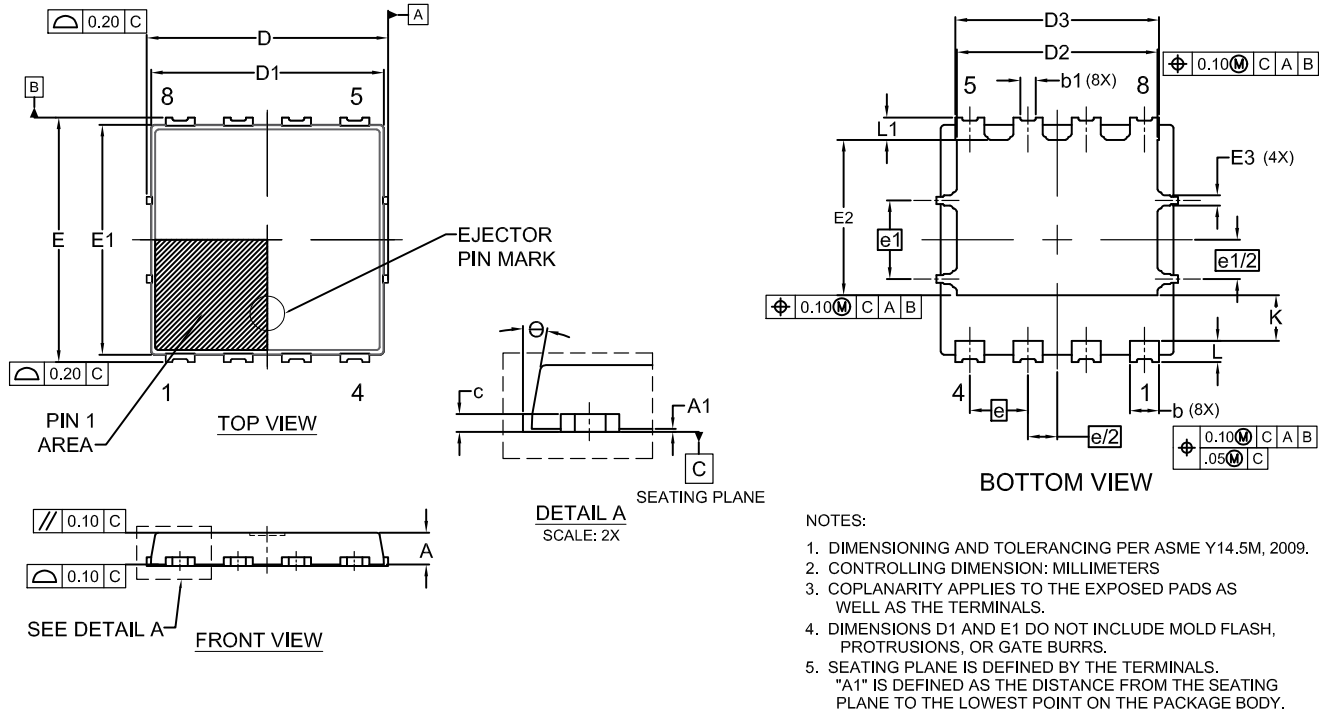
DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NTMTS002N08MC	NTMTS 002N08MC	DFNW8 (Pb-Free)	3,000 / Tape & Reel

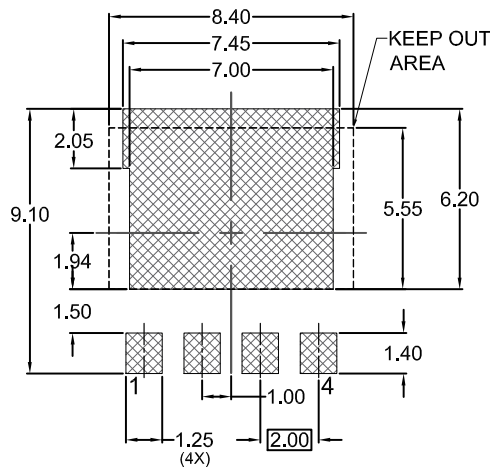
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).


TDFNW8 8.30x8.40x1.10, 2.00P
CASE 507AP
ISSUE E

DATE 08 MAY 2024



*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	1.00	1.10	1.20
A1	0.00	—	0.05
b	0.90	1.00	1.10
b1	0.35	0.45	0.55
c	0.23	0.28	0.33
D	8.20	8.30	8.40
D1	7.90	8.00	8.10
D2	6.80	6.90	7.00
D3	6.90	7.00	7.10
E	8.30	8.40	8.50
E1	7.80	7.90	8.00
E2	5.24	5.34	5.44
E3	0.25	0.35	0.45
e	2.00 BSC		
e/2	1.00 BSC		
e1	2.70 BSC		
e1/2	1.35 BSC		
K	1.50	1.57	1.70
L	0.64	0.74	0.84
L1	0.67	0.77	0.87
Θ	0°	—	12°

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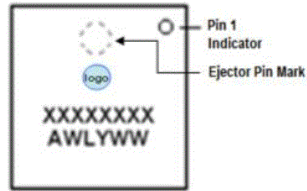
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TDFNW8 8.30x8.40x1.10, 2.00P
CASE 507AP
ISSUE E

DATE 08 MAY 2024

GENERIC
MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot Code
Y = Year Code
WW = Work Week Code

*This information is generic. Please refer to device data sheet for actual part marking.
Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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