

MOSFET – N-Channel Shielded Gate POWERTRENCH®

150 V, 15 mΩ, 61.3 A

NVDS015N15MC

Features

- Shielded Gate MOSFET Technology
- Max $R_{DS(on)}$ = 15 mΩ at V_{GS} = 10 V, I_D = 29 A
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Primary Side for 48 V Isolated Bus
- SR for MV Secondary Applications

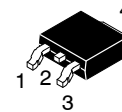
MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Symbol	Parameter			Value	Unit
V_{DSS}	Drain-to-Source Voltage			150	V
V_{GS}	Gate-to-Source Voltage			±20	V
I_D	Continuous Drain Current $R_{\theta JC}$ (Note 2)	Steady State	T_C = 25°C	61.3	A
			T_C = 100°C	43.4	
P_D	Power Dissipation $R_{\theta JC}$ (Note 2)	Steady State	T_C = 25°C	107.1	W
			T_C = 100°C	53.6	
I_D	Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State	T_A = 25°C	10.5	A
			T_A = 100°C	7.4	
P_D	Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	Steady State	T_A = 25°C	3.1	W
			T_A = 100°C	1.6	
I_{DM}	Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		382	A
T_J, T_{stg}	Operating Junction and Storage Temperature Range			-55 to +175	°C
I_S	Source Current (Body Diode)			89.3	A
E_{AS}	Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)}$ = 4.4 A)			1301	mJ
T_L	Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			260	°C

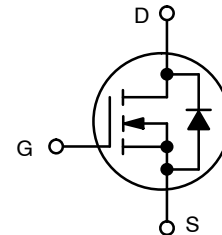
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
150 V	15 mΩ @ 10 V	61.3 A

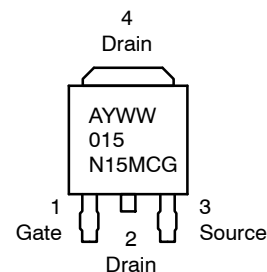


DPAK
CASE 369C



N-CHANNEL MOSFET

MARKING DIAGRAM



015N15MCG = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
NVDS015N15MCT4G	DPAK (Pb-Free)	2,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NVDS015N15MC

THERMAL RESISTANCE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Junction-to-Case – Steady State (Note 2)	1.4	°C/W
$R_{\theta JA}$	Junction-to-Ambient – Steady State (Notes 1, 2)	47.9	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
--------	-----------	----------------	-----	-----	-----	------

OFF CHARACTERISTICS

$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	150			V
$V_{(BR)DSS}/T_J$	Drain-to-Source Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, ref to 25°C		83		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{GS} = 0\text{ V}, V_{DS} = 120\text{ V}$			1.0	μA
		$T_J = 125^\circ\text{C}$		1.1		
I_{GSS}	Gate-to-Source Leakage Current	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS

$V_{GS(TH)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 162\text{ }\mu\text{A}$	2.5		4.5	V
$V_{GS(TH)}/T_J$	Negative Threshold Temperature Coefficient	$I_D = 162\text{ }\mu\text{A}$, ref to 25°C		-8.2		mV/°C
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 29\text{ A}$		11.8	15	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 29\text{ A}$		58		S

CHARGES, CAPACITANCES & GATE RESISTANCE

C_{ISS}	Input Capacitance	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 75\text{ V}$		2120		pF
C_{OSS}	Output Capacitance			595		
C_{RSS}	Reverse Transfer Capacitance			10.5		
$Q_{G(TOT)}$	Total Gate Charge	$V_{GS} = 10\text{ V}, V_{DS} = 75\text{ V}; I_D = 29\text{ A}$		27		nC
$Q_{G(TH)}$	Threshold Gate Charge			7		
Q_{GS}	Gate-to-Source Charge			11		
Q_{GD}	Gate-to-Drain Charge			4		
V_{GP}	Plateau Voltage			5.5		V

SWITCHING CHARACTERISTICS (Note 3)

$t_{d(ON)}$	Turn-On Delay Time	$V_{GS} = 10\text{ V}, V_{DD} = 75\text{ V}, I_D = 29\text{ A}, R_G = 6\text{ }\Omega$		16		ns
t_r	Rise Time			5		
$t_{d(OFF)}$	Turn-Off Delay Time			21		
t_f	Fall Time			4		

DRAIN-SOURCE DIODE CHARACTERISTICS

V_{SD}	Forward Diode Voltage	$V_{GS} = 0\text{ V}, I_S = 29\text{ A}$	$T_J = 25^\circ\text{C}$		0.89	1.2	V
t_{RR}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, V_{DD} = 75\text{ V}$ $dI_S/dt = 300\text{ A}/\mu\text{s}, I_S = 29\text{ A}$		49			ns
Q_{RR}	Reverse Recovery Charge			197			nC
t_{RR}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, V_{DD} = 75\text{ V}$ $dI_S/dt = 1000\text{ A}/\mu\text{s}, I_S = 29\text{ A}$		34			ns
Q_{RR}	Reverse Recovery Charge			345			nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

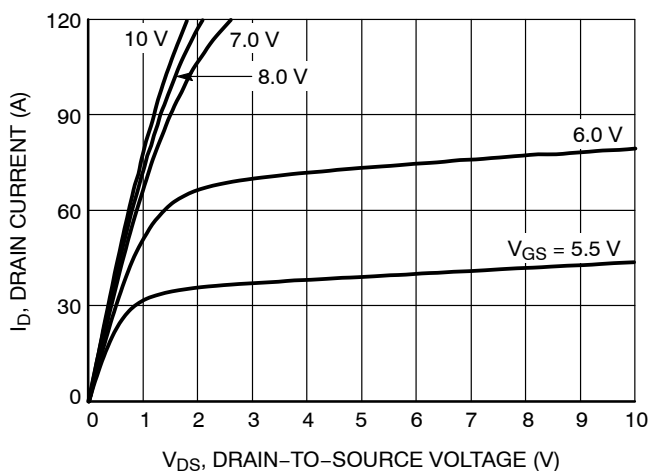


Figure 1. On-Region Characteristics

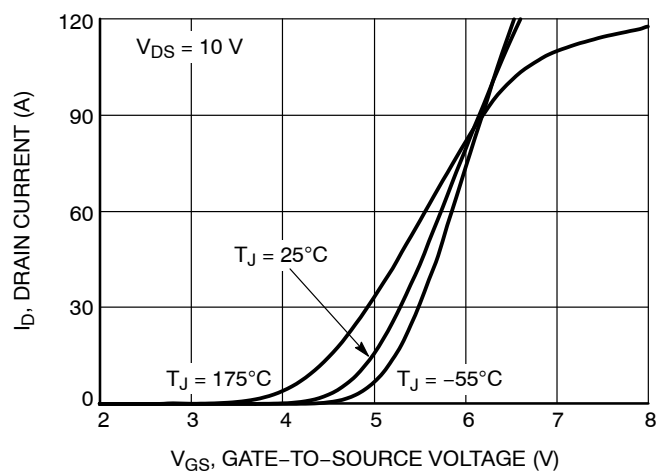


Figure 2. Transfer Characteristics

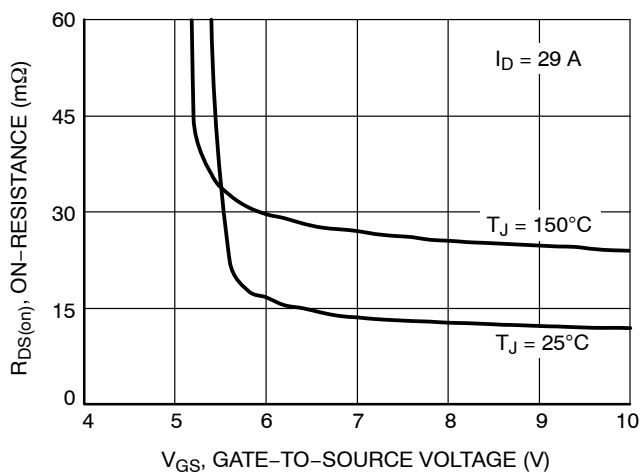


Figure 3. On-Resistance vs. Gate-to-Source Voltage

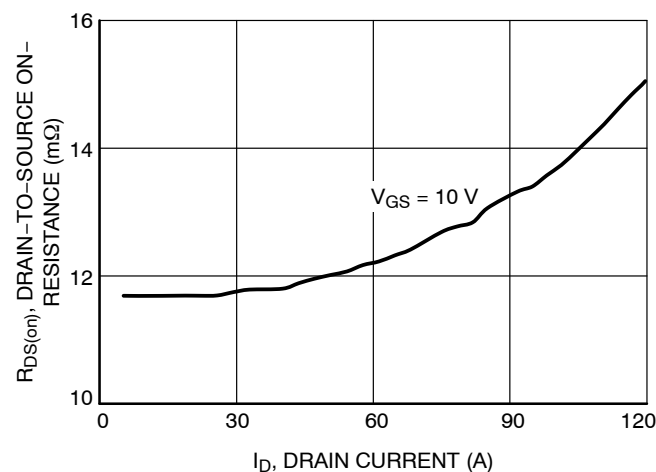


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

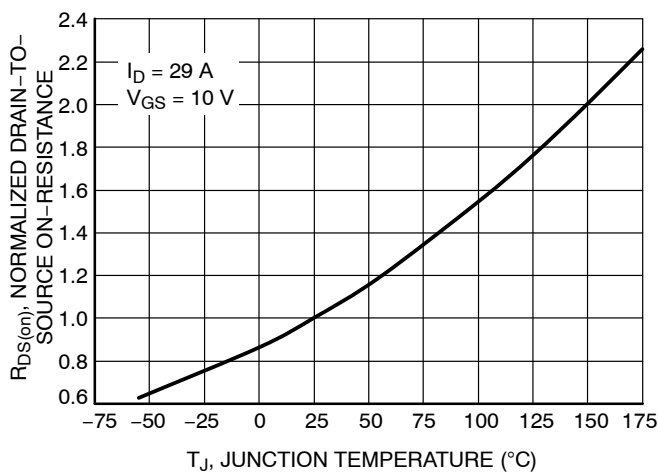


Figure 5. Normalized On-Resistance vs. Junction Temperature

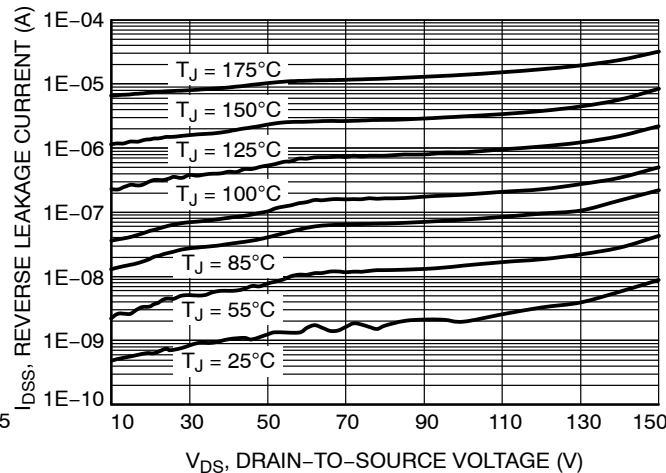


Figure 6. Drain-to-Source Leakage Current vs. Voltage

NVDS015N15MC

TYPICAL CHARACTERISTICS (continue)

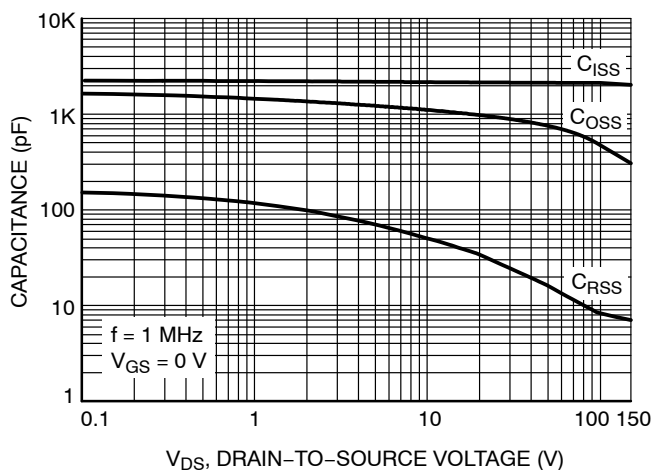


Figure 7. Capacitance vs. Drain-to-Source Voltage

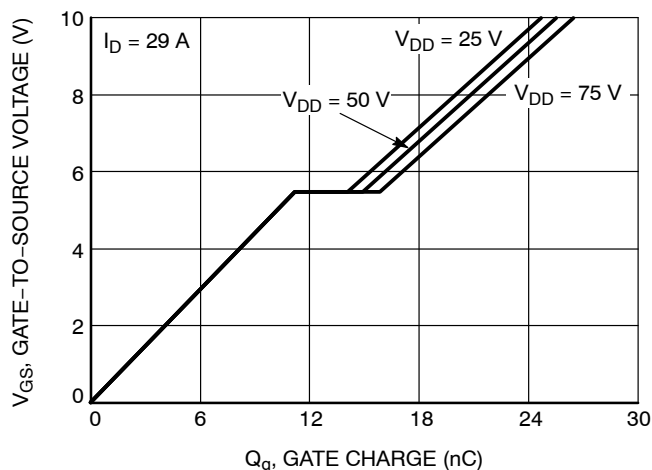


Figure 8. Gate Charge Characteristics

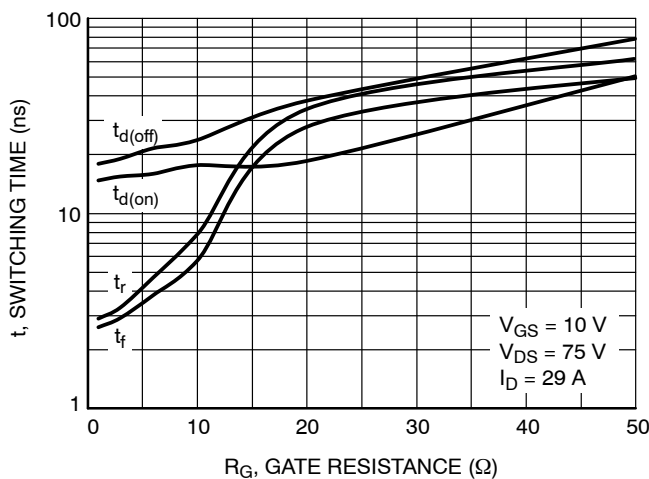


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

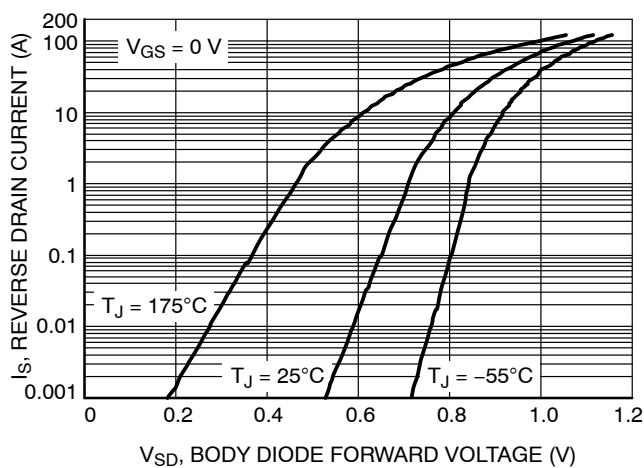


Figure 10. Source-to-Drain Diode Forward Voltage vs. Source Current

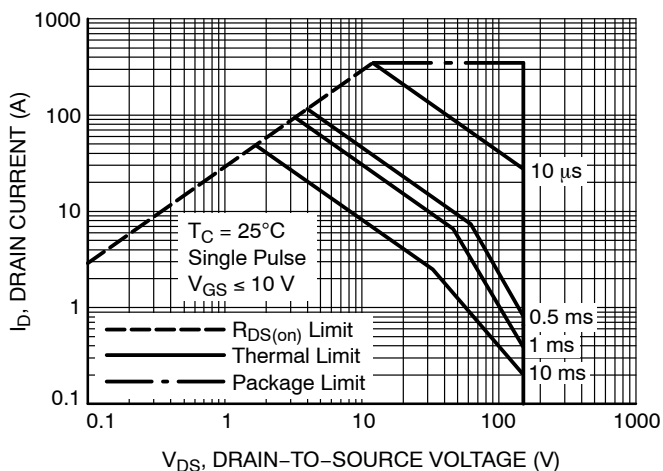


Figure 11. Forward Bias Safe Operating Area

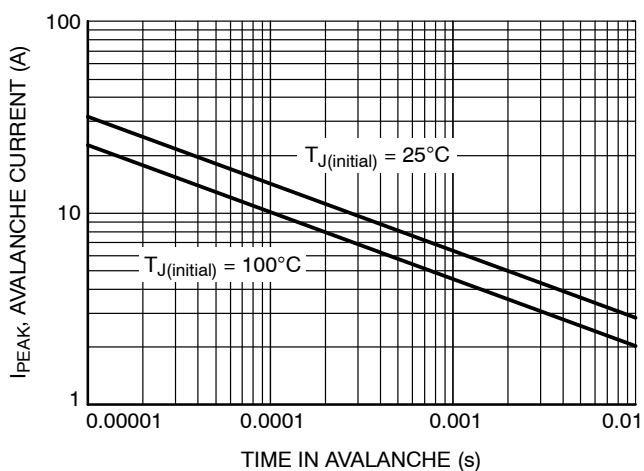


Figure 12. Unclamped Inductive Switching Capability

NVDS015N15MC

TYPICAL CHARACTERISTICS (continue)

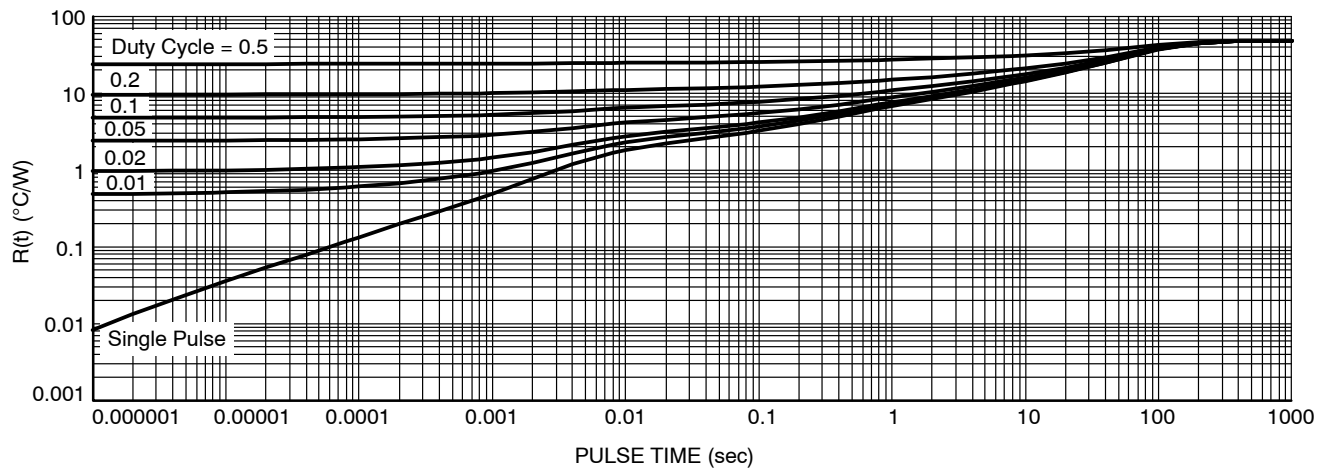
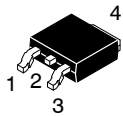


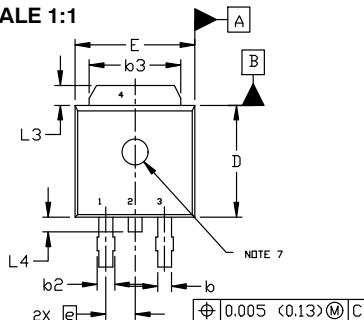
Figure 13. Transient Thermal Impedance



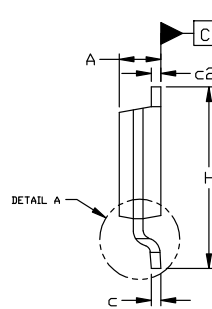
DPAK (SINGLE GAUGE)
CASE 369C
ISSUE G

DATE 31 MAY 2023

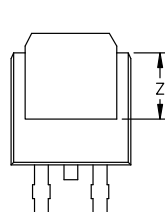
SCALE 1:1



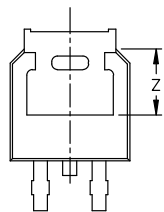
TOP VIEW



SIDE VIEW

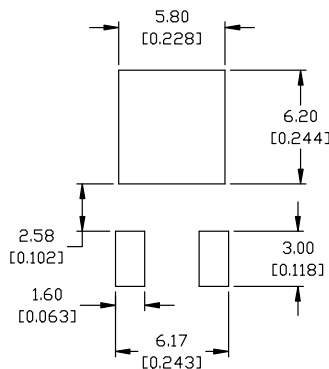


BOTTOM VIEW



BOTTOM VIEW

ALTERNATE
CONSTRUCTIONS



RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

STYLE 1:

PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:

PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:

PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:

PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:

PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:

PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:

PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:

PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:

PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:

PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

NOTES:

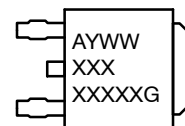
- DIMENSIONING AND TOLERANCING ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: INCHES
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
- DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
- OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090	BSC	2.29	BSC
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114	REF	2.90	REF
L2	0.020	BSC	0.51	BSC
L3	0.035	0.050	0.89	1.27
L4	----	0.040	---	1.01
Z	0.155	----	3.93	---

GENERIC
MARKING DIAGRAM*



IC



Discrete

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON10527D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	DPAK (SINGLE GAUGE)	PAGE 1 OF 1

onsemi and Onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales