

MOSFET – Dual, N-Channel, Logic Level, POWER trench®

40 V, 12 A, 8.2 mΩ

FDMC9430L-F085

Features

- Typical $R_{DS(on)} = 6.3 \text{ m}\Omega$ at $V_{GS} = 10 \text{ V}$, $I_D = 12 \text{ A}$
- Typical $Q_{g(tot)} = 15 \text{ nC}$ at $V_{GS} = 10 \text{ V}$, $I_D = 12 \text{ A}$
- UIS Capability
- This Device is Pb-Free, Halide Free and RoHS Compliant
- AEC Qualified AEC-Q101

Applications

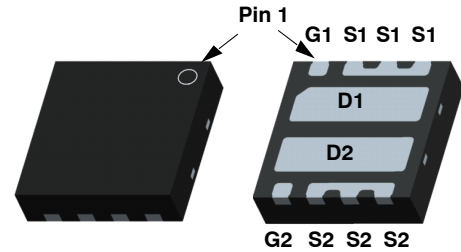
- Battery Protection
- Load Switching
- Point of Load

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-to-Source Voltage	40	V
V_{GS}	Gate-to-Source Voltage	± 12	V
I_D	Drain Current – Continuous ($V_{GS} = 10$) (Note 1) $T_C = 25^\circ\text{C}$	12	A
	Pulsed Drain Current $T_C = 25^\circ\text{C}$	See Figure 4	
E_{AS}	Single Pulse Avalanche Energy (Note 2)	21.6	mJ
P_D	Power Dissipation	11.4	W
	Derate Above 25°C	0.1	W/ $^\circ\text{C}$
T_J, T_{stg}	Operating and Storage Temperature	-55 to $+150$	$^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	13	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Maximum Thermal Resistance, Junction-to-Ambient (Note 3)	65	$^\circ\text{C}/\text{W}$

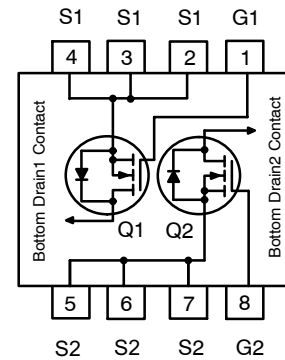
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Current is limited by bondwire configuration.
2. Starting $T_J = 25^\circ\text{C}$, $L = 0.3 \text{ mH}$, $I_{AS} = 12 \text{ A}$, $V_{DD} = 40 \text{ V}$ during inductor charging and $V_{DD} = 0 \text{ V}$ during time in avalanche.
3. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in^2 pad of 2 oz copper.



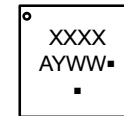
WDFN8
3x3, 0.65P
CASE 511DG

PIN ASSIGNMENT



Dual N-Channel MOSFET

MARKING DIAGRAM



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
FDMC9430L-F085	WDFN8 (Pb-Free, Halide Free)	3000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

FDMC9430L–F085

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

B _{VDS}	Drain-to-Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	40	–	–	V
I _{DSS}	Drain-to-Source Leakage Current	V _{DS} = 40 V, V _{GS} = 0 V	–	–	1	μA
		T _J = 25°C	–	–	–	–
		T _J = 150°C (Note 4)	–	–	0.2	mA
I _{GSS}	Gate-to-Source Leakage Current	V _{GS} = ±12 V	–	–	±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate-to-Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	1	1.8	3	V
R _{DS(on)}	Drain-to-Source On Resistance	I _D = 10 A, V _{GS} = 4.5 V	–	8.9	11.5	mΩ
		I _D = 12 A, V _{GS} = 10 V	–	6.3	8.0	–
		T _J = 25°C	–	–	–	–
		T _J = 150°C (Note 4)	–	10.2	13.0	–

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 20 V, V _{GS} = 0 V, f = 1 MHz	–	984	–	pF
C _{oss}	Output Capacitance		–	315	–	–
C _{rss}	Reverse Transfer Capacitance		–	18	–	–
R _g	Gate Resistance	V _{GS} = 0.5 V, f = 1 MHz	–	1.1	–	Ω
Q _{g(ToT)}	Total Gate Charge	V _{GS} = 0 to 10 V	–	15	22	nC
Q _{g(th)}	Threshold Gate Charge	V _{GS} = 0 to 1 V	–	0.9	–	–
Q _{gs}	Gate-to-Source Gate Charge		–	2.6	–	–
Q _{gd}	Gate-to-Drain “Miller” Charge		–	2.1	–	–

SWITCHING CHARACTERISTICS

t _{on}	Turn-On Time	V _{DD} = 20 V, I _D = 12 A, V _{GS} = 10 V, R _{GEN} = 6 Ω	–	–	13	ns
t _{d(on)}	Turn-On Delay		–	7	–	–
t _r	Rise Time		–	2	–	–
t _{d(off)}	Turn-Off Delay		–	17	–	–
t _f	Fall Time		–	2	–	–
t _{off}	Turn-Off Time		–	–	28	–

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Source-to-Drain Diode Voltage	I _{SD} = 12 A, V _{GS} = 0 V	–	–	1.2	V
		I _{SD} = 6 A, V _{GS} = 0 V	–	–	1.1	–
t _{rr}	Reverse-Recovery Time	V _{DD} = 32 V, I _F = 12 A, dI _{SD} /dt = 100 A/μs	–	32	48	ns
Q _{rr}	Reverse-Recovery Charge		–	16	24	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at T_J = 150°C. Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS

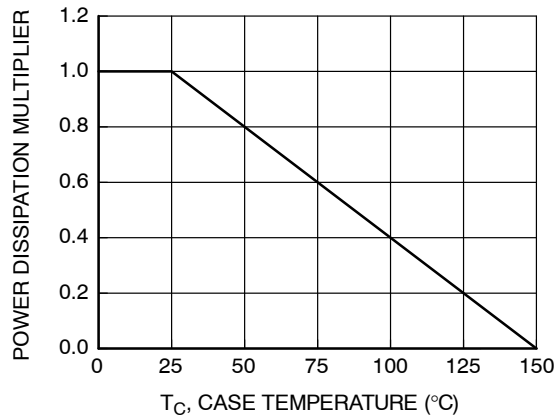


Figure 1. Normalized Power Dissipation vs. Case Temperature

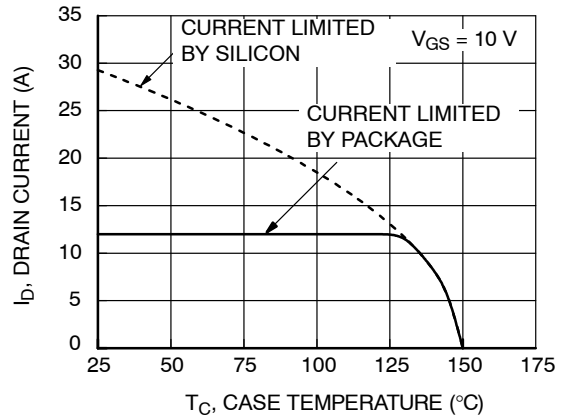


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

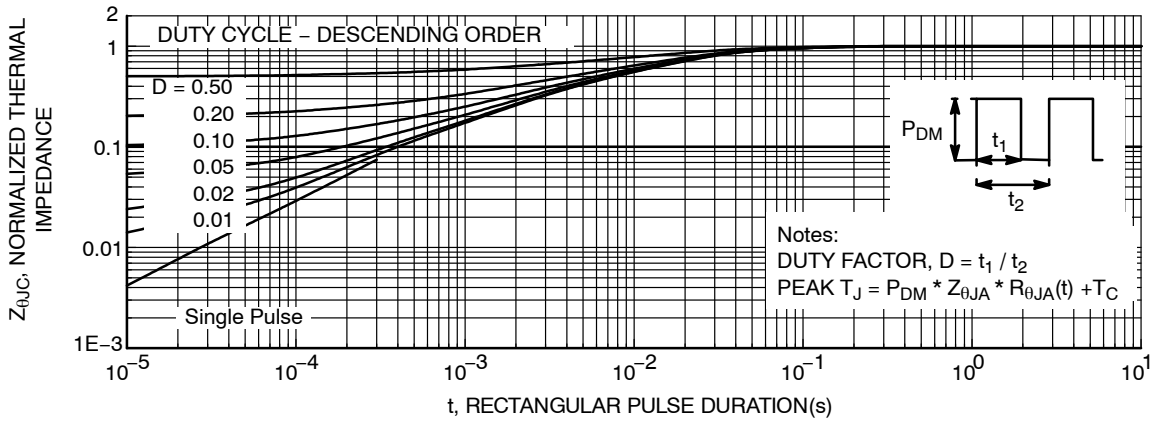


Figure 3. Normalized Maximum Transient Thermal Impedance

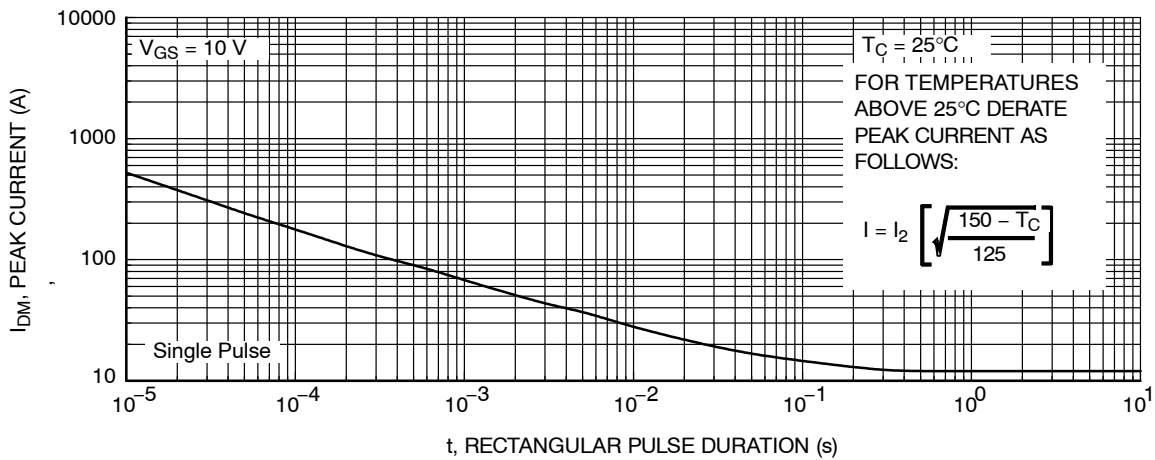


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS

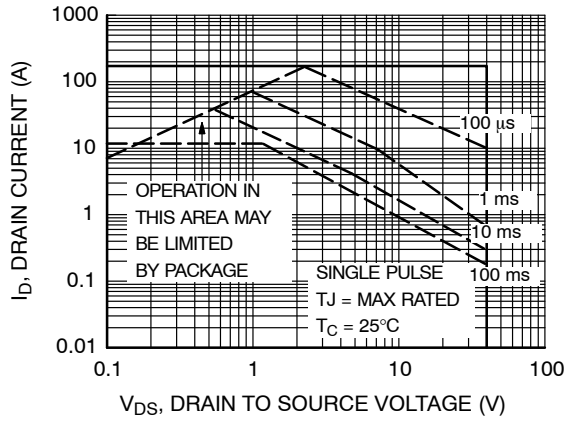
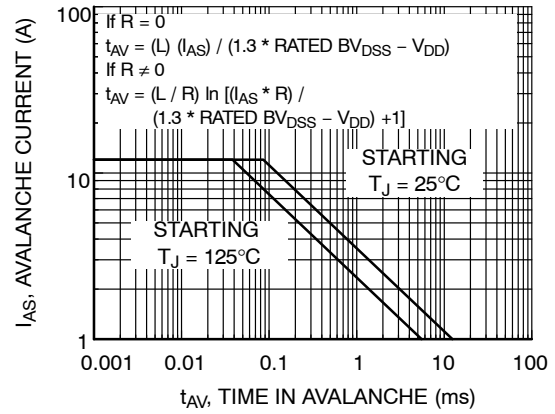


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to onsemi Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

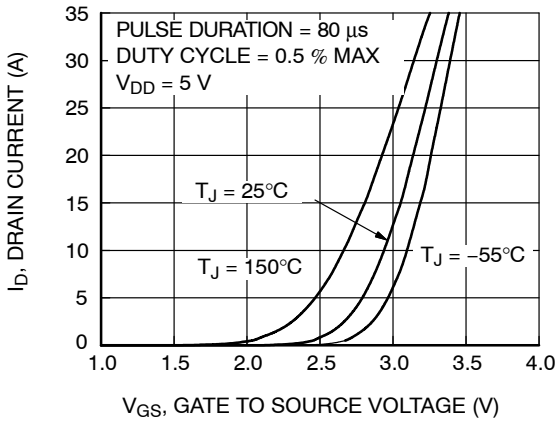


Figure 7. Transfer Characteristics

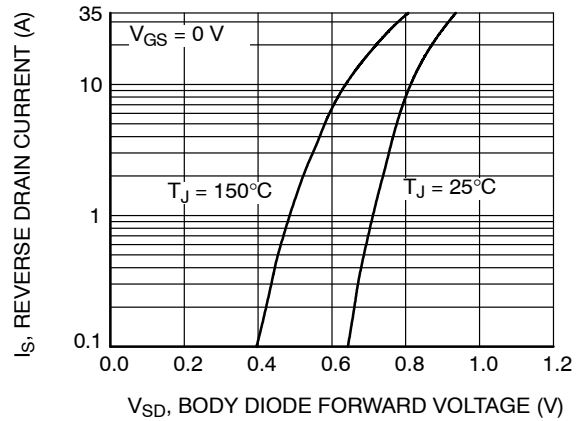


Figure 8. Forward Diode Characteristics

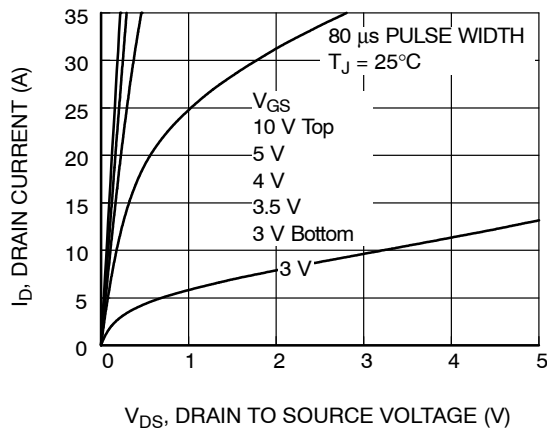


Figure 9. Saturation Characteristics

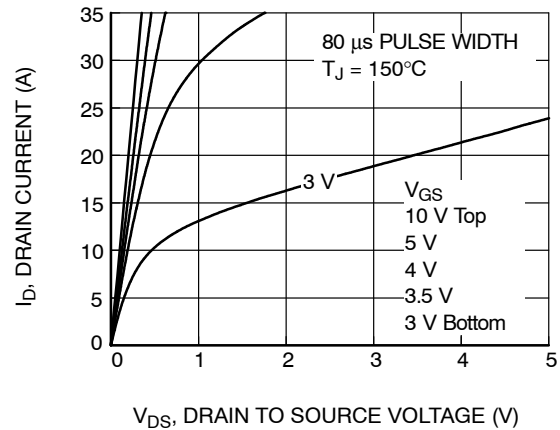


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS

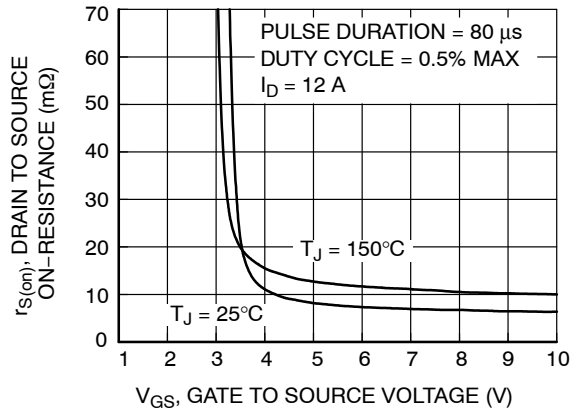


Figure 11. $R_{DS(on)}$ vs. Gate Voltage

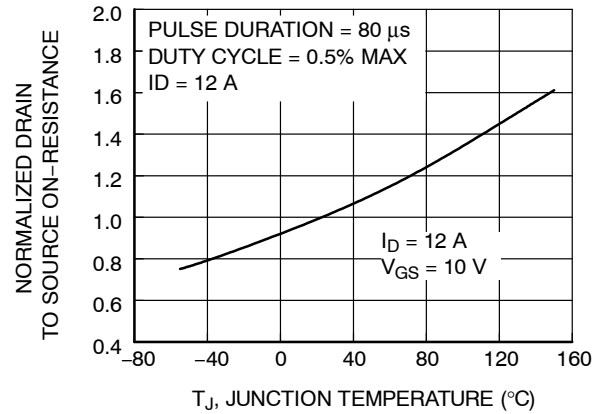


Figure 12. Normalized $R_{DS(on)}$ vs. Junction Temperature

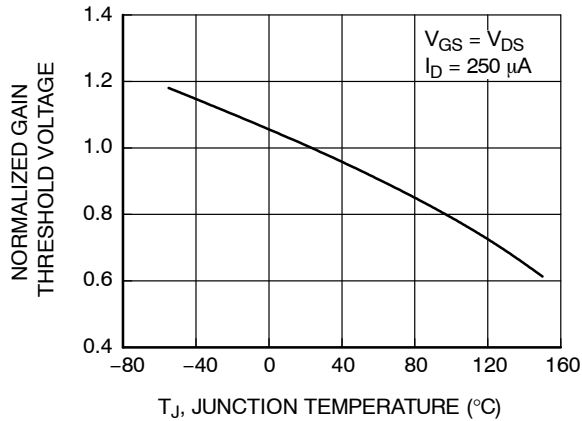


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

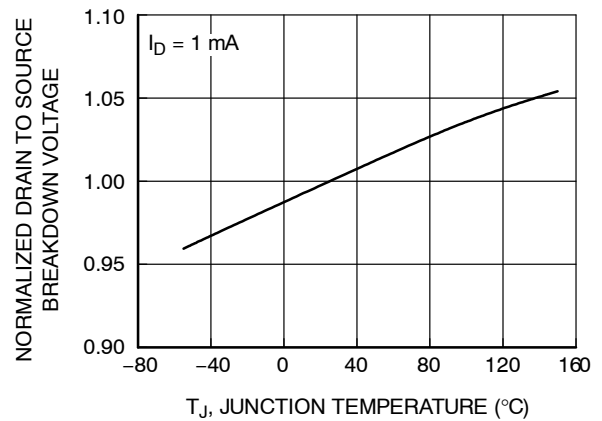


Figure 14. Normalized Drain-to-Source Breakdown Voltage vs. Junction Temperature

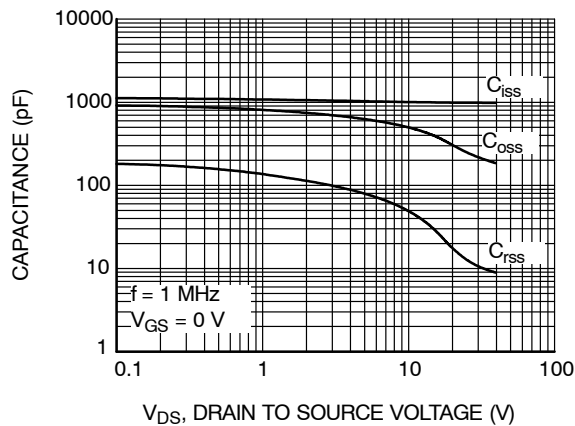


Figure 15. Capacitance vs. Drain-to-Source Voltage

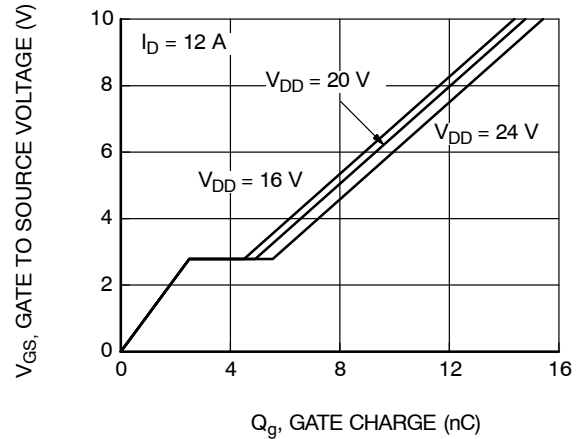
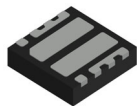
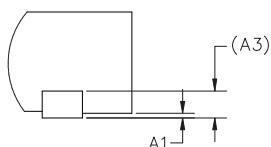
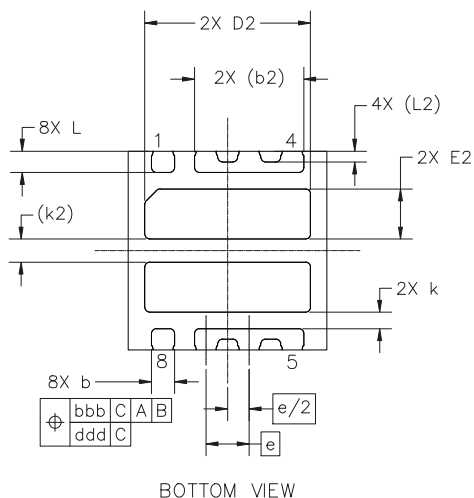
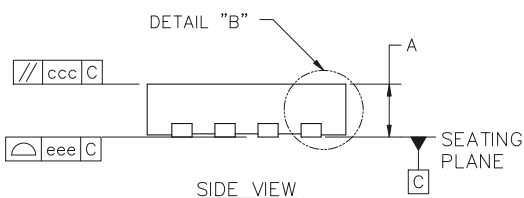
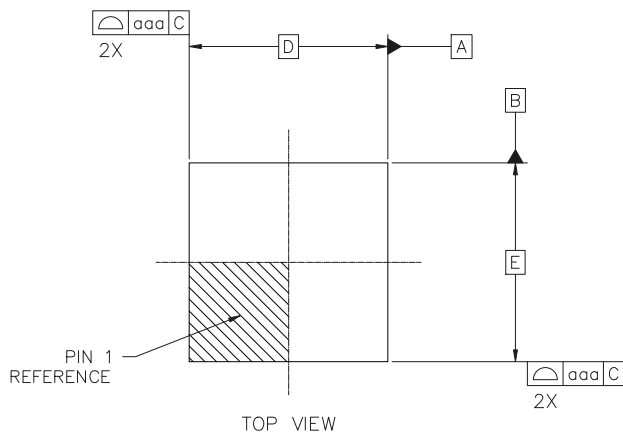


Figure 16. Gate Charge vs. Gate-to-Source Voltage

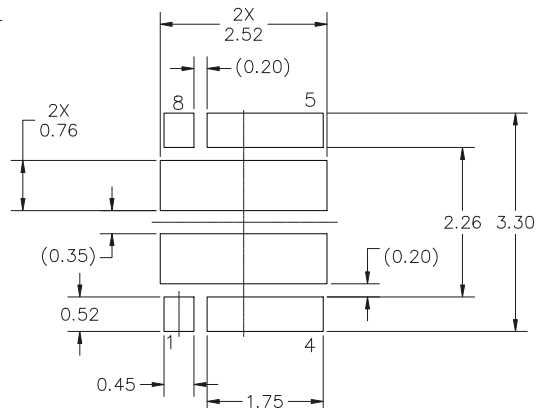


WDFN8 3.00x3.00x0.75, 0.65P
CASE 511DG
ISSUE B

DATE 15 NOV 2024



DETAIL "B"
SCALE 2:1



MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	---	0.05
A3	0.20 REF		
b	0.30	0.35	0.40
b2	1.65 REF		
D	3.00 BSC		
D2	2.45	2.50	2.55
E	3.00 BSC		
E2	0.71	0.76	0.81
e	0.65 BSC		
k	0.22	---	---
k2	0.35 REF		
L	0.27	0.32	0.37
L2	0.16 REF		
TOLERANCE FORM AND POSITION			
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		

NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

RECOMMENDED MOUNTING FOOTPRINT

- * For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, [SOLDDRM/D](#).

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DESCRIPTION:	WDFN8 3.00x3.00x0.75, 0.65P	PAGE 1 OF 1

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