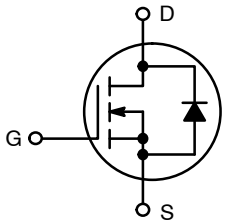
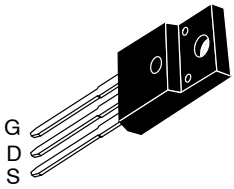
MOSFET - Power, N-Channel, SUPERFET® III, FAST

650 V, 95 mΩ, 30 A

NTPF095N65S3H

V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
650 V	95 mΩ @ 10 V	30 A





TO−220 FULLPAK
CASE 221D

Description

SUPERFET III MOSFET is **onsemi**'s brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provides superior switching performance, and withstand extreme dv/dt rate.

Consequently, SUPERFET III FAST MOSFET series helps minimize various power systems and improve system efficiency.

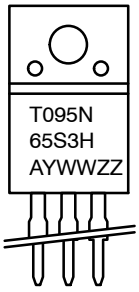
Features

- 700 V @ T_J = 150°C
- Typ. $R_{DS(on)}$ = 77 mΩ
- Ultra Low Gate Charge (Typ. Q_g = 58 nC)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)}$ = 522 pF)
- 100% Avalanche Tested
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Computing / Display Power Supplies
- Telecom / Server Power Supplies
- Industrial Power Supplies
- Lighting / Charger / Adapter

MARKING DIAGRAM



T095N65S3H	= Specific Device Code
A	= Assembly Location
YWW	= Date Code (Year and Week)
ZZ	= Assembly Lot Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

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ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise noted)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to Source Voltage		650	V
V_{GSS}	Gate to Source Voltage	DC	±30	V
		AC (f > 1 Hz)	±30	V
I_D	Drain Current	Continuous (T_C = 25°C)	30*	A
		Continuous (T_C = 100°C)	18*	
I_{DM}	Drain Current	Pulsed (Note 1)	84*	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		284	mJ
I_{AS}	Avalanche Current (Note 2)		5.5	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		2.08	mJ
dv/dt	MOSFET dv/dt		120	V/ns
	Peak Diode Recovery dv/dt (Note 3)		20	
P_D	Power Dissipation	(T_C = 25°C)	40	W
		Derate Above 25°C	0.32	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		−55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8″ from Case for 5 s		260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

*Drain current limited by maximum junction temperature.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. I_{AS} = 5.5 A, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 15 A, di/dt ≤ 200 A/μs, V_{DD} ≤ 400 V, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	3.07	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Shipping
NTPF095N65S3H	T095N65S3H	TO−220 FULLPAK (Pb-Free / Halogen Free)	1000 Units / Tube

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	650			V
		V_{GS} = 0 V, I_D = 1 mA, T_J = 150°C	700			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 10 mA, Referenced to 25°C		0.63		V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650 V, V_{GS} = 0 V			1	μA
		V_{DS} = 520 V, T_C = 125°C		1.8		
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±30 V, V_{DS} = 0 V			±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 2.8 mA	2.4		4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 15 A		77	95	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 15 A		30		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 400 V, V_{GS} = 0 V, f = 250 kHz		2833		pF
C_{oss}	Output Capacitance			43		pF
$C_{oss(eff.)}$	Effective Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		522		pF
$C_{oss(er.)}$	Energy Related Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		75		pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	V_{DS} = 400 V, I_D = 15 A, V_{GS} = 10 V (Note 4)		58		nC
Q_{gs}	Gate to Source Gate Charge			14		nC
Q_{gd}	Gate to Drain “Miller” Charge			15		nC
ESR	Equivalent Series Resistance	f = 1 MHz		1.2		Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 400 V, I_D = 15 A, V_{GS} = 10 V, R_g = 4.7 Ω (Note 4)		24		ns
t_r	Turn-On Rise Time			7.4		ns
$t_{d(off)}$	Turn-Off Delay Time			69		ns
t_f	Turn-Off Fall Time			2.4		ns
SOURCE-DRAIN DIODE CHARACTERISTICS						
I_S	Maximum Continuous Source to Drain Diode Forward Current				30	A
I_{SM}	Maximum Pulsed Source to Drain Diode Forward Current				84	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 15 A			1.2	V
t_{rr}	Reverse Recovery Time	V_{DD} = 400 V, I_{SD} = 15 A, dI_F/dt = 100 A/μs		367		ns
Q_{rr}	Reverse Recovery Charge			6.3		μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL CHARACTERISTICS (T_C = 25°C UNLESS OTHERWISE NOTED)

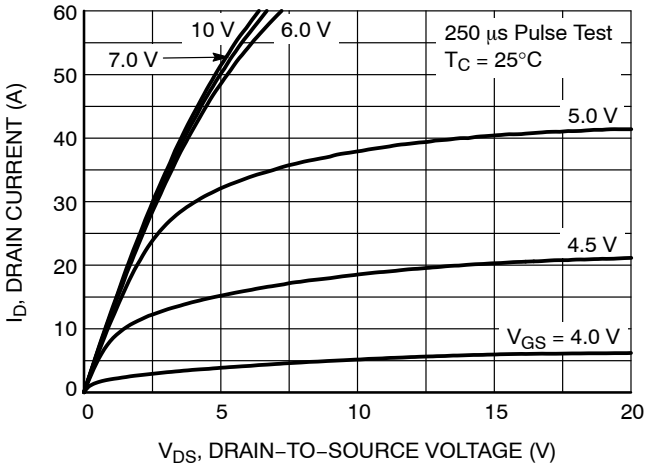

Figure 1. On−Region Characteristics

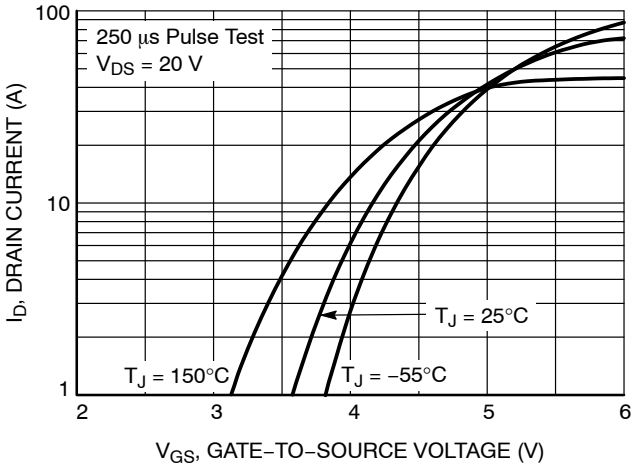

Figure 2. Transfer Characteristics

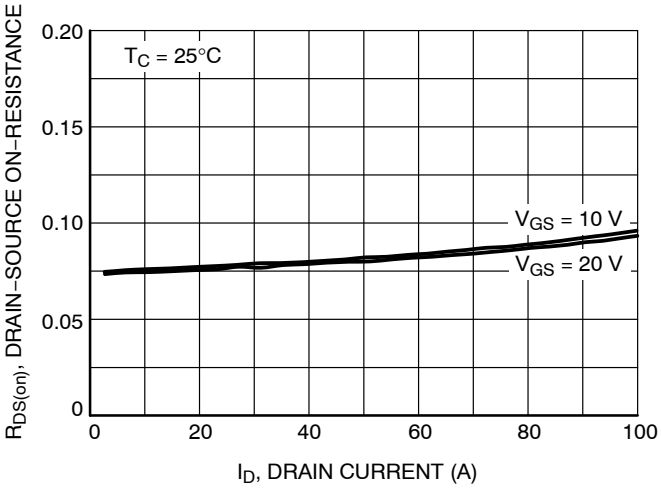

Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

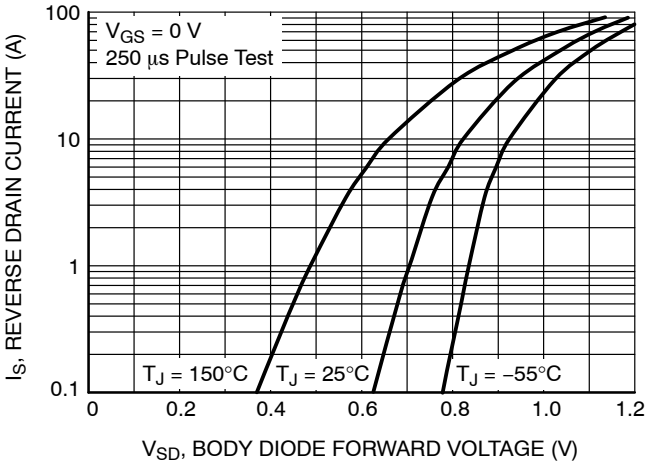

Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

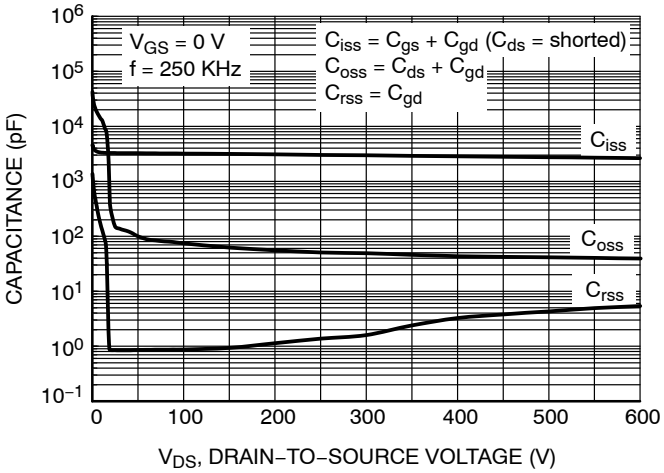

Figure 5. Capacitance Characteristics

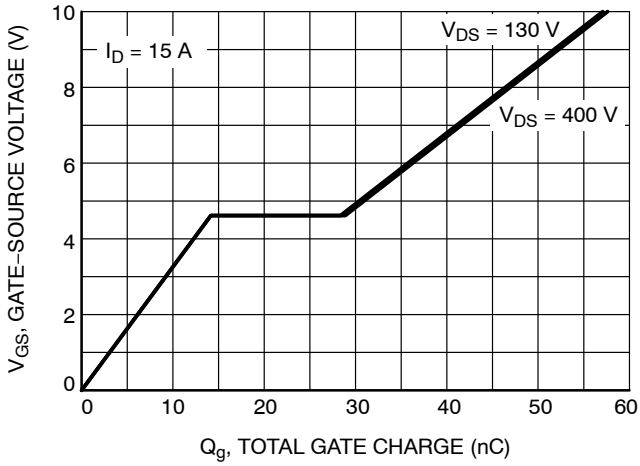

Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS (T_C = 25°C UNLESS OTHERWISE NOTED)

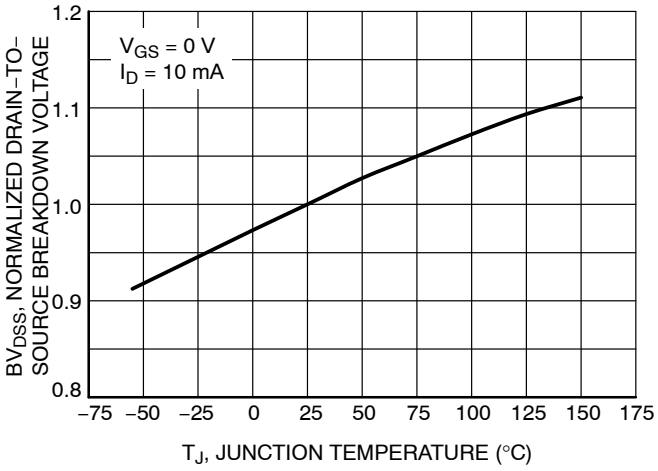

Figure 7. Breakdown Voltage Variation vs. Temperature

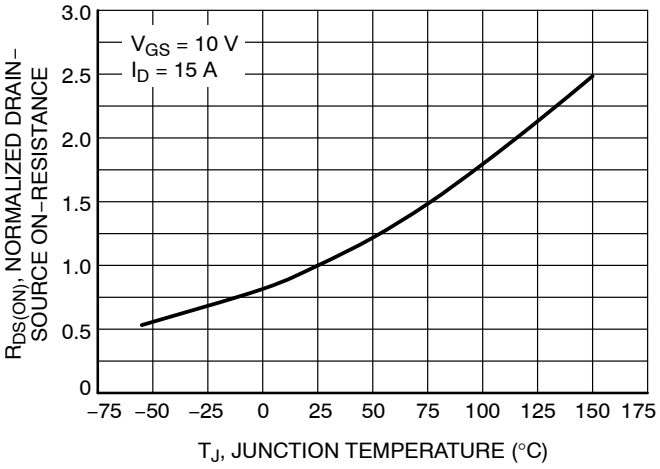

Figure 8. On−Resistance Variation vs. Temperature

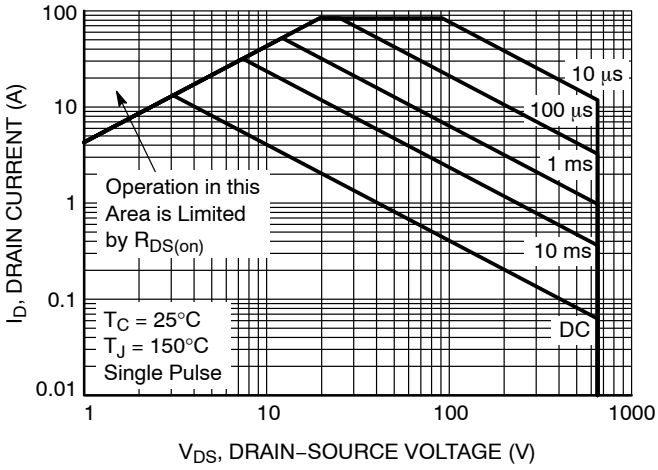

Figure 9. Maximum Safe Operating Area

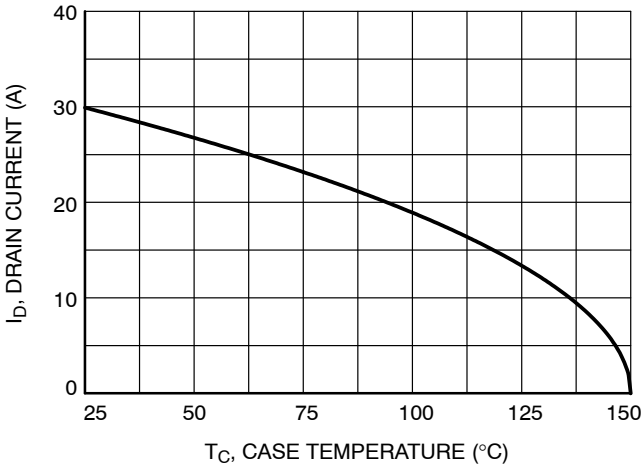

Figure 10. Maximum Drain Current vs. Case Temperature

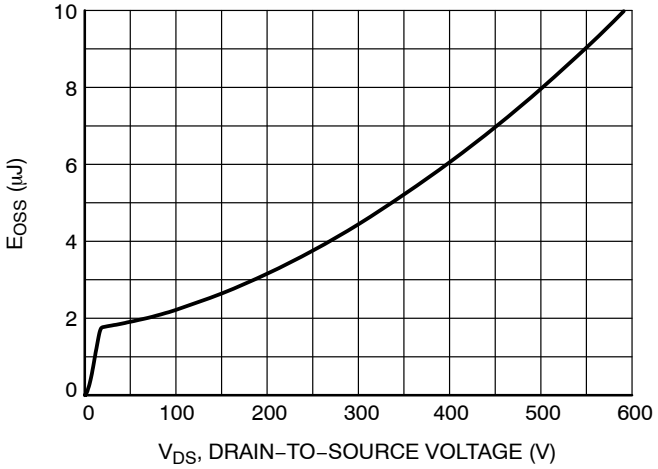

Figure 11. E_{OSS} vs. Drain to Source Voltage

TYPICAL CHARACTERISTICS (T_C = 25°C UNLESS OTHERWISE NOTED)

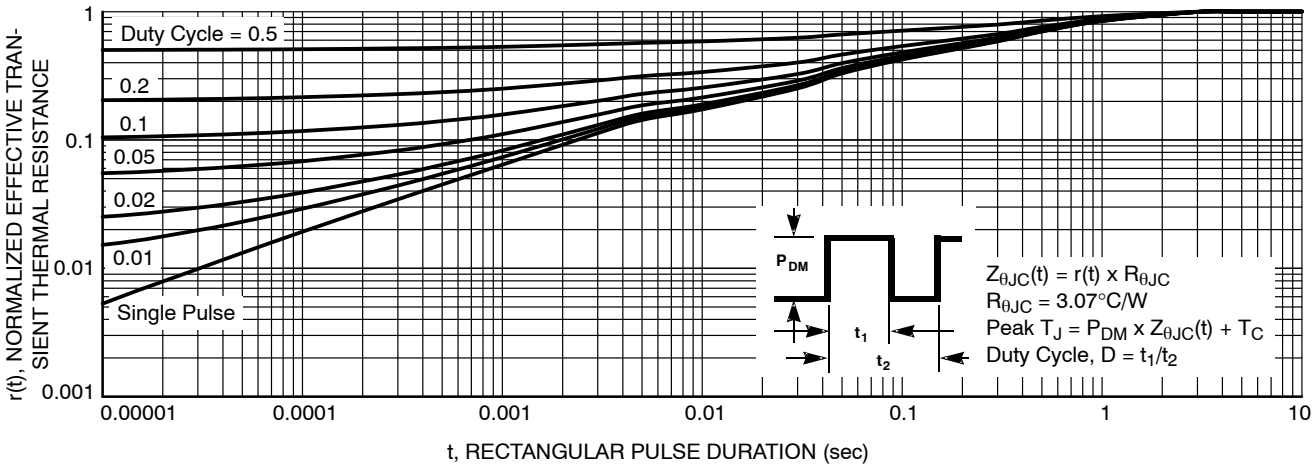

Figure 12. Transient Thermal Impedance

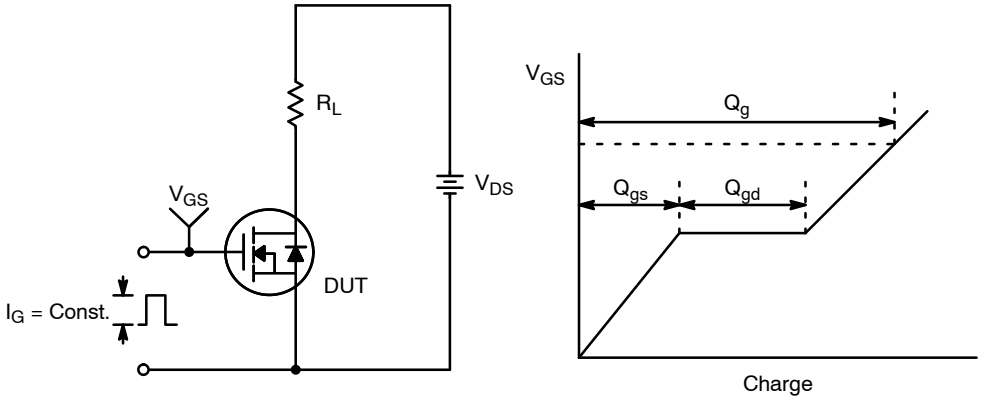

Figure 13. Gate Charge Test Circuit & Waveform

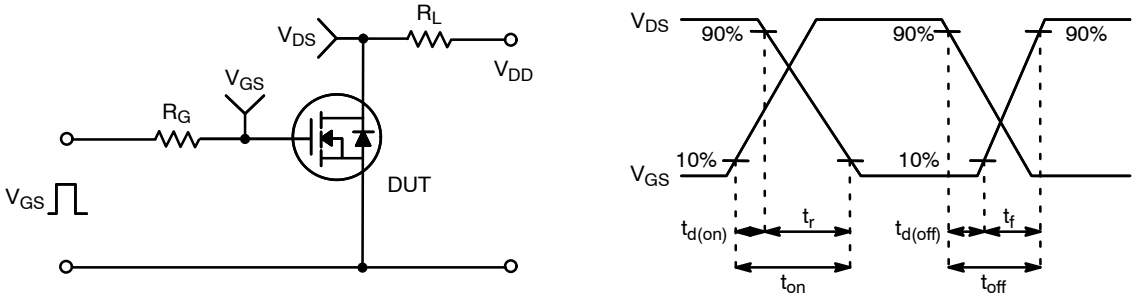

Figure 14. Resistive Switching Test Circuit & Waveforms

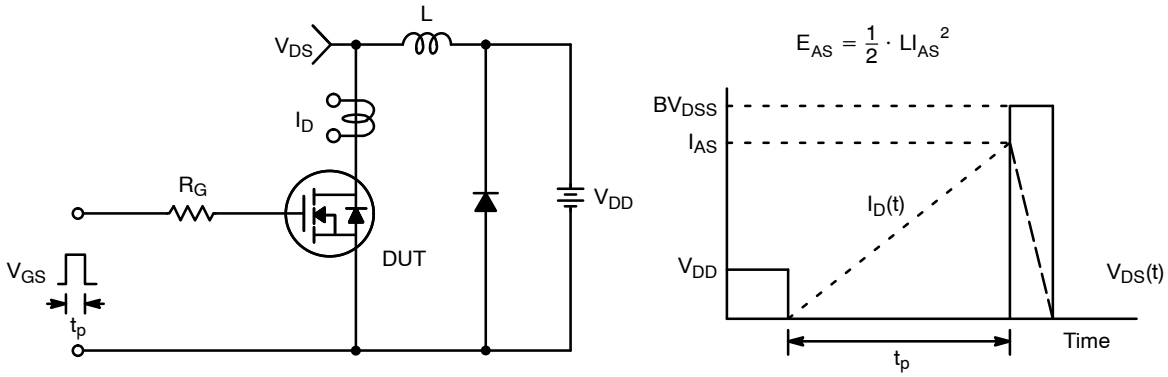

Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

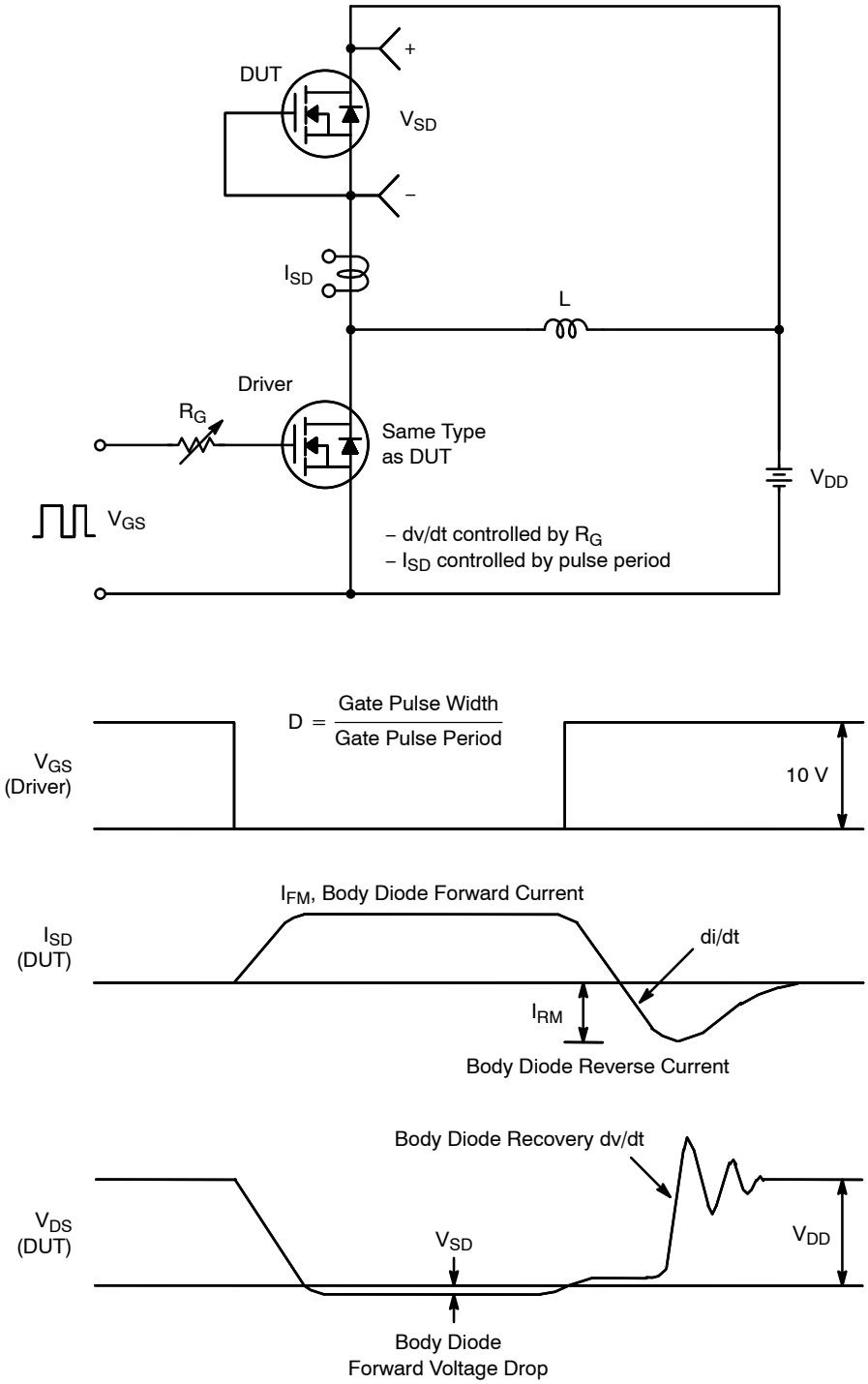

Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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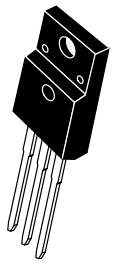
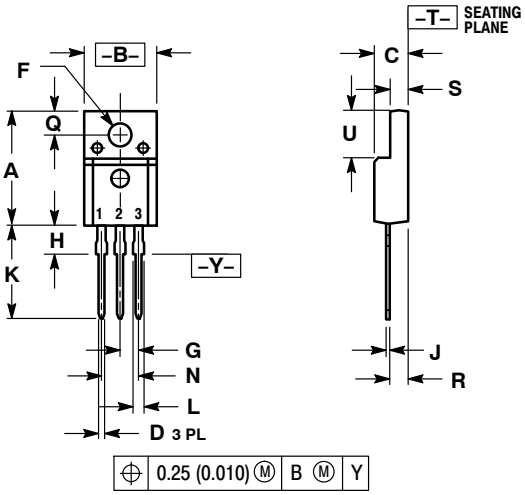


SCALE 1:1

TO−220 FULLPAK
CASE 221D−03
ISSUE K

DATE 27 FEB 2009



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH
3. 221D−01 THRU 221D−02 OBSOLETE, NEW STANDARD 221D−03.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.617	0.635	15.67	16.12
B	0.392	0.419	9.96	10.63
C	0.177	0.193	4.50	4.90
D	0.024	0.039	0.60	1.00
F	0.116	0.129	2.95	3.28
G	0.100 BSC		2.54 BSC	
H	0.118	0.135	3.00	3.43
J	0.018	0.025	0.45	0.63
K	0.503	0.541	12.78	13.73
L	0.048	0.058	1.23	1.47
N	0.200 BSC		5.08 BSC	
Q	0.122	0.138	3.10	3.50
R	0.099	0.117	2.51	2.96
S	0.092	0.113	2.34	2.87
U	0.239	0.271	6.06	6.88

STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 2:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

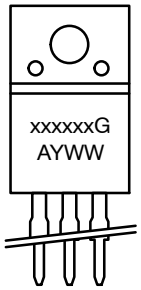
STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. CATHODE

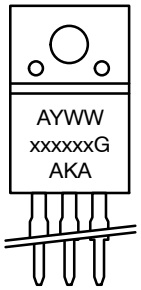
STYLE 5:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 6:
PIN 1. MT 1
2. MT 2
3. GATE

MARKING DIAGRAMS



Bipolar



Rectifier

xxxxxx	= Specific Device Code
G	= Pb−Free Package
A	= Assembly Location
Y	= Year
WW	= Work Week

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Y	= Year
WW	= Work Week
xxxxxx	= Device Code
G	= Pb−Free Package
AKA	= Polarity Designator

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