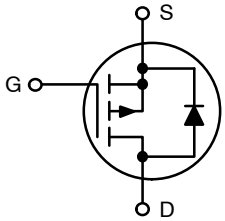
MOSFET – P-Channel, QFET®

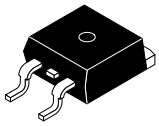
-200 V, -11.5 A, 470 mΩ

FQB12P20

V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
−200 V	0.47 Ω @ −10 V	−11.5 A



P−CHANNEL MOSFET



D²PAK−3 (TO−263, 3−LEAD)
CASE 418AJ

General Description

These P−Channel enhancement mode power field effect transistors are produced using **onsemi**'s proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on−state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switching DC/DC converters.

Features

- −11.5 A, −200 V, $R_{DS(on)}$ = 0.47 Ω @ V_{GS} = −10 V
- Low Gate Charge (Typical 31 nC)
- Low Crss (typical 30 pF)
- Fast Switching
- 100% Avalanche Tested
- Improved dv/dt Capability
- These Devices are Pb−Free and are RoHS Compliant

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

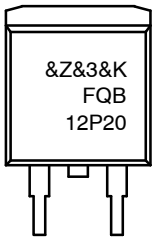
Symbol	Parameter	FQB12P20	Unit
V_{DSS}	Drain−Source Voltage	−200	V
I_D	Drain Current − Continuous (T_C = 25°C)	−11.5	A
	− Continuous (T_C = 100°C)	−7.27	A
I_{DM}	Drain Current − Pulsed (Note 1)	−46	A
V_{GSS}	Gate−Source Voltage	+30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	810	mJ
I_{AR}	Avalanche Current (Note 1)	−11.5	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	12	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	−5.5	V/ns
P_D	Power Dissipation (T_A = 25°C) *	3.13	W
	Power Dissipation (T_C = 25°C)	120	W
	− Derate above 25°C	0.96	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range	−55 to +150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

*When mounted on the minimum pad size recommended (PCB Mount)

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 9.2 mH, I_{AS} = −11.5 A, V_{DD} = −50 V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ −11.5 A, di/dt ≤ 300 A/µs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C

MARKING DIAGRAM



FQB12P20 = Specific Device Code
&Z = Assembly Plant Code
&3 = Digit Date Code
&K = Lot Run Traceability Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

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THERMAL RESISTANCE MAXIMUM RATINGS

Symbol	Parameter	Typ	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction−to−Case	–	1.04	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient *	–	40	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient	–	62.5	°C/W

*When mounted on the minimum pad size recommended (PCB Mount)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain−Source Breakdown Voltage	V_{GS} = 0 V, I_D = −250 μA	−200	–	–	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = −250 μA, Referenced to 25°C	–	–	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = −200 V, V_{GS} = 0 V	–	–	−1	μA
		V_{DS} = −160 V, T_C = 125°C	–	–	−10	μA
I_{GSSF}	Gate−Body Leakage Current, Forward	V_{GS} = −30 V, V_{DS} = 0 V	–	–	−100	nA
I_{GSSR}	Gate−Body Leakage Current, Reverse	V_{GS} = 30 V, V_{DS} = 0 V	–	–	100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = −250 μA	−3.0	–	−5.0	V
$R_{DS(on)}$	Static Drain−Source On−Resistance	V_{GS} = −10 V, I_D = −5.75 A	–	0.36	0.47	Ω
g_{FS}	Forward Transconductance	V_{DS} = −40 V, I_D = −5.75 A (Note 4)	–	6.4	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = −25 V, V_{GS} = 0 V, f = 1.0 MHz	–	920	1200	pF
C_{oss}	Output Capacitance		–	190	250	pF
C_{rss}	Reverse Transfer Capacitance		–	30	40	pF
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = −100 V, I_D = −11.5 A, R_G = 25 Ω (Note 4, 5)	–	20	50	ns
t_r	Turn−On Rise Time		–	195	400	ns
$t_{d(off)}$	Turn−Off Delay Time		–	40	90	ns
t_f	Turn−Off Fall Time		–	60	130	ns
Q_g	Total Gate Charge	V_{DS} = −160 V, I_D = −11.5 A, V_{GS} = −10 V (Note 4, 5)	–	31	40	nC
Q_{gs}	Gate−Source Charge		–	8.1	–	nC
Qg_d	Gate−Drain Charge		–	16	–	nC
DRAIN−SOURCE DIODE CHARACTERISTICS AND MAXIMUMUM RATINGS						
I_S	Maximum Continuous Drain−Source Diode Forward Current		–	–	−11.5	A
I_{SM}	Maximum Pulsed Drain−Source Diode Forward Current		–	–	−46	A
V_{SD}	Drain−Source Diode Forward Voltage	V_{GS} = 0 V, I_S = −11.5 A	–	–	−5.0	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = −11.5 A, dI_F / dt = 100 A/μs (Note 4)	–	180	–	ns
Q_{rr}	Reverse Recovery Charge		–	1.44	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse width ≤ 300 μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

TYPICAL CHARACTERISTICS

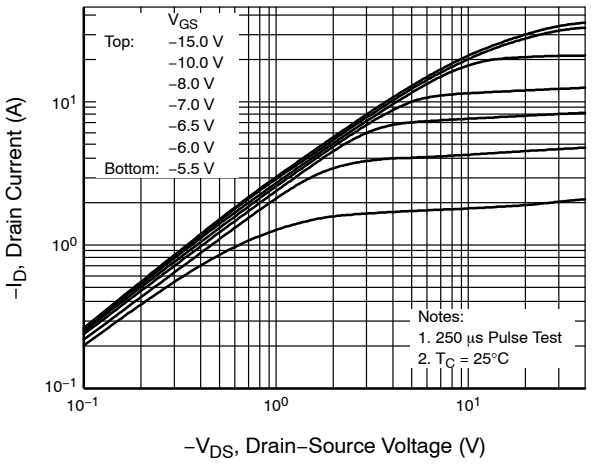

Figure 1. On Characteristics

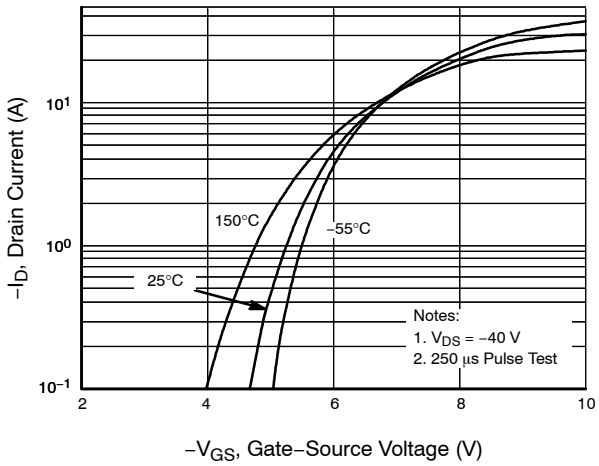

Figure 2. Transfer Characteristics

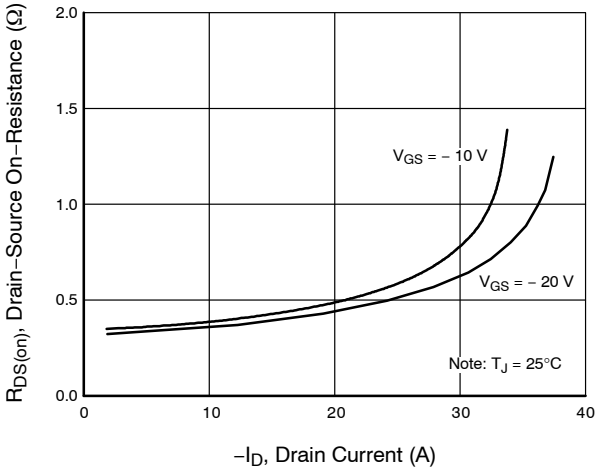

Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

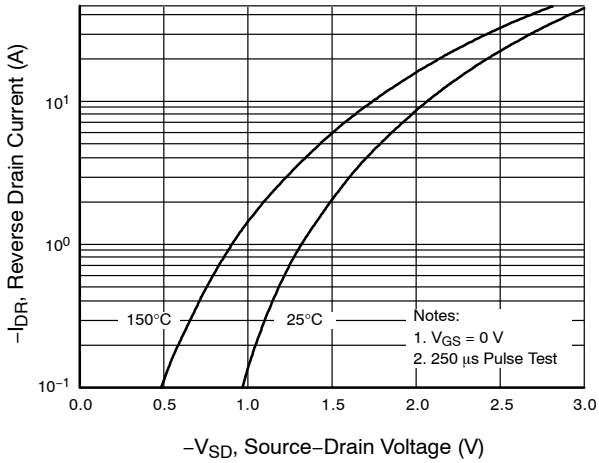

Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

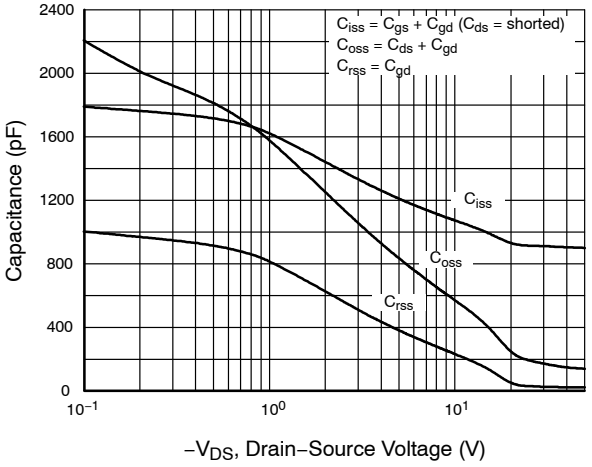

Figure 5. Capacitance Characteristics

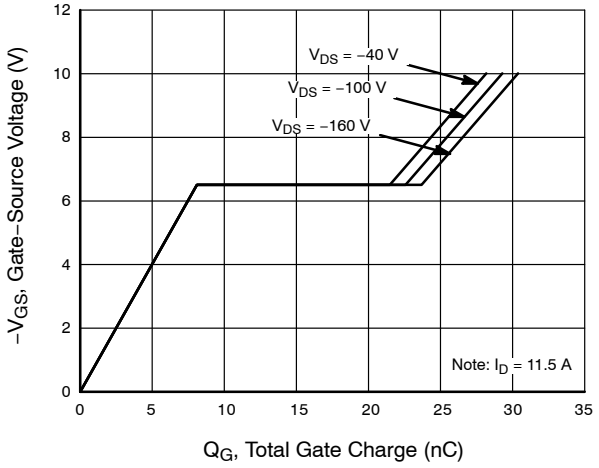

Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS (continued)

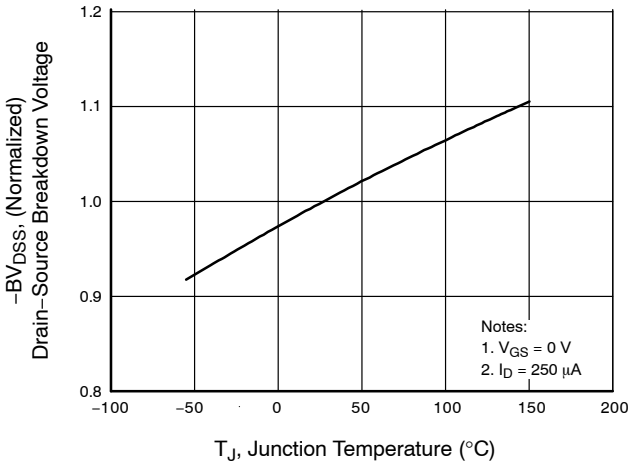

Figure 7. Breakdown Voltage Variation vs. Temperature

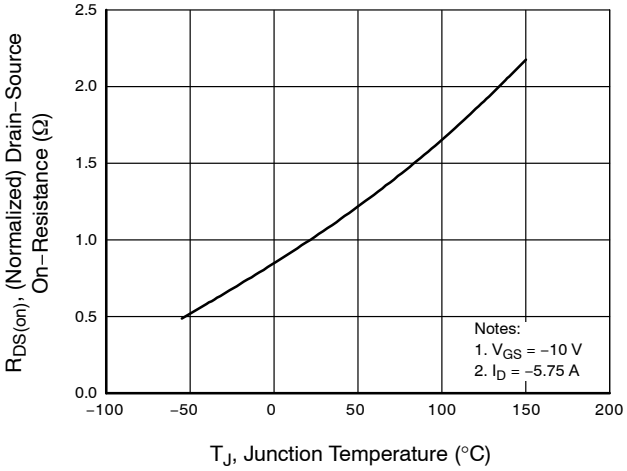

Figure 8. On–Resistance Variation vs. Temperature

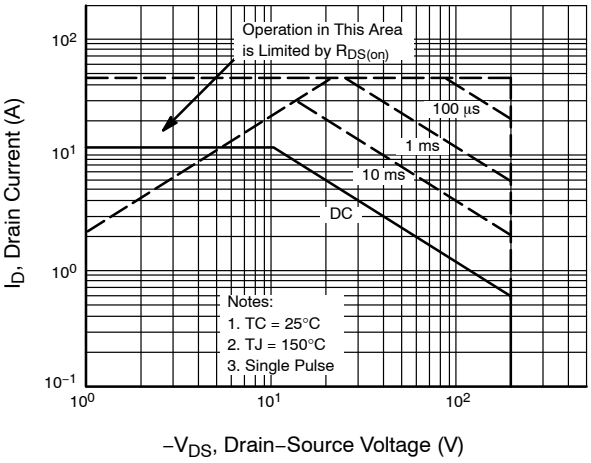

Figure 9. Maximum Safe Operating Area

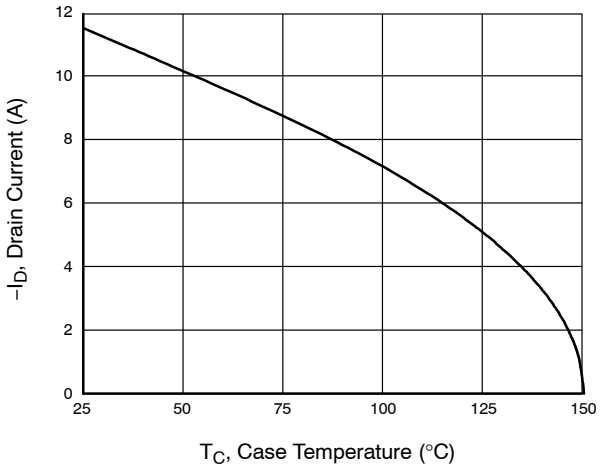

Figure 10. Maximum Drain Current vs. Case Temperature

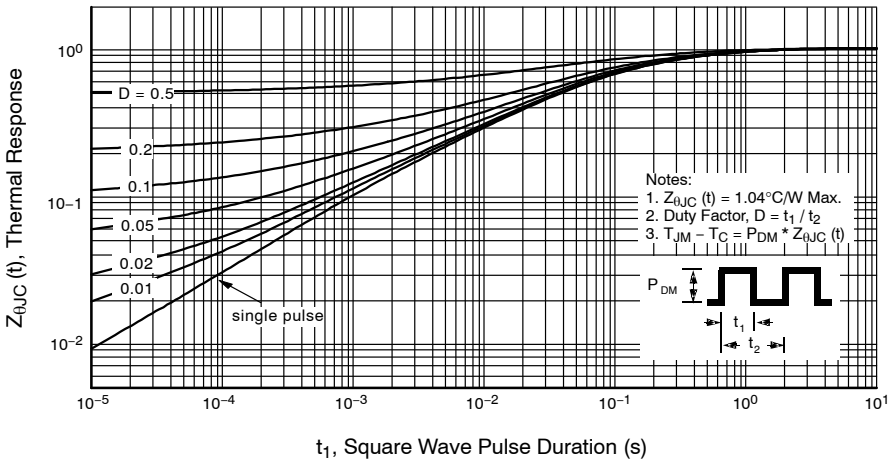

Figure 11. Capacitance Characteristics

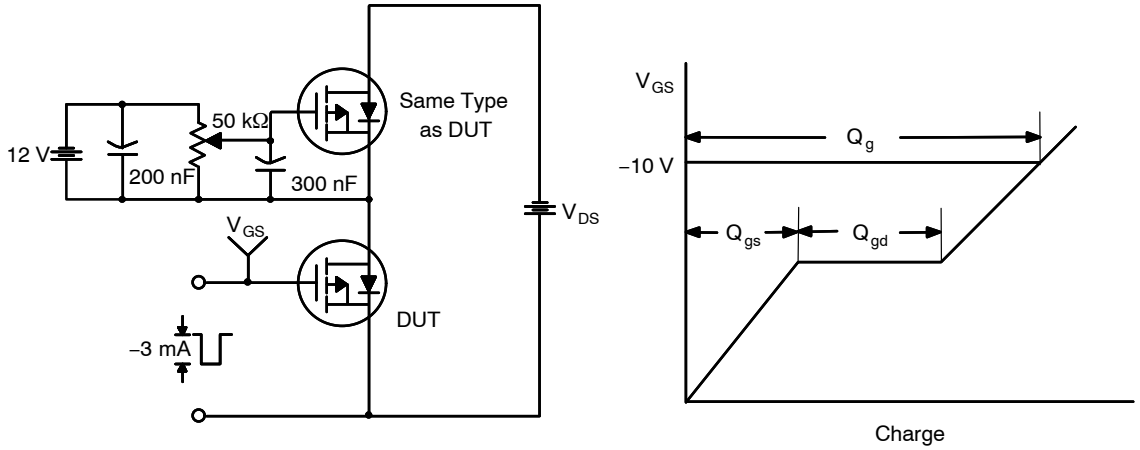

Figure 12. Gate Charge Test Circuit & Waveform

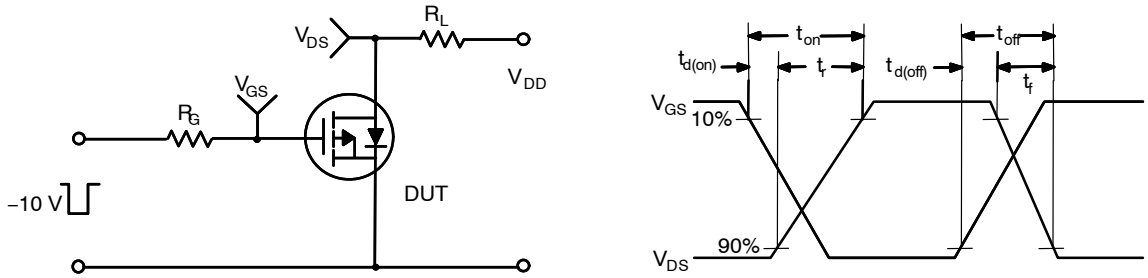

Figure 13. Resistive Switching Test Circuit & Waveforms

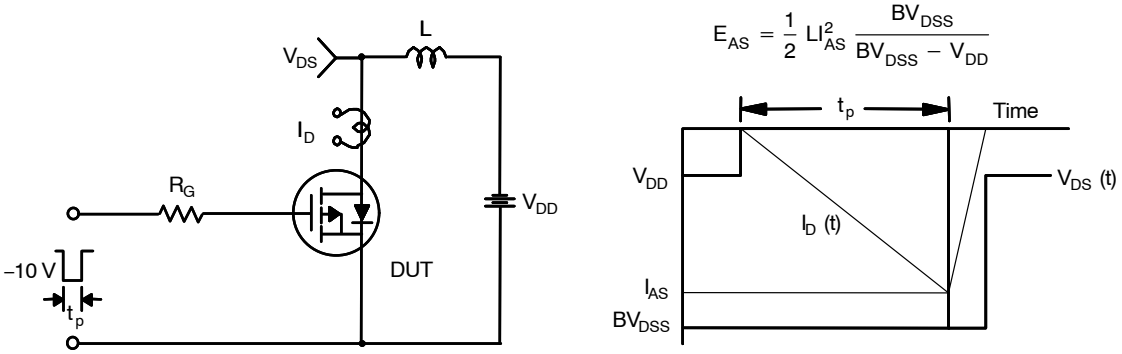

Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

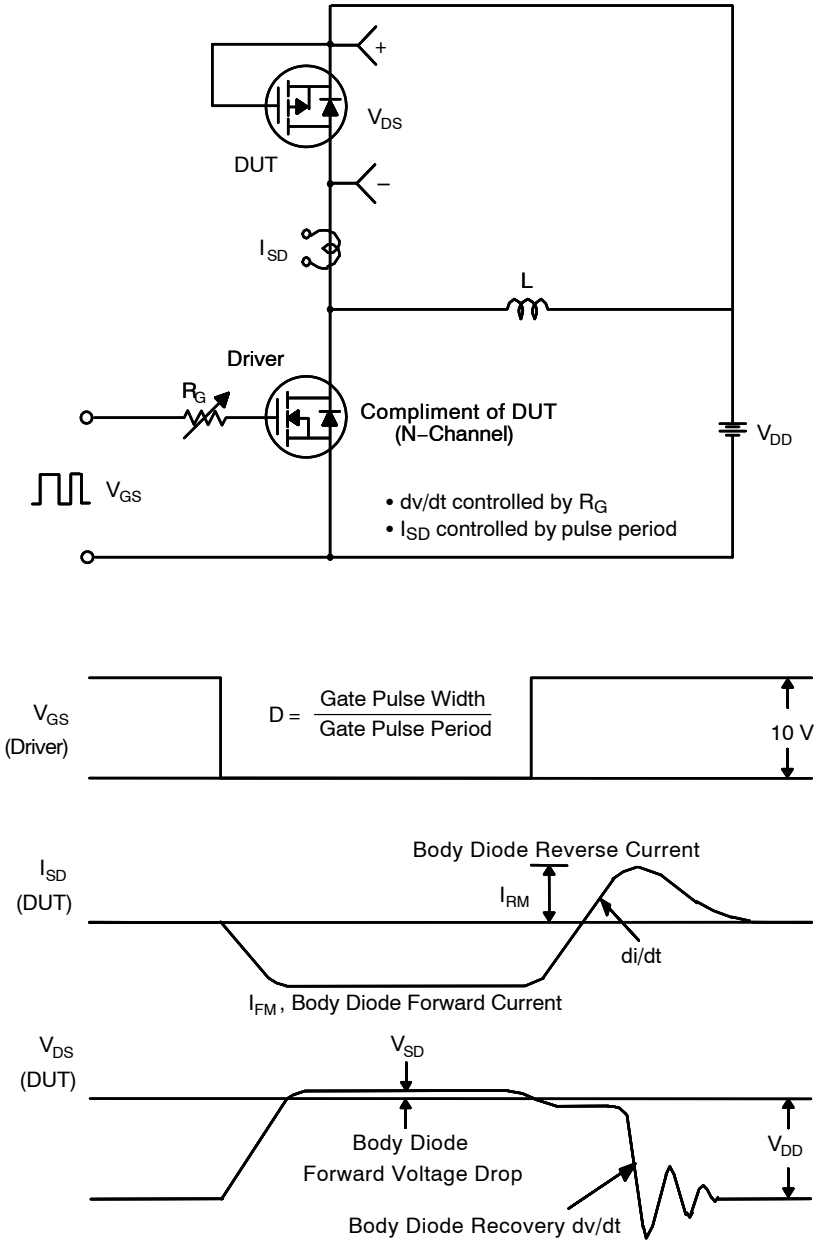

Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

PACKAGE MARKING AND ORDERING INFORMATION

Device	Marking	Package	Reel Size	Tape Width	Shipping†
FQB12P20TM	FQB12P20	D^2PAK (Pb–Free)	330 mm	24 mm	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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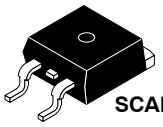
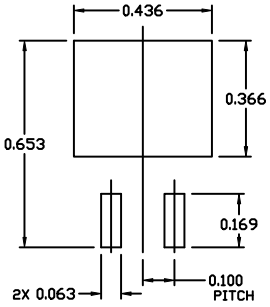


SCALE 1:1

D²PAK–3 (TO–263, 3–LEAD)

CASE 418AJ
ISSUE F

DATE 11 MAR 2021



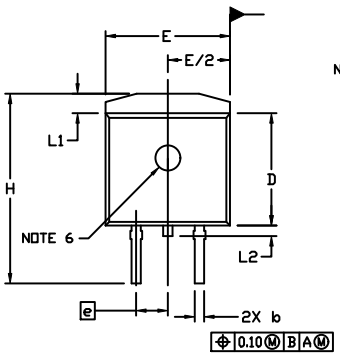
RECOMMENDED
MOUNTING FOOTPRINT

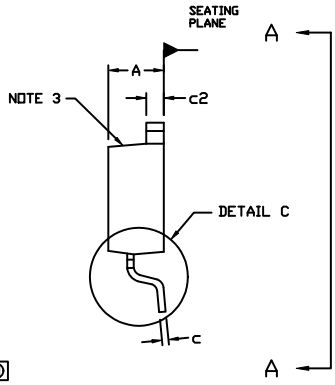
* For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

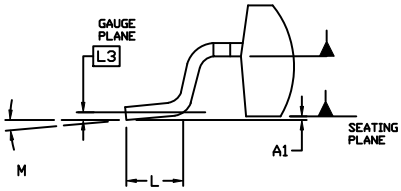
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. CHAMFER OPTIONAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
5. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1.
6. OPTIONAL MOLD FEATURE.
7. ①, ② ... OPTIONAL CONSTRUCTION FEATURE CALL OUTS.

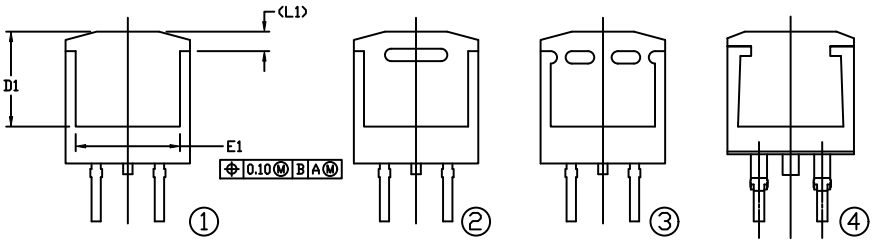
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.
A	0.160	0.190	4.06	4.83
A1	0.000	0.010	0.00	0.25
b	0.020	0.039	0.51	0.99
c	0.012	0.029	0.30	0.74
c2	0.045	0.065	1.14	1.65
D	0.330	0.380	8.38	9.65
D1	0.260	---	6.60	---
E	0.380	0.420	9.65	10.67
E1	0.245	---	6.22	---
e	0.100 BSC		2.54 BSC	
H	0.575	0.625	14.60	15.88
L	0.070	0.110	1.78	2.79
L1	---	0.066	---	1.68
L2	---	0.070	---	1.78
L3	0.010 BSC		0.25 BSC	
M	0°	8°	0°	8°







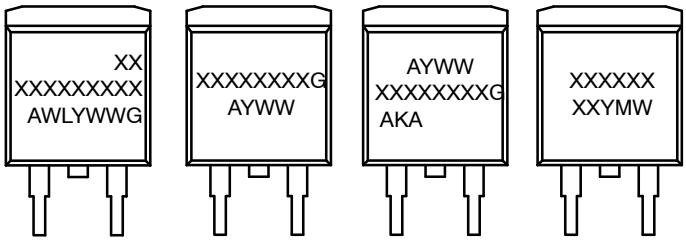
DETAIL C
TIP LEADFORM
ROTATED 90° CW



VIEW A–A

VIEW A–A
OPTIONAL CONSTRUCTIONS

GENERIC MARKING DIAGRAMS*



IC | Standard | Rectifier | SSG

XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
W = Week Code (SSG)
M = Month Code (SSG)
G = Pb–Free Package
AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot " ▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	D²PAK–3 (TO–263, 3–LEAD)	PAGE 1 OF 1

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