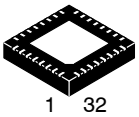
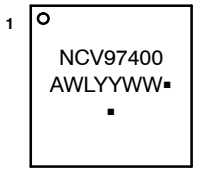
Automotive Multi-Output Power Management IC (PMIC) for Safety Applications

NCV97400



QFNW32
CASE 484AB

MARKING DIAGRAM



NCV97400 = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NCV97400MW00R2G	QFNW32 (Pb−Free)	5,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Description

The NCV97400 is a 4−output monolithic regulator consisting of 3 buck regulators and 1 boost regulator with supervisory functions including window voltage monitoring on all outputs and a window watchdog timer. This product is ideal for ADAS (Advanced Driver Assistance Systems) applications and utilizes an independent voltage reference and an adjustable independent oscillator to realize the supervisory features.

A 40 V non−synchronous buck regulator converts the battery supply voltage to a 3.3 V output, and delivers up to 3 A (peak). This output rail may be used as the input voltage for the 2 synchronous secondary buck converters and the non−synchronous secondary boost converter. Each secondary buck is adjustable and can be set from 2.5 V to 0.8 V with 2 A peak current limit and can be supplied by up to 3.6 V from a separate supply. The secondary boost output voltage is fixed and is intended to supply a low current 5.0 V rail for In−Vehicle Networking circuits (IVN).

All internal MOSFETs are N−channel devices, and bootstrap circuits are used to drive high side MOSFETs. All 4 SMPS outputs use peak current mode control with internal slope compensation. The IC incorporates an internal regulator that supplies charge to the low−voltage gate drivers.

The NCV97400 is a functional safety solution that reduces the time required to develop safety systems that comply with the International Standards Organization (ISO) 26262. The device includes a range of integrated safety features such as dedicated feedback references, output voltage monitoring, and window watchdog timer.

Features Voltage Options

- 3 Enabled Buck Converters
- 1 Boost Converter for IVN Supply
- Wide Input of 4.1 to 40 V with Undervoltage Lockout (UVLO)
- Fixed, 2 MHz Base Switching Frequency
- Pseudo−random Spread Spectrum for Improved EMI
- Window Watchdog with Independent References
- Cycle−by−cycle Current Limit Protection
- External Frequency Synchronization
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- QFN Package with Wettable Flanks (pin edge plating)
- This Device is Pb−Free and Halide Free

Typical Applications

- Safety Applications
- ADAS (Advanced Driver Assistance Systems)
- Body Electronics
- Telematics

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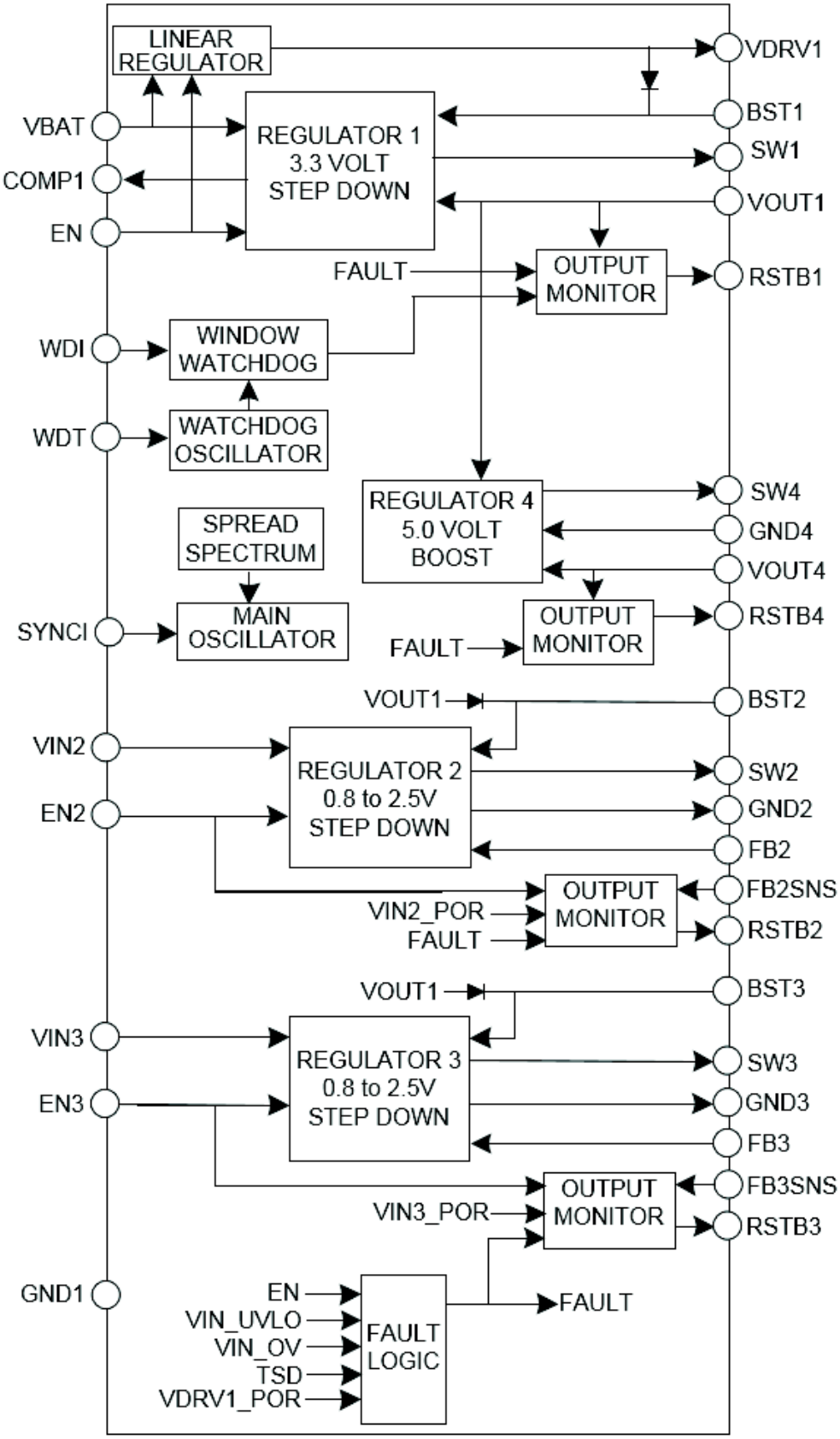

Figure 1. NCV97400 Block Diagram

TYPICAL APPLICATION

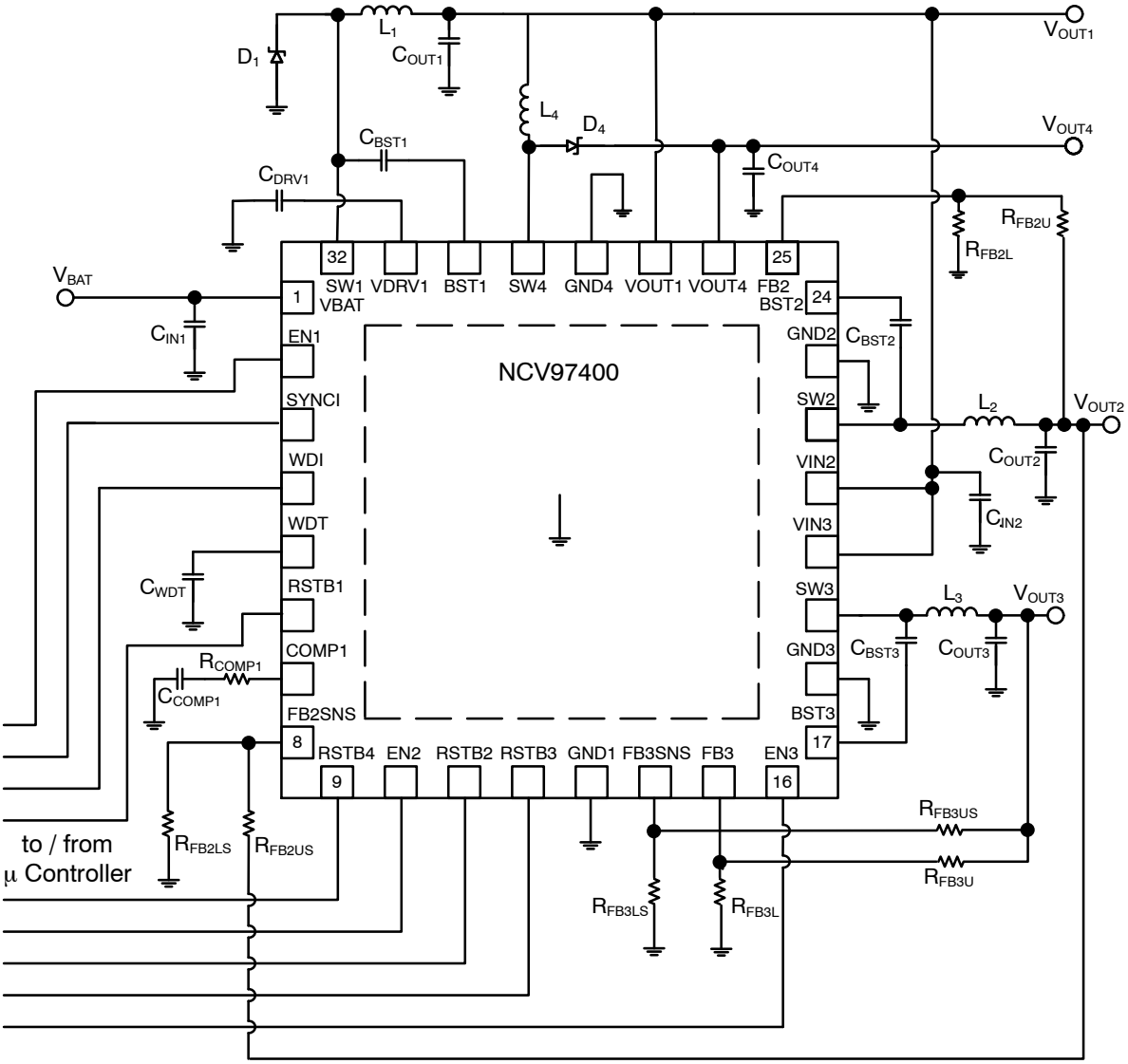

Figure 2. NCV97400 Typical Application

Table 1. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Min/Max Voltage VBAT		−0.3 to 40	V
Max Voltage VBAT to SW1		45	V
Min/Max Voltage SW1		−0.7 to 40	V
Min Voltage SW1, SW2, SW3 − 20 ns		−3.0	V
Min/Max Voltage BST1, EN		−0.3 to 40	V
Min/Max Voltage BST2 BST3, SW4		−0.3 to 7.2	V
Min/Max Voltage on EN2, EN3, WDI, SYNCI, SW2, SW3, VOUT4, RSTB1, RSTB2, RSTB3, RSTB4		−0.3 to 6	V
Max Voltage BST1 to SW1, BST2 to SW2, BST3 to SW3		3.6	V
Min/Max Voltage VIN2, VIN3, FB2, FB3, FB2SNS, FB3SNS, VDRV1, COMP1, WDT, VOUT1		−0.3 to 3.6	V
Thermal Resistance, 5x5 QFN Junction−to−Ambient (Note 1)	$R_{\theta JA}$	25	°C/W
Storage Temperature range		−55 to +150	°C
Operating Junction Temperature Range	T_J	−40 to +150	°C
ESD withstand Voltage Human Body Model	V_{ESD}	2.0	kV
Moisture Sensitivity	MSL	Level 1	
Peak Reflow Soldering Temperature		260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Mounted on 1 sq. in. of a 4−layer PCB with 1 oz. copper thickness.

Table 2. PIN FUNCTION DESCRIPTIONS

Pin No.	Symbol	Description
1	VBAT	Input voltage from battery. Place an input filter capacitor in close proximity to this pin.
2	EN	High−voltage (battery), TTL−compatible, master enable signal. Grounding this input stops all outputs and reduces Iq to a minimum (shutdown mode).
3	SYNCI	Synchronization input. Connecting an external clock to the SYNCI pin synchronizes switching to the rising edge of the SYNCI voltage. If unused, the SYNCI pin should be grounded.
4	WDI	CMOS compatible Watchdog pulse input from a CPU. To be valid, the time between rising edges of this signal must be within the watchdog window time.
5	WDT	Watchdog delay programming. Connect a capacitor between this pin and ground to adjust the watchdog window time.
6	RSTB1	Reset output with adjustable delay. Goes low when the switcher 1 output is out of regulation, during Thermal Shutdown, VBAT over or undervoltage or when a watchdog pulse is not received from the microcontroller.
7	COMP1	Output of the error amplifier for switcher 1
8	FB2_SNS	Feedback of switcher 2 dedicated to voltage monitoring. When not used, short to FB2 (pin 25).
9	RSTB4	Reset output with adjustable delay for switcher 4. Goes low when the output is out of regulation.
10	EN2	TTL−compatible low−voltage enable input for switcher 2. Grounding this input stops switcher 2.
11	RSTB2	Reset output with adjustable delay for switcher 2. Goes low when the output is out of regulation.
12	RSTB3	Reset output with adjustable delay for switcher 3. Goes low when the output is out of regulation.
13	GND1	Ground reference for the IC.
14	FB3_SNS	Feedback of switcher 3 dedicated to voltage monitoring. When not used, short to FB3 (pin 15).
15	FB3	Output voltage sensing for switcher 3, provides adjustability.
16	EN3	TTL−compatible low−voltage enable input for switcher 3. Grounding this input stops switcher 3.
17	BST3	Bootstrap input provides drive voltage higher than VIN3 to the high−side N−channel switch for optimum switch $R_{DS(on)}$ and highest efficiency.
18	GND3	Ground connection for the source of the low−side switch of switcher 3.
19	SW3	Switching node of the switcher 3 buck regulator. Connect the output inductor to this pin.
20	VIN3	Low Voltage Input for switcher 3. Place an input filter capacitor in close proximity to this pin. Can be connected to Pin 27 – VOUT1.
21	VIN2	Low Voltage Input for switcher 2. Place an input filter capacitor in close proximity to this pin. Can be connected to Pin 27 – VOUT1.
22	SW2	Switching node of the switcher 2 buck regulator. Connect the output inductor to this pin.
23	GND2	Ground connection for the source of the low−side switch of switcher 2.
24	BST2	Bootstrap input provides drive voltage higher than VIN2 to the high−side N−channel switch for optimum switch $R_{DS(on)}$ and highest efficiency.
25	FB2	Output voltage sensing for switcher 2, provides adjustability.
26	VOUT4	Output voltage sensing for switcher 4.
27	VOUT1	Output voltage sensing for switcher 1.
28	GND4	Ground connection for the source of the low−side switch of switcher 4.
29	SW4	Switching node of the switcher 4 boost regulator. Connect the input inductor and anode of the flyback diode to this pin.
30	BST1	Bootstrap input provides drive voltage higher than VBAT to the N−channel Power Switch for optimum switch $R_{DS(on)}$ and highest efficiency.
31	VDRV1	Internal supply voltage for driving the low−voltage internal switch. Connect a 0.1 μF to 1.0 μF capacitor from this pin to ground.
32	SW1	Switching node of the switcher 1 buck regulator. Connect the output inductor and cathode of the freewheeling diode to this pin.
Exposed Pad		Must be connected to GND1 (electrical ground) and to a low thermal resistance path to the ambient temperature environment.

Table 3. ELECTRICAL CHARACTERISTICS
(V_{BAT} = 4.5 V to 28 V, EN = EN2 = EN3 = 5 V, BSTx = SWx + 3.0 V, C_{DRV1} = 0.1 μF. Min/Max values are valid for the temperature range −40°C ≤ T_J ≤ 150°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
QUIESCENT CURRENT						
Quiescent Current, shutdown	I_{qSD}	V_{BAT} = 13.2 V, T_J = 25°C, V_{EN} = 0 V	–	5	10	μA
UNDERVOLTAGE LOCKOUT – VBAT (UVLO)						
VBAT UVLO Start Threshold	V_{UV1ST}	V_{BAT} rising	4.45	–	4.85	V
VBAT UVLO Stop Threshold	V_{UV1SP}	V_{BAT} falling	3.7	–	4.1	V
VBAT UVLO Hysteresis	V_{UV1HY}		–	0.75	–	V
ENABLE						
Logic Low	V_{ENLO}, V_{EN2LO}, V_{EN3LO}		–	–	0.8	V
Logic High	V_{ENHI}, V_{EN2HI}, V_{EN3HI}		2.0	–	–	V
Enable Pin Input Current	I_{EN}	V_{EN} = 5 V	–	15	20	μA
	I_{EN2}, I_{EN3}	V_{EN2}= V_{EN3} = 5 V	30	50	70	μA
EN Response Time	t_{EN_SW1}	time from EN high to SW1 switching	–	140	–	μs
	t_{EN_SWX}	time from end of t_{EN_SW1} to SW2, 3 & 4 ready	–	3.1	–	ms
	t_{EN_REG4}	time from EN high to VOUT4 in regulation	–	6	–	ms
EN2, EN3 Response Time	t_{ENX_SWX}	after t_{EN_SWX}, the time from EN2 to EN3 high to SW2 or SW3 switching	–	20	–	μs
Disable Response Time	t_{DISABL}	time EN Voltage must be < V_{ENLO} in order to force restart	–	2	10	μs
SOFT−START						
Soft−Start Ramp Time	t_{SS1}	from SW1 switch start to VOUT1 regulation	0.8	1.4	2.0	ms
	t_{SS2}	from the later of t_{EN_SWX} end or EN2 high to VOUT2 regulation	0.8	1.4	2.0	ms
	t_{SS3}	from the later of t_{EN_SWX} end or EN3 high to VOUT3 regulation	0.8	1.4	2.0	ms
	t_{SS4}	from the end of t_{EN_SWX} to VOUT4 regulation	1.6	2.8	4.0	ms
OUTPUT VOLTAGE						
Switcher 1 Output	V_{OUT}		3.23	3.3	3.37	V
Switchers 2 and 3 FB Pin Voltage (During Regulation)	V_{FB2R}, V_{FB3R}	OUTx connected to FBx through a 10 kΩ resistor	0.786	0.800	0.814	V
Switcher 4 Output	V_{OUT4}		4.9	5.0	5.1	V
ERROR AMPLIFIER – SWITCHER 1						
Transconductance	g_m $g_{m(HV)}$	V_{COMP} = 1.1 V 4.5 V < V_{BAT} < 18 V 20 V < V_{BAT} < 28 V	0.6 0.35	1.0 0.55	1.4 0.75	mmho
Output Resistance	R_{OUT}		–	1.4	–	MΩ
COMP Source Current Limit	I_{SOURCE}	V_{OUT} = 2.8 V, V_{COMP} = 1.1 V 4.5 V < V_{BAT} < 18 V 20 V < V_{BAT} < 28 V	50 25	75 40	100 55	μA
COMP Sink Current Limit	I_{SINK}	V_{OUT} = 3.8 V, V_{COMP} = 1.1 V 4.5 V < V_{BAT} < 18 V 20 V < V_{BAT} < 28 V	50 25	75 40	100 55	μA

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
ERROR AMPLIFIER – SWITCHER 1						
Minimum COMP Voltage	V_{CMPMIN}	V_{OUT} = 3.8 V		0.15	0.3	V
Maximum COMP Voltage	V_{CMPMAX}	V_{OUT} = 2.8 V	1.3	1.6		V
OSCILLATOR						
Base Switching Frequency – Switcher 1	f_{SW1}	4.5 < V_{BAT} < 18 V (see Spread Spectrum Section)	1.8	2.0	2.2	MHz
Switching Frequency – Switcher 1	$f_{SW1(HV)}$	20 V < V_{BAT} < 28 V	0.9	1.0	1.1	MHz
Base Switching Frequency – Switchers 2,3, & 4	f_{SW2}, f_{SW3}, f_{SW4}	(see Spread Spectrum Section)	1.8	2.0	2.2	MHz
Maximum Spread Spectrum Frequency	f_{SS-MAX}	(see Spread Spectrum Section)	–	2.60	2.85	MHz
SYNCHRONIZATION						
SYNCI Pin Input Current	I_{SYNCI}	V_{SYNCI} = 5.0 V	30	50	70	μA
SYNCI Input High Voltage	V_{SYNCIH}		2.0	–	–	V
SYNCI Input Low Voltage	V_{SYNCIL}		–	–	0.8	V
SYNCI High Pulse Width	t_{SYNCIH}	V_{SYNCI} > V_{SYNCIH}	40	–	–	ns
SYNCI Low Pulse Width	t_{SYNCIL}	V_{SYNCI} < V_{SYNCIL}	40	–	–	ns
External Synchronization Frequency	f_{SYNCI}		1.8	–	2.6	MHz
Master Reassertion Time	$t_{SYNCIMR}$	Time between last synchronized SW rising edge and first unsynchronized SW rising edge.	–	650	810	ns
VBAT OVERVOLTAGE SHUTDOWN MONITOR						
Overvoltage Stop Threshold	V_{OV1SP}	V_{BAT} rising	37	–	40	V
Overvoltage Start Threshold	V_{OV1ST}	V_{BAT} falling	34	–	–	V
Overvoltage Hysteresis	V_{OV1HY}		0.6	–	2.7	V
VBAT FREQUENCY FOLDBACK MONITOR						
Frequency Foldback Threshold	V_{FL1U} V_{FL1D}	V_{BAT} rising V_{BAT} falling	18.4 18	–	20 19.8	V
Frequency Foldback Hysteresis	V_{FL1HY}		0.2	0.3	0.4	V
SLOPE COMPENSATION						
Ramp Slope – Switcher 1 (With respect to switch current)	S_{ramp1} $S_{ramp1(HV)}$	4.5 < V_{BAT} < 18 V 20 V < V_{BAT} < 28 V	1.8 0.8	–	3.4 1.6	A/μs
Ramp Slope – Switchers 2 & 3	S_{ramp2}		1.9	–	3.7	A/μs
Ramp Slope – Switcher 4	S_{ramp4}		0.55	0.8	1.05	A/μs
POWER SWITCH – SWITCHER 1						
ON Resistance	R_{DS1ON}	V_{BST1}=V_{SW1}+3.0 V, I_{SW1}=500 mA	–	–	360	mΩ
Leakage current VBAT to SW1	I_{LKSW1}	V_{EN}=0 V, V_{SW1}=0 V, V_{BAT}=18 V	–	–	10	μA
Minimum ON Time	t_{ON1MIN}	Measured at SW1 pin	45	–	70	ns
Minimum OFF Time	$t_{OFF1MIN}$	Measured at SW1 pin	30	50	70	ns
POWER SWITCHES – SWITCHER 2						
High−Side ON Resistance	R_{HS2ON}	V_{BST2}=V_{SW2}+3.0 V, I_{SW2}=500 mA	–	–	280	mΩ
Low−Side ON Resistance	R_{LS2ON}	V_{BST2}=V_{SW2}+3.0 V, I_{SW2}=500 mA	–	–	230	mΩ
Leakage Current (high−side switch)	I_{LKSW2}	V_{EN2}=0 V, V_{SW2}=0 V, V_{IN2}=3.3 V	–	–	5	μA
Minimum ON Time	t_{ON2MIN}	Measured at SW2 pin	60	80	95	ns
Minimum OFF Time	$t_{OFF2MIN}$	Measured at SW2 pin	35	55	75	ns
Non−overlap Time			–	10	–	ns

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
POWER SWITCHES – SWITCHER 3						
High−Side ON Resistance	R_{HS3ON}	V_{BST3}=V_{SW3}+3.0 V, I_{SW3}=500 mA	–	–	280	mΩ
Low−Side ON Resistance	R_{LS3ON}	V_{BST3}=V_{SW3}+3.0 V, I_{SW3}=500 mA	–	–	230	mΩ
Leakage current (high−side switch)	I_{LKSW3}	V_{EN3}=0 V, V_{SW3}=0 V, V_{IN3}=3.3 V	–	–	5	μA
Minimum ON Time	t_{ON3MIN}	Measured at SW3 pin	60	80	95	ns
Minimum OFF Time	$t_{OFF3MIN}$	Measured at SW3 pin	35	55	75	ns
Non−overlap Time	t_{NOVLP}		–	10	–	ns
POWER SWITCH – SWITCHER 4						
ON Resistance	R_{DS4ON}	I_{SW4}=100 mA	–	–	1.0	Ω
Switch Leakage Current	I_{LKSW4}	V_{EN}=0 V, V_{SW4}=5.0 V	–	–	5	μA
Minimum ON Time	t_{ON4MIN}	Measured at SW4 pin	65	85	100	ns
Minimum OFF Time	$t_{OFF4MIN}$	Measured at SW4 pin	35	55	75	ns
PEAK CURRENT LIMITS						
Current Limit Threshold – Switcher 1	I_{LIM1}		3.9	4.4	4.9	A
Current Limit Threshold – Switcher 2	I_{LIM2}		2.6	2.9	3.2	A
Current Limit Threshold – Switcher 3	I_{LIM3}		2.6	2.9	3.2	A
Current Limit Threshold – Switcher 4	I_{LIM4}		0.72	0.9	1.08	A
SHORT CIRCUIT FREQUENCY FOLDBACK – SWITCHER 1						
Lowest Foldback Frequency Lowest Foldback Frequency – High V_{IN}	f_{SW1AF} $f_{SW1AFHV}$	V_{OUT} = 0 V, 4.5 V < V_{BAT} < 18 V V_{OUT} = 0 V, 20 V < V_{BAT} < 28 V	450 225	550 275	650 325	kHz
HICCUP MODE						
Hiccup Mode	f_{SW1HIC}	SW1 pin shorted to ground or VOUT1 VOUT1 = 0 V	24	32	40	kHz
	f_{SW2HIC}	SW2 pin shorted to ground or VOUT2	24	32	40	
	f_{SW3HIC}	SW3 pin shorted to ground or VOUT3	24	32	40	
	f_{SW4HIC}	SW4 pin connected to +3.3 V through 20 Ω. 0 V at the VOUT4 pin.	24	32	40	
Switching Reactivation Delay	t_{SW4HIC}	SW4 pin shorted to VOUT1	–	1.9	–	ms
WINDOW WATCHDOG						
Watchdog Oscillator Frequency	f_{WD}	C_{WDT} = 1000 pF C_{WDT} = 100 pF	8.2 77	10.6 100	13.0 122	kHz
First Watchdog Timeout	$t_{WD_timeout}$	Watchdog timeout after rising edge at RSTB1 C_{WDT} = 1000 pF 900 pF < C_{WDT} < 1100 pF C_{WDT} = 100 pF 90 pF < C_{WDT} < 110 pF	 2300 2070 240 221	 2840 – 300 –	 3700 4090 385 430	ms
Watchdog Window Time	t_{WD}	C_{WDT} = 1000 pF 900 pF < C_{WDT} < 1100 pF C_{WDT} = 100 pF 90 pF < C_{WDT} < 110 pF	150 138 15.9 14.7	189 – 20 –	250 273 27 28.7	ms
Watchdog Closed Window Time	t_{WD_CLS}		–	t_{WD}/4	–	ms
Watchdog Input WDI Threshold Voltage	V_{WDH} V_{WDL} V_{WD_HYS}	V_{WD} increasing V_{WI} decreasing	– 0.8 150	– – –	2.0 – 500	V V mV
Watchdog Input WDI Current	I_{WDI}	V_{WD} = 5 V	30	50	70	μA

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
RESET						
Low Voltage Reset Threshold – Switcher 1	V_{UV1FAL} V_{UV1RIS}	V_{OUT1} decreasing V_{OUT1} increasing	2.97 3.04	3.05 3.12	3.14 3.20	V
High Voltage Reset Threshold – Switcher 1	V_{OV1FAL} V_{OV1RIS}	V_{OUT1} decreasing V_{OUT1} increasing	3.40 3.47	3.48 3.55	3.56 3.63	V
Low Voltage Reset Threshold – Switcher 2 & 3 (at FBxSNS)	V_{UV2FAL} V_{UV2RIS}	FBxSNS decreasing FBxSNS increasing	0.720 0.736	0.740 0.756	0.760 0.776	V
High Voltage Reset Threshold – Switcher 2 & 3 (at FBxSNS)	V_{OV2FAL} V_{OV2RIS}	FBxSNS decreasing FBxSNS increasing	0.824 0.840	0.844 0.860	0.864 0.880	V
Low Voltage Reset Threshold – Switcher 4	V_{UV4FAL} V_{UV4RIS}	V_{OUT4} decreasing V_{OUT4} increasing	4.50 4.60	4.63 4.73	4.75 4.85	V
High Voltage Reset Threshold – Switcher 4	V_{OV4FAL} V_{OV4RIS}	V_{OUT4} decreasing V_{OUT4} increasing	5.15 5.25	5.28 5.38	5.40 5.50	V
Reset Hysteresis (ratio of VOUTx)	K_{RES_HYS}		0.5	2	–	%
Noise−Filtering Delay	t_{RES_FILT}		5	–	25	μs
Reset Delay Time	t_{RESET}	I_{RSTBx} = 1 mA I_{RSTBx} = 500 μA I_{RSTBx} = 100 μA	– 4.0 18	1.0 5.0 24	40 6.0 32	μs ms ms
Reset Output Low level	V_{RESL}	I_{RSTBx} = 1 mA	–	–	0.4	V
BOOTSTRAP VOLTAGE SUPPLY						
Output Voltage	V_{DRV1}		3.1	3.3	3.5	V
V_{DRV1} POR Start Threshold	V_{DRV1ST}		2.7	2.875	3.05	V
V_{DRV1} POR Stop Threshold	V_{DRV1SP}		2.55	2.75	2.95	V
SW2 & SW3 INPUT UNDERVOLTAGE MONITORS						
VIN2 POR Start Threshold	V_{IN2ST}		2.7	2.875	3.05	V
VIN2 POR Stop Threshold	V_{IN2SP}		2.55	2.75	2.95	V
VIN3 POR Start Threshold	V_{IN3ST}		2.7	2.875	3.05	V
VIN3 POR Stop Threshold	V_{IN3SP}		2.55	2.75	2.95	V
THERMAL SHUTDOWN						
Thermal Shutdown Activation Temperature	T_{SD}		150	–	190	°C
Hysteresis	T_{HYS}		5	–	20	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

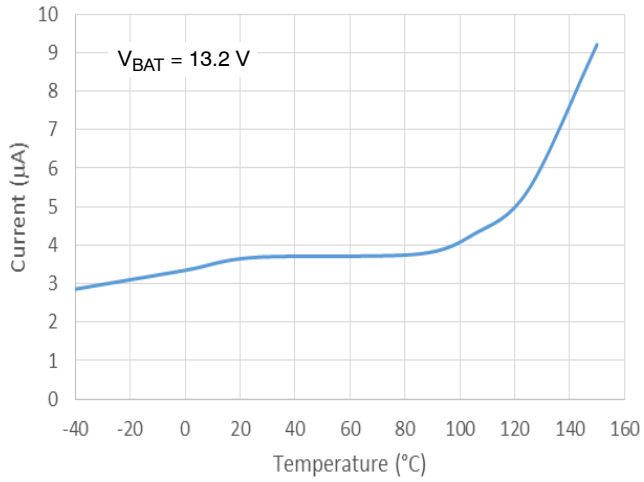


Figure 3. Shutdown V_{BAT} Quiescent Current vs. Temperature

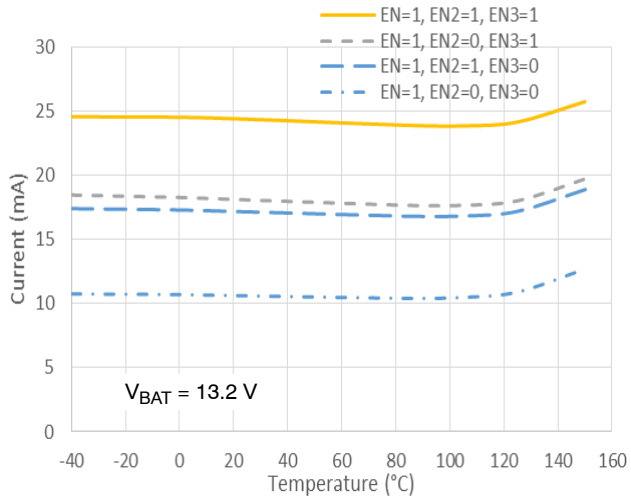


Figure 4. Operating V_{BAT} Quiescent Current vs. Temperature

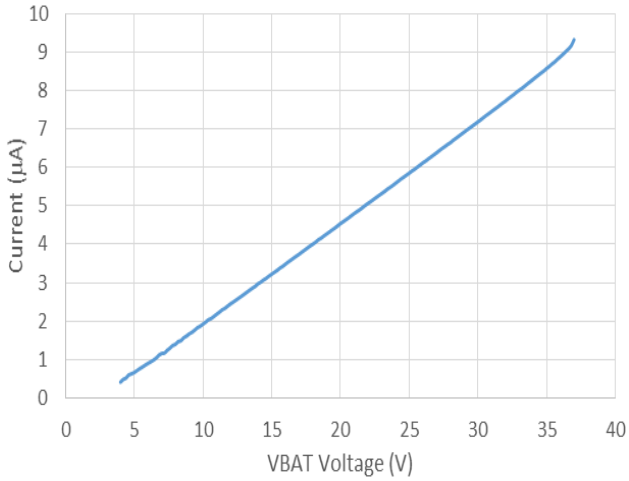


Figure 5. Shutdown V_{BAT} Quiescent Current vs. V_{BAT} Voltage

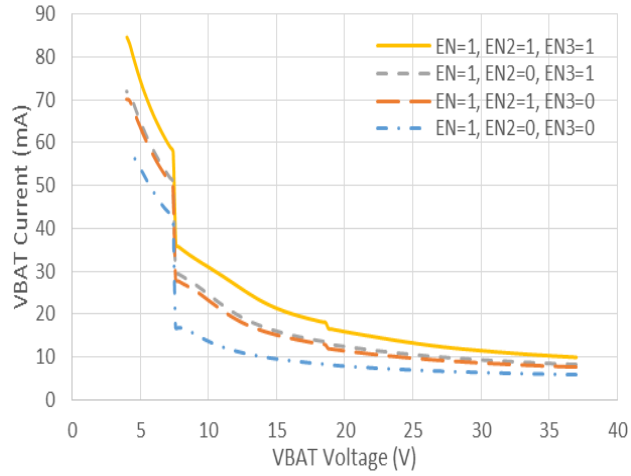


Figure 6. Operating V_{BAT} Quiescent Current vs. V_{BAT} Voltage

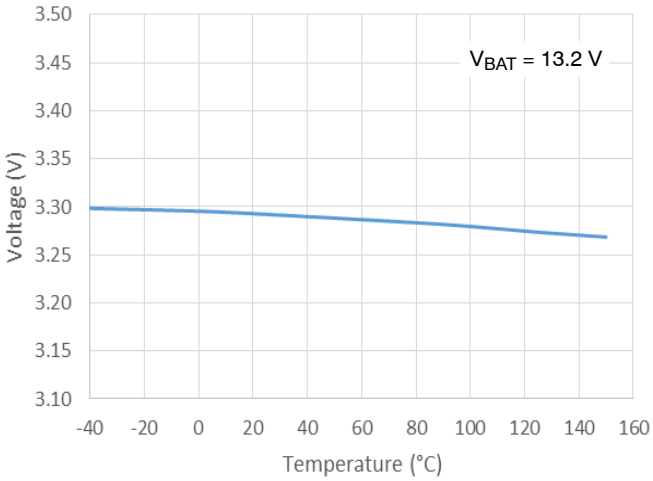


Figure 7. V_{DRV} Voltage vs. Temperature

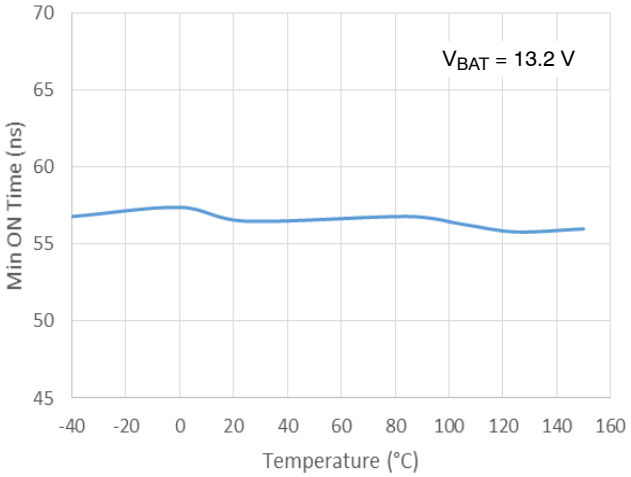


Figure 8. Switcher 1 Min ON Time vs. Temperature

TYPICAL CHARACTERISTICS

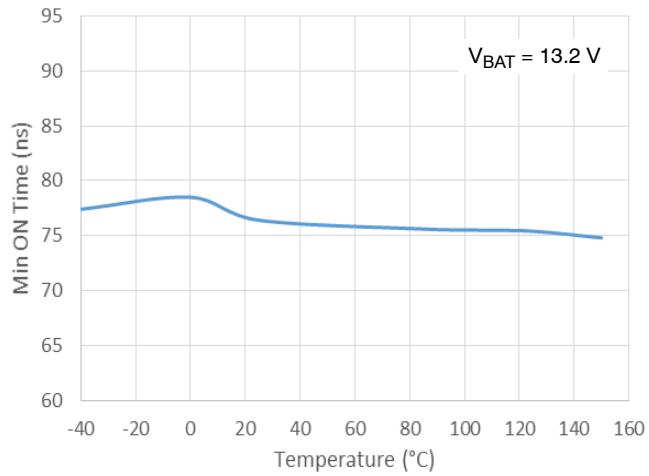


Figure 9. Switcher 2 Min ON Time vs. Temperature

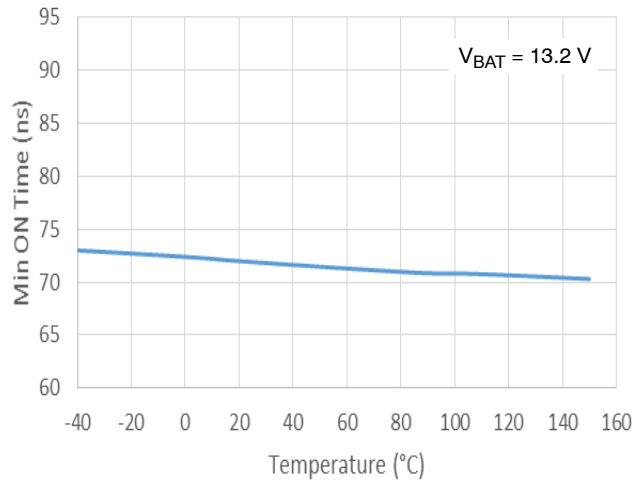


Figure 10. Switcher 3 Min ON Time vs. Temperature

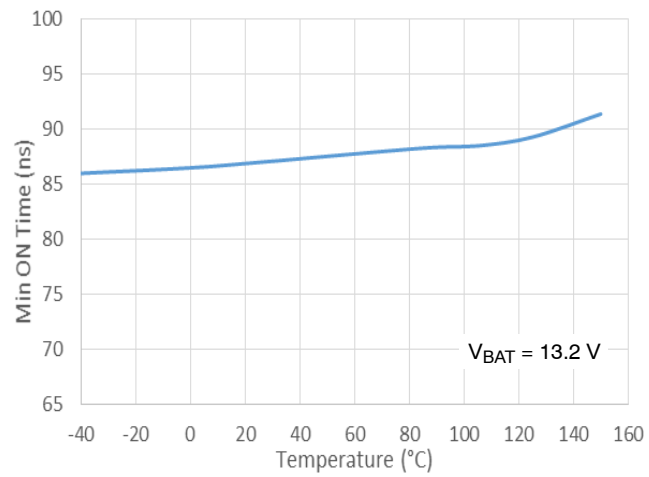


Figure 11. Switcher 4 Min ON Time vs. Temperature

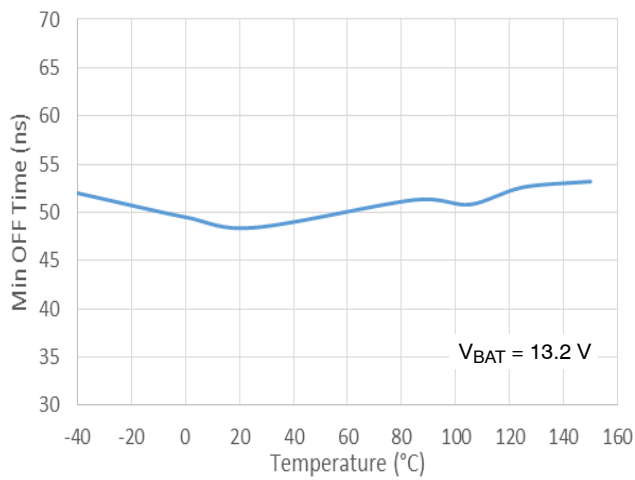


Figure 12. Switcher 1 Min OFF Time vs. Temperature

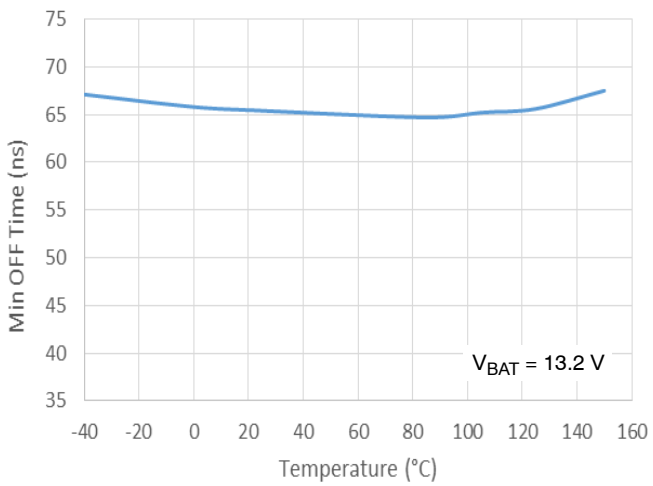


Figure 13. Switcher 2 Min OFF Time vs. Temperature

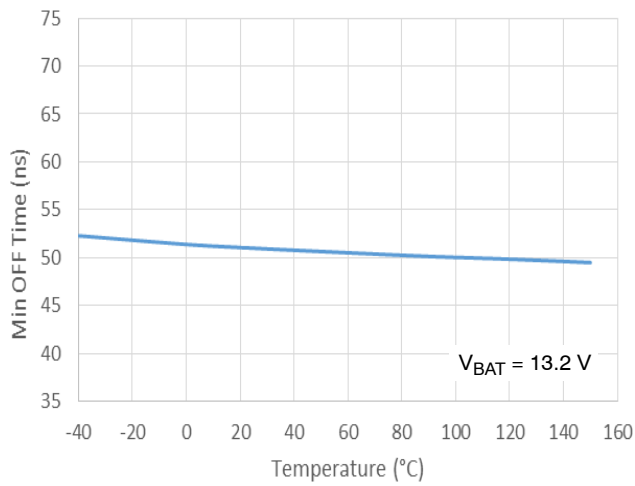


Figure 14. Switcher 3 Min OFF Time vs. Temperature

TYPICAL CHARACTERISTICS

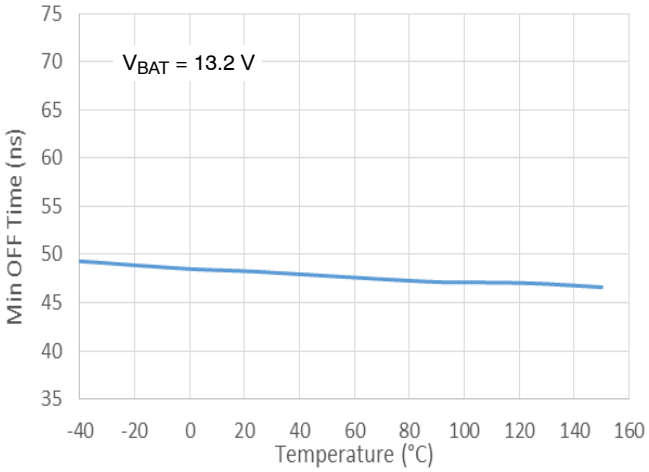


Figure 15. Switcher 4 Min OFF Time vs. Temperature

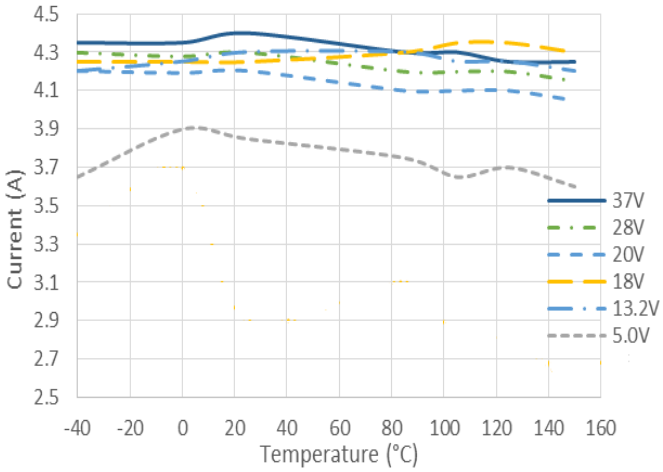


Figure 16. Switcher 1 Load Current Limit vs. Temperature

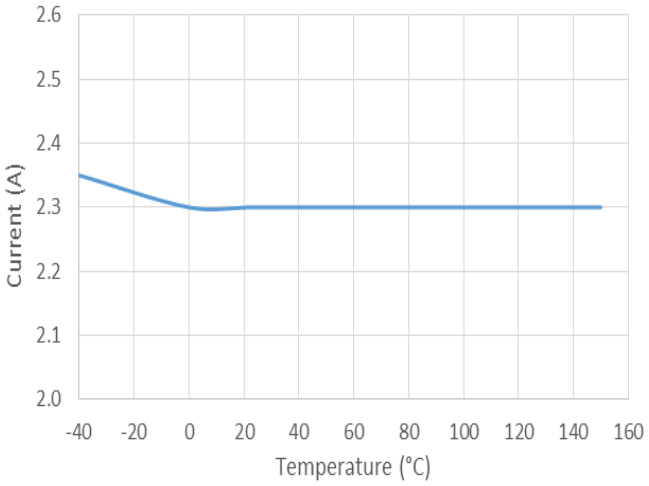


Figure 17. Switcher 2 Load Current Limit vs. Temperature – 1.8 V Output

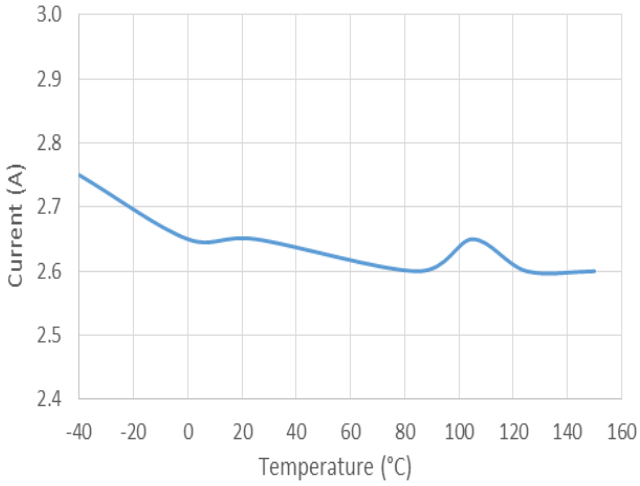


Figure 18. Switcher 3 Load Current Limit vs. Temperature – 1.2 V Output

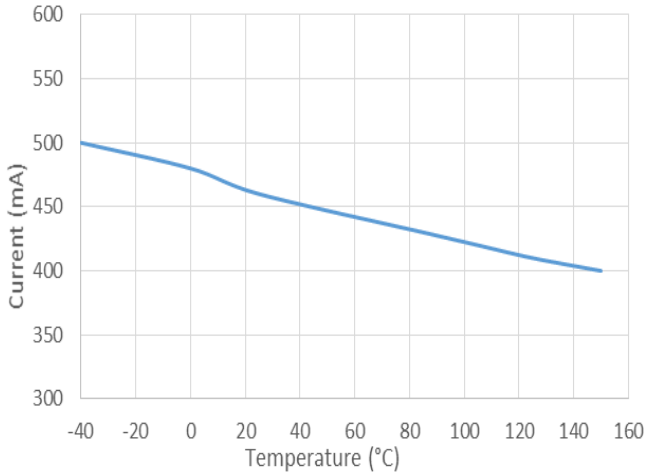


Figure 19. Switcher 4 Load Current Limit vs. Temperature

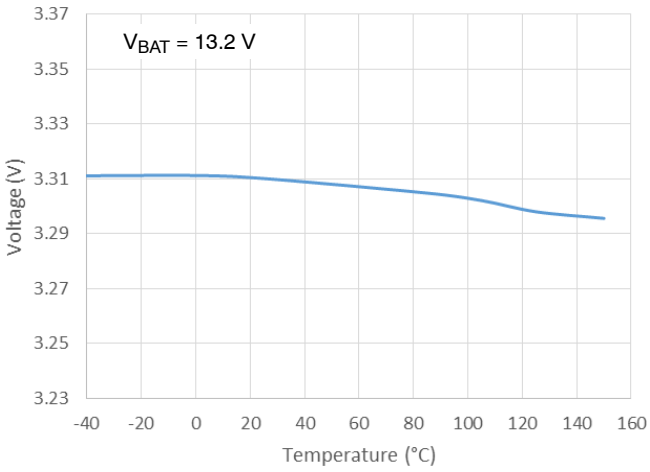


Figure 20. Switcher 1 Output Voltage vs. Temperature

TYPICAL CHARACTERISTICS

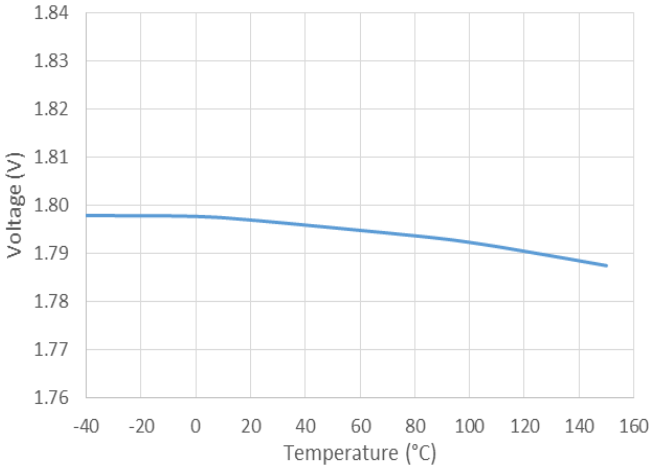


Figure 21. Switcher 2 Output Voltage vs. Temperature

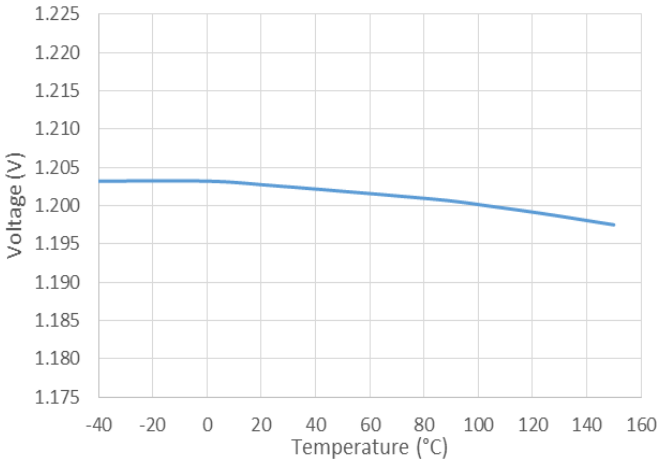


Figure 22. Switcher 3 Output Voltage vs. Temperature

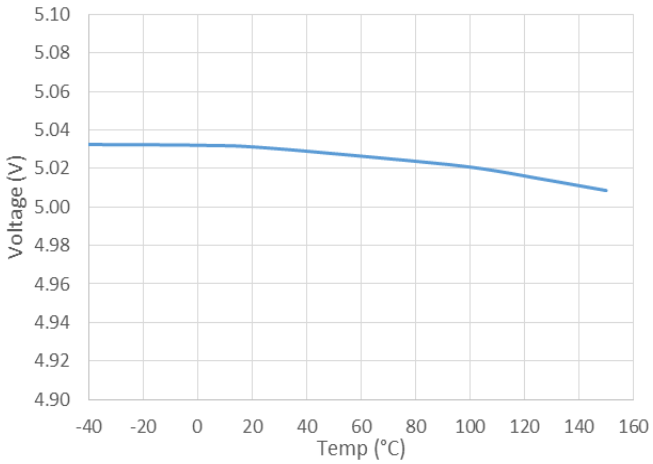


Figure 23. Switcher 4 Output Voltage vs. Temperature

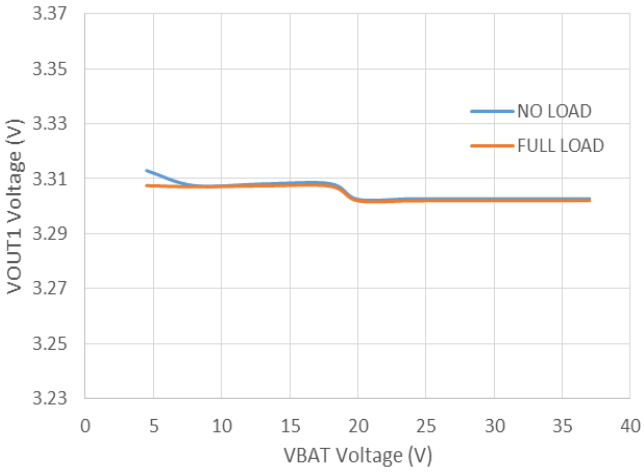


Figure 24. Switcher 1 Output Voltage vs. V_{BAT} Voltage

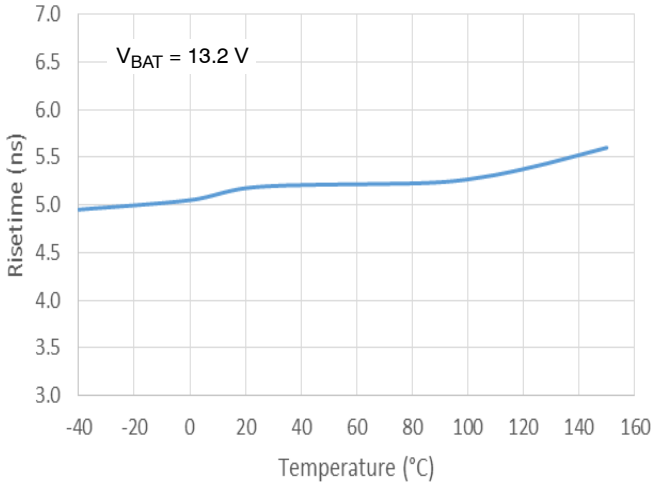


Figure 25. Switchnode 1 2.8 A Load Risetime vs. Temperature

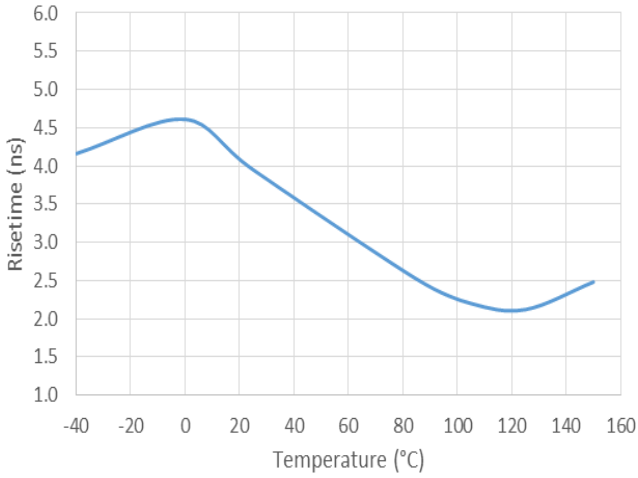


Figure 26. Switchnode 2 2.0 A Load Risetime vs. Temperature

TYPICAL CHARACTERISTICS

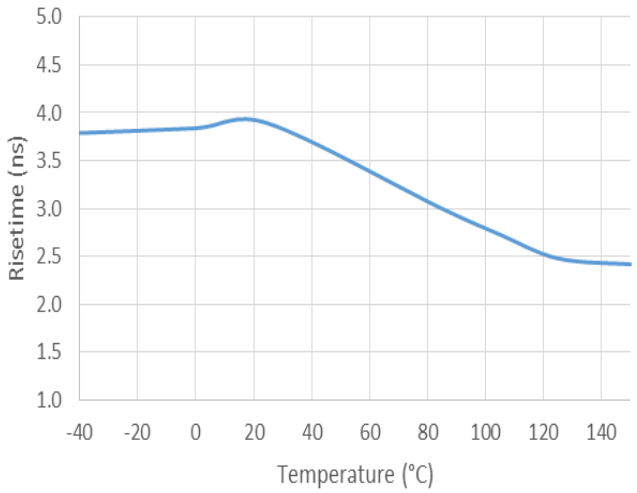


Figure 27. Switchnode 3 2.0 A Load Risetime vs. Temperature

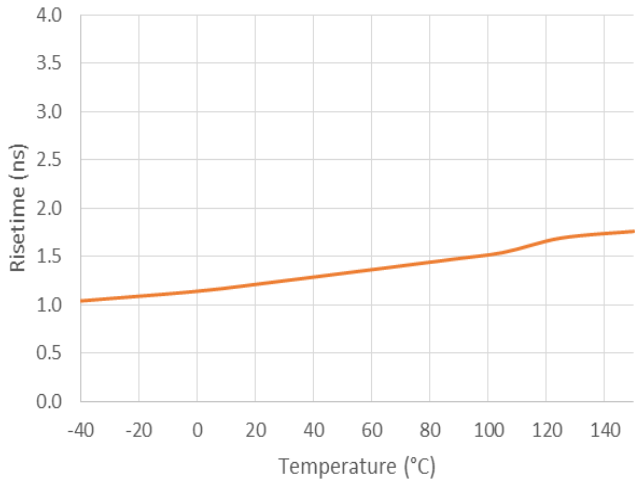


Figure 28. Switchnode 4 250 mA Load Risetime vs. Temperature

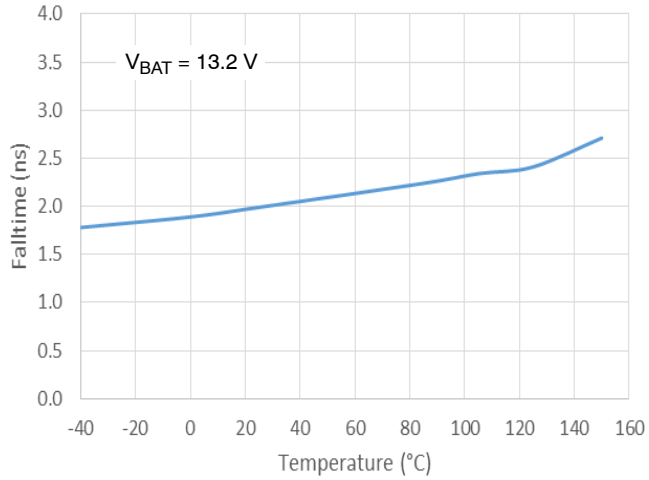


Figure 29. Switchnode 1 2.8 A Load Falltime vs. Temperature

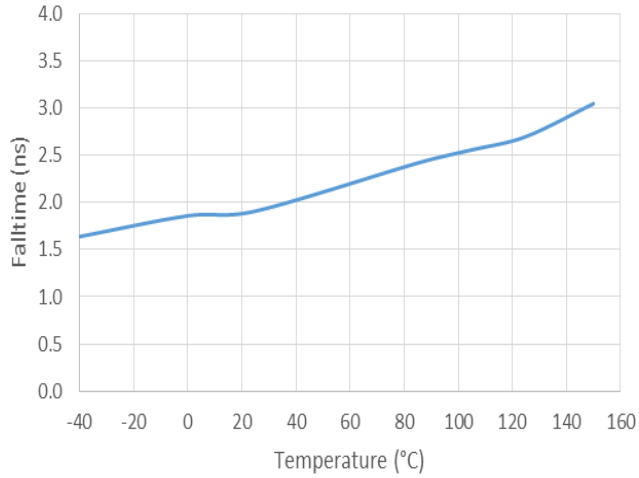


Figure 30. Switchnode 2 2.0 A Load Falltime vs. Temperature

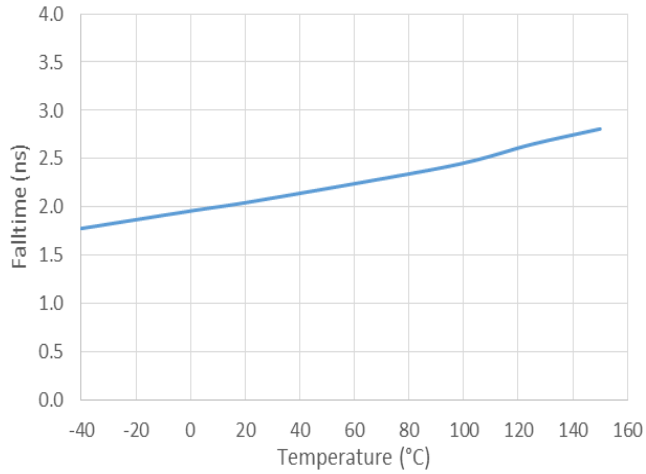


Figure 31. Switchnode 3 2.0 A Load Falltime vs. Temperature

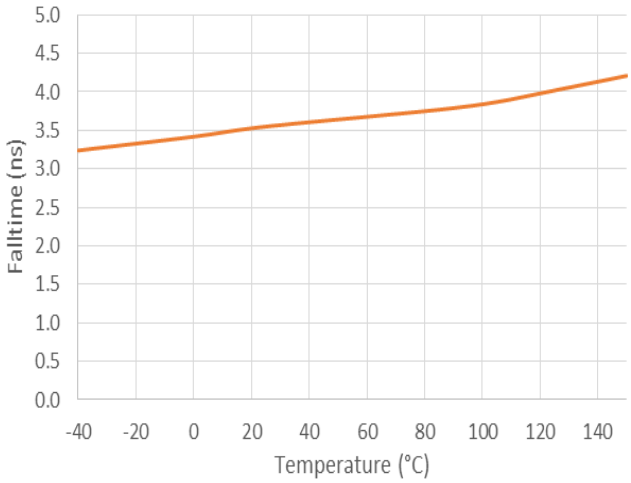


Figure 32. Switchnode 4 250 mA Load Falltime vs. Temperature

TYPICAL CHARACTERISTICS

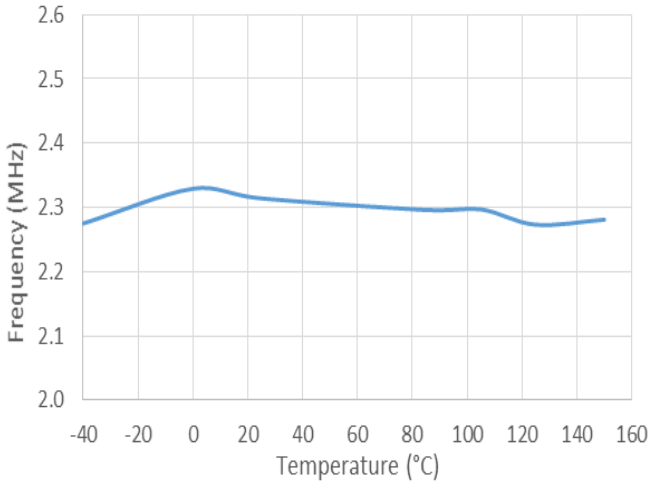


Figure 33. Switching Frequency (Spread Spectrum average) vs. Temperature

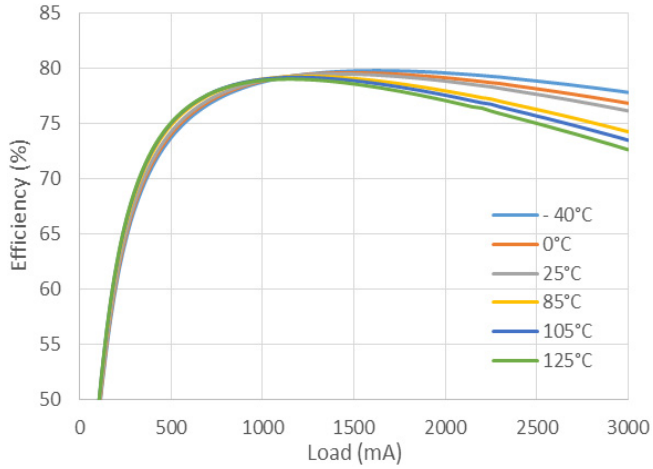


Figure 34. Switcher 1 Efficiency with V_{BAT} = 13.2 V vs. Load

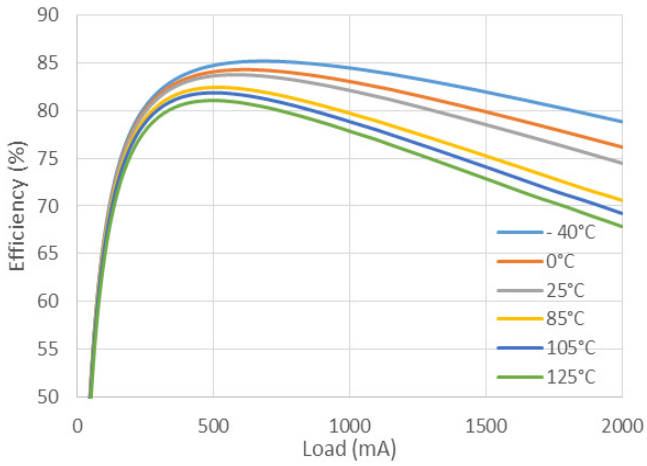


Figure 35. Switcher 2 Efficiency vs. Load V_{OUT2} = 1.8 V

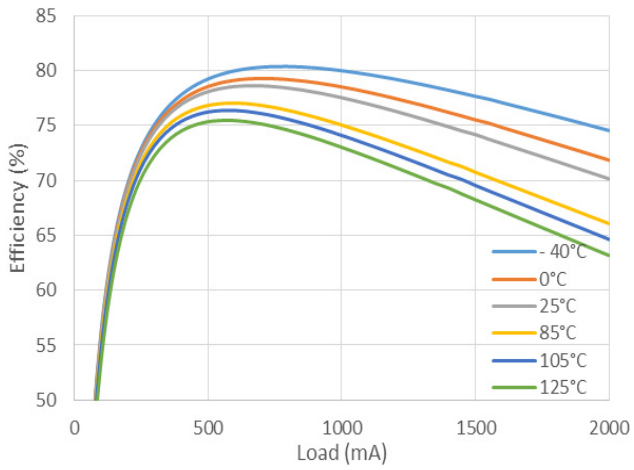


Figure 36. Switcher 3 Efficiency vs. Load V_{OUT3} = 1.2 V

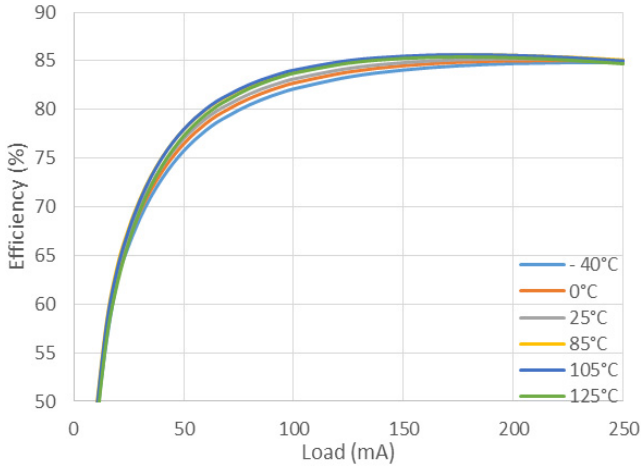


Figure 37. Switcher 4 Efficiency vs. Load

APPLICATION INFORMATION

General Description

The NCV97400 consists of one 2 MHz battery−connected 2.5 A switcher (switcher 1) with two low−voltage 2 MHz 1.5 A switchers (switchers 2 and 3) and a downstream low−current boost converter (switcher 4).

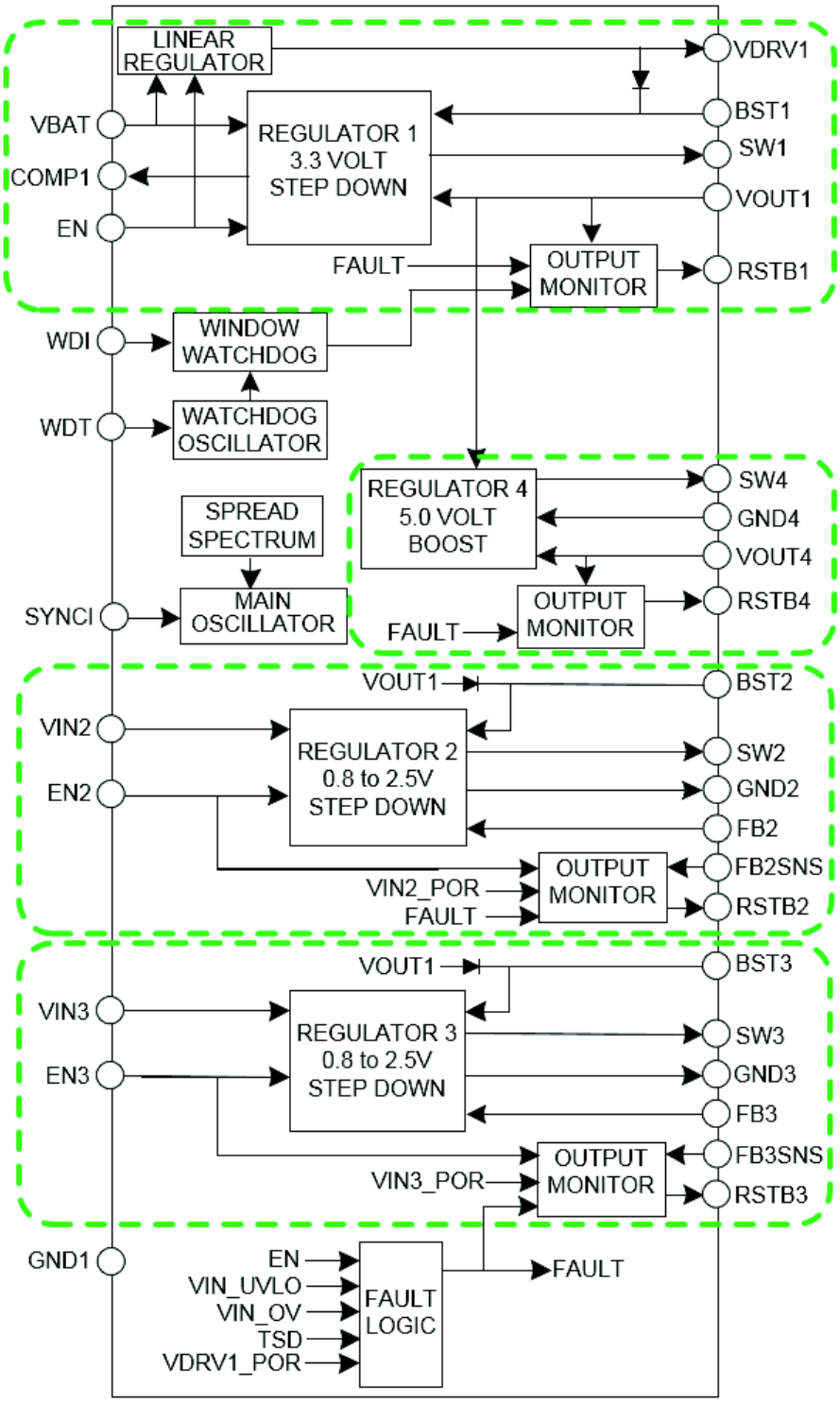


Figure 38. NCV97400 Simplified Block Diagram

Input Voltage

The main supply for the NCV97400 is the VBAT pin, which must always be connected to a voltage source between 4.1 V and 37 V.

- Below 4.1 V (max) an under−voltage lockout (UVLO) circuit inhibits all switching and resets the soft−start circuits.
- Above 40 V (max) an over−voltage shutdown (OVSD) circuit inhibits all switching and allows the NCV97400 to survive a 45 V load dump condition. Normal operation resumes when VBAT decreases below 34 V (min)

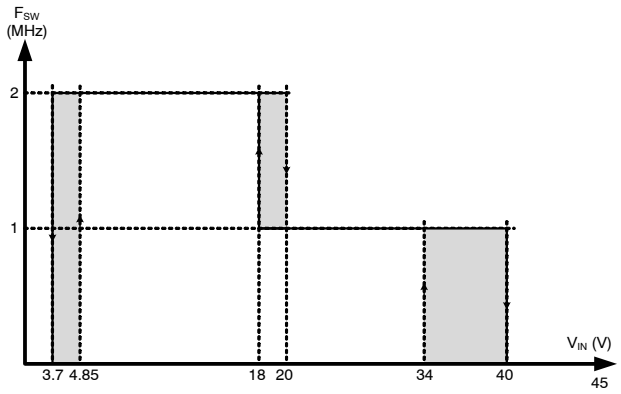


Figure 39. Input Voltage Range

Enable and Soft−Start

The NCV97400 can be completely disabled (shutdown mode) by connecting the master enable (EN) pin to GND. As a result, all outputs are stopped and the internal current consumption drops below 10 μA.

The EN pin is designed to accept either a logic−level signal or the battery voltage. If connecting EN to battery, and battery voltage could exceed 40 V, make the connection through a 10 k resistor. Upon receiving an input greater than 2 V, the EN pin allows switcher 1 to begin soft−start and ramp up to 3.3 V (typically in 1.4 ms). After the soft−start of VOUT1 is complete, switcher 4 (the boost regulator) begins its soft−start and ramps up to 5.0 V. Switcher 4 does not have its own enable input pin and is linked to the master enable input.

Switcher 2 and switcher 3 each have a dedicated enable input pin which can be activated a short time after the master enable is activated. Upon enabling, switcher 2 (or switcher 3) begins soft−start and ramps up the output to its final value (typically in 1.4 ms). Please note that until switcher 1 completes soft start, switcher 2 and switcher 3 are disabled internally. Figure 5 shows the startup sequence when EN, EN2, and EN3 are activated at the same time:

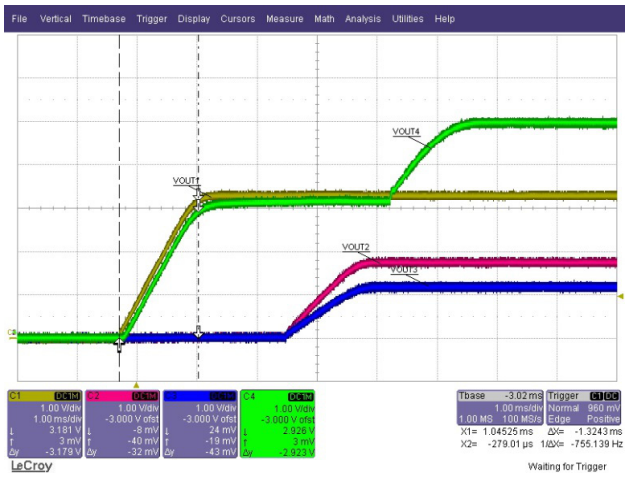


Figure 40. Soft Start Timing

The outputs can be sequenced automatically by connecting the ENx pins to the RSTBx pins. As an example, connect EN2 to RSTB4 and connect EN3 to RSTB2. The startup sequence will now be as in Figure 6:

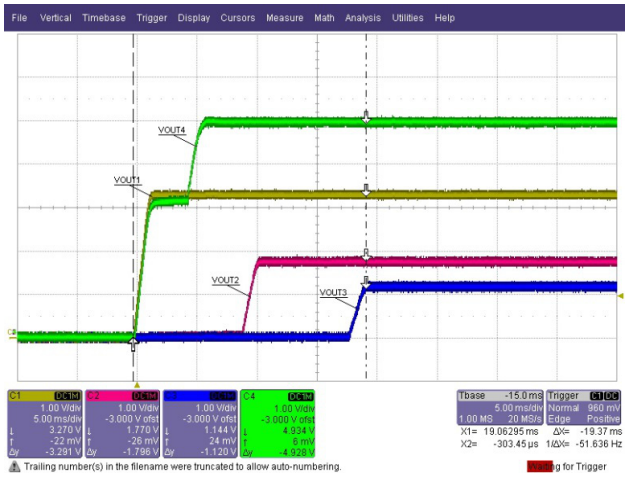


Figure 41. Soft Start Timing with Automatic Sequencing

Oscillator

All 4 switching regulators in the NCV97400 share the same oscillator, which, by default, operates at 2.0 MHz with pseudo−random spread spectrum (spread spectrum described in next section). The switching frequency can be controlled using the external synchronization input pin, SYNCI. Manually adjusting the switching frequency using the SYNCI pin will adjust the switching frequency for all 4 regulators since they share a common oscillator.

2 types of frequency adjustments can occur with the NCV97400: maximum duty cycle foldback and high voltage frequency foldback. These frequency foldback mechanisms take place outside the main oscillator in logic and only affect the regulators meeting the criteria. The main oscillator frequency remains unchanged.

"Maximum duty cycle foldback" is not actually an enforced frequency change, but refers to the apparent frequency if output voltage regulation causes duty cycle to reach 100% of the 2 MHz switching period – effectively skipping the OFF time for that period. When the power switch is turned off, it is always turned on again at the start of the next 2 MHz period. Due to this, the effective switching period can be multiples of the 2 MHz period. Logic monitoring duty cycle allows it to exceed 90% for up to 3 consecutive 2 MHz switching periods before enforcing a minimum OFF time at the end of the fourth period. If this occurs, the apparent frequency will be 500 kHz, and the regulator has reached maximum duty cycle. Once the load decreases (or in the case of Switcher 1, the input voltage increases), the OFF time can again be controlled by the output voltage regulator.

At high input voltages (above 20 V), switcher 1 frequency folds back to 1 MHz operation to properly maintain the output voltage when the conversion ratio needs to be lower than the minimum on time allows at 2 MHz operation. Once the input voltage drops back below 18 V, 2 MHz operation will resume. The switching frequency of switchers 2, 3 and 4 are unaffected by high VBAT voltage.

Spread Spectrum

In SMPS devices, switching translates to higher efficiency and switching at high frequency can reduce the size of external components. Unfortunately, switching also leads to a higher EMI profile. Spread spectrum is a method used to reduce the peak electromagnetic emissions of a switching regulator.

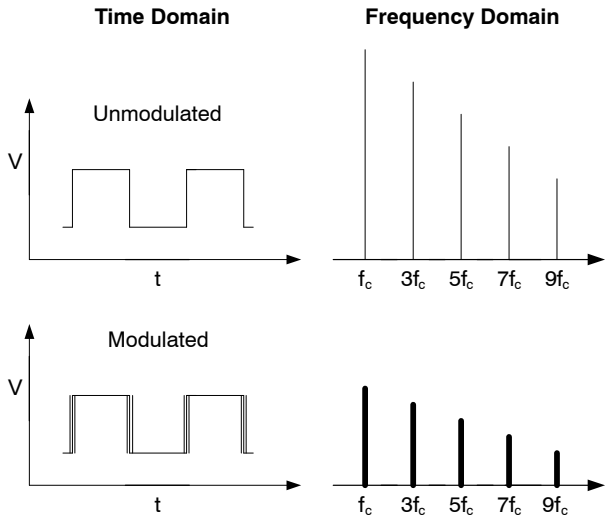


Figure 42. Spread Spectrum Comparison

The NCV97400 includes built–in spread spectrum in order to reduce peak radiated emissions. The NCV97400 uses a pseudo–random generator to sequence the oscillator frequency between the base frequency and a maximum spread spectrum frequency (shown in the table below). Frequencies are each offset by 40 kHz. Over time, each frequency is used an equal number of times in order to ensure an even spread of the energy into the wider band, and reduces the peak energy at the base frequency.

Table 4. PSEUDO–RANDOM FREQUENCY BINS

Pseudo Random Bin	Switching Frequency
0000	2.00 MHz
0001	2.04 MHz
0010	2.08 MHz
0011	2.12 MHz
0100	2.16 MHz
0101	2.20 MHz
0110	2.24 MHz
0111	2.28 MHz
1000	2.32 MHz
1001	2.36 MHz
1010	2.40 MHz
1011	2.44 MHz
1100	2.48 MHz
1101	2.52 MHz
1110	2.56 MHz
1111	2.60 MHz

The period of each switch cycle will change inversely to the switching frequency but the duty cycle will remain constant to properly maintain the output.

EMI and Input Filter

In addition to spread spectrum, an input filter is recommended to further reduce emissions due to switching heavy loads.

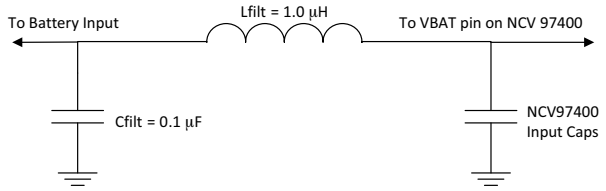


Figure 43. LC Input Filter

When connecting the battery voltage to other circuits on the PCB, be sure to connect them to the battery input side, not the NCV97400 side, of the LC filter. This will give the best possible noise performance.

Current Limit and Short Circuit Frequency Foldback

Each switching regulator has a peak current limit to protect the inductor and downstream components in case of a short circuit or transient event. Due to the ripple current through the inductor, the maximum dc output current of each converter is lower than the peak current limit. If the peak current limit is reached during the switch cycle, the switch turns off for the remainder of the cycle and turns on again at the start of the next cycle.

During severe output overloads or short circuit conditions, the primary regulator (switcher 1) automatically reduces its switching frequency and enters analog foldback. This creates a duty cycle small enough to limit the power in the output components while maintaining the ability to automatically reestablish the output voltage if the overload is removed. This foldback changes the main oscillator and will apply to all 4 regulators. Once the overload or short circuit is removed, 2 MHz operation will resume.

If the output current is still too high (after short circuit frequency foldback for switcher 1 or after peak current limit is reached for switchers 2, 3, and 4), the overloaded regulator may automatically enter an auto−recovery burst mode (hiccup mode) to self−protect and further reduce dissipated power in the output components. When an overload is detected, the switcher disables its output, remains off for the hiccup time, and then goes through the power−on reset procedure. If the overload has been removed, the output re−enables and operates normally. If the short is still present, the cycle begins again until the short is removed. Hiccup mode is continuous at a typical rate of 32 kHz until the short is removed.

External Frequency Synchronization

The NCV97400 can be synchronized to an external clock signal. If the IC does not have its switching frequency controlled by the SYNCI input, it operates normally at the default switching frequency, typically 2.0 MHz with spread spectrum.

The SYNCI pin is used as a synchronization input during normal operation and is ignored during startup, shutdown, overvoltage, and other transient conditions. When the switching frequency is controlled by the SYNCI input, synchronization starts within 2 ms of soft start completion. Please keep in mind that spread spectrum will be disabled when the oscillator is being synchronized with an external clock.

A rising edge on the SYNCI pin causes the current oscillator period to end and a new period to start. The switchnode of switcher 1 goes high 90 ns after a SYNCI rising edge, and the switchnode of switcher 4 goes low 350 ns after a SYNCI rising edge. If another rising edge does not arrive at the SYNCI pin within the Master Reassertion time, the NCV97400 resumes with the default switching frequency. This allows for uninterrupted operation in the event that the external clock is turned off.

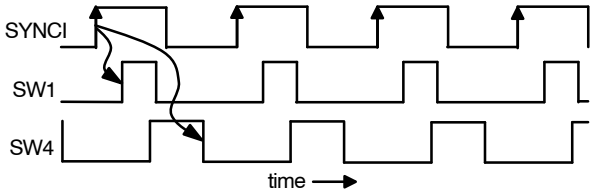


Figure 44. External Synchronization Timing

Reset & Delay

When the voltage on the VOUTx pin (or FBxSNS pin for SW2 and SW3) drops below or goes above the reset threshold, the corresponding open−drain output RSTBx is asserted (pulled low). All RSTBx outputs are also asserted during VBAT overvoltage and undervoltage faults, and during thermal shutdown. The RSTB2 & RSTB3 pins are also asserted (pulled low) when the associated switcher is disabled, and RSTB1 is asserted in response to a Watchdog Fault.

Each of the RSTB signals can either be used as a reset with delay or as a power good (no delay). The delay is determined by the current into the RSTBx pin, set by a resistor, show in Figure 45, below.

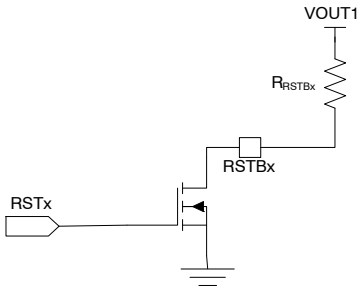


Figure 45. Reset Delay Circuit

Use the following equation to determine the ideal reset delay time using currents less than 500 μA:

$$t_{delay} = \frac{2475}{I_{RSTBx}}$$

where:

t_{delay}: ideal reset delay time [ms]

I_{RSTBx}: current into the RSTBx pin [μA]

Using I_{RSTBx} = 1 mA removes the delay and allows the reset to function as a “power good” pin.

The RSTBx resistor is commonly tied to VOUT1. Typical delay times for a 3.3 V pull−up can be achieved with the following resistor values:

Table 5. RESET DELAY TIMES

R_{RSTBx} (kΩ)	t_{DLY} (ms)
3.3	0
6.6	5
10	7.5
15	11.3
20	15.0
25	18.8
33	24.8

Functional Safety

The NCV97400 has been developed according to ISO−26262 targeting ASIL B/C applications. With this in mind, we've specifically included the following items to make this power supply compatible with your safety application:

1. There are 2 independent bandgaps for the internal reference voltages. The primary bandgap is used for the internal supplies and the regulation of each power supply output. The second bandgap is primarily used as a safety mechanism as a reference to which the RSTBx circuits are compared.
2. Each output voltage has a separate window voltage monitoring circuit that's comparing the output feedback signal to the internal reference generated by the second bandgap. Each output voltage is monitored for overvoltage and undervoltage conditions. Please see "Reset & Delay" for more details.
3. A window watchdog is included to monitor an incoming watchdog signal from a microcontroller. This behavior is detailed in the "Watchdog" section.

Watchdog

The 97400 contains a window watchdog function, which is exclusively tied to the RSTB1 output 1 of the PMIC. The watchdog function requires the microcontroller to send a pulse to show that it's still active. The watchdog oscillator runs independently of the switching oscillator. Window watchdog is active when SW1 is in regulation and RSTB1 is high. It is inactive when SW1 is out of regulation and RSTB1 is low. Watchdog timeout trigger mode with long timing begins on the rising edge of RSTB1. If no watchdog pulse is received during the timeout time $t_{WD_timeout}$, RSTB1 is pulled low for the delay time, t_{RESET}, and the watchdog timeout time starts again.

$$t_{WD_timeout}(ms) = 2.81 \times C_WDT(pF) + 18$$

Once a successful watch pulse is received on the WDI pin, a closed window time, t_{WD_CLS}, is in effect. If a pulse is received on the WDI pin during this time, RSTB1 is asserted. During normal operation, a successful watchdog pulse is required on the WDI pin during the watchdog window time, t_{WD}, but not during the closed window time, t_{WD_CLS}. If a valid watchdog pulse is not received on the WDI pin, RSTB1 is pulled low to signal the fault. Once the RSTB1 signal is released, the watchdog will start again and the watchdog timeout time, $t_{WD_timeout}$, begins again. VOUT1 is not affected by the watchdog circuitry and will remain in regulation during a watchdog fault.

In the event that the WDI pin is held high and no pulse is received for the duration of the watchdog timeout time or for the watchdog window time, RSTB1 is pulled low to signal the fault. Once the RSTB1 signal is released, the watchdog may start again and resumes the normal watchdog window time.

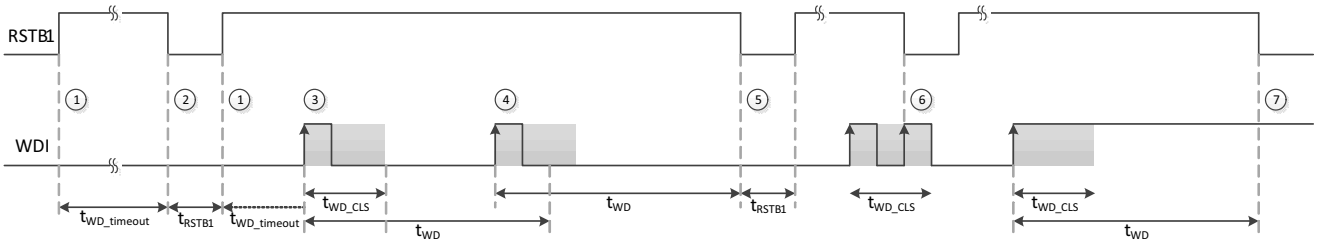


Figure 46. Watchdog Function and Timing

1. Rising edge on RSTB1 triggers the start of watchdog timeout mode.
2. No watchdog trigger within the watchdog timeout time $t_{WD_timeout}$. RSTB1 pulled low.
3. Window trigger mode active after rising edge on the WDI pin.
4. First successful watchdog trigger within the window time t_{WD}.
5. Watchdog trigger failed, no rising edge at WDI pin within window time t_{WD}. RSTB1 pulled low.
6. Watchdog trigger failed, rising edge at WDI pin within boundary time t_{WD_CLS}. RSTB1 pulled low.
7. Watchdog trigger failed, signal at WDI pin permanent high. RSTB1 pulled low.

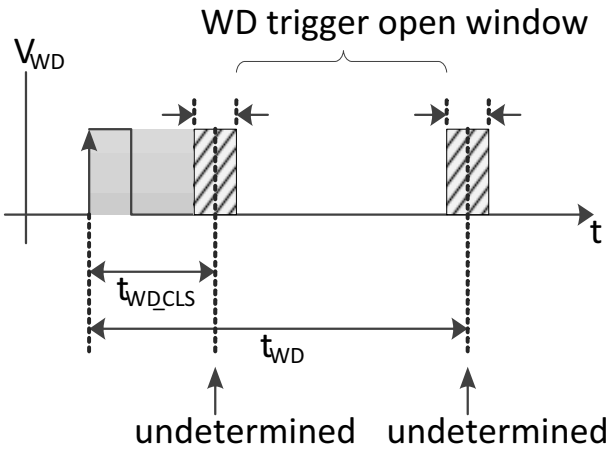


Figure 47. Watchdog Window with Tolerances

Debug Mode

The NCV97400 includes a user selectable "debug mode" that disables spread spectrum and the watchdog to make it easier to take certain measurements during evaluation. While the watchdog is disabled, it is unable to assert a fault on the RSTB1 signal.

To enter and remain in debug mode, connect the WDT pin to GND and connect the SYNCI pin high (a voltage greater than 2 V). If either of these 2 criteria are not met, the NCV97400 will resume normal operation. Further, if the WDT pin is held low while the SYNCI is not held high, a fault will be triggered on RSTB1.

SWITCHER 1

The primary dc−dc output for the NCV97400 is 3.3 V, set by an internal resistor divider. This buck regulator is non−synchronous and requires an external low−side freewheeling diode to operate.

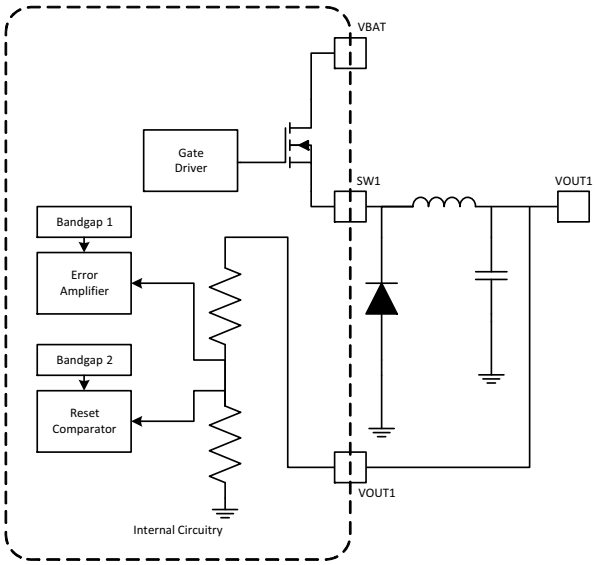


Figure 48. Switcher 1 Block Diagram

Internally, connected to the VOUT1 pin, the primary feedback regulates the output and the secondary path compares to the second reference for the reset circuitry.

The EN pin controls the enable circuitry for the switcher 1 output. It can accept a logic−level input and is also capable of high voltages and can be connected directly to VBAT.

Error Amplifier

Switcher 1 uses a transconductance type error amplifier. The output voltage of the error amplifier controls the peak inductor current at which the power switch shuts off. The Current Mode control method employed allows the use of a simple, type II compensation to optimize the dynamic response according to system requirements.

The compensation components must be connected between the output of the error amplifier and the electrical ground (between pins COMP1 and GND). For most applications, the following compensation circuitry is recommended:

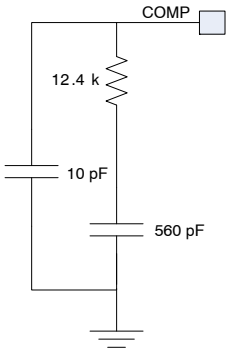


Figure 49. Recommended Compensation for Switcher 1

Slope Compensation

A fixed slope compensation signal is generated internally and added to the sensed current to avoid increased output voltage ripple due to bifurcation of inductor ripple current at duty cycles above 50% (sub−harmonics oscillations). The fixed amplitude of the slope compensation signal requires the inductor to be greater than a minimum value in order to avoid sub−harmonic oscillations. For the 3.3 V output, the recommended inductor value is between 2.2 μH and 4.7 μH.

To determine the minimum inductor required to avoid sub−harmonic oscillations, please refer to the following equation:

$$L_{min} = \frac{V_{OUT}}{2 \cdot S_{ramp}}$$

where:

L_{min}: minimum inductor required to avoid sub−harmonic oscillations [μH]

V_{OUT}: output voltage [V]

S_{ramp}: internal slope compensation [A/μs]

Drive and Bootstrap

At the DRV1 pin an internal regulator provides a ground−referenced voltage to an external capacitor (C_{DRV1}), to allow fast recharge of the external bootstrap capacitor (C_{BST1}) used to supply power to the power switch gate driver. If the voltage at the DRV1 pin goes below the DRV1 POR Threshold V_{DRV1SP}, switching is inhibited and the soft−start circuit is reset, until the DRV1 pin voltage goes back up above V_{DRV1ST}.

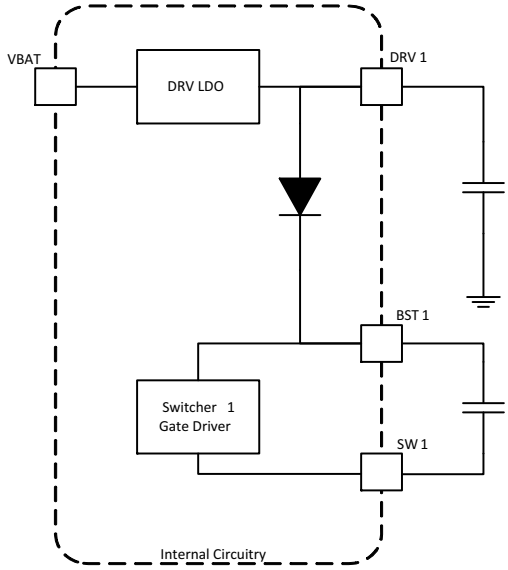


Figure 50. Switcher 1 Drive and Bootstrap Circuitry

In order for the bootstrap capacitor to stay charged, the switch node needs to be pulled down to ground regularly. In very light load condition, when switcher 1 skips switching cycles to keep the output voltage in regulation, the bootstrap voltage could collapse and the regulator stop switching. To prevent this, an approximately 10 mA internal load is connected on VOUT1 to operate correctly in all cases. When the NCV97200 is enabled and VBAT is below approximately 7.5 V, the internal load is increased to approximately 60 mA.

A fast−charge circuit ensures the bootstrap capacitor is always charged prior to starting the switcher after it has been enabled.

Soft Start

Upon being enabled or released from a fault condition, and after the DRV1 voltage is established, a soft−start circuit ramps the switching regulator error amplifier reference voltage to the final value. During soft−start, the average switching frequency is lower than its normal mode value until the output voltage approaches regulation.

Current Limit

Due to the ripple on the inductor current, the average output current of a buck converter is lower than the peak current set point of the regulator. Figure 51 shows − for a 4.7 μH inductor − how the variation of inductor peak current with input voltage affects the maximum DC current switcher 1 can deliver to a load. Figure 52 shows the same for 2.2 μH inductor.

Internal slope compensation S_{ramp1} also reduces switcher 1 peak current limit proportional to the duty cycle. The amount of this reduction for switcher 1 is the product of S_{ramp1}, switching period, and 3.3 divided by VBAT.

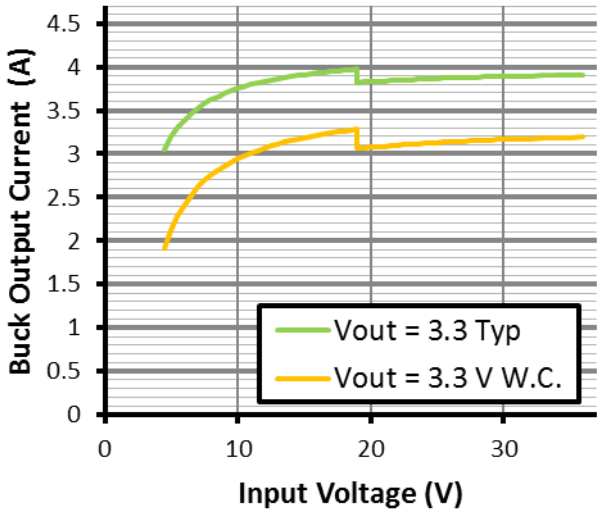


Figure 51. Switcher 1 Dc Output Current vs. VIN with a 4.7 μH Inductor

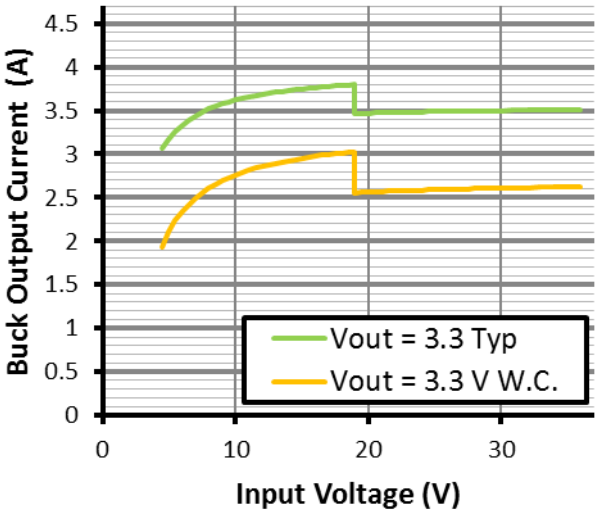


Figure 52. Switcher 1 Dc Output Current vs. VIN with a 2.2 μH Inductor

High Voltage Frequency Foldback

To limit the power lost in generating the drive voltage for the power switch, the switching frequency is reduced by a factor of 2 when the input voltage exceeds the V_{BAT} Frequency Foldback Threshold V_{FL1U} (see Figure 53) Frequency reduction is automatically terminated when the input voltage drops back below the V_{BAT} Frequency Foldback threshold V_{FL1D}.

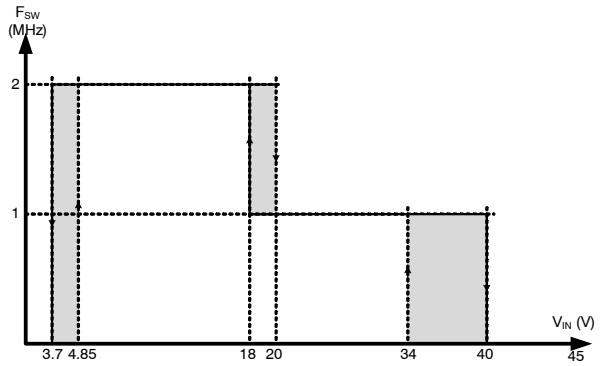


Figure 53. High Voltage Frequency Foldback

Inductor Selection

A 3.3 μH inductor is recommended for Switcher 1, although values between 2.2 μH and 4.7 μH may give more optimized performance in some applications. The relationship between several operating parameters are given by the equation below.

$$L = \frac{V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN,max}}\right)}{\delta I_r \cdot f_{sw} \cdot I_{OUT}}$$

where:

V_{OUT}: dc output voltage [V]
$V_{IN,max}$: maximum dc input voltage [V]
δI_r: inductor current ripple [%]
f_{sw}: switching frequency [Hz]
I_{OUT}: dc output current [A]

Discontinuous Mode

The regulator operates in Continuous Conduction Mode (CCM) when average inductor current exceeds half the peak−to−peak ripple current, and in Discontinuous Conduction Mode (DCM) when it does not. The borderline between these modes can be found using the following equation:

$$I_{BCM} = \frac{1}{2} \cdot \frac{\left(1 - \frac{V_{OUT}}{V_{IN,max}}\right)}{f_{sw}} \cdot \frac{V_{OUT}}{L}$$

where:

I_{BCM}: borderline conduction mode output current [A]
V_{OUT}: dc output voltage [V]
$V_{IN,max}$: maximum dc input voltage [V]
f_{sw}: switching frequency [Hz]
L: inductor value [H]

Average output currents above IBCM will cause operation in CCM while average output currents below IBCM will cause operation in DCM.

SWITCHERS 2 AND 3

The secondary dc−dc outputs (switcher 2 and switcher 3) for the NCV97400 are adjustable down to 0.8 V and can each be set by an external resistor divider. These buck regulators are synchronous and both high−side and low−side switches are internal to the IC. As an example: please see the following diagram for the switcher 2 architecture:

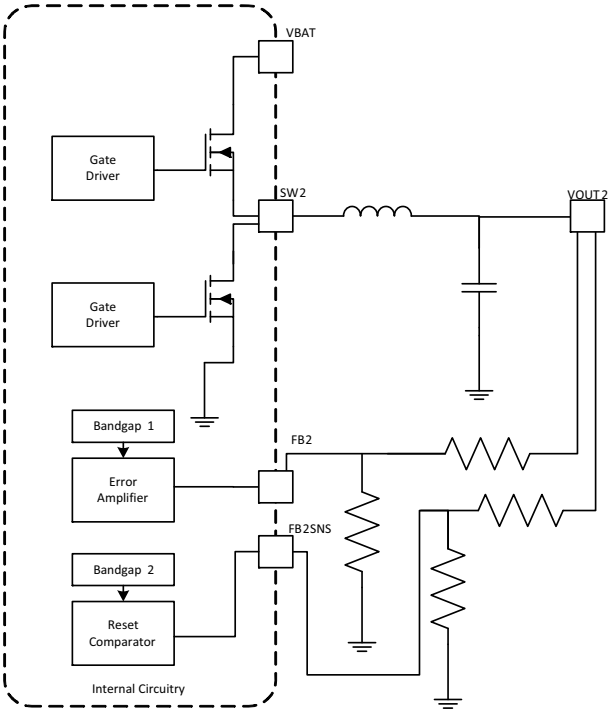


Figure 54. Switcher 2 Block Diagram

Since the output for switcher 2 is adjustable, the resistor divider is external and the primary feedback node, FB2, is monitored internally and compared to the reference for proper output regulation. The secondary external resistor divider, connected to FB2SNS, is monitored internally by the reset circuitry and compared to the second reference. When not using the NCV97400 in a safety application, you may use one resistor divider and directly connect FB2SNS to FB2. There is a similar set of pins for switcher 3.

The EN2 pin controls the enable circuitry for the switcher 2 output. It can accept a logic−level input and is sometimes connected to VOUT1 or to RSTB1. The EN3 pin controls switcher 3 in the same way. Both EN2 and EN3 are disabled internally when the primary enable input, EN, is pulled low.

If the voltage at the VIN2 or the VIN3 pin goes below the VIN2 (or VIN3) POR Threshold V_{INxSP}, switching is inhibited and the soft−start circuit is reset, until the VIN2 (or VIN3) pin voltage goes back up above V_{INxST}.

Error Amplifier

Switchers 2 & 3 each use a voltage type error amplifier. The compensation for these regulators is internal and cannot be adjusted.

Slope Compensation

A fixed slope compensation signal is generated internally and added to the sensed current to avoid increased output voltage ripple due to bifurcation of inductor ripple current at duty cycles above 50% (sub−harmonics oscillations). The fixed amplitude of the slope compensation signal requires the inductor to be greater than a minimum value, depending on output voltage, in order to avoid sub−harmonic oscillations. For a 1.2 V output, for example, the recommended inductor value is 1.0 μH.

To determine the minimum inductor required to avoid sub−harmonic oscillations, please refer to the following equation:

$$L_{min} = \frac{V_{OUT}}{2 \cdot S_{ramp}}$$

where:

L_{min}: minimum inductor required to avoid sub−harmonic oscillations [μH]

V_{OUT}: output voltage [V]

S_{ramp}: internal slope compensation [A/μs]

Bootstrap

Since the internal high−side FET gate drivers are low voltage, BST2 and BST3 are connected through internal diodes to the VOUT1 pin (see Figure 1). Connection of a 0.1 uF capacitor from VOUT1 to ground close to the VOUT1 pin is recommended in order to allow fast recharge of the external bootstrap capacitor (C_{BST2} and C_{BST3}) used to supply power to the power switch gate driver.

Soft Start

Upon being enabled or released from a fault condition, and after the VIN2 (or VIN3) voltage is established (and once switcher 1 has completed soft start), a soft−start circuit ramps the switching regulator error amplifier reference voltage to the final value. The typical soft−start duration is 1.4 ms.

Current Limit

Due to the ripple on the inductor current, the average output current of a buck converter is lower than the peak current set point of the regulator. Table 6 shows some examples of common setups:

Table 6. SW2&3 WORST CASE DC OUTPUT CURRENT

Output Voltage (V)	Inductor Value (μH)	Worst Case Max Dc Output (A)	Typical Max Dc Output (A)
2.5	2.2	0.8	1.6
1.8	1.5	1.1	1.9
1.2	1.0	1.4	2.0
0.8	1.0	1.6	2.2

Output Voltage Selection

The voltage outputs for switcher 2 and switcher 3 are adjustable and can be set with an external resistor divider. The feedback reference for both switchers is 0.8 V.

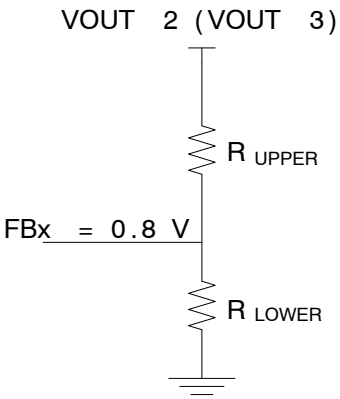


Figure 55. Output Voltage Selection with Feedback Divider

The upper resistor should typically be 10 kΩ and is part of the internal feedback loop. To maintain stability over all conditions, it is recommended to only change the lower feedback resistor to set the output voltage. Use the following equation:

$$R_{LOWER}(k\Omega) = \frac{8}{VOUT - 0.8}$$

Some common setups are listed below:

Desired Output (V)	V_{REF} (V)	R_{UPPER} (kΩ, 1%)	R_{LOWER} (kΩ, 1%)
0.8	0.8	10.0	NP
0.9	0.8	10.0	80.6
1.2	0.8	10.0	20.0
1.8	0.8	10.0	8.06
2.5	0.8	10.0	4.75

For safety applications, please be sure to use a second, parallel, feedback divider and connect the feedback to FBxSNS. This provides isolation between the 2 distinct feedback paths. For applications that don't require isolated feedback paths, you may short the FBxSNS pin directly to the FBx pin of the respective switcher.

Inductor Selection

By default, the following inductor values are recommended for the switchers 2 and 3, based on output voltage:

Output Voltage	Inductor Value
0.8 V	1.0 μH
1.2 V	1.0 μH or 1.2 μH
1.5 V	1.5 μH or 2.2 μH
1.8 V	1.5 μH or 2.2 μH
2.5 V	2.2 μH or 3.3 μH

If you'd like to choose a different value, please follow the equation, below.

$$L = \frac{V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN,max}}\right)}{\delta I_r \cdot f_{sw} \cdot I_{OUT}}$$

where:

V_{OUT}: dc output voltage [V]
$V_{IN,max}$: maximum dc input voltage [V]
δI_r: inductor current ripple [%]
f_{sw}: switching frequency [Hz]
I_{OUT}: dc output current [A]

Noise Performance for Heavy Load

For heavy load conditions (> 1 A) on the downstream switching outputs, a snubber circuit is recommended for improved noise performance. The following circuit can be used for all output voltage combinations:

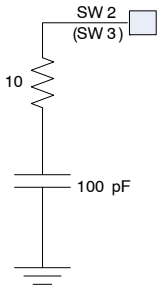


Figure 56. RC Snubber for Noise Performance at Heavy Load

In order to minimize noise on the Switcher 2 & Switcher 3 inputs (VOUT1), Switcher 3 switches in−phase with Switcher 1, and Switcher 2 switches out−of−phase with Switcher 1.

SWITCHER 4

The NCV97400 contains a boost regulator, switcher 4, which boosts the 3.3 V from the switcher 1 to 5.0 V. This non−synchronous boost regulator requires an external freewheeling diode. Switcher 4 is intended to be used for in−vehicle networks (e.g. CAN) and can supply up to 250 mA dc.

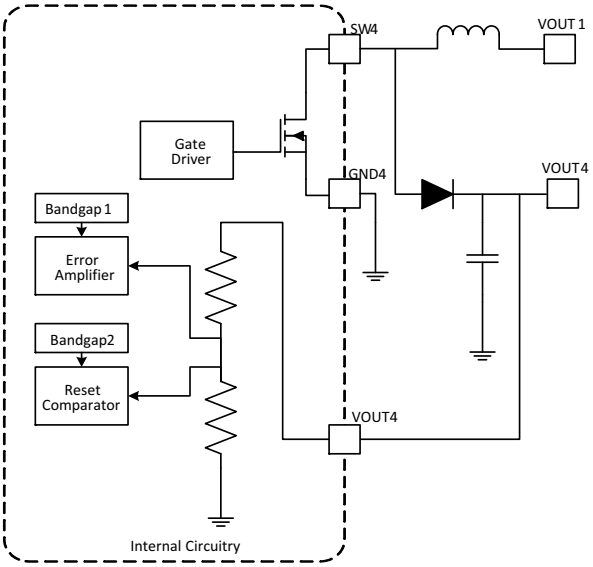


Figure 57. Switcher 4 Block Diagram

Internally, connected to the VOUT4 pin, the primary feedback regulates the output and the secondary path compares to the second reference for the reset circuitry.

The EN pin controls the enable circuitry for the switcher 4 output. Once switcher 1 has completed soft−start and the output is in regulation, switcher 4 is automatically enabled.

Error Amplifier

Switcher 4 uses a voltage type error amplifier. The compensation for this regulator is internal and cannot be adjusted.

Soft Start

Upon being enabled or released from a fault condition, and once switcher 1 has completed soft start, a soft−start circuit ramps the switcher 4 error amplifier reference voltage to the final value.

Please note that since this is a boost regulator, the VOUT4 output will be a diode voltage below VOUT1 until it starts switching in regulation. This is normal behavior – please see the scope capture below:

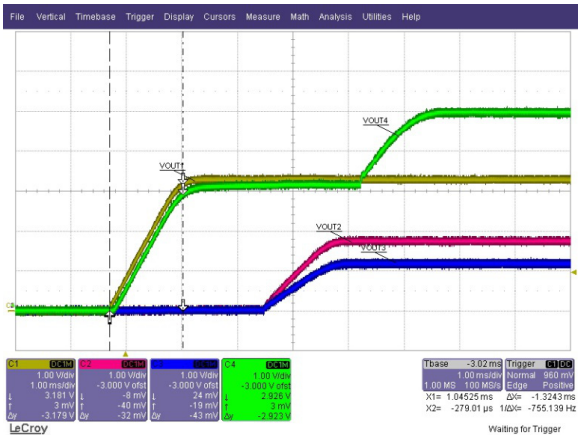


Figure 58. Switcher 4 Soft−start

Current Limit

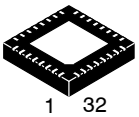
Due to the ripple on the inductor current, the average output current of the boost converter is lower than the peak current set point of the regulator. Table 7 shows some examples of common setups.

Table 7. SW4 WORST CASE DC OUTPUT CURRENT

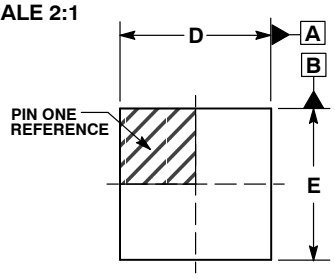
Output Voltage (V)	Inductor Value (uH)	Worst Case Max Dc Output (mA)	Typical Max Dc Output (mA)
5.0	4.7	300	375
5.0	2.2	250	325

QFNW32 5x5, 0.5P
CASE 484AB
ISSUE D

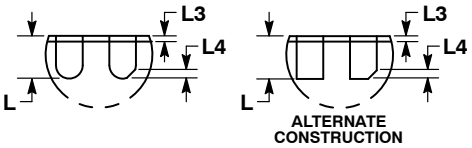
DATE 07 SEP 2018



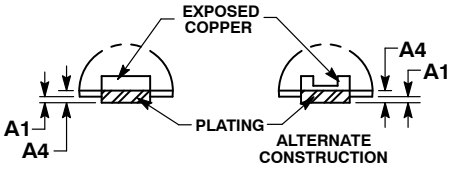
SCALE 2:1



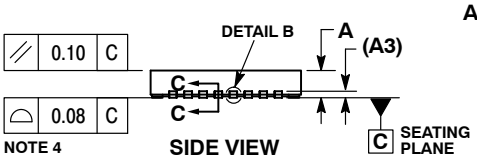
TOP VIEW



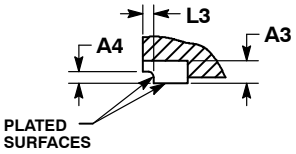
DETAIL A



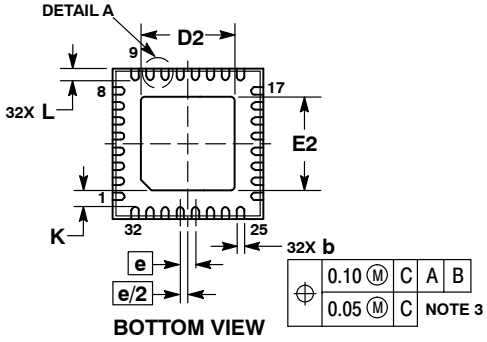
DETAIL B



SIDE VIEW



SECTION C–C

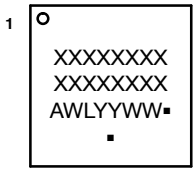


BOTTOM VIEW

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.10 AND 0.20MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	---	---	0.05
A3	0.20 REF		
A4	0.10	---	---
b	0.20	0.25	0.30
D	4.90	5.00	5.10
D2	3.00	3.10	3.20
E	4.90	5.00	5.10
E2	3.00	3.10	3.20
e	0.50 BSC		
K	0.35	---	---
L	0.30	0.40	0.50
L3	---	---	0.10
L4	0.08 REF		

GENERIC MARKING DIAGRAM*

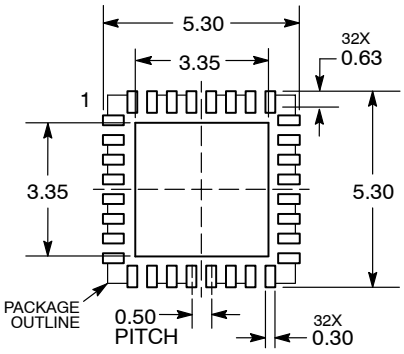


XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb–Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	QFNW32 5x5, 0.5P		PAGE 1 OF 1

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