# NTD4809NH, NVD4809NH

# Power MOSFET

## 30 V, 58 A, Single N−Channel, DPAK/IPAK

**ON Semiconductor®**

**http://onsemi.com**

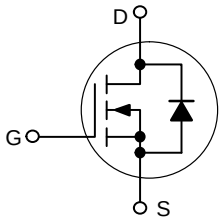
| $V_{(BR)DSS}$ | $R_{DS(on)}$ MAX | $I_D$ MAX |
|---|---|---|
| 30 V | 9.0 mΩ @ 10 V | 58 A |
| | 12.5 mΩ @ 4.5 V | |

### Features

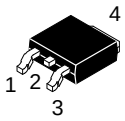
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- AEC−Q101 Qualified and PPAP Capable − NVD4809NH
- These Devices are Pb−Free and are RoHS Compliant

### Applications

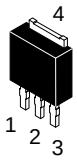
- CPU Power Delivery
- DC−DC Converters
- Low Side Switching




**N−Channel**




**DPAK**
**CASE 369AA**
**(Bent Lead)**
**STYLE 2**



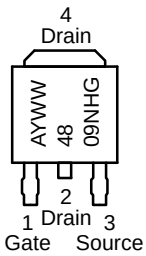

**IPAK**
**CASE 369AD**
**(Straight Lead)**
**STYLE 2**

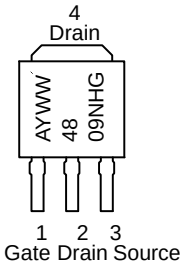
**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Parameter | | | Symbol | Value | Unit |
|---|---|---|---|---|---|
| Drain−to−Source Voltage | | | $V_{DSS}$ | 30 | V |
| Gate−to−Source Voltage | | | $V_{GS}$ | ±20 | V |
| Continuous Drain Current ($R_{\theta JA}$) (Note 1) | Steady State | $T_A$ = 25°C | $I_D$ | 11.5 | A |
| | | $T_A$ = 85°C | | 9.0 | |
| Power Dissipation ($R_{\theta JA}$) (Note 1) | | $T_A$ = 25°C | $P_D$ | 2.0 | W |
| Continuous Drain Current ($R_{\theta JA}$) (Note 2) | | $T_A$ = 25°C | $I_D$ | 9.0 | A |
| | | $T_A$ = 85°C | | 7.0 | |
| Power Dissipation ($R_{\theta JA}$) (Note 2) | | $T_A$ = 25°C | $P_D$ | 1.3 | W |
| Continuous Drain Current ($R_{\theta JC}$) (Note 1) | | $T_C$ = 25°C | $I_D$ | 58 | A |
| | | $T_C$ = 85°C | | 45 | |
| Power Dissipation ($R_{\theta JC}$) (Note 1) | | $T_C$ = 25°C | $P_D$ | 52 | W |
| Pulsed Drain Current | $t_p$=10μs | $T_A$ = 25°C | $I_{DM}$ | 130 | A |
| Current Limited by Package | | $T_A$ = 25°C | $I_{DmaxPkg}$ | 45 | A |
| Operating Junction and Storage Temperature | | | $T_J$, $T_{stg}$ | −55 to 175 | °C |
| Source Current (Body Diode) | | | $I_S$ | 43 | A |
| Drain to Source dV/dt | | | dV/dt | 6.0 | V/ns |
| Single Pulse Drain−to−Source Avalanche Energy ($V_{DD}$ = 24 V, $V_{GS}$ = 10 V, L = 1.0 mH, $I_{L(pk)}$ = 15 A, $R_G$ = 25 Ω) | | | $E_{AS}$ | 112.5 | mJ |
| Lead Temperature for Soldering Purposes (1/8″ from case for 10 s) | | | $T_L$ | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**MARKING DIAGRAMS & PIN ASSIGNMENTS**




A = Assembly Location*
Y = Year
WW = Work Week
4809NH = Device Code
G = Pb−Free Package

* The Assembly Location code (A) is front side optional. In cases where the Assembly Location is stamped in the package, the front side assembly code may be blank.

**ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

© Semiconductor Components Industries, LLC, 2014

## THERMAL RESISTANCE MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Junction−to−Case (Drain) | $R_{\theta JC}$ | 2.9 | °C/W |
| Junction−to−TAB (Drain) | $R_{\theta JC-TAB}$ | 3.5 | |
| Junction−to−Ambient − Steady State (Note 1) | $R_{\theta JA}$ | 74 | |
| Junction−to−Ambient − Steady State (Note 2) | $R_{\theta JA}$ | 116 | |

1. Surface−mounted on FR4 board using 1 in sq pad size, 1 oz Cu.
2. Surface−mounted on FR4 board using the minimum recommended pad size.

## ELECTRICAL CHARACTERISTICS ($T_J$ = 25°C unless otherwise noted)

| Parameter | Symbol | Test Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| Drain−to−Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 μA | | 30 | | | V |
| Drain−to−Source Breakdown Voltage Temperature Coefficient | $V_{(BR)DSS}/T_J$ | | | | 25 | | mV/°C |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 24 V | $T_J$ = 25°C | | | 1.0 | μA |
| | | | $T_J$ = 125°C | | | 10 | |
| Gate−to−Source Leakage Current | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ±20 V | | | | ±100 | nA |
| **ON CHARACTERISTICS** (Note 3) | | | | | | | |
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | | 1.5 | 2.1 | 2.5 | V |
| Negative Threshold Temperature Coefficient | $V_{GS(TH)}/T_J$ | | | | 5.7 | | mV/°C |
| Drain−to−Source On Resistance | $R_{DS(on)}$ | $V_{GS}$ = 10 to 11.5 V | $I_D$ = 30 A | | 7.0 | 9.0 | mΩ |
| | | | $I_D$ = 15 A | | 7.0 | | |
| | | $V_{GS}$ = 4.5 V | $I_D$ = 30 A | | 10.45 | 12.5 | |
| | | | $I_D$ = 15 A | | 9.95 | | |
| Forward Transconductance | $g_{FS}$ | $V_{DS}$ = 15 V, $I_D$ = 15 A | | | 9.0 | | S |
| **CHARGES AND CAPACITANCES** | | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{GS}$ = 0 V, f = 1.0 MHz, $V_{DS}$ = 12 V | | | 1596 | 2155 | pF |
| Output Capacitance | $C_{oss}$ | | | | 331 | 447 | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | | 190 | 294 | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS}$ = 4.5 V, $V_{DS}$ = 15 V, $I_D$ = 30 A | | | 12.5 | 15 | nC |
| Threshold Gate Charge | $Q_{G(TH)}$ | | | | 2.4 | 3.6 | |
| Gate−to−Source Charge | $Q_{GS}$ | | | | 5.3 | 7.9 | |
| Gate−to−Drain Charge | $Q_{GD}$ | | | | 5.1 | 7.7 | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS}$ = 11.5 V, $V_{DS}$ = 15 V, $I_D$ = 30 A | | | 29.3 | 44 | nC |
| **SWITCHING CHARACTERISTICS** (Note 4) | | | | | | | |
| Turn−On Delay Time | $t_{d(on)}$ | $V_{GS}$ = 4.5 V, $V_{DS}$ = 15 V, $I_D$ = 15 A, $R_G$ = 3.0 Ω | | | 12.0 | 18 | ns |
| Rise Time | $t_r$ | | | | 20 | 30 | |
| Turn−Off Delay Time | $t_{d(off)}$ | | | | 14 | 21 | |
| Fall Time | $t_f$ | | | | 5.0 | 7.5 | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted) (continued)

| Parameter | Symbol | Test Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Turn−On Delay Time | $t_{d(on)}$ | $V_{GS}$ = 11.5 V, $V_{DS}$ = 15 V, $I_D$ = 15 A, $R_G$ = 3.0 Ω | | | 7.0 | 10.4 | ns |
| Rise Time | $t_r$ | | | | 18 | 27 | |
| Turn−Off Delay Time | $t_{d(off)}$ | | | | 22 | 33 | |
| Fall Time | $t_f$ | | | | 3.0 | 4.6 | |
| **DRAIN−SOURCE DIODE CHARACTERISTICS** | | | | | | | |
| Forward Diode Voltage | $V_{SD}$ | $V_{GS}$ = 0 V, $I_S$ = 30 A | $T_J$ = 25°C | | 0.95 | 1.2 | V |
| | | | $T_J$ = 125°C | | 0.83 | | |
| Reverse Recovery Time | $t_{RR}$ | $V_{GS}$ = 0 V, dIs/dt = 100 A/μs, $I_S$ = 30 A | | | 15.6 | | ns |
| Charge Time | ta | | | | 10.6 | | |
| Discharge Time | tb | | | | 5.0 | | |
| Reverse Recovery Time | $Q_{RR}$ | | | | 7.5 | | nC |
| **PACKAGE PARASITIC VALUES** | | | | | | | |
| Source Inductance | $L_S$ | $T_A$ = 25°C | | | 2.49 | | nH |
| Drain Inductance, DPAK | $L_D$ | | | | 0.0164 | | |
| Drain Inductance, IPAK | $L_D$ | | | | 1.88 | | |
| Gate Inductance | $L_G$ | | | | 3.46 | | |
| Gate Resistance | $R_G$ | | | | 0.75 | | Ω |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

## TYPICAL PERFORMANCE CURVES

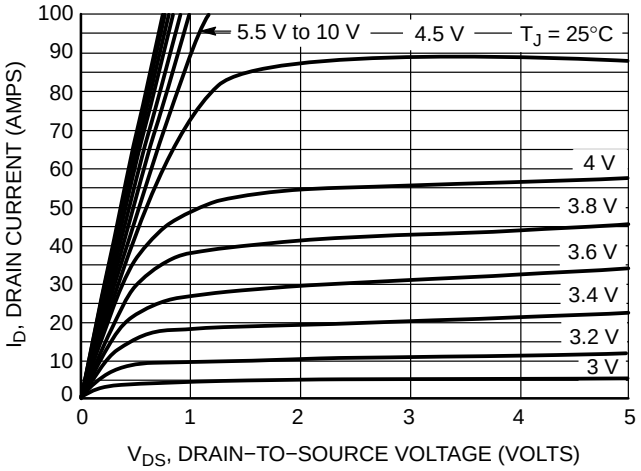



**Figure 1. On−Region Characteristics**

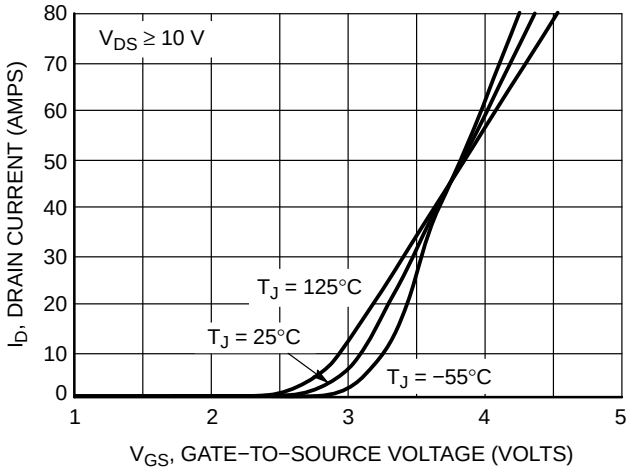



**Figure 2. Transfer Characteristics**

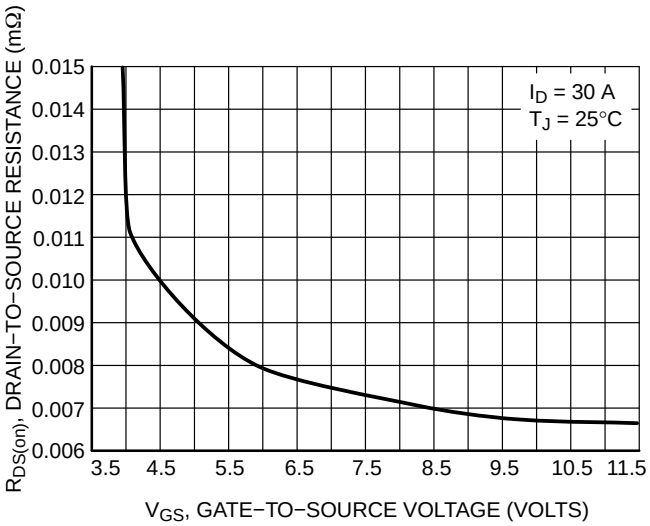



**Figure 3. On−Resistance vs. Gate−to−Source Voltage**

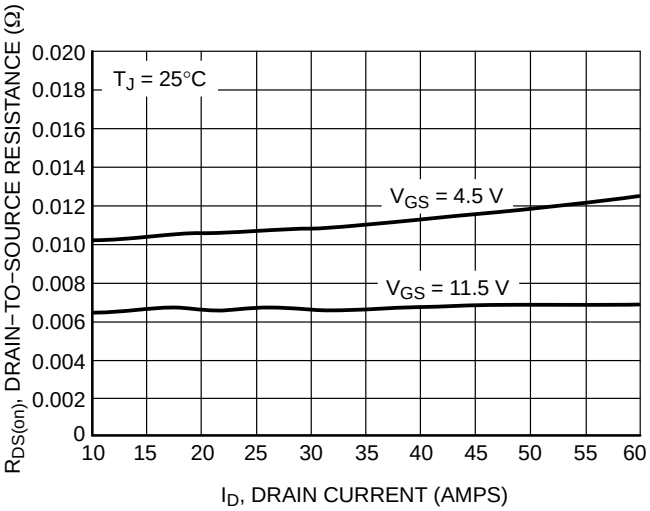



**Figure 4. On−Resistance vs. Drain Current and Gate Voltage**

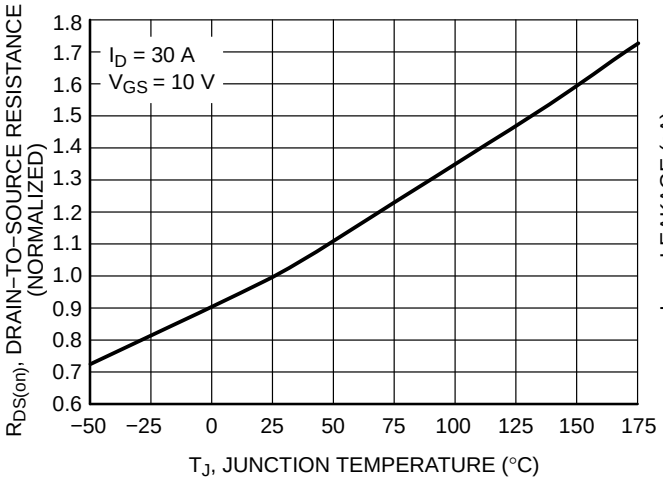



**Figure 5. On−Resistance Variation with Temperature**

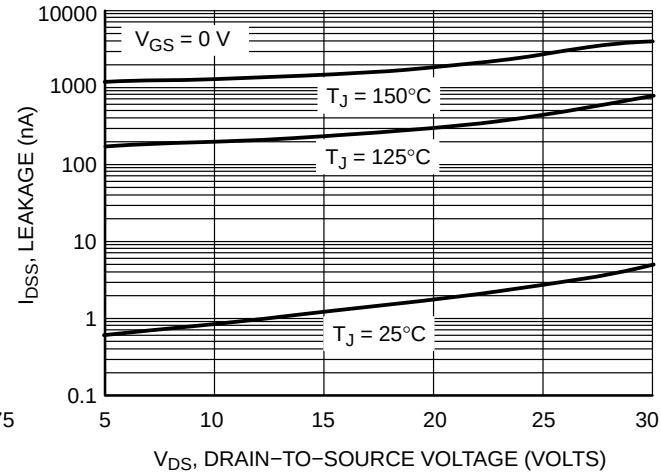



**Figure 6. Drain−to−Source Leakage Current vs. Drain Voltage**

## TYPICAL PERFORMANCE CURVES

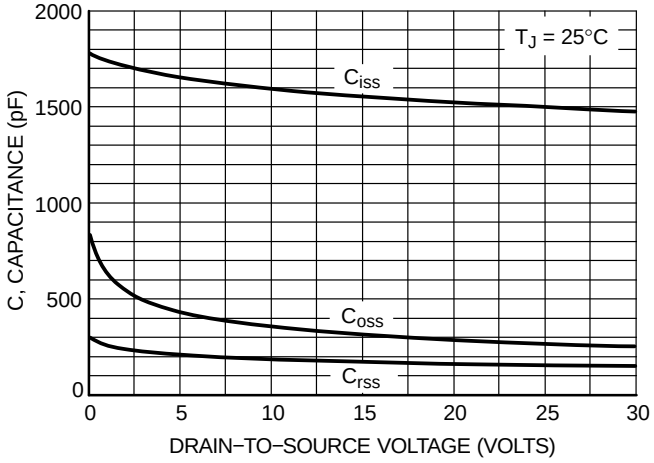



**Figure 7. Capacitance Variation**

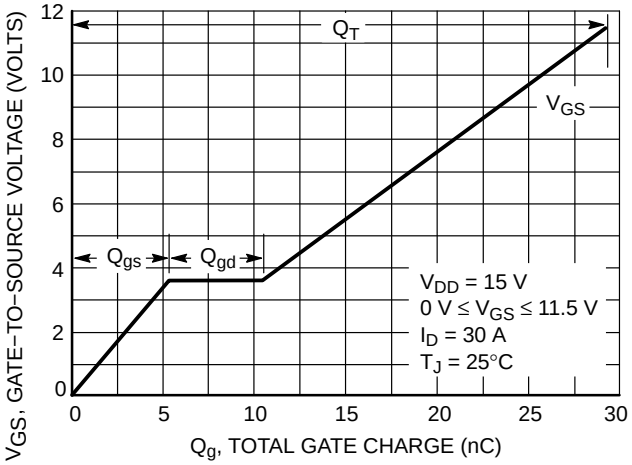



**Figure 8. Gate−to−Source Voltage vs. Total Charge**

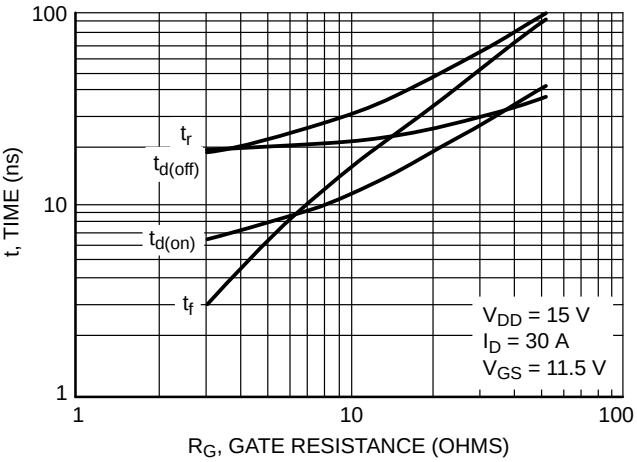



**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**

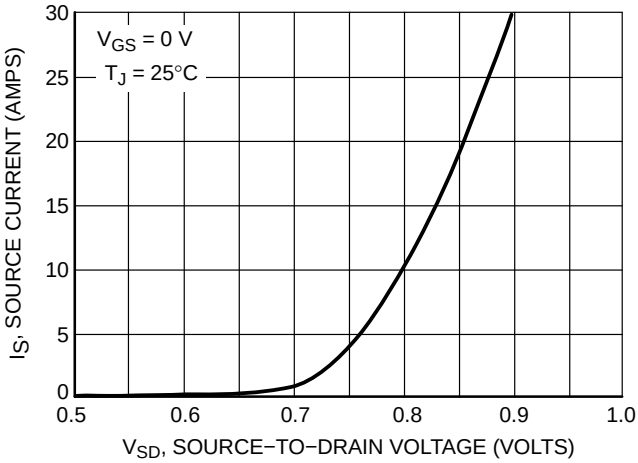



**Figure 10. Diode Forward Voltage vs. Current**

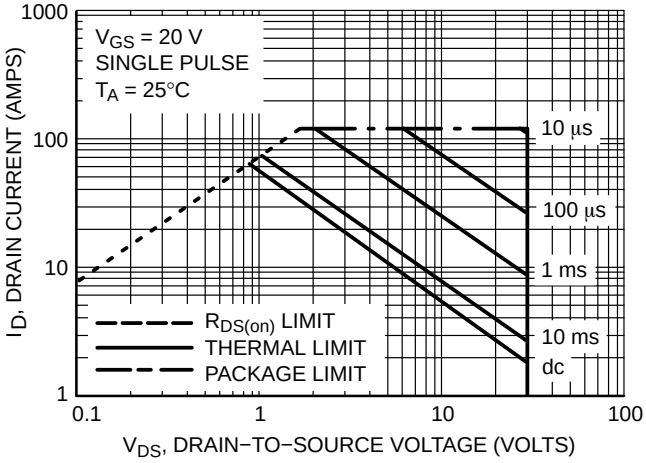



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

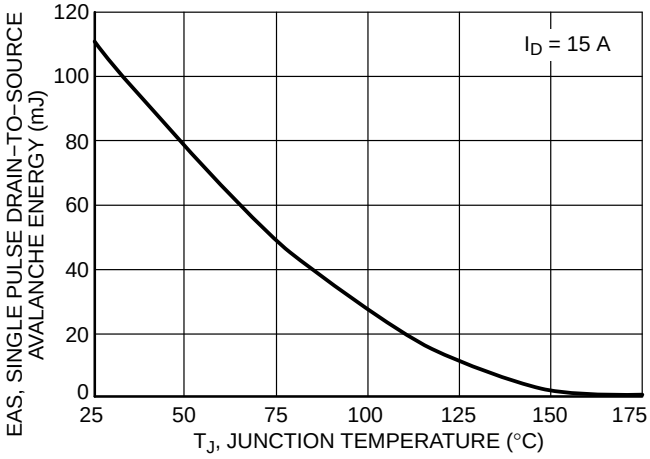



**Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature**

## TYPICAL PERFORMANCE CURVES

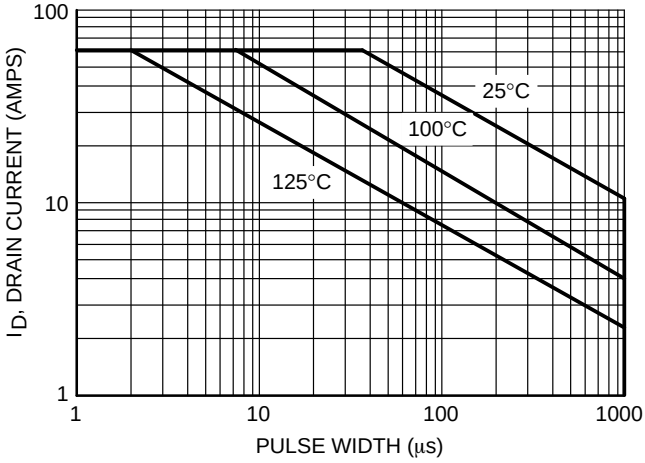



**Figure 13. Avalanche Characteristics**

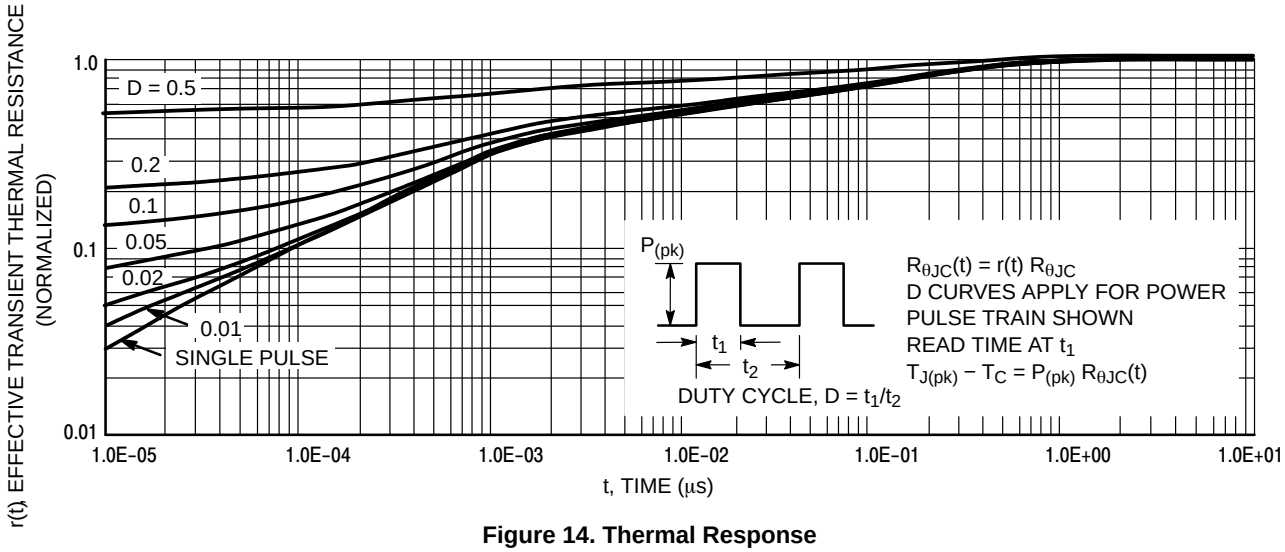
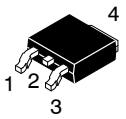



**Figure 14. Thermal Response**

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NTD4809NHT4G | DPAK<br>(Pb−Free) | 2500 / Tape & Reel |
| NTD4809NH−35G | IPAK Trimmed Lead<br>(3.5 ± 0.15 mm)<br>(Pb−Free) | 75 Units / Rail |
| NVD4809NHT4G | DPAK<br>(Pb−Free) | 2500 / Tape & Reel |

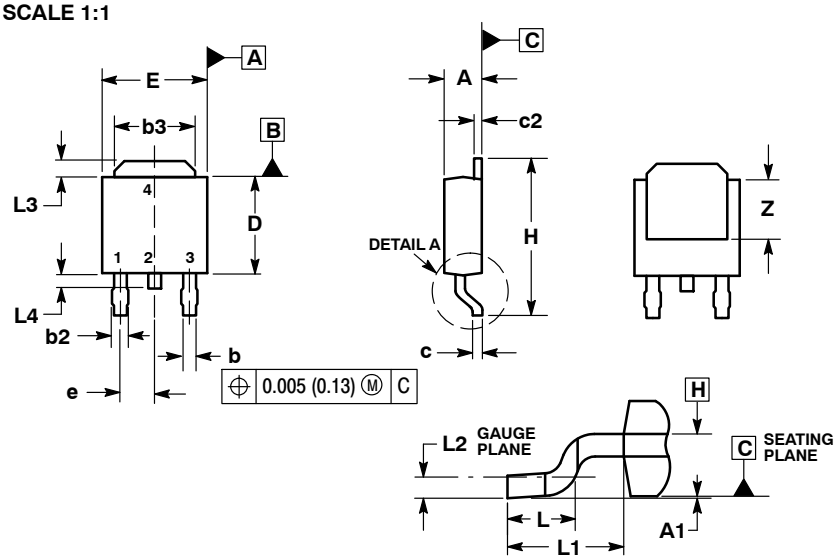
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.




**SCALE 1:1**

## DPAK (SINGLE GUAGE)
CASE 369AA
ISSUE B

DATE 03 JUN 2010




**DETAIL A**
**ROTATED 90° CW**

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.086 | 0.094 | 2.18 | 2.38 |
| A1 | 0.000 | 0.005 | 0.00 | 0.13 |
| b | 0.025 | 0.035 | 0.63 | 0.89 |
| b2 | 0.030 | 0.045 | 0.76 | 1.14 |
| b3 | 0.180 | 0.215 | 4.57 | 5.46 |
| c | 0.018 | 0.024 | 0.46 | 0.61 |
| c2 | 0.018 | 0.024 | 0.46 | 0.61 |
| D | 0.235 | 0.245 | 5.97 | 6.22 |
| E | 0.250 | 0.265 | 6.35 | 6.73 |
| e | 0.090 BSC | | 2.29 BSC | |
| H | 0.370 | 0.410 | 9.40 | 10.41 |
| L | 0.055 | 0.070 | 1.40 | 1.78 |
| L1 | 0.108 REF | | 2.74 REF | |
| L2 | 0.020 BSC | | 0.51 BSC | |
| L3 | 0.035 | 0.050 | 0.89 | 1.27 |
| L4 | --- | 0.040 | --- | 1.01 |
| Z | 0.155 | --- | 3.93 | --- |

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

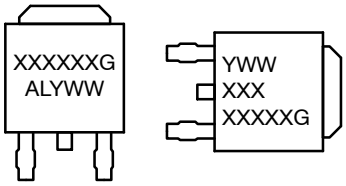
STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

## GENERIC MARKING DIAGRAM*

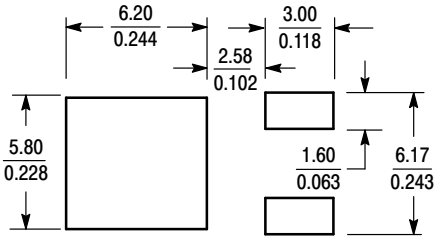



**IC** **Discrete**

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

## SOLDERING FOOTPRINT*

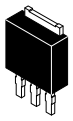



SCALE 3:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98AON13126D** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| **DESCRIPTION:** | **DPAK (SINGLE GAUGE)** | **PAGE 1 OF 1** |

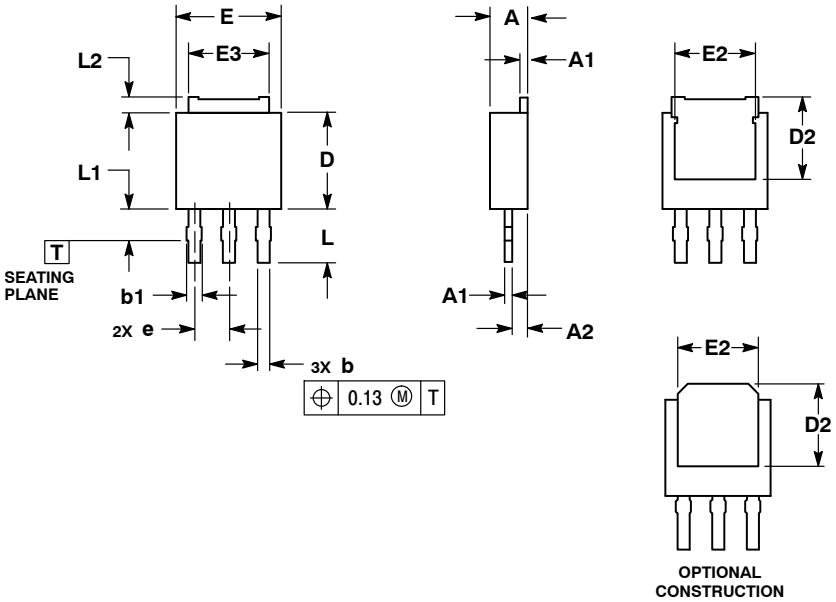
**onsemi** and onsemi are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.



SCALE 1:1

**3.5 MM IPAK, STRAIGHT LEAD**
CASE 369AD
ISSUE B

DATE 18 APR 2013




NOTES:
1.. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2.. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD GATE OR MOLD FLASH.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 2.19 | 2.38 |
| A1 | 0.46 | 0.60 |
| A2 | 0.87 | 1.10 |
| b | 0.69 | 0.89 |
| b1 | 0.77 | 1.10 |
| D | 5.97 | 6.22 |
| D2 | 4.80 | --- |
| E | 6.35 | 6.73 |
| E2 | 4.57 | 5.45 |
| E3 | 4.45 | 5.46 |
| e | 2.28 BSC | |
| L | 3.40 | 3.60 |
| L1 | --- | 2.10 |
| L2 | 0.89 | 1.27 |

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

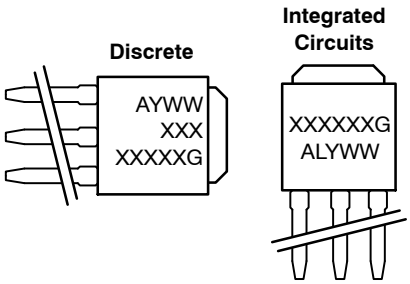
STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

## GENERIC MARKING DIAGRAMS*




XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

| DOCUMENT NUMBER: | 98AON23319D | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
|---|---|---|
| DESCRIPTION: | 3.5 MM IPAK, STRAIGHT LEAD | PAGE 1 OF 1 |

**onsemi** and onsemi are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

**onsemi**, onsemi, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
**Technical Library:** www.onsemi.com/design/resources/technical−documentation
**onsemi Website:** www.onsemi.com

**ONLINE SUPPORT**: www.onsemi.com/support
**For additional information, please contact your local Sales Representative at**
www.onsemi.com/support/sales