

MOSFET – Single, N-Channel, POWERTRENCH®

30 V, 6.5 A, 23 mΩ

FDN537N

General Description

This N-Channel MOSFET is produced using onsemi advanced POWERTRENCH® process that has been optimized for $r_{DS(on)}$, switching performance and ruggedness.

Features

- Max $r_{DS(on)}$ = 23 mΩ @ $V_{GS} = 10$ V, $I_D = 6.5$ A
- Max $r_{DS(on)}$ = 36 mΩ @ $V_{GS} = 4.5$ V, $I_D = 6.0$ A
- High Performance Trench Technology for Extremely Low $r_{DS(on)}$
- High Power and Current Handling Capability in a Widely Used Surface Mount Package
- Fast Switching Speed
- 100% UIL Tested
- This Device is Pb-Free and is RoHS Compliant

Application

- Primary DC-DC Switch

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

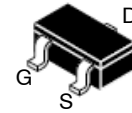
Symbol	Parameter	Value	Unit
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage (Note 3)	± 20	V
I_D	Drain Current	Continuous (Package limited) $T_C = 25^\circ\text{C}$	A
		Continuous (Note 1a) $T_A = 25^\circ\text{C}$	
		Pulsed	
P_D	Power Dissipation	(Note 1a)	W
		(Note 1b)	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

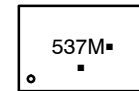
Symbol	Parameter	Max	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	80	$^\circ\text{C}/\text{W}$
	Thermal Resistance, Junction-to-Ambient (Note 1b)	180	

V_{DS}	$R_{DS(on)}$ MAX	I_D MAX
30 V	23 mΩ @ 10 V	6.5 A
	36 mΩ @ 4.5 V	



SOT-23/SUPERSOT™ -23, 3 LEAD, 1.4x2.9
CASE 527AG

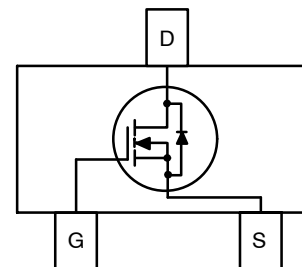
MARKING DIAGRAM



537 = Specific Device Code
M = Month Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

FDN537N

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	30	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C	–	18	–	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24 V, V _{GS} = 0 V	–	–	1	μA
I _{GSS}	Gate to Source Leakage Current, Forward	V _{GS} = 20 V, V _{DS} = 0 V	–	–	100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	1.2	1.8	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C	–	–6	–	mV/°C
r _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 6.5 A	–	19	23	mΩ
		V _{GS} = 4.5 V, I _D = 6.0 A	–	25	36	
		V _{GS} = 10 V, I _D = 6.5 A, T _J = 125°C	–	25	30	
g _{FS}	Forward Transconductance	V _{DD} = 5 V, I _D = 6.5 A	–	24	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	–	360	465	pF
C _{oss}	Output Capacitance		–	143	180	pF
C _{rss}	Reverse Transfer Capacitance		–	22	35	pF
R _g	Gate Resistance		–	1.0	–	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 15 V, I _D = 6.5 A, V _{GS} = 10 V, R _{GEN} = 6 Ω	–	5	10	ns
t _r	Rise Time		–	1	10	ns
t _{d(off)}	Turn-Off Delay Time		–	11	19	ns
t _f	Fall Time		–	1	10	ns
Q _{g(TOT)}	Total Gate Charge	V _{GS} = 0 V to 10 V, V _{DD} = 15 V, I _D = 6.5 A	–	6.0	8.4	nC
		V _{GS} = 0 V to 4.5 V, V _{DD} = 15 V, I _D = 6.5 A	–	3.0	4.2	nC
Q _{gs}	Gate to Source Charge	V _{DD} = 15 V, I _D = 6.5 A	–	1.2	–	nC
Q _{gd}	Gate to Drain “Miller” Charge		–	1.1	–	nC

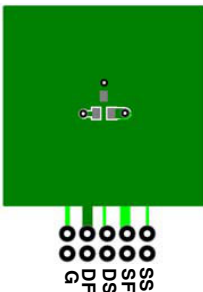
DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = 6.5 A (Note 2)	–	0.86	1.2	V
t _{rr}	Reverse Recovery Time	I _F = 6.5 A, di/dt = 100 A/μs	–	14	22	ns
Q _{rr}	Reverse Recovery Charge		–	3	10	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

- R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.



a) 80°C/W when mounted on a 1 in² pad of 2 oz copper



b) 180°C/W when mounted on a minimum pad

- Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%.
- As an N-ch device, the negative V_{GS} rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

TYPICAL CHARACTERISTICS

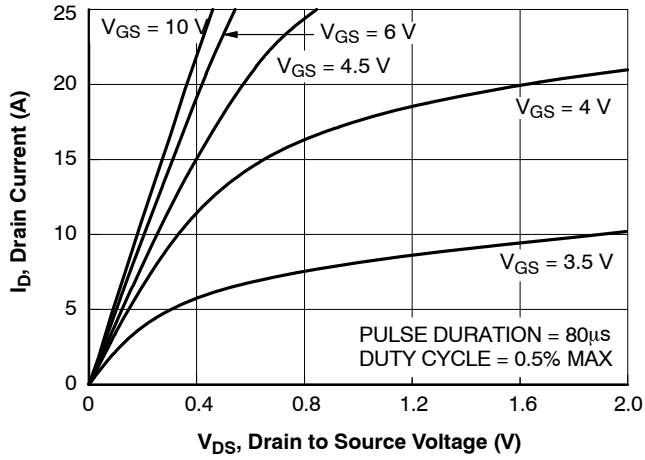
(T_J = 25°C unless otherwise noted)

Figure 1. On Region Characteristics

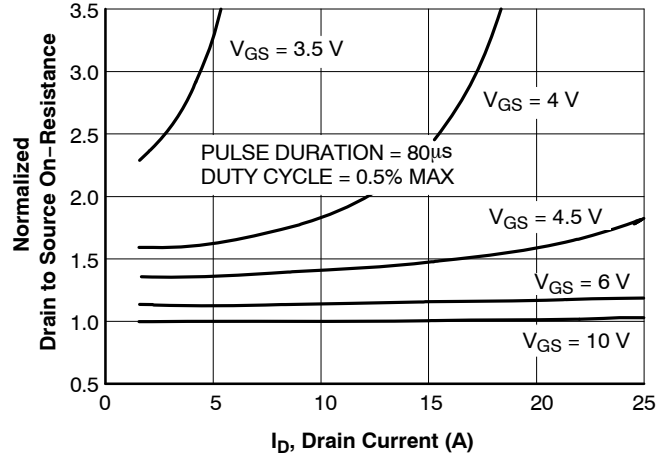


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

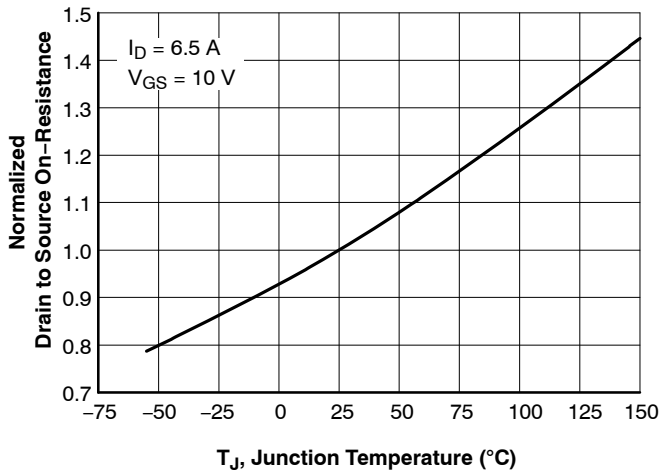


Figure 3. Normalized On-Resistance vs Junction Temperature

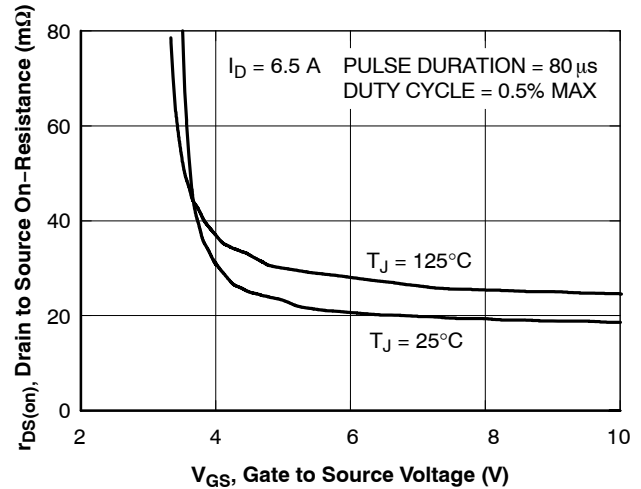


Figure 4. On-Resistance vs Gate to Source Voltage

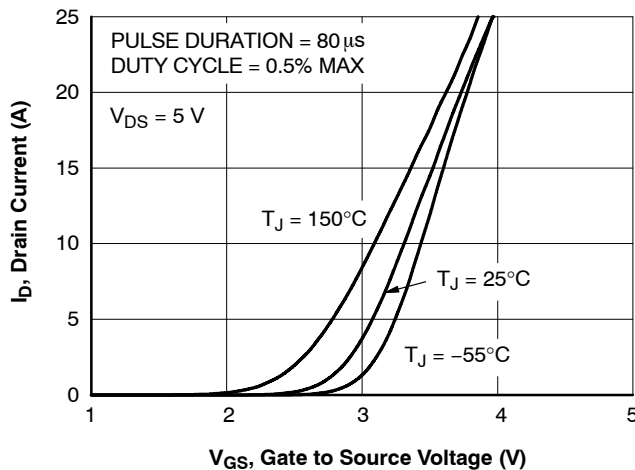


Figure 5. Transfer Characteristics

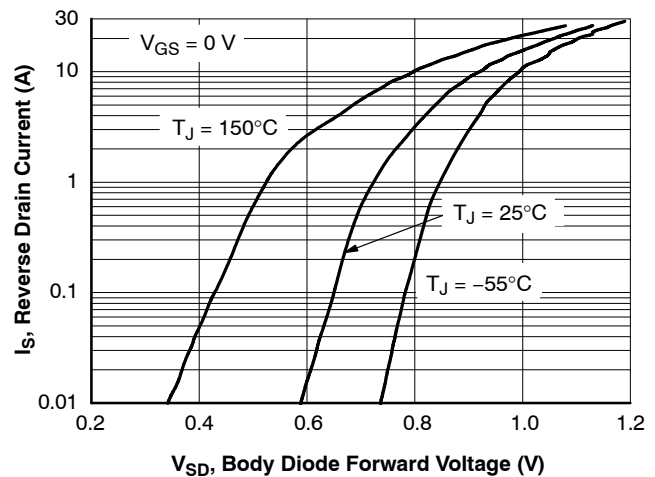


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

TYPICAL CHARACTERISTICS (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

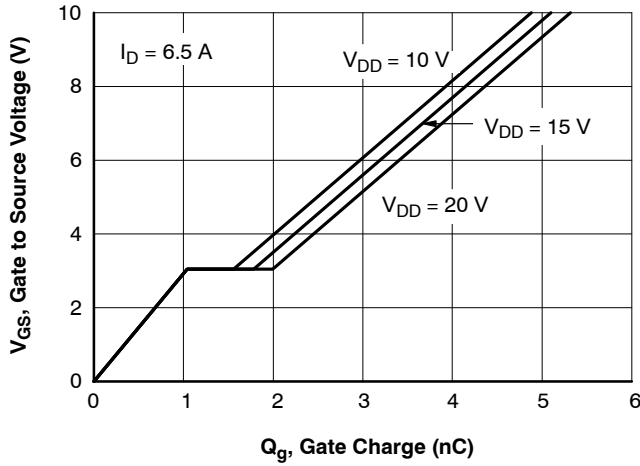


Figure 7. Gate Charge Characteristics

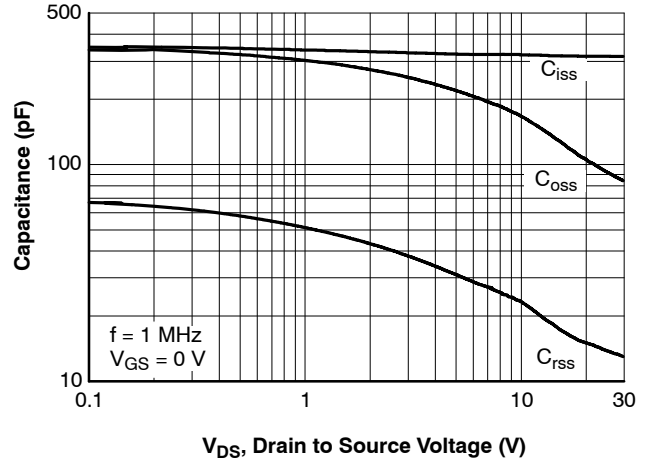


Figure 8. Capacitance vs Drain to Source Voltage

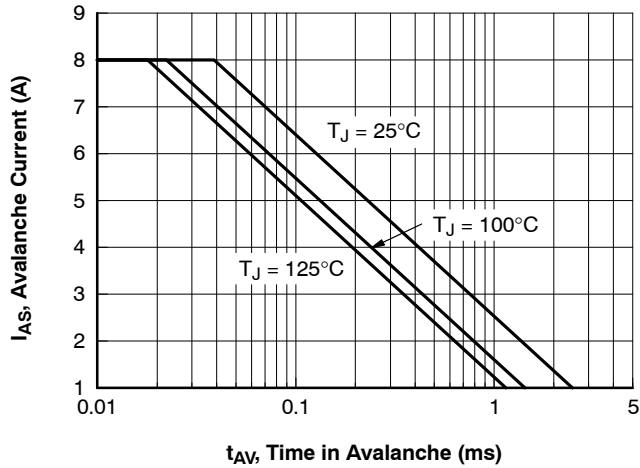


Figure 9. Unclamped Inductive Switching Capability

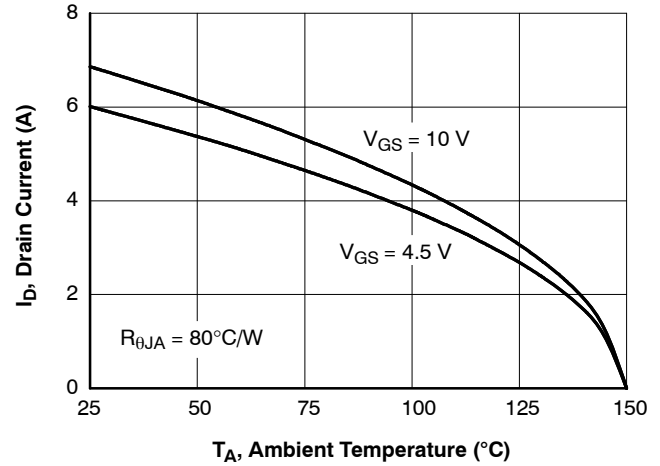


Figure 10. Maximum Continuous Drain Current vs Ambient Temperature

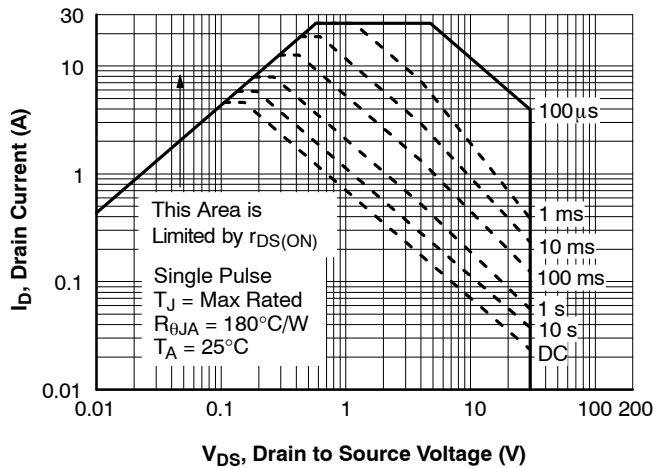


Figure 11. Forward Bias Safe Operating Area

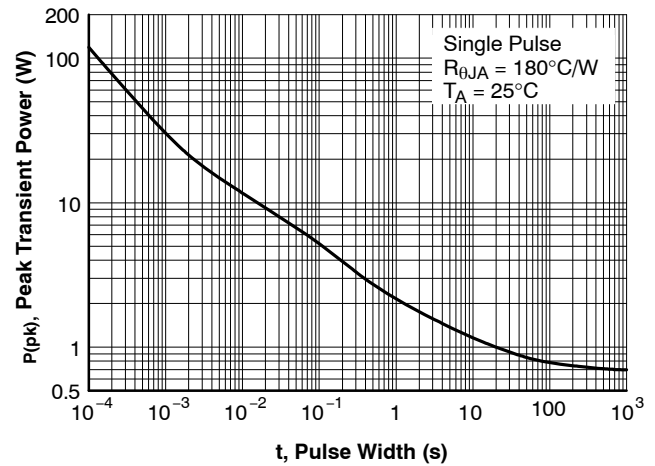


Figure 12. Single Pulse Maximum Power Dissipation

FDN537N

TYPICAL CHARACTERISTICS (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

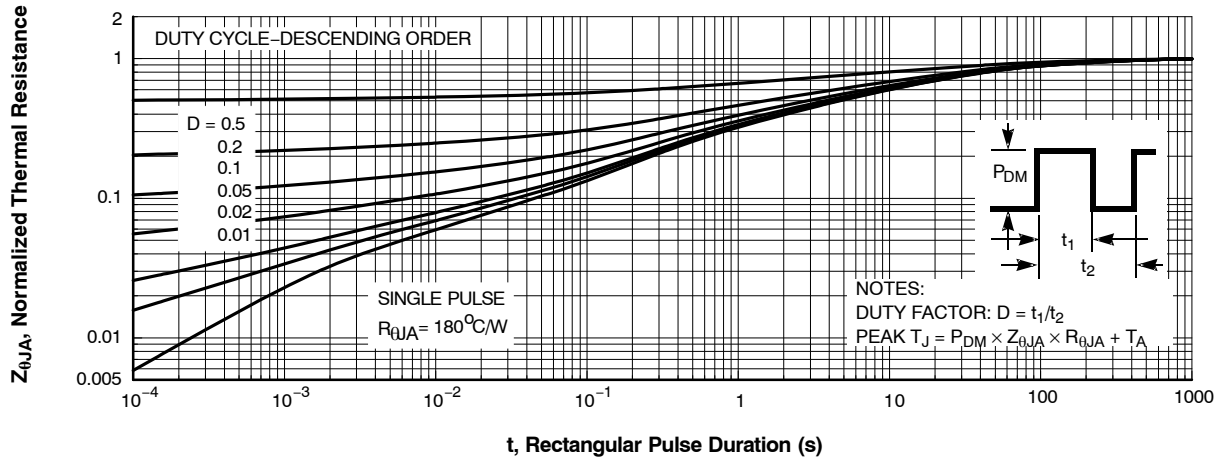


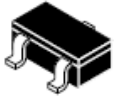
Figure 13. Junction-to-Ambient Transient Thermal Response Curve

PACKAGE MARKING AND ORDERING INFORMATION

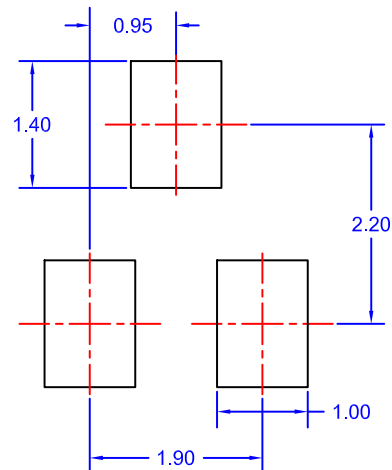
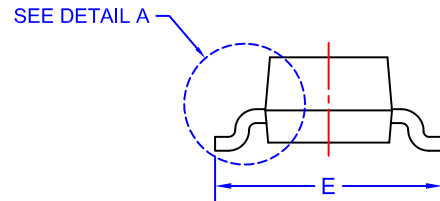
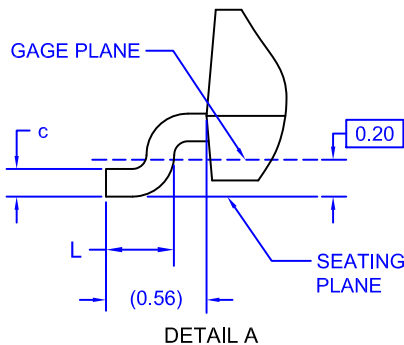
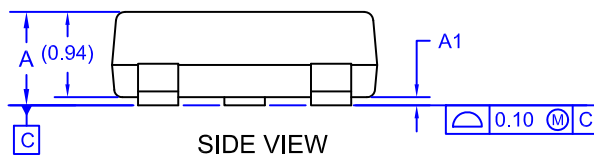
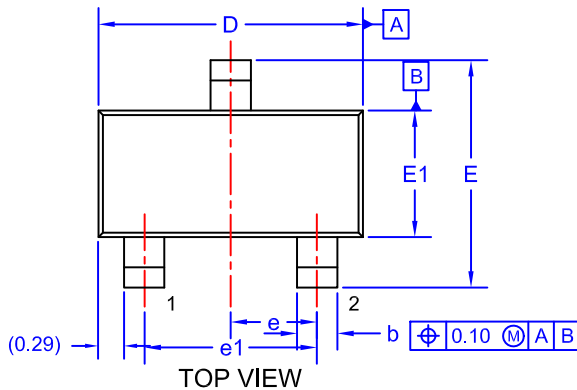
Device	Device Marking	Package	Shipping [†]
FDN537N	537	SOT-23/SUPERSOT-23, 3 LEAD, 1.4x2.9 (Pb-Free, Halide Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

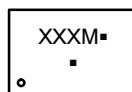
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SOT-23/SUPERSOT™ –23, 3 LEAD, 1.4x2.9
CASE 527AG
ISSUE A

DATE 09 DEC 2019



*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*


XXX = Specific Device Code
M = Month Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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