

MOSFET – Power, N-Channel**80 V, 3.6 mΩ****NVCR4LS3D6N08M7A****Features**

- Typical $R_{DS(on)} = 2.8 \text{ m}\Omega$ at $V_{GS} = 10 \text{ V}$
- Typical $Q_{g(tot)} = 68 \text{ nC}$ at $V_{GS} = 10 \text{ V}$
- AEC-Q101 Qualified
- RoHS Compliant

DIMENSION (μm)

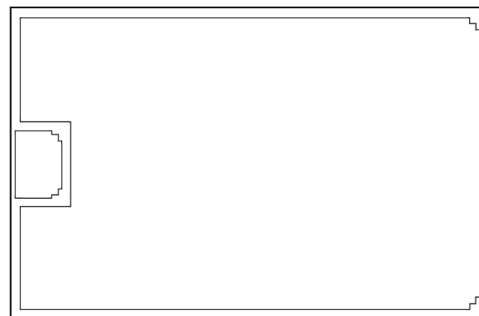
Die Size	3810 × 2463.8
Die Size (Sawn)	3790 ±15 × 2443.8 ±15
Source Attach Area	3606.3 × 2236.4
Gate Attach Area	359.9 × 517.5
Die Thickness	101.6 ±19.1

Gate and Source: AlSiCu
 Drain: Ti–NiV–Ag (back side of die)
 Passivation: Polyimide
 Wafer Diameter: 8 inch
 Wafer Sawn on UV Tape
 Bad Dice Identified in Inking
 Gross Die Counts: 2768

The Chip is 100% Probed to Meet the Conditions and Limits
 Specified at $T_J = 25^\circ\text{C}$.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}$, $V_{GS} = 0 \text{ V}$	80	–	–	V
I_{DSS}	Drain to Source Leakage Current	$V_{DS} = 80 \text{ V}$, $V_{GS} = 0 \text{ V}$	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}$, $V_{DS} = 0 \text{ V}$	–	–	±100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250 \mu\text{A}$	2.0	–	4.0	V
$*R_{DS(on)}$	Bare Die Drain to Source On Resistance	$I_D = 5 \text{ A}$, $V_{GS} = 10 \text{ V}$	–	2.8	3.6	mΩ
V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 5 \text{ A}$, $V_{GS} = 0 \text{ V}$	–	–	1.2	V
E_{AS}	Single Pulse Drain-to-Source Avalanche Energy	$L = 3 \text{ mH}$, $I_{AS} = 16.6 \text{ A}$	413	–	–	mJ

*Accurate $R_{DS(on)}$ test at die level is not feasible for this thin die as limited by the test contact precision attainable in a die form. The max $R_{DS(on)}$ specification is defined from the historical performance of the die in package but is not guaranteed by test in production. The die $R_{DS(on)}$ performance depends on the Source wire/ribbon bonding layout.

**ORDERING INFORMATION**

Device	Package
NVCR4LS3D6N08M7A	Wafer Sawn on Foil

RECOMMENDED STORAGE CONDITIONS

Temperature	22 to 28°C
RH	40 to 66%

NVCR4LS3D6N08M7A

MOSFET MAXIMUM RATINGS in Reference to the FDDL86367–F085 electrical data in D–PAK

($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain to Source Voltage	80	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Continuous Drain Current $R_{\theta JC}$ ($V_{GS} = 10$) (Note 1) $T_C = 25^\circ\text{C}$ $T_C = 100^\circ\text{C}$	164 116	A
E_{AS}	Single Pulse Avalanche Energy (Note 2)	82	mJ
P_D	Power Dissipation $R_{\theta JC}$	227	W
	Derate Above 25°C	1.5	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature	-55 to $+175$	$^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.66	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient (Note 3)	52	$^\circ\text{C}/\text{W}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Current is limited by silicon.
- Starting $T_J = 25^\circ\text{C}$, $L = 40\ \mu\text{H}$, $I_{AS} = 64\ \text{A}$, $V_{DD} = 80\ \text{V}$ during inductor charging and $V_{DD} = 0\ \text{V}$ during time in avalanche.
- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2oz copper.

ELECTRICAL CHARACTERISTICS in Reference to the FDDL86367–F085 electrical data in D–PAK

($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$	80	–	–	V
I_{DSS}	Drain to Source Leakage Current	$V_{DS} = 80\ \text{V}$, $V_{GS} = 0\ \text{V}$	$T_J = 25^\circ\text{C}$	–	–	1 μA
			$T_J = 175^\circ\text{C}$ (Note 4)	–	–	1 mA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}$	–	–	± 100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\ \mu\text{A}$	2.0	3.0	4.0	V
$R_{DS(on)}$	Drain to Source on Resistance	$I_D = 80\ \text{A}$, $V_{GS} = 10\ \text{V}$	$T_J = 25^\circ\text{C}$	–	3.3	4.2 m Ω
			$T_J = 175^\circ\text{C}$ (Note 4)	–	6.6	8.4 m Ω

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 40\ \text{V}$, $V_{GS} = 0\ \text{V}$, $f = 1\ \text{MHz}$	–	4840	–	pF
C_{oss}	Output Capacitance		–	814	–	pF
C_{rss}	Reverse Transfer Capacitance		–	31	–	pF
R_g	Gate Resistance	$f = 1\ \text{MHz}$	–	2.3	–	Ω
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0$ to $10\ \text{V}$, $V_{DD} = 40\ \text{V}$, $I_D = 80\ \text{A}$	–	68	–	nC
$Q_{g(th)}$	Threshold Gate Charge	$V_{GS} = 0$ to $2\ \text{V}$, $V_{DD} = 40\ \text{V}$, $I_D = 80\ \text{A}$	–	8.8	–	nC
Q_{gs}	Gate to Source Gate Charge	$V_{DD} = 40\ \text{V}$, $I_D = 80\ \text{A}$	–	22	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	14	–	nC

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay	$V_{DD} = 40\ \text{V}$, $I_D = 80\ \text{A}$, $V_{GS} = 10\ \text{V}$, $R_{GEN} = 6\ \Omega$	–	20	–	ns
t_r	Rise Time		–	49	–	ns
$t_{d(off)}$	Turn-Off Delay		–	36	–	ns
t_f	Fall Time		–	16	–	ns

DRAIN–SOURCE DIODE CHARACTERISTIC

V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 80\ \text{A}$, $V_{GS} = 0\ \text{V}$	–	–	1.3	V
		$I_{SD} = 40\ \text{A}$, $V_{GS} = 0\ \text{V}$	–	–	1.2	V
t_{rr}	Reverse Recovery Time	$I_F = 80\ \text{A}$, $dI_{SD}/dt = 100\ \text{A}/\mu\text{s}$, $V_{DD} = 64\ \text{V}$	–	68	–	ns
Q_{rr}	Reverse Recovery Charge		–	66	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- The maximum value is specified by design at $T_J = 175^\circ\text{C}$. Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS

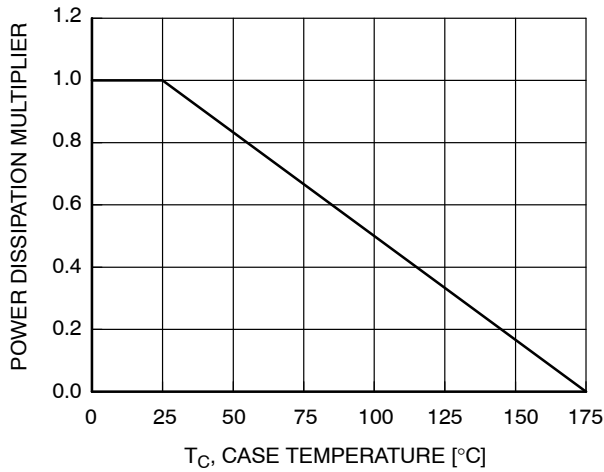


Figure 1. Normalized Power Dissipation vs. Case Temperature

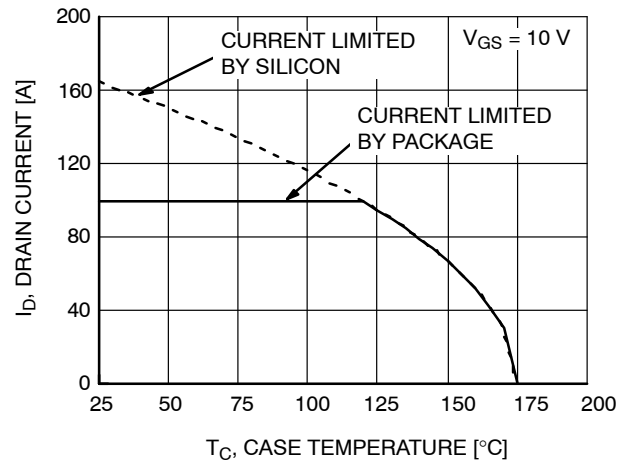


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

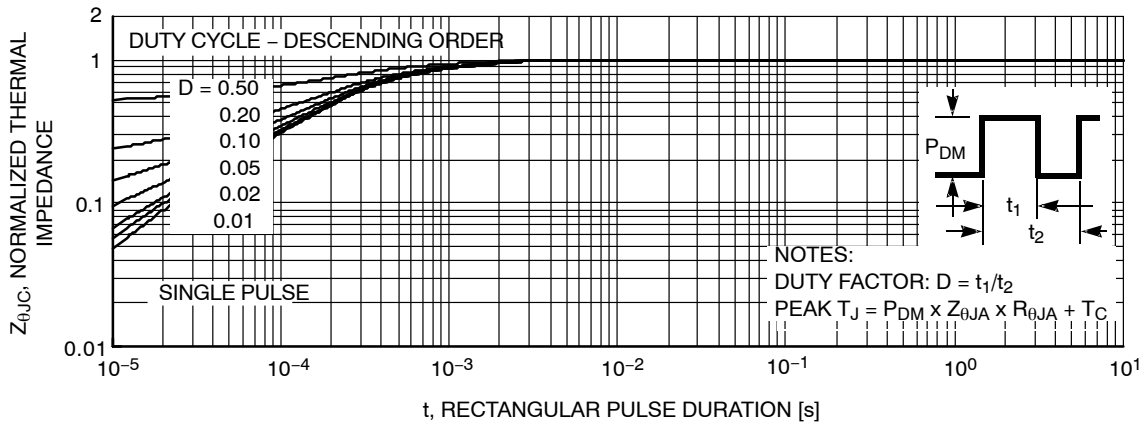


Figure 3. Normalized Maximum Transient Thermal Impedance

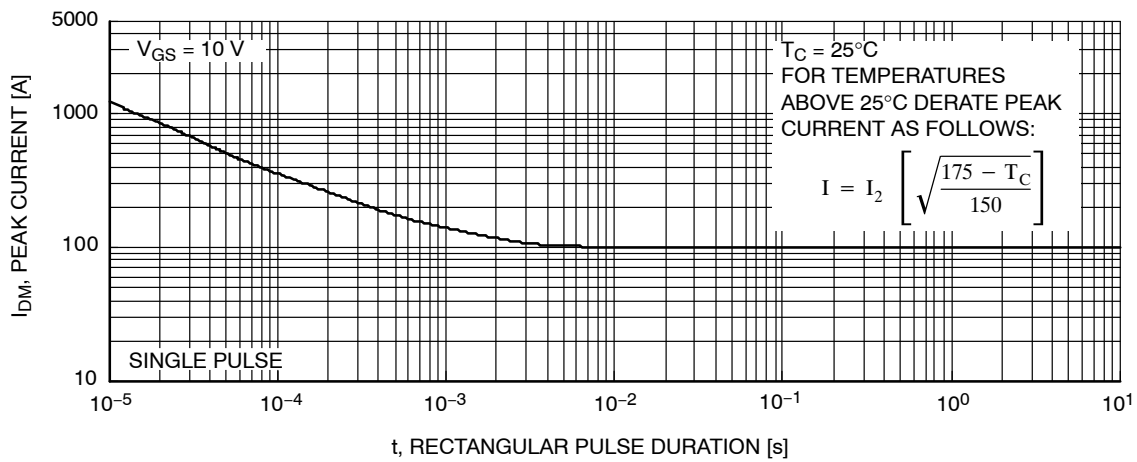


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS (continued)

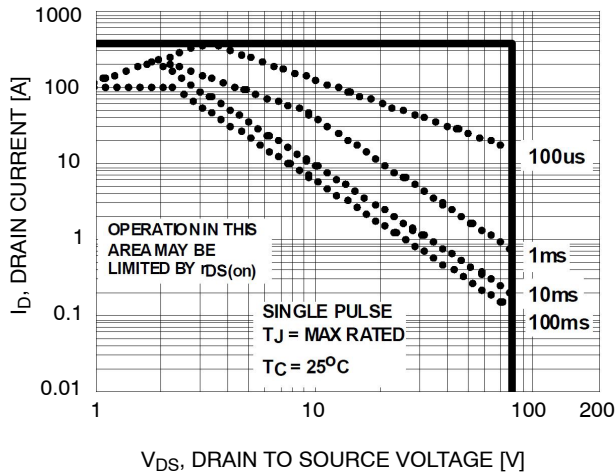
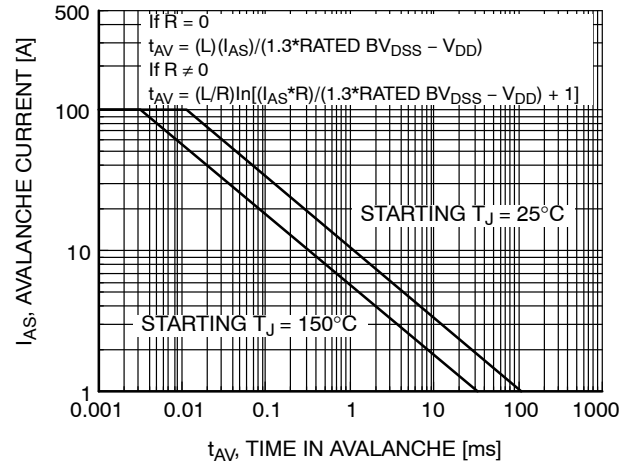


Figure 5. Forward Bias Safe Operating Area



(Note: Refer to onsemi Applications Notes [AN7514](#) and [AN7515](#))

Figure 6. Unclamped Inductive Switching Capability

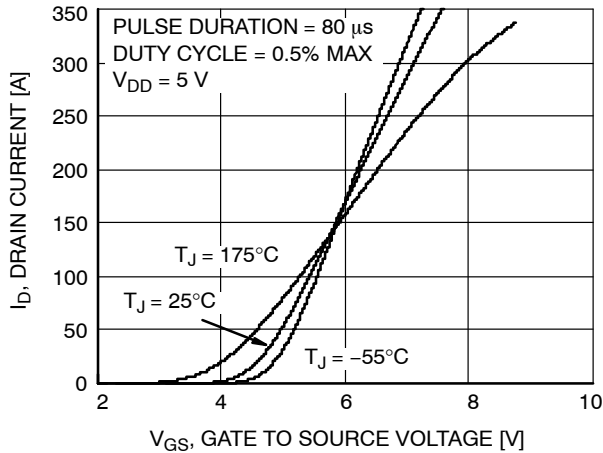


Figure 7. Transfer Characteristics

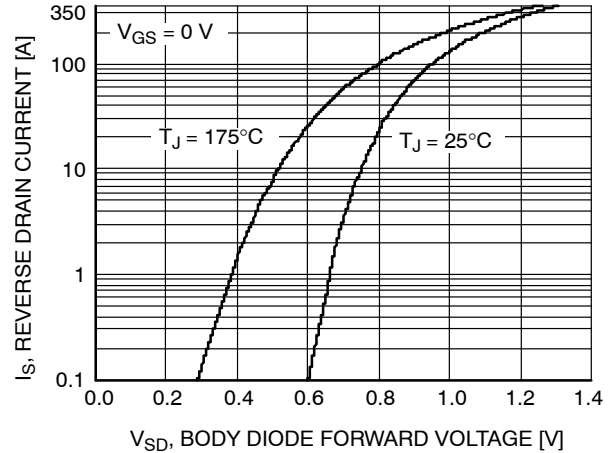


Figure 8. Forward Diode Characteristics

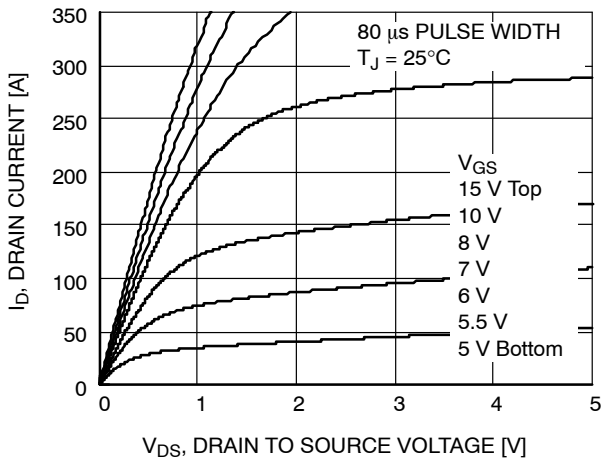


Figure 9. Saturation Characteristics

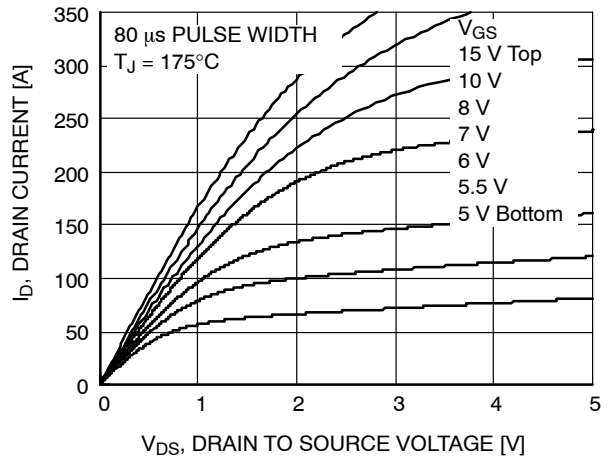


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS (continued)

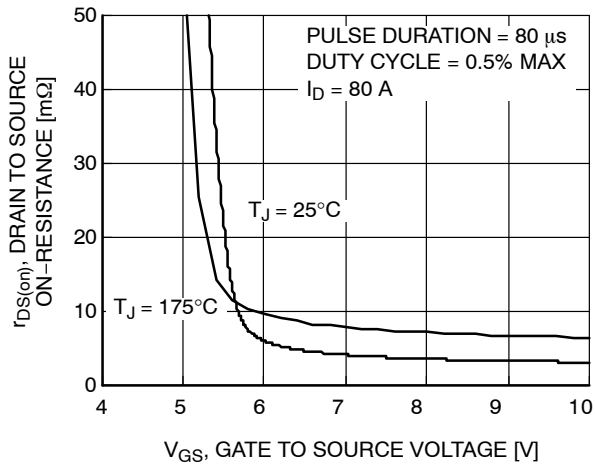


Figure 11. $R_{DS(on)}$ vs. Gate Voltage

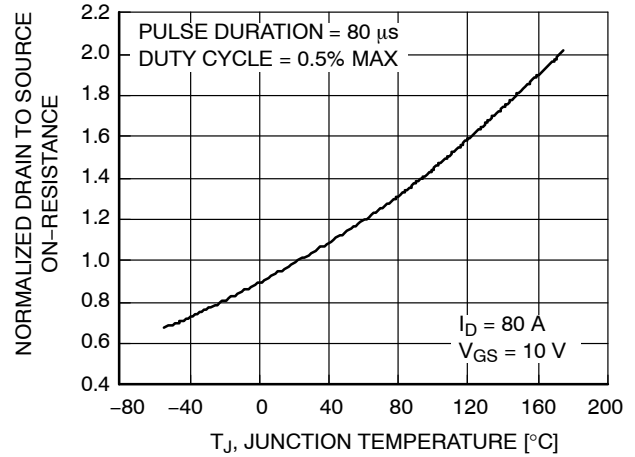


Figure 12. Normalized $R_{DS(on)}$ vs. Junction Temperature

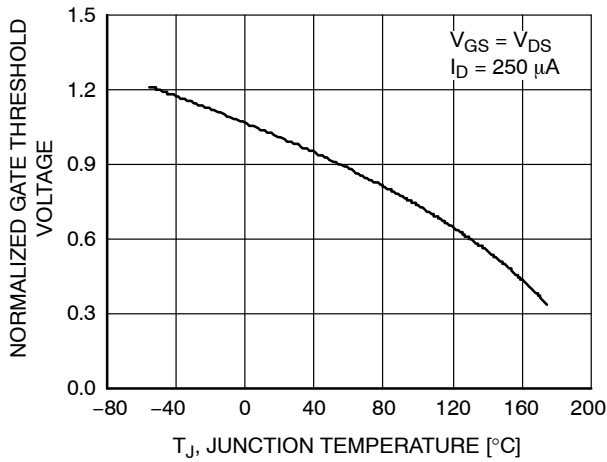


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

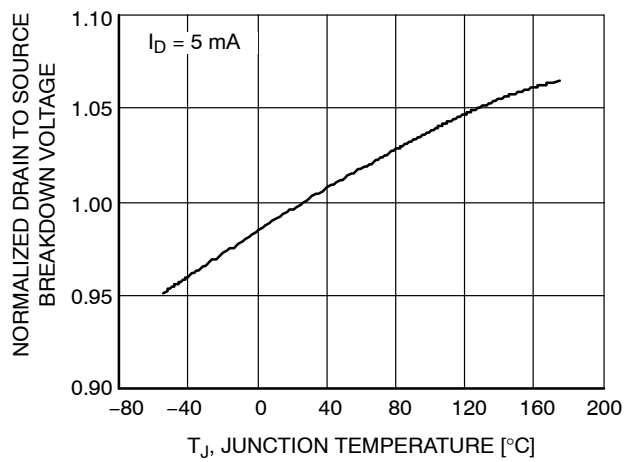


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

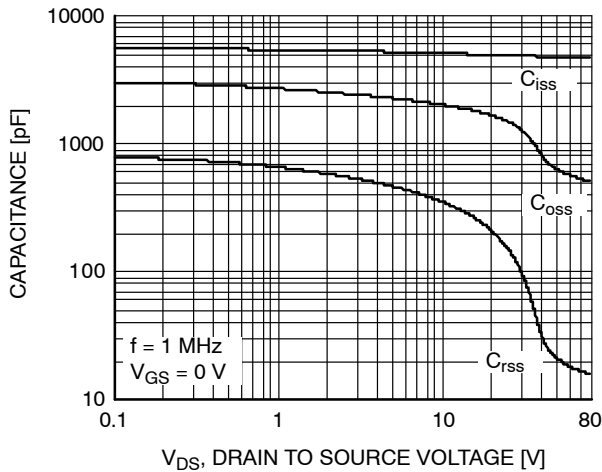


Figure 15. Capacitance vs. Drain to Source Voltage

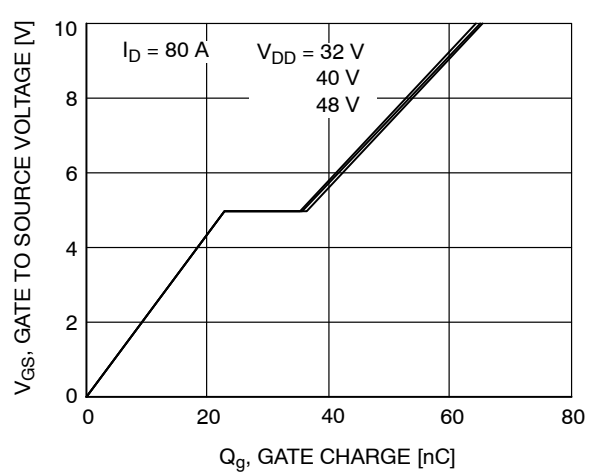


Figure 16. Gate Charge vs. Gate to Source Voltage

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