MOSFET - N-Channel, Shielded Gate PowerTrench
120 V, 2.95 mΩ, 181 A

FDP2D9N12C

ON Semiconductor®

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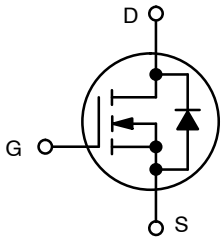
$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
120 V	2.95 mΩ @ 10 V	181 A

Features
- Shielded Gate MOSFET Technology
- Max $R_{DS(on)}$ = 2.95 mΩ at V_{GS} = 10 V, I_D = 181 A
- 50% Lower Qrr than Other MOSFET Suppliers
- Lowers Switching Noise/EMI
- 100% UIL Tested
- These Devices are Pb−Free, Halogen−Free and are RoHS Compliant

Typical Applications
- Synchronous Rectification for ATX / Server / Telecom PSU
- Motor Drives and Uninterruptible Power Supplies
- Micro Solar Inverter



N−CHANNEL MOSFET

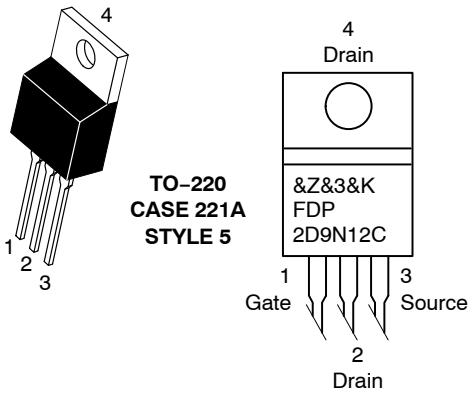
MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	120	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Note 2)	Steady State	T_C = 25°C	I_D	181	A
Power Dissipation $R_{\theta JC}$ (Note 2)			P_D	179	W
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State	T_A = 25°C	I_D	19.5	A
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)			P_D	2.0	W
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	933	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +150	°C
Source Current (Body Diode)			I_S	172	A
Single Pulse Drain−to−Source Avalanche Energy (I_{AV} = 99 A_{pk}, L = 0.1 mH)			E_{AS}	490	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8″ from case for 10 s)			T_L	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface−mounted on FR4 board using a 1 in^2 pad size, 1 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

MARKING DIAGRAM



&Z = Assembly Plant Code
&3 = Date Code (Year & Week)
&K = Lot

ORDERING INFORMATION

Device	Package	Shipping†
FDP2D9N12C	TO−220 (Pb−Free)	50 / Tube, 800 / Box

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction−to−Case − Steady State (Note 2)	$R_{\theta JC}$	0.7	°C/W
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	62.5	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		120			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = 250 μA, ref to 25°C			46		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 96 V	T_J = 25°C			1	μA
			T_J = 150°C			100	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 664 μA		2.0	3.1	4.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	I_D = 664 μA, ref to 25°C			−8.6		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 95 A			2.7	2.95	mΩ
		V_{GS} = 6 V, I_D = 57 A			3.5	5.1	mΩ
Forward Transconductance	g_{FS}	V_{DS} = 10 V, I_D = 50 A			215		S
CHARGES, CAPACITANCES & GATE RESISTANCE							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 60 V			7910	12883	pF
Output Capacitance	C_{OSS}				3825		
Reverse Transfer Capacitance	C_{RSS}				32		
Gate−Resistance	R_G				0.78	1.9	Ω
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 60 V; I_D = 95 A			98	137	nC
Threshold Gate Charge	$Q_{G(TH)}$				23		
Gate−to−Source Charge	Q_{GS}				35		
Gate−to−Drain Charge	Q_{GD}				15		
Plateau Voltage	V_{GP}				5.0		V
Output Charge	Q_{OSS}	V_{DD} = 60 V, V_{GS} = 0 V			325		nC
SWITCHING CHARACTERISTICS (Note 4)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DD} = 60 V, I_D = 95 A, R_G = 6.0 Ω			43		ns
Rise Time	t_r				31		
Turn−Off Delay Time	$t_{d(OFF)}$				72		
Fall Time	t_f				24		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 95 A	T_J = 25°C		0.9	1.3	V
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, V_{DD} = 60 V dI_S/dt = 300 A/μs, I_S = 100 A			88		ns
Charge Time	t_a				48		
Discharge Time	t_b				40		
Reverse Recovery Charge	Q_{RR}				500		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

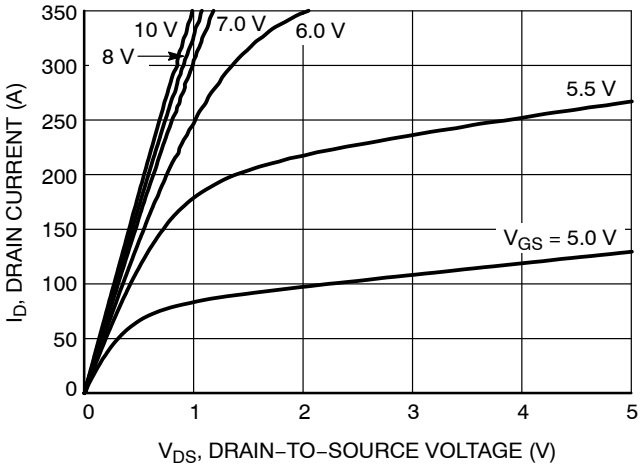


Figure 1. On−Region Characteristics

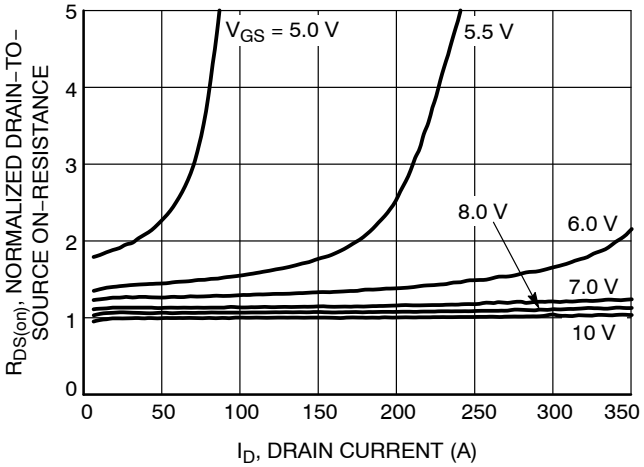


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

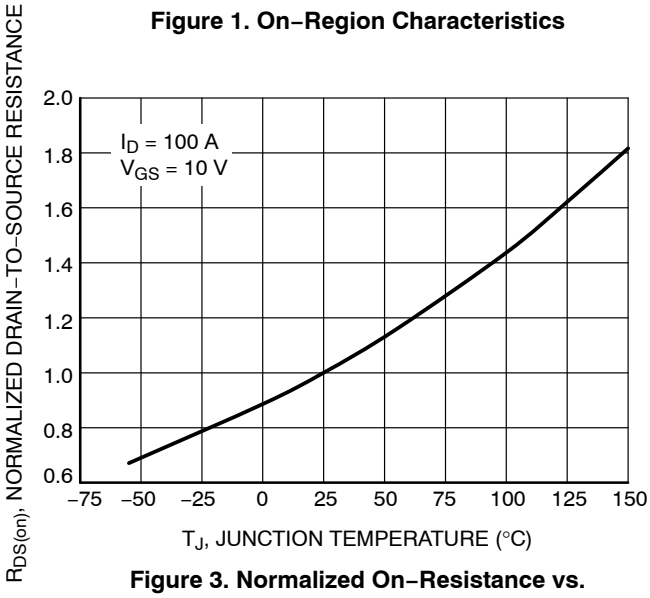


Figure 3. Normalized On−Resistance vs. Junction Temperature

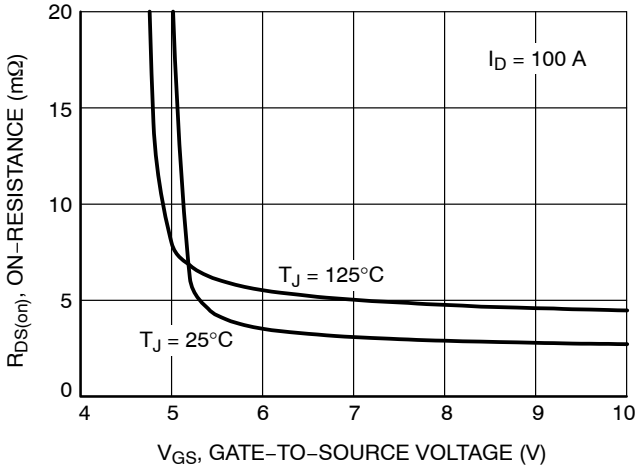


Figure 4. On−Resistance vs. Gate−to−Source Voltage

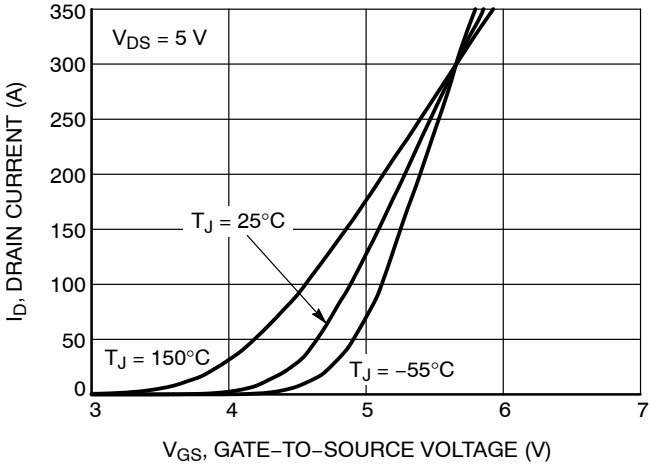


Figure 5. Transfer Characteristics

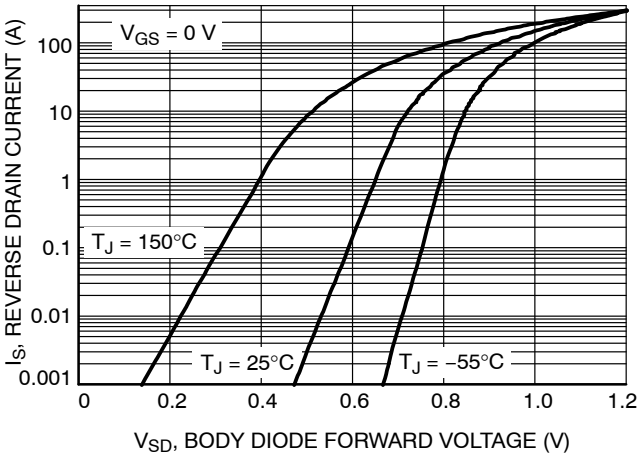


Figure 6. Source−to−Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS

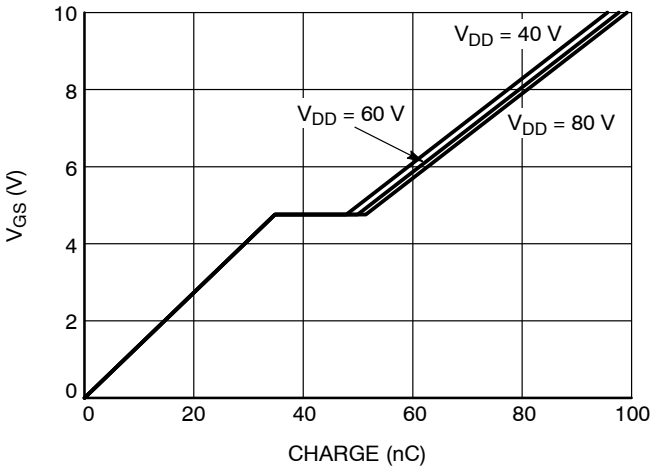


Figure 7. Gate Charge Characteristics

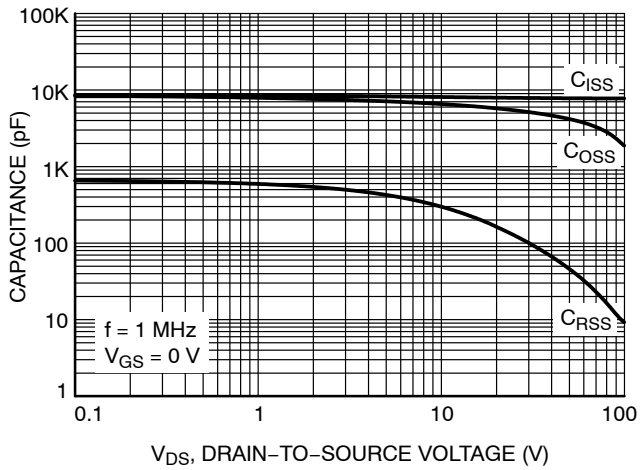


Figure 8. Capacitance vs. Drain−to−Source Voltage

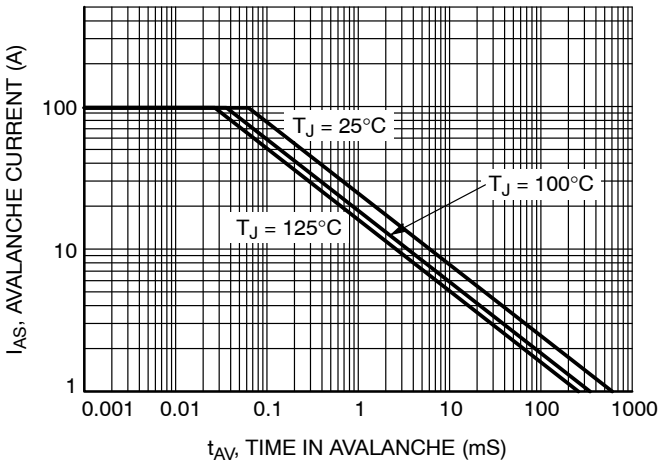


Figure 9. Unclamped Inductive Switching Capability

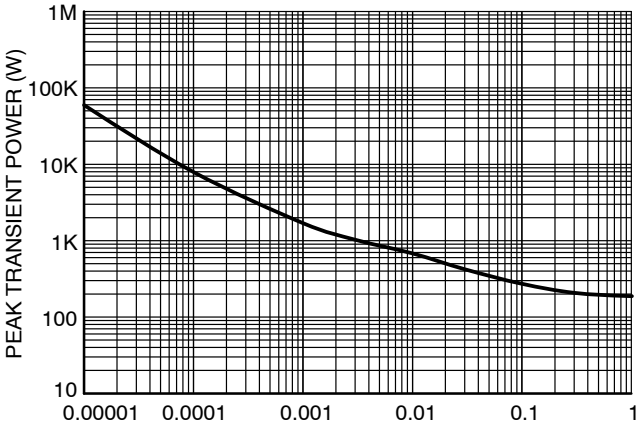


Figure 10. Peak Power

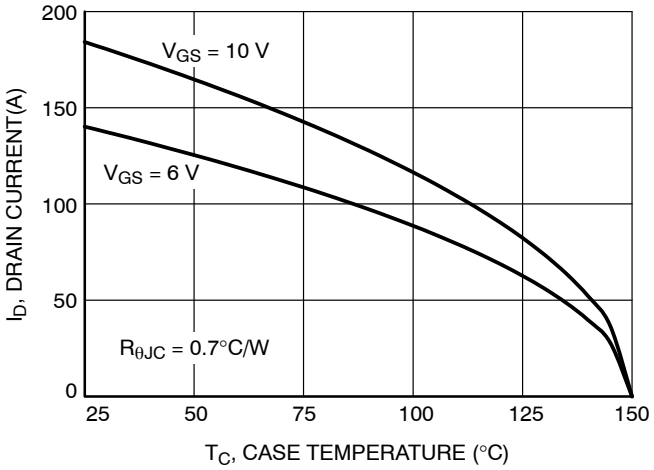


Figure 11. Drain Current vs. Case Temperature

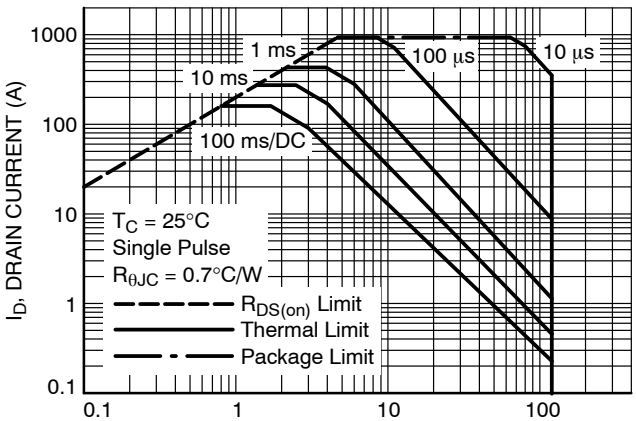


Figure 12. Forward Bias Safe Operating Area

TYPICAL CHARACTERISTICS

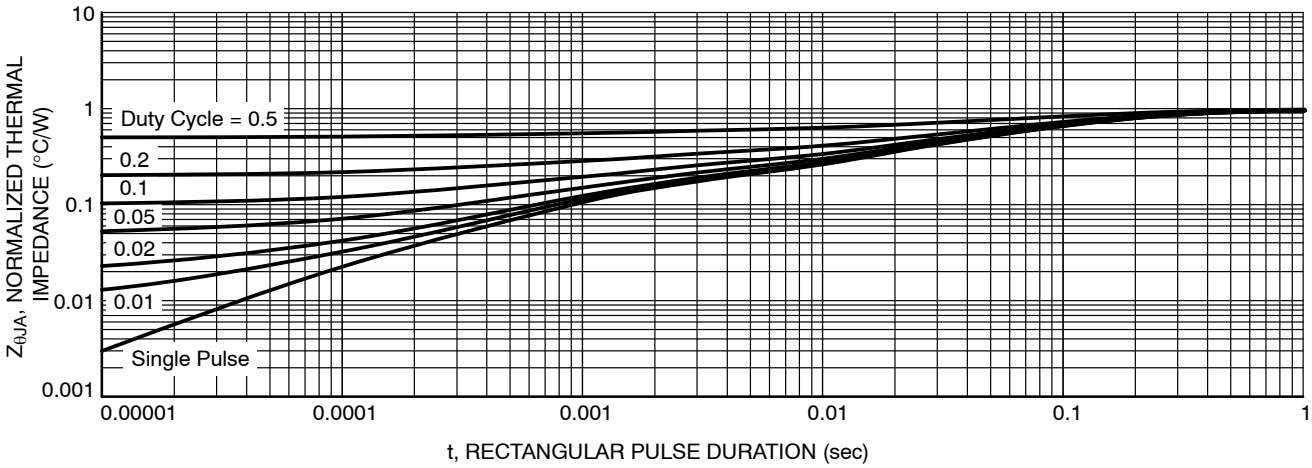
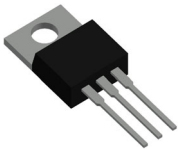
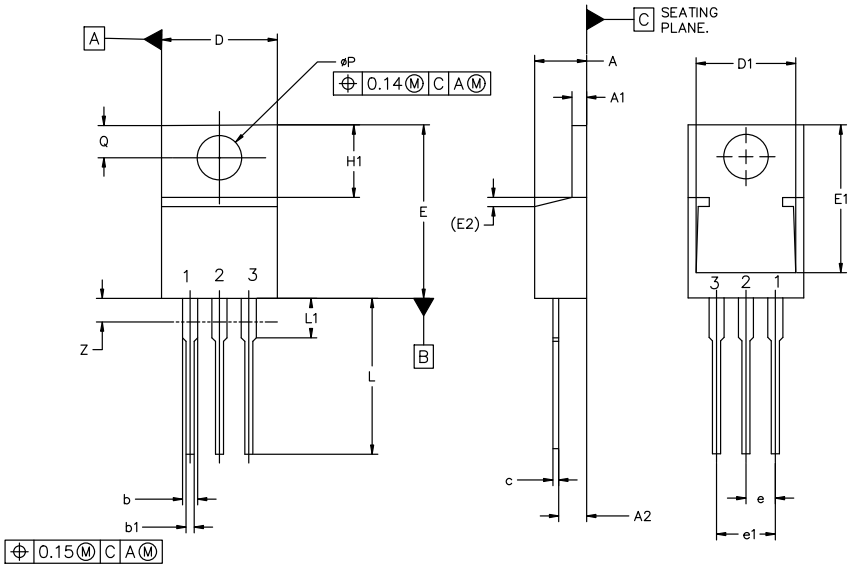


Figure 13. Transient Thermal Impedance



TO−220−3 10.10x15.12x4.45, 2.54P
CASE 221A
ISSUE AL

DATE 05 FEB 2025



MILLIMETERS			
DIM	MIN	NOM	MAX
A	4.07	4.45	4.83
A1	1.15	1.28	1.41
A2	2.04	2.42	2.79
b	1.15	1.34	1.52
b1	0.64	0.80	0.96
c	0.36	0.49	0.61
D	9.66	10.10	10.53
D1	8.43	8.63	8.83
E	14.48	15.12	15.75
E1	12.58	12.78	12.98
E2	1.27 REF		

MILLIMETERS			
DIM	MIN	NOM	MAX
e	2.42	2.54	2.66
e1	4.83	5.08	5.33
H1	5.97	6.22	6.47
L	12.70	13.49	14.27
L1	2.80	3.45	4.10
Q	2.54	2.79	3.04
øP	3.60	3.85	4.09
Z	–.––	–.––	3.48

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 8:
PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE

STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 10:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE

STYLE 11:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. NOT CONNECTED

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