

MOSFET – N-Channel, UniFET™

500 V, 48 A, 105 mΩ

FDH50N50, FDA50N50

Description

UniFET MOSFET is ON Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.

Features

- $R_{DS(on)} = 89 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 24 \text{ A}$
- Low Gate Charge (Typ. 105 nC)
- Low C_{rss} (Typ. 45 pF)
- 100% Avalanche Tested
- Improved dv/dt Capability
- These Devices are Pb-Free and are RoHS Compliant

Applications

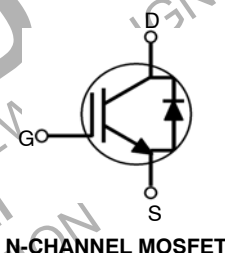
- Lighting
- Uninterruptible Power Supply
- AC-DC Power Supply



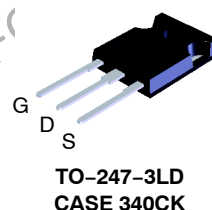
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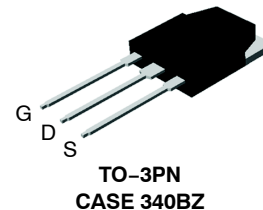
V_{DS}	$R_{DS(on)} \text{ MAX}$	$I_D \text{ MAX}$
500 V	105 mΩ @ 10 V	48 A



N-CHANNEL MOSFET

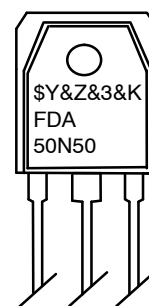
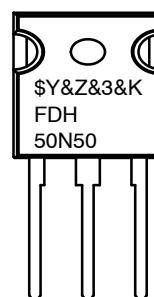


TO-247-3LD
CASE 340CK



TO-3PN
CASE 340BZ

MARKING DIAGRAM



\$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FDH50N50, FDA50N50	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FDH50N50, FDA50N50

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	FDH50N50–F133/ FDA50N50	Unit
V _{DSS}	Drain to Source Voltage	500	V
I _D	Drain Current – –Continuous (T _C = 25°C) –Continuous (T _C = 100°C)	48 30.8	A A
I _{DM}	Drain Current –Pulsed (Note 1)	192	A
V _{GSS}	Gate–Source Voltage	±20	V
E _{AS}	Single Pulsed Avalanche Energy (Note 2)	1868	mJ
I _{AR}	Avalanche Current (Note 1)	48	A
E _{AR}	Repetitive Avalanche Energy (Note 1)	62.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	20	V/ns
P _D	Power Dissipation (T _C = 25°C) –Derate Above 25°C	625 5	W W/°C
T _J , T _{STG}	Operating and Storage Temperature Range	–55 to + 150	°C
T _L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Second	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive Rating: Pulse width limited by maximum junction temperature.

2. L = 1.46 mH, I_{AS} = 48 A, V_{DD} = 50 V, R_G = 25 Ω, Starting T_J = 25 °C.

3. I_{SD} ≤ 48 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25 °C.

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Mark	Package	Package Method	Reel Size	Tape Width	Quantity
FDH50N50–F133	FDH50N50	TO–247–3	Tube	N/A	N/A	30 Units
FDA50N50	FDA50N50	TO–3PN	Tube	N/A	N/A	30 Units

THERMAL CHARACTERISTICS

Symbol	Parameter	FDH50N50–F133/ FDA50N50	Unit
R _{θJC}	Thermal Resistance, Junction to Case, Max.	0.2	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient, Max.	40	

FDH50N50, FDA50N50

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	500	–	–	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	–	0.5	–	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 500 V, V _{GS} = 0 V	–	–	25	μA
		V _{DS} = 400 V, T _C = 125°C	–	–	250	μA
I _{GSSF}	Gate–Body Leakage Current, Forward	V _{GS} = 20 V, V _{DS} = 0 V	–	–	100	nA
I _{GSSR}	Gate–Body Leakage Current, Reverse	V _{GS} = –20 V, V _{DS} = 0 V	–	–	–100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	3.0	–	5.0	V
R _{DS(on)}	Static Drain–Source On–Resistance	V _{GS} = 10 V, I _D = 24 A	–	0.089	0.105	Ω
g _{FS}	Forward Transconductance	V _{DS} = 40 V, I _D = 48 A	–	20	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz	–	4979	6460	pF
C _{oss}	Output Capacitance		–	760	1000	pF
C _{rss}	Reverse Transfer Capacitance		–	50	65	pF
C _{oss}	Output Capacitance	V _{DS} = 400 V, V _{GS} = 0 V, f = 1 MHz	–	161	–	pF
C _{oss(eff.)}	Effective Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V	–	342	–	pF

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 250 V, I _D = 48 A, V _{GS} = 10 V, R _G = 25 Ω (Note 4)	–	105	220	ns
t _r	Turn-On Rise Time		–	360	730	ns
t _{d(off)}	Turn-Off Delay Time		–	225	460	ns
t _f	Turn-Off Fall Time		–	230	470	ns
Q _g	Total Gate Charge	V _{DS} = 400 V, I _D = 48 A, V _{GS} = 10 V (Note 4)	–	105	137	nC
Q _{gs}	Gate–Source Charge		–	33	–	nC
Q _{gd}	Gate–Drain Charge		–	45	–	nC

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I _S	Maximum Continuous Drain–Source Diode Forward Current		–	–	48	A
I _{SM}	Maximum Pulsed Drain–Source Diode Forward Current		–	–	192	A
V _{SD}	Source to Drain Diode Voltage	V _{GS} = 0 V, I _S = 48 A	–	–	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 48 A, dI _F /dt = 100 A/μs	–	580	–	ns
Q _{rr}	Reverse Recovery Charge		–	10	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially Independent of Operating Temperature Typical Characteristics.

TYPICAL CHARACTERISTICS

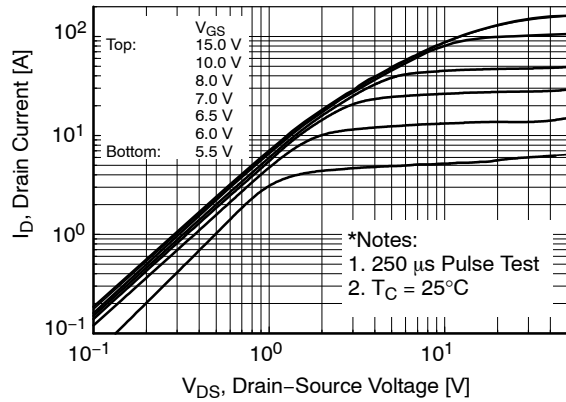


Figure 1. On-Region Characteristics

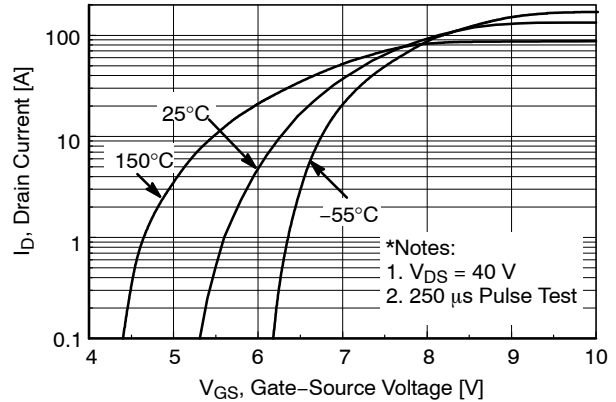


Figure 2. Transfer Characteristics

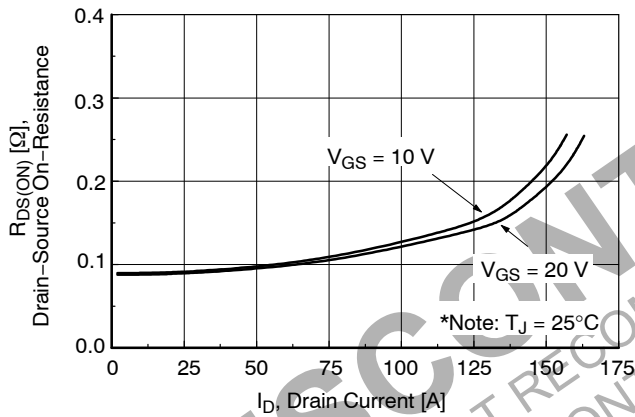


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

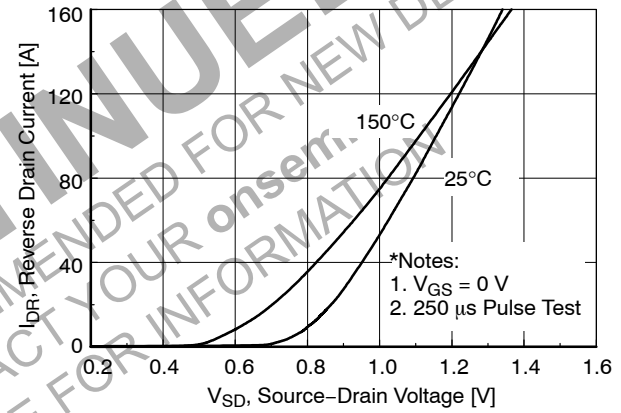


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

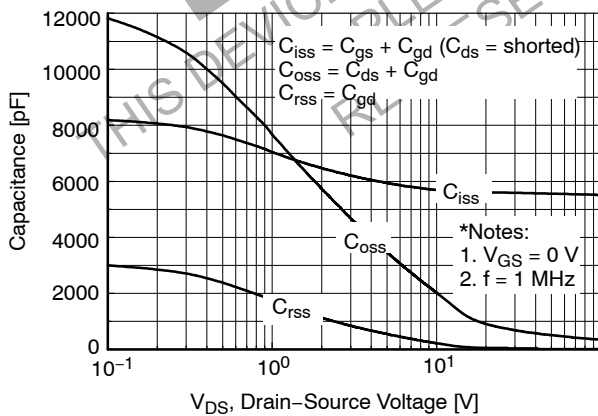


Figure 5. Capacitance Characteristics

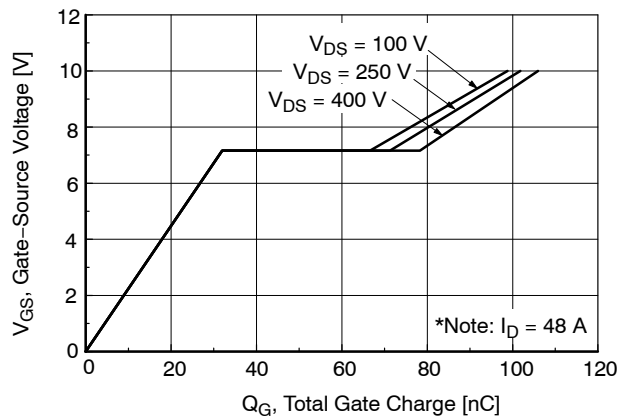


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS

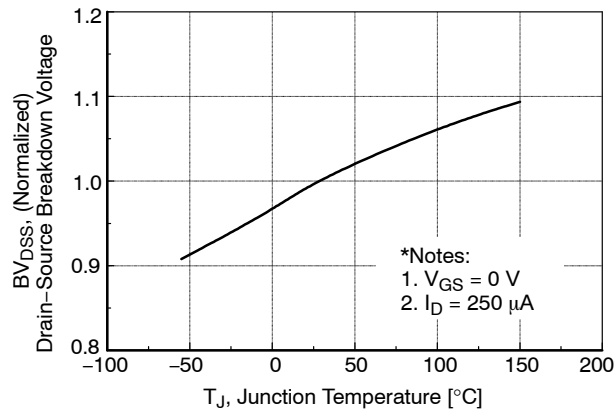


Figure 7. Breakdown Voltage Variation vs. Temperature

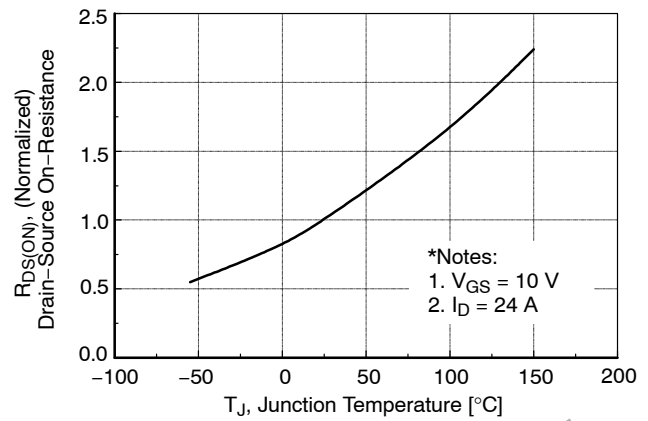


Figure 8. On-Resistance Variation vs. Temperature

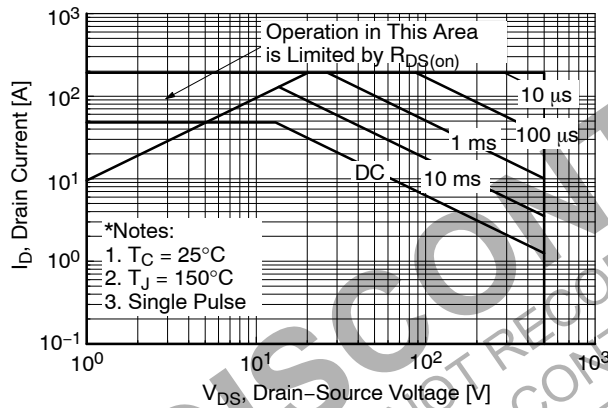


Figure 9. Maximum Safe Operating Area

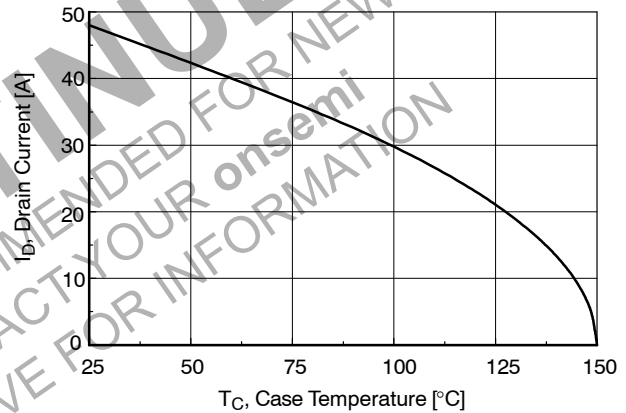


Figure 10. Maximum Drain Current vs. Case Temperature

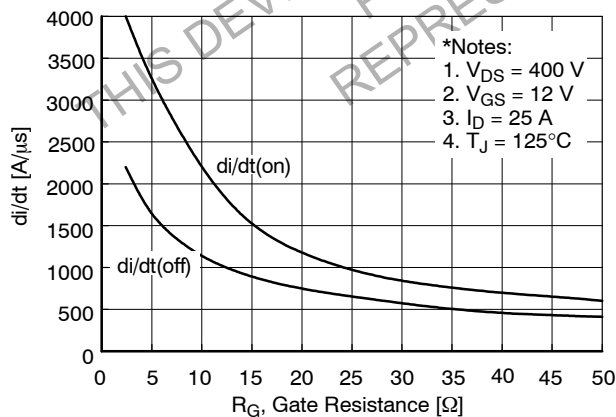


Figure 11. Typical Drain Current Slope vs. Gate Resistance

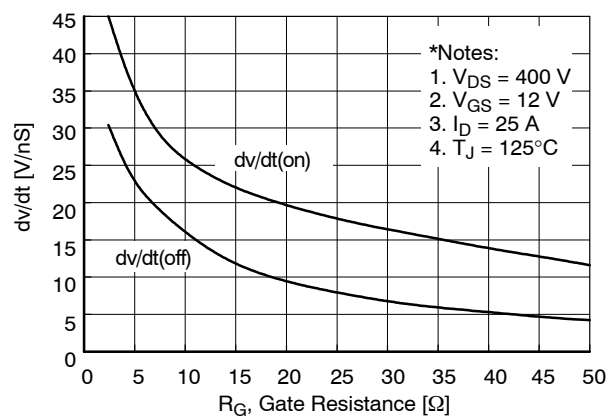


Figure 12. Typical Drain-Source Voltage Slope vs. Gate Resistance

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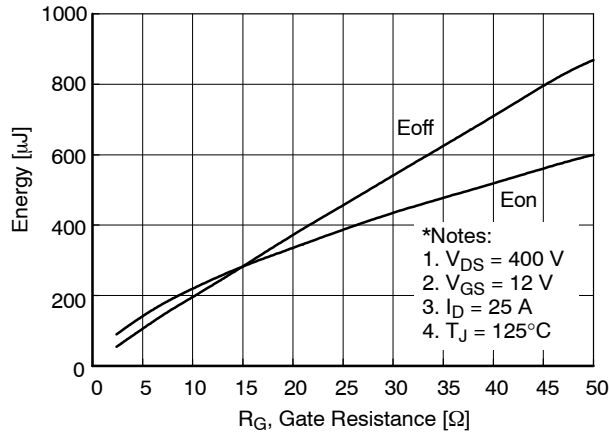


Figure 13. Typical Switching Losses vs. Gate Resistance

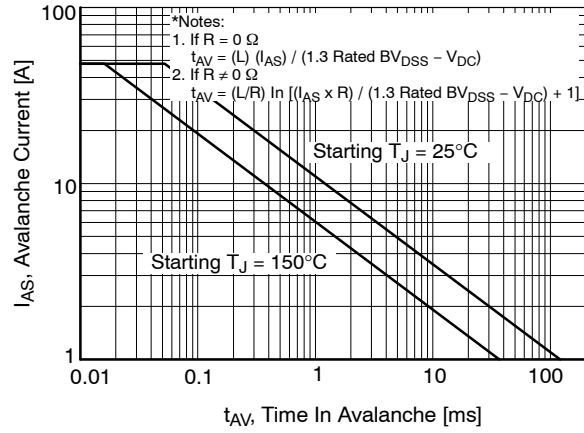


Figure 14. Unclamped Inductive Switching Capability

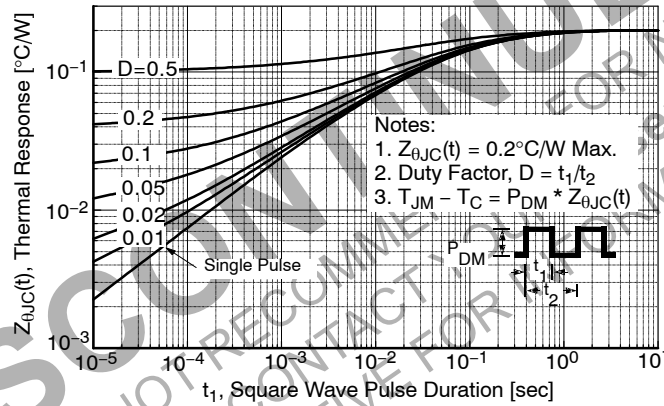
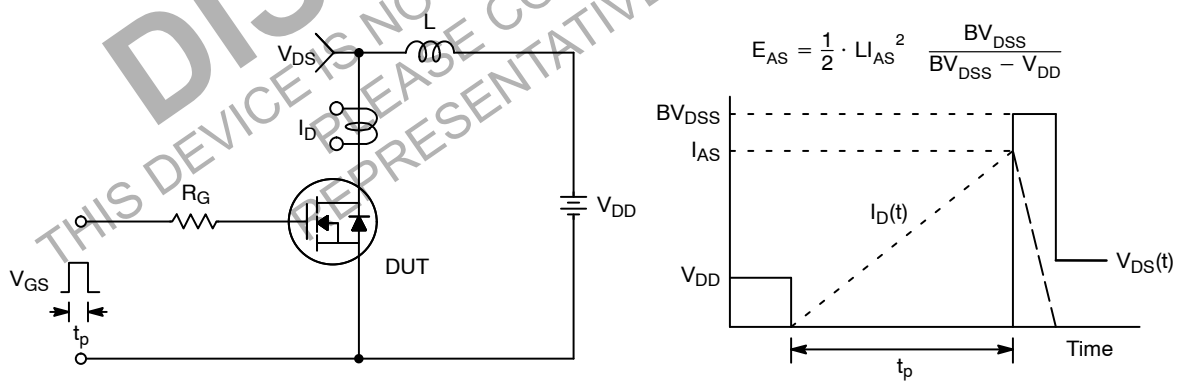
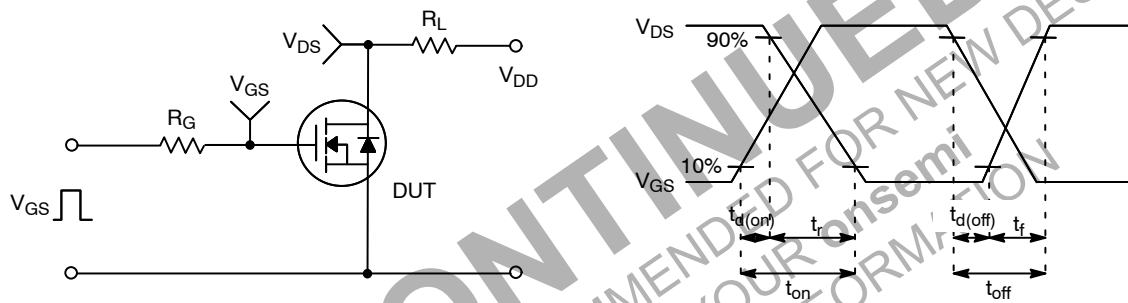
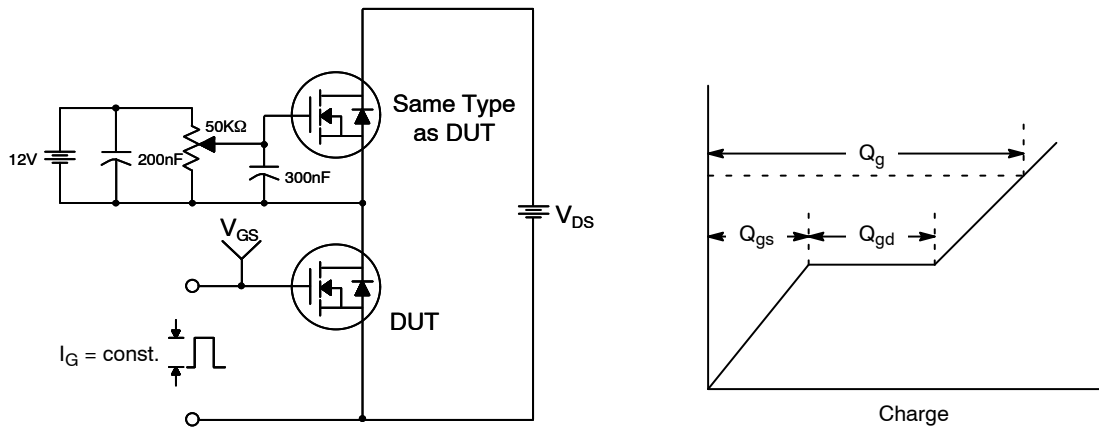


Figure 15. Transient Thermal Resistance Curve

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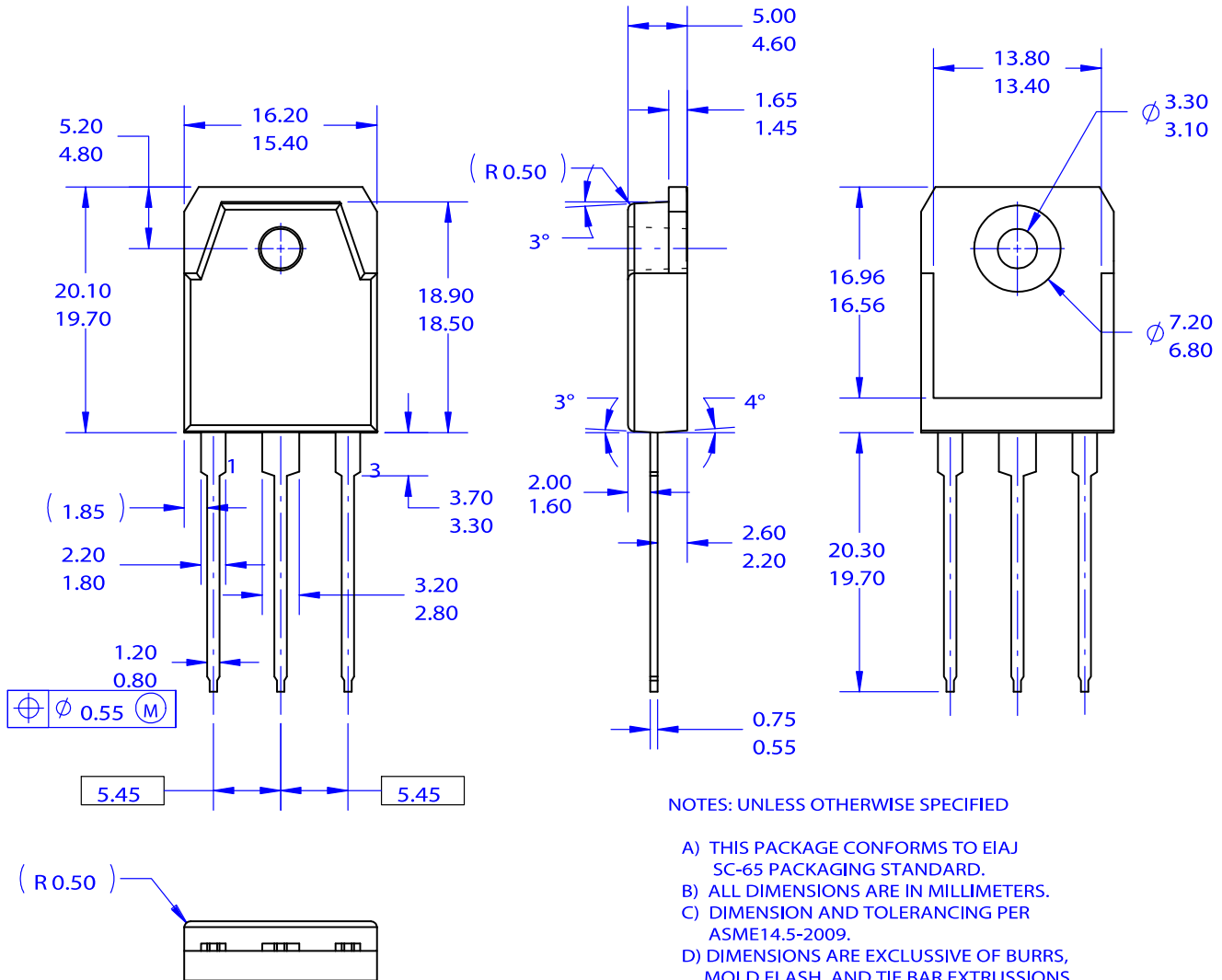
The diagram illustrates the timing relationships for a MOSFET switching event. It includes the following waveforms and parameters:

- V_{GS} (Gate Voltage):** A square wave pulse. The pulse width is defined by the duty cycle $D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$. The pulse amplitude is 10 V.
- V_{DS} (Drain-Source Voltage):** A square wave pulse that transitions from 0 V to V_{DD} when the MOSFET is turned on.
- I_{SD} (Source Drain Current):** The current flowing through the MOSFET during the on-state.
- Body Diode Forward Current:** The current flowing through the body diode when the MOSFET is in the linear region.
- Body Diode Reverse Current:** The current flowing through the body diode when the MOSFET is in the saturation region.
- Body Diode Recovery dv/dt :** The rate of change of drain-source voltage during the reverse recovery of the body diode.

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ISSUE O

DATE 31 OCT 2016



NOTES: UNLESS OTHERWISE SPECIFIED

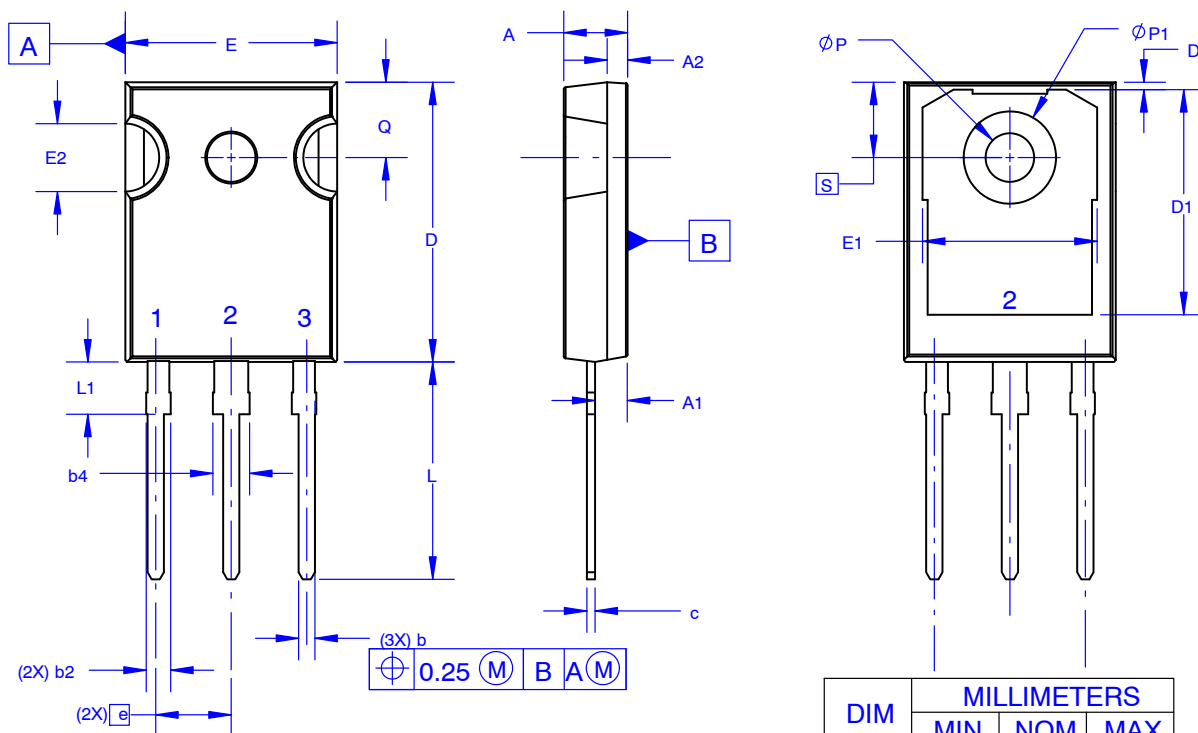
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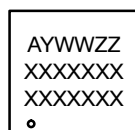
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ISSUE A

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E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

GENERIC
MARKING DIAGRAM*


XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.20	2.40	2.60
A2	1.40	1.50	1.60
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D	20.32	20.57	20.82
D1	13.08	~	~
D2	0.51	0.93	1.35
E	15.37	15.62	15.87
E1	12.81	~	~
E2	4.96	5.08	5.20
e	~	5.56	~
L	15.75	16.00	16.25
L1	3.69	3.81	3.93
ϕP	3.51	3.58	3.65
$\phi P1$	6.60	6.80	7.00
Q	5.34	5.46	5.58
S	5.34	5.46	5.58

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