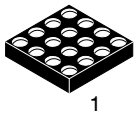
# Four Channel Load-Switch / LDO Configurable PMIC

# FAN53840, FAN53841




**WLCSP16 1.52x1.52x0.432**
**CASE 567ZM**

### General Description

The FAN53840 family are low Iq PMICs intended for mobile power application camera modules. The PMIC contains a high−power regulated channel for digital rails which can operate with an input as low as 1.0 V. Three channels are designed for ultra−low noise and high PSRR for sensitive analog/RF circuit loads. Each channel can be configured to operate as a pass−through load−switch, which reduces the input to output voltage drop and operating currents in critical low power applications.

The device is available in 16−bump, 0.35 mm pitch, Wafer−Level Chip−Scale Package (WLCSP).

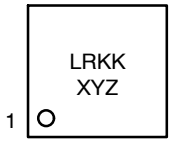
### Features

- LDO1:
  - 1.2 A Output Current Capability
  - Programmable Output Voltage 0.8 V to 1.504 V in 8 mV Steps
  - 1.0 V to 2.0 V Input Voltage Range
  - 1.1% to −1.5% Accuracy
- LDO2, LDO3, and LDO4:
  - 300 mA Output Current Capability
  - Programmable Output Voltage 1.5 V to 3.412 V in 8 mV Steps
  - 1.9 V to 5.5 V Input Voltage Range
  - Less than 20 μV (typ) Noise
- Load−Switch Operation:
  - 100/200 mΩ Maximum Channel Resistance
  - Low Operating Currents
  - Input Voltages Down to 1.0 V and 1.8 V
- Operation Guaranteed with System Voltage Down to 2.6 V
- Soft−Start Function (SS) to Limit Inrush Current
- Current Limit to Protect Against Short Circuit
- $I^2C$ Protection Fault (UVLO and OCP in LDO Operation) Registers
- $I^2C$ Serial Control to Program Output Voltage and Features
- System UVLO and Thermal Global Shutdown Protection for LDOs
- Pb−Free Devices

### Applications

- Smart Phones
- Wearables
- Smart Watch
- Health Monitoring
- Sensor Drive
- Energy Harvesting
- Utility and Safety Modules
- RF Modules

### MARKING DIAGRAM




| | |
|---|---|
| LR | = Specific Device Code |
| KK | = Lot Run Code |
| X | = Alphabetical Year Code |
| Y | = 2−weeks Date Code |
| Z | = Assembly Plant Code |

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

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## ORDERING INFORMATION

| Part Number | Mark-ing | I/O Logic Level (Note 1) | I²C Address (Note 2) | LDO1 VOUT | LDO2 VOUT | LDO3 VOUT | LDO4 VOUT | Interrupt Pin Polarity | Temperature Range | Package | Shipping† |
|---|---|---|---|---|---|---|---|---|---|---|---|
| FAN53840UC00X | LR | 1.8 V | 7'h20 | 1.2 V | 2.85 V | 1.8 V | 1.8 V | Active Low | −40°C to +85°C | 20−Bump WLCSP (Pb−Free) | 3000 / Tape & Reel |
| FAN53841UC00X | L9 | 1.2 V | | | | | | | | | |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

1. RESET_B, SDA, SCL (open drain type pins)
2. I2C address is configurable. See I2C section for more information on setting the device address

## APPLICATION CIRCUIT

### Application Circuit Diagram

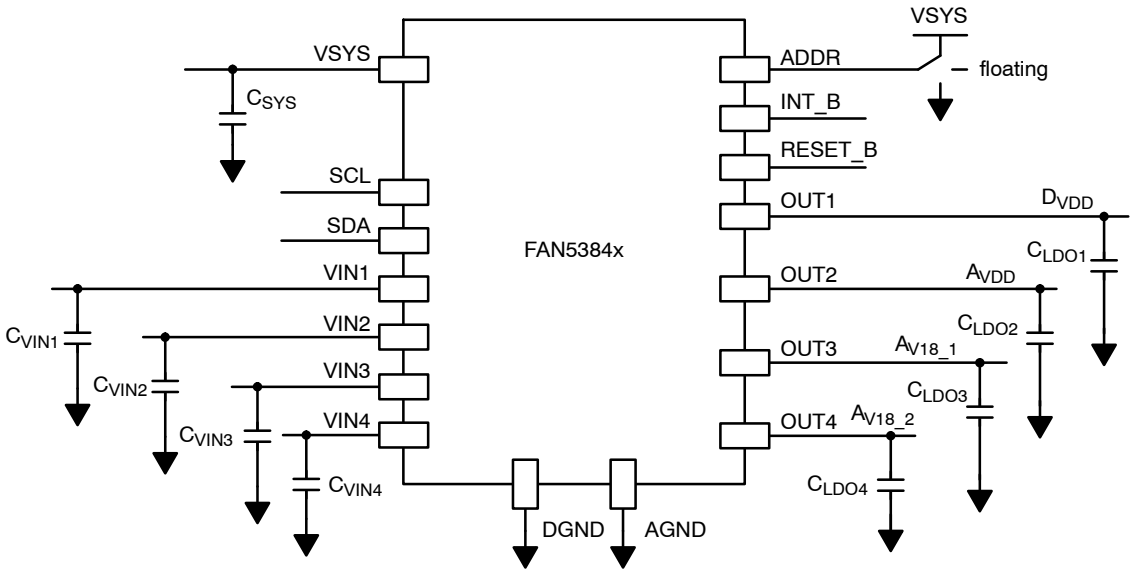



**Figure 1. LDO Mode**

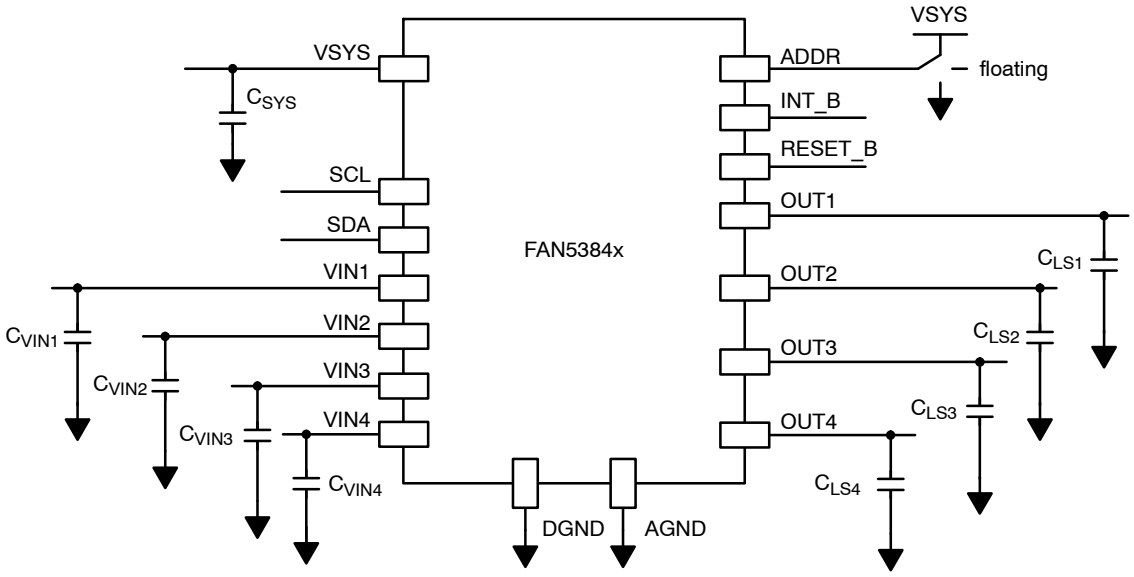


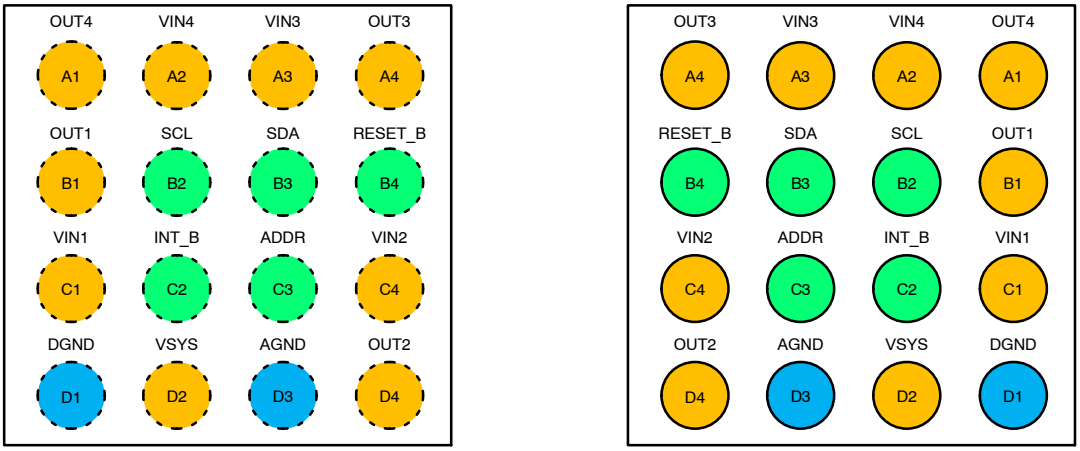

**Figure 2. Load Switch Mode**

### Application Circuit Components

**Table 1. RECOMMENDED EXTERNAL COMPONENTS**

| Component | Manufacturer | Part Number | Value | Case Size | Voltage Rating |
|---|---|---|---|---|---|
| $C_{VIN1}$, $C_{VIN2}$, $C_{VIN3}$, $C_{VIN4}$ | Murata | GRM033R61A105ME15 | 1.0 μF | 0201/0603 (0.6 mm x 0.3 mm) | 10 V |
| $C_{VSYS}$ | Murata | GRM033R61A105ME15 | 1.0 μF | 0201/0503 (0.5 mm x 0.3 mm) | 10 V |
| $C_{LDO1}$ | Taiyo Yuden | JMK105CBJ106MV−F | 10 μF | 0402/1005 (1.0 mm x 0.5 mm) | 6.3 V |
| $C_{LDO2}$, $C_{LDO3}$, $C_{LDO4}$ | Murata | GRM033R60J225ME47D | 2.2 μF | 0201/0603 (0.6 mm x 0.3 mm) | 6.3 V |
| $C_{LS1}$, $C_{LS2}$, $C_{LS3}$, $C_{LS4}$ | Murata | GRM033R60J104KE19 | 0.1 μF | 0201/0603 (0.6 mm x 0.3 mm) | 6.3 V |

## PRODUCT PIN ASSIGNMENTS




Top View (Bumps Down) Bottom View (Bumps Up)

**Figure 3. Pin Configuration**

### PIN DEFINITIONS

| Pin | Pin Name | Description |
|---|---|---|
| A1 | OUT4 | This is the output pin for Channel 4. Place $C_{LDO4}$ (or $C_{LS4}$) as close to this pin as possible. |
| A2 | VIN4 | Input power pin for Channel 4. Place $C_{VIN4}$ as close to this pin as possible. If Channel 4 is unused, it is recommended to tie to VSYS. |
| A3 | VIN3 | This is the input power pin for Channel 3. Place $C_{VIN3}$ as close to this pin as possible. If Channel 3 is unused, it is recommended to tie to VSYS. |
| A4 | OUT3 | This is the output pin for Channel 3. Place $C_{LDO3}$ (or $C_{LS3}$) as close to this pin as possible. |
| B1 | OUT1 | This is the output pin for Channel 1. Place $C_{LDO1}$ (or $C_{LS1}$) as close to this pin as possible. |
| B2 | SCL | $I^2C$ Clock pin. Node should be tied high through a pull−up resistor. |
| B3 | SDA | $I^2C$ Data pin. Node should be tied high through a pull−up resistor. |
| B4 | RESET_B | RESET_B pin is used to enable basic circuits necessary for controlling the PMIC. The RESET_B pin has an internal 4 MΩ (typ) pull−down and should always be connected to a logic high or low. |
| C1 | VIN1 | Input power pin for Channel 1. Place $C_{VIN1}$ as close to this pin as possible. If Channel 1 is unused, it is recommended to tie to VSYS. |
| C2 | INT_B | Fault interrupt pin is an open−drain configuration and pulls low to indicate an interrupt event has occurred. This pin returns to Hi−Z when all $I^2C$ interrupt bits equal 0. An external pull−up resistor is required. |
| C3 | ADDR | $I^2C$ address select pin. Either tie to ground, VSYS, or leave unconnected for desired $I^2C$ address. |
| C4 | VIN2 | Input power pin for Channel 2. Place $C_{VIN2}$ as close to this pin as possible. If Channel 2 is unused, it is recommended to tie to VSYS. |
| D1 | DGND | Digital/Analog ground connection. If used as separate return for Channel 1 load, connect the return plane to AGND at a via on a plane below the AGND plane. |
| D2 | VSYS | System power pin. Route trace from system to this pin. Connect the $C_{VSYS}$ capacitor as close as possible to the pin. |
| D3 | AGND | Digital/Analog ground connection. Tie to power plane. |
| D4 | OUT2 | This is the output pin for Channel 2. Place $C_{LDO2}$ (or $C_{LS2}$) as close to this pin as possible. |

## PRODUCT BLOCK DIAGRAM

### Block Diagram

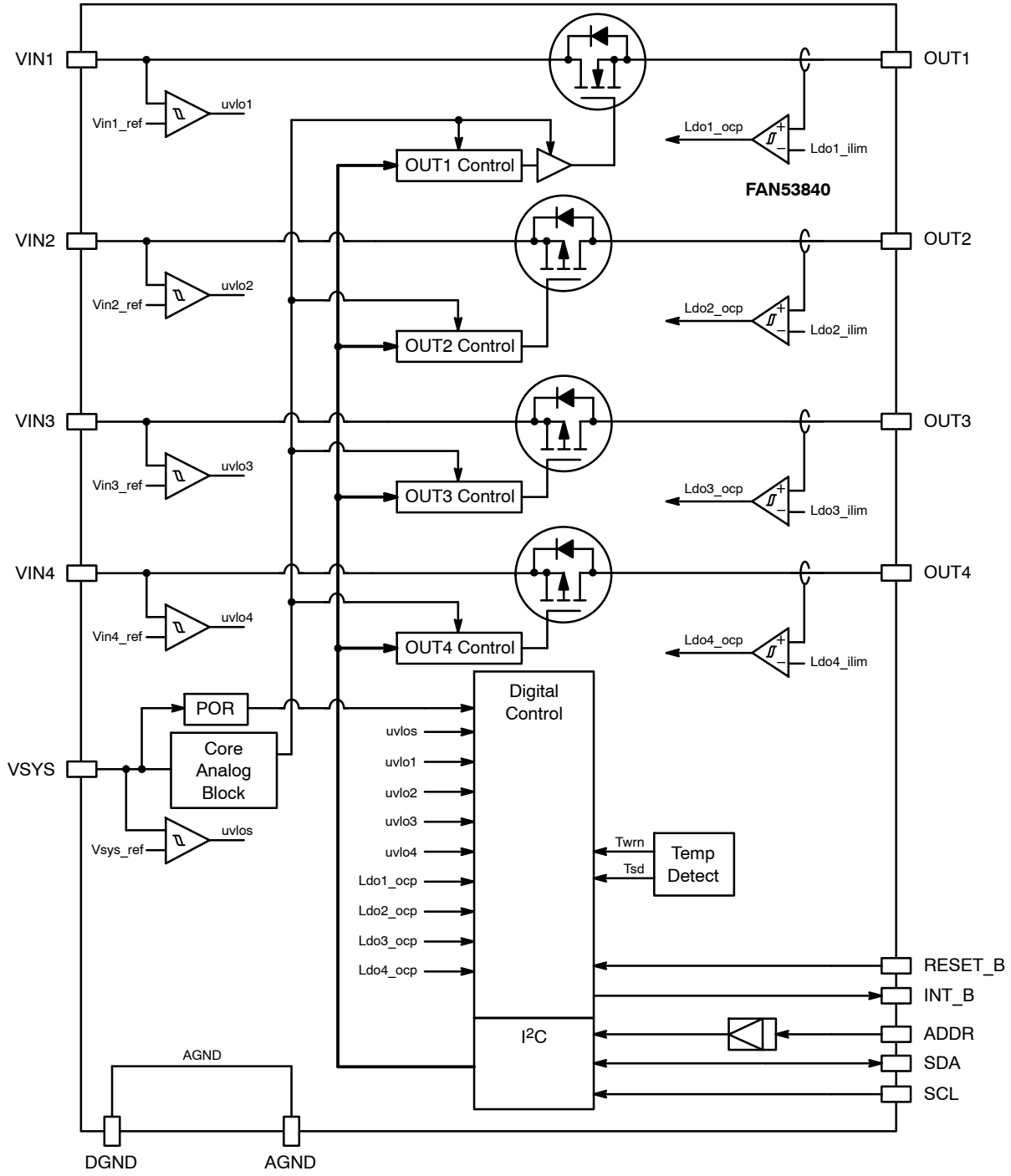



**Figure 4. Block Diagram**

## MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{SYS}$ | System Supply Voltage Range | | −0.3 | – | 6.0 | V |
| $V_{IN1}$ | Low−Voltage Supply Range | | −0.3 | – | 6.0 | V |
| $V_{IN2}$, $V_{IN3}$, $V_{IN4}$ | High−Voltage Supply Range | | −0.3 | – | 6.0 | V |
| $V_{CTRL}$ | SDA, SCL, and RESET_B | | −0.3 | – | 6.0 | V |
| $V_{INTB}$ | INT_B | | −0.3 | – | 6.0 | V |
| $V_{OUT1/2/3/4}$ | All Supply Output Pins | | −0.3 | – | $V_{IN1/2/3/4}$ + 0.3 V | V |
| Ipin_max | Pin Current | | – | – | 1.5 | A |
| ESD | ESD – HBM | Human Body Model | – | 2.0 | – | kV |
| ESD | ESD – CDM | Charged Device Model | – | 500 | – | V |
| $T_J$ | Junction Temperature | | −40 | – | +150 | °C |
| $T_{STG}$ | Storage Temperature | | −65 | – | +150 | °C |
| $T_L$ | Soldering Temperature | | – | – | +260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## THERMAL CHARACTERISTICS

| Symbol | Characteristic | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $\theta_{JA}$ | Thermal Resistance Junction/Air | 1S PCB @ 0.5 W Dissipation | – | 126 | – | °C/W |
| $\theta_{JB}$ | Thermal Resistance Junction/Board | 2S2P w/ Vias @0.5 W Dissipation | – | 45 | – | °C/W |

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{SYS}$ | Supply Voltage Range – CHAN1 | VSYS relative to OUT1 | $V_{OUT1}$ + 1.95 V | – | 5.5 | V |
| $V_{SYS}$ | Supply Voltage Range – CHAN2/3/4 | VSYS relative to OUT2/3/4 | 2.6 | – | 5.5 | V |
| $V_{IN1}$ | CHAN1 Input Supply Voltage Range | LDO and LS Modes | 1.0 | – | 2.0 | V |
| $V_{IN1}$ | CHAN1 LDO Mode Headroom | $V_{VIN1} - V_{OUT1}$ | 200 | – | | mV |
| $V_{IN2/3/4}$ | CHAN2/3/4 LDO Mode Supply Voltage Range | | 1.9 | – | 5.5 | V |
| $V_{IN2/3/4}$ | CHAN2/3/4 LDO Mode Headroom | $V_{VIN2} - V_{OUT2}$, $V_{VIN3} - V_{OUT3}$, and $V_{VIN4} - V_{OUT4}$ | 300 | – | – | mV |
| $V_{IN2/3/4}$ | CHAN2/3/4 LS Mode Supply Voltage Range (Note 3) | Any Channel in LDO Mode | 1.8 | – | 5.0 | V |
| | | CHAN1/2/3/4 = LS Mode | 1.7 | – | 5.0 | V |
| $P_D$ | Max Power Dissipation | $P_D$ = (125°C – 85°C) / 45°C/W = 0.88 W | – | – | 0.88 | W |
| $T_A$ | Ambient Temperature | | −40 | – | +85 | °C |
| $T_J$ | Junction Temperature | | −40 | – | +125 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. Please refer to the Under Voltage Lockout (UVLO) section in Device Operation for details.

## ELECTRICAL CHARACTERISTICS

Unless otherwise noted, the device is characterized for minimums and maximums across the ranges listed in the Recommended Operating Conditions. All limits are characterized using components from Recommended External Components table.

Production testing and testing for typical values is performed at $T_A$ = 25°C, For LDO Mode: $V_{VSYS}$ = 3.45 V, $V_{VIN1}$ = 1.3 V, $V_{VIN2}$ = 3.45 V, $V_{VIN3}$ and $V_{VIN4}$ = 1.95 V; For LS Mode: $V_{VSYS}$ = 3.80 V, $V_{VIN1}$ = $V_{VIN3}$ = $V_{VIN4}$ = 1.8 V and $V_{VIN2}$ = 5.0 V.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **POWER SUPPLY UVLO** | | | | | | |
| $V_{SYS\ UVLO_RS}$ | System Under−Voltage Lockout Threshold | Rising $V_{VSYS}$ | 2.30 | 2.35 | 2.40 | V |
| $V_{SYS\ UVLO_FL}$ | System Under−Voltage Lockout Threshold | Falling $V_{VSYS}$ | 2.20 | 2.25 | 2.30 | V |
| $V_{VIN1\ UVLO_RS}$ | Channel 1 Under−Voltage Lockout Threshold | Rising $V_{VIN1}$ | 0.90 | 0.95 | 1.00 | V |
| $V_{VIN1\ UVLO_FL}$ | Channel 1 Under−Voltage Lockout Threshold | Falling $V_{VIN1}$ | 0.80 | 0.85 | 0.92 | V |
| $V_{VIN_H\ UVLO_RS}$ | Channel 2/3/4 Under−Voltage Lockout Threshold | Rising $V_{VIN2/3/4}$ | 1.80 | 1.85 | 1.90 | V |
| $V_{VIN_H\ UVLO_FL}$ | Channel 2/3/4 Under−Voltage Lockout Threshold | Falling $V_{VIN2/3/4}$ | 1.70 | 1.75 | 1.80 | V |
| **CHANNEL 1 QUIESCENT CURRENT** | | | | | | |
| $IQ_{LD1}$ | Quiescent Current, LDO Mode | $I_{OUT1}$ = 0 A, total $I_{VSYS}$ and $I_{VIN1}$ currents when LDO_LS1_SELECT = 0, CHAN1_EN = 1 and all other channels disabled. | – | 67 | 75 | μA |
| $IQ_{LS1}$ | Quiescent Current, LS Mode | $I_{OUT1}$ = 0 A, total $I_{VSYS}$ and $I_{VIN1}$ currents when all LDO_LSx_SELECT = 1, CHAN1_EN = 1 and all other channels are disabled. | – | 1.29 | 3.0 | μA |
| **CHANNEL 1 OUTPUT VOLTAGE** | | | | | | |
| $VO_{L1_ACC}$ | LDO1 Output Voltage Accuracy | $I_{OUT1}$ = 1 mA and 1200 mA, $V_{VIN1}$ = 2.0 V, $V_{VSYS}$ = 3.45 V, $V_{OUT1}$ = 0.8 to 1.5 V | −1.5 | – | +1.1 | % |
| $V_{L1_DO_600}$ | LDO1 Dropout Voltage (Note 4) | $I_{OUT1}$ = 600 mA, $V_{OUT1}$= 1.20 V, and $V_{VSYS}$ = 3.00 V | – | 50 | 85 | mV |
| $V_{L1_DO_1000}$ | LDO1 Dropout Voltage (Note 4) | $I_{OUT1}$ = 1000 mA, $V_{OUT1}$ = 1.05 V, and $V_{VSYS}$ = 3.00 V | – | 77 | 125 | mV |
| **CHANNEL 1 DRAIN−SOURCE ON RESISTANCE** | | | | | | |
| $RDS_{ON1}$ | LS1 $R_{DS(on)}$ | $V_{VIN1}$ = 1.8 V, $V_{VSYS}$ = 3.2 V, all LDO_LSx_SELECT = 1, CHAN1_EN = 1, and $I_{OUT1}$ = 50 mA | – | 76 | 175 | mΩ |
| **CHANNEL 1 CURRENT LIMIT** | | | | | | |
| $I_{LIM_H1}$ | Current Limit | $V_{VIN1} \geq V_{OUT1}$ +300 mV and $V_{VIN1}$ = 1.1 to 2.0 V, $V_{VSYS} \geq V_{OUT1}$ + 1.95 V | 1250 | 1400 | 1700 | mA |
| $T_{L1\ OC_RST}$ | Over−Current Restart Timer | | – | 20 | – | ms |
| $T_{L1\ OC_DEB}$ | Over−Current Debounce Timer | $I^2C$ Register 0x07h = 11 | – | 1.0 | – | ms |
| **CHANNEL 1 OUTPUT PROTECTION** | | | | | | |
| $R_{L1_DCHG}$ | Output Discharge | | 80 | 100 | 120 | Ω |

**ELECTRICAL CHARACTERISTICS** (continued)
Unless otherwise noted, the device is characterized for minimums and maximums across the ranges listed in the Recommended Operating Conditions. All limits are characterized using components from Recommended External Components table.

Production testing and testing for typical values is performed at $T_A$ = 25°C, For LDO Mode: $V_{VSYS}$ = 3.45 V, $V_{VIN1}$ = 1.3 V, $V_{VIN2}$ = 3.45 V, $V_{VIN3}$ and $V_{VIN4}$ = 1.95 V; For LS Mode: $V_{VSYS}$ = 3.80 V, $V_{VIN1}$ = $V_{VIN3}$ = $V_{VIN4}$ = 1.8 V and $V_{VIN2}$ = 5.0 V.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **CHANNEL 2 QUIESCENT CURRENT** | | | | | | |
| $IQ_{LD2}$ | Quiescent Current, LDO Mode | $I_{OUT2}$ = 0 A, total $I_{VSYS}$ and $I_{VIN2}$ currents when LDO_LS2_SELECT = 0, CHAN2_EN = 1 and all other channels disabled. | – | 55 | 63 | μA |
| $IQ_{LS2}$ | Quiescent Current, LS Mode | $I_{OUT2}$ = 0 A, total $I_{VSYS}$ and $I_{VIN2}$ currents when all LDO_LSx_SELECT = 1, CHAN2_EN = 1 and all other channels are disabled. | – | 1.32 | 3.5 | μA |
| **CHANNEL 2 OUTPUT VOLTAGE** | | | | | | |
| $VO_{L2_ACC}$ | LDO2 Output Voltage Accuracy | IOUT = 1 mA and 300 mA, VSYS = 3.45 V, VIN2 ≥3.45 V and VIN2 ≥ VOUT + 300 mV, VOUT = 1.5 to 3.412 V | −1.3 | – | +1.0 | % |
| $V_{L2_DO}$ | LDO2 Dropout Voltage (Note 4) | $V_{OUT2}$ = 1.8 V, $V_{VSYS}$ = 3.45 V, $I_{OUT2}$ = 300 mA | – | 66 | 100 | mV |
| **CHANNEL 2 DRAIN−SOURCE ON RESISTANCE** | | | | | | |
| $RDS_{ON2}$ | LS2 $R_{DS(on)}$ | $V_{VIN2}$ = 5 V, $V_{VSYS}$ = 3.2 V, all LDO_LSx_SELECT = 1, CHAN2_EN = 1, $I_{OUT2}$ = 50 mA | – | 76 | 100 | mΩ |
| **CHANNEL 2 CURRENT LIMIT** | | | | | | |
| $I_{LIM_L2}$ | Current Limit | $V_{VIN2} \geq V_{OUT2}$ + 500 mV and $V_{VIN2}$ = 2.0 to 5.5 V, $V_{VSYS}$ = 3.45 V | 320 | 400 | 480 | mA |
| $T_{L2\ OC_RST}$ | Over−Current Restart Timer | | – | 20 | – | ms |
| $T_{L2\ OC_DEB}$ | Over−Current Debounce Timer | $I^2C$ Register 0x07h = 11 | – | 1.0 | – | ms |
| **CHANNEL 2 OUTPUT PROTECTION** | | | | | | |
| $R_{L2_DCHG}$ | Output Discharge | | 80 | 100 | 120 | Ω |
| **CHANNEL 3/4 QUIESCENT CURRENT** | | | | | | |
| $IQ_{LD3/4}$ | Quiescent Current, LDO Mode | $I_{OUT3}$ = 0 A, total $I_{VSYS}$ and $I_{VIN3}$ currents when LDO_LS3/4_SELECT = 0, CHAN3/4_EN = 1 and all other channels disabled. | – | 55 | 63 | μA |
| $IQ_{LS3/4}$ | Quiescent Current, LS Mode | $I_{OUT3}$ = 0 A, total $I_{VSYS}$ and $I_{VIN3}$ currents when all LDO_LSx_SELECT = 1, CHAN3/4_EN = 1 and all other channels are disabled. | – | 2.62 | 8 | μA |
| **CHANNEL 3/4 OUTPUT VOLTAGE** | | | | | | |
| $VO_{L3/4_ACC}$ | LDO3/4 Output Voltage Accuracy | $I_{OUT3/4}$ = 1 mA and 300 mA, $V_{VSYS}$ = 3.45 V, $V_{VIN3/4} \geq$ 3.45 V and ≥ $V_{OUT3/4}$ +300 mV, $V_{OUT3/4}$ = 1.5 to 3.412 V | −1.0 | – | +1.0 | % |
| $V_{L3/4_DO}$ | LDO3/4 Dropout Voltage (Note 4) | $V_{OUT3/4}$ = 1.8 V, $V_{VSYS}$ = 3.45 V, $I_{OUT3/4}$ = 300 mA | – | 68 | 100 | mV |

**ELECTRICAL CHARACTERISTICS** (continued)
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| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **CHANNEL 3/4 DRAIN−SOURCE ON RESISTANCE** | | | | | | |
| $RDS_{ON3/4}$ | LS3/4 $R_{DS(on)}$ | $V_{VIN3/4}$ = 1.8 V, $V_{VSYS}$ = 3.2 V, all LDO_LSx_SELECT = 1, CHAN3/4_EN = 1, $I_{OUT3/4}$ = 50 mA | – | 76 | 100 | mΩ |
| **CHANNEL 3/4 CURRENT LIMIT** | | | | | | |
| $I_{LIM_L3/4}$ | Current Limit | $V_{VIN3/4} \geq V_{OUT3/4}$ + 500 mV and $V_{VIN3/4}$ = 2.0 to 5.5 V, $V_{VSYS}$ = 3.45 V | 320 | 400 | 480 | mA |
| $T_{L3/4\ OC_RST}$ | Over−Current Restart Timer | | – | 20 | – | ms |
| $T_{L3/4\ OC_DEB}$ | Over−Current Debounce Timer | $I^2C$ Register 0x07h = 11 | – | 1.0 | – | ms |
| **CHANNEL 3/4 OUTPUT PROTECTION** | | | | | | |
| $R_{L3/4_DCHG}$ | Output Discharge | | 80 | 100 | 120 | Ω |
| **I/O LEVELS** | | | | | | |
| $V_{IL}$ | RESET_B Logic Low Threshold | FAN53840 | | | 0.4 | V |
| | | FAN53841 | | | 0.325 | |
| $V_{IH}$ | RESET_B Logic High Threshold | FAN53840 | 1.2 | | $V_{IN}$ | |
| | | FAN53841 | 0.825 | | $V_{IN}$ | |
| $V_{OL_INT_B}$ | INT_B $V_{OLmax}$ | $I_{sink}$ = 3 mA | – | – | 0.3 | V |
| $I_{INT_B}$ | INT_B Leakage | $V_{INT_B}$ = 5.5 V | – | – | 0.5 | μA |
| $R_{ADDR}$ | ADDR Input Resistance | $V_{VSYS}$ = 2.6 to 5.5 V | – | 893 | – | kΩ |
| $I_{ADDR}$ | ADDR Current | $V_{VSYS}$ = 2.6 to 5.5 V | – | 1.57 | – | μA |
| $ADDR_{VIH}$ | ADDR High | | – | 80 | 93 | %$V_{VSYS}$ |
| $ADDR_{VIL}$ | ADDR Low | | 8.0 | 20 | – | %$V_{VSYS}$ |
| **IQ CONDITIONS** | | | | | | |
| $I_{Q\ VSYS_SD}$ | System Shutdown Current | $I_{VSYS}$ when $V_{VSYS}$= 5.5 V, all CHANx_EN bits = 0, RESET_B = SDA = SCL = Low, and $T_J$ = 85°C | – | – | 3.0 | μA |
| $I_{Q\ VIN1_SD}$ | Channel 1 Shutdown Current | $I_{VIN1}$ when $V_{VIN1}$= 2.0 V, all CHANx_EN bits = 0, RESET_B = SDA = SCL = Low, $T_J$ = 85°C | – | – | 0.3 | μA |
| $I_{Q\ VIN2/3/4_SD}$ | Channel 2/3/4 Shutdown Current | $I_{VIN2}$ when $V_{VIN2}$ = 5.5 V; or $I_{VIN3}$ when $V_{VIN3}$ = 5.5 V; or $I_{VIN4}$ when $V_{VIN4}$ = 5.5 V. All CHANx_EN bits = 0, RESET_B = SDA = SCL = Low, $T_J$ = 85°C | – | – | 2.5 | μA |
| $I_{Q_STBY_LDO}$ | LDO Mode Standby Current | All channels configured as LDO, all enabled with no load. (Note 5) | – | 200 | 230 | μA |
| $I_{Q_STBY_LS}$ | LS Mode Standby Current | All channels configured as LS, all enabled with no load. (Note 6) | – | 5 | 13.0 | μA |

**ELECTRICAL CHARACTERISTICS** (continued)
Unless otherwise noted, the device is characterized for minimums and maximums across the ranges listed in the Recommended Operating Conditions. All limits are characterized using components from Recommended External Components table.

Production testing and testing for typical values is performed at $T_A$ = 25°C, For LDO Mode: $V_{VSYS}$ = 3.45 V, $V_{VIN1}$ = 1.3 V, $V_{VIN2}$ = 3.45 V, $V_{VIN3}$ and $V_{VIN4}$ = 1.95 V; For LS Mode: $V_{VSYS}$ = 3.80 V, $V_{VIN1}$ = $V_{VIN3}$ = $V_{VIN4}$ = 1.8 V and $V_{VIN2}$ = 5.0 V.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **IQ CONDITIONS** | | | | | | |
| $I_{SLP_LDO}$ | LDO Mode Sleep Current | All channels configured as LDO, all disabled with no load. (Note 7) | – | 9.8 | 20 | μA |
| $I_{SLP_LS}$ | LS Mode Sleep Current | All channels configured as LS, all disabled with no load. (Note 8) | – | 1.3 | 5 | μA |
| **I²C TIMING AND PERFORMANCE*** | | | | | | |
| $V_{IL}$ | SDA and SCL Low Threshold | FAN53840 | −0.5 | – | 0.3 $V_{DD}$ | V |
| | | FAN53841 | −0.5 | – | 0.325 | V |
| $V_{IH}$ | SDA and SCL High Threshold | FAN53840 | 0.7 $V_{DD}$ | – | 5.5 | V |
| | | FAN53841 | 0.825 | – | 5.5 | V |
| $V_{OL}$ | SDA Logic Low Output | 3 mA Sink | – | – | 0.24 | V |
| $I_{OL}$ | SDA Sink Current | | 20 | – | – | mA |
| $f_{SCL}$ | SCL Clock Frequency | Fast Mode Plus | – | – | 1000 | kHz |
| $t_{BUF}$ | Bus−Free Time Between STOP and START Conditions | Fast Mode Plus | 0.5 | – | – | μs |
| $t_{HD;STA}$ | Start or Repeated Start Hold Time | Fast Mode Plus | 260 | – | – | ns |
| $t_{LOW}$ | SCL Low Period | Fast Mode Plus | 0.5 | – | – | μs |
| $t_{HIGH}$ | SCL High Period | Fast Mode−Plus | 260 | – | – | ns |
| $t_{SU;STA}$ | Repeated Start Setup Time | Fast Mode−Plus | 260 | – | – | ns |
| $t_{SU;DAT}$ | Data Setup Time | Fast Mode Plus | 50 | – | – | ns |
| $t_{VD;DAT}$ | Data Valid Time | Fast Mode Plus | – | – | 450 | ns |
| $t_{VD;ACK}$ | Data Valid Acknowledge Time | Fast Mode Plus | – | – | 450 | ns |
| $t_R$ | SDA and SCL Rise Time | Fast Mode Plus | – | – | 120 | ns |
| $t_F$ | SCL and SDA Fall Time | Fast Mode Plus | 20 x $V_{DD}$ / 5.5 V | – | 120 | ns |
| $t_{SU;STO}$ | Stop Condition Setup Time | Fast Mode Plus | 260 | – | – | ns |
| $C_i$ | Input Capacitance | | – | – | 10 | pF |
| $C_b$ | Capacitive Load for SDA and SCL | | – | – | 550 | pF |
| $t_{SP}$ | Pulse width of spikes which must be suppressed by input filter | SCL, SDA only | 0 | – | 50 | ns |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. LDOx Dropout Voltage is measured by lowering $V_{VINx}$ until $V_{OUTx}$ = VOUT_TARGET − 50 mV.
5. Total $I_{VSYS}$, $I_{VIN1}$, $I_{VIN2}$, $I_{VIN3}$, and $I_{VIN4}$ when RESET_B = High, all CHANx_EN = 1, and all LDO_LSx_SELECT = 0.
6. Total $I_{VSYS}$, $I_{VIN1}$, $I_{VIN2}$, $I_{VIN3}$, and $I_{VIN4}$ when RESET_B = High, all CHANx_EN = 1, and all LDO_LSx_SELECT = 1.
7. Total $I_{VSYS}$, $I_{VIN1}$, $I_{VIN2}$, $I_{VIN3}$, and $I_{VIN4}$ when RESET_B = High, SCL = SDA = Low, all CHANx_EN = 0, and all LDO_LSx_SELECT = 0.
8. Total $I_{VSYS}$, $I_{VIN1}$, $I_{VIN2}$, $I_{VIN3}$, and $I_{VIN4}$ when RESET_B = High, SCL = SDA = Low, all CHANx_EN = 0, and all LDO_LSx_SELECT = 1.

**Guarantee Levels:**
*Guaranteed by Design Only. Not Characterized or Production Tested.

## SYSTEM CHARACTERISTICS

Unless otherwise noted, the device is characterized for minimums and maximums across the ranges listed in the Recommended Operating Conditions. All limits are characterized using components from Recommended External Components table.

Production testing and testing for typical values is performed at $T_A$ = 25°C, For LDO Mode: $V_{VSYS}$ = 3.45 V, $V_{VIN1}$ = 1.3 V, $V_{VIN2}$ = 3.45 V, $V_{VIN3}$ and $V_{VIN4}$ = 1.95 V; For LS Mode: $V_{VSYS}$ = 3.80 V, $V_{VIN1}$ = $V_{VIN3}$ = $V_{VIN4}$ = 1.8 V and $V_{VIN2}$ = 5.0 V.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **CHANNEL 1 STARTUP** | | | | | | |
| $T_{SS_LDO1}$ | LDO1 StartUp Time | Measured from CHAN1_EN bit = High to 90% of $V_{OUT1}$ = 1.20 V with $I_{OUT1}$ = 10 mA | – | 185 | – | µs |
| $T_{SS_LS1}$ | LS1 Startup Time | Measured from CHAN1_EN bit = High to 90% of $V_{VIN1}$ = 1.8 V with $I_{OUT1}$ = 10 mA | – | 55 | – | µs |
| **CHANNEL 1 PSRR & NOISE** | | | | | | |
| $PSRR_{L1_VIN}$ | Power Supply Rejection Ratio on LDO1 | (Note 9) Freq = 100 kHz | – | 25 | – | dB |
| $V_{N_L1}$ | LDO1 Output Noise | $V_{VIN1}$ = 1.3 V, $V_{OUT1}$ = 1.2, Freq: 10 Hz to 100 kHz, $I_{OUT1}$ = 100 mA | – | 23 | 35 | $\mu V_{rms}$ |
| **CHANNEL 1 REGULATION & TRANSIENT PERFORMANCE** | | | | | | |
| $REG_{L1_LD}$ | LDO1 Load Regulation | $I_{OUT1}$ = 1 mA to 1000 mA, $V_{VSYS}$ = 3.45 V, $V_{VIN1}$ = 1.3 V, $V_{OUT1}$ = 1.05 V, Load used for comparison = 500 mA. | −0.5 | – | +0.5 | % |
| $REG_{L1_LN}$ | LDO1 Line Regulation | $V_{VSYS}$ = 3.45 to 4.5 V, $V_{OUT1}$ + 300 mV ≤ $V_{VIN1}$ ≤ 2.0, $I_{OUT1}$ = 50 mA | −0.05 | – | +0.05 | % |
| $V_{L1\ TR_LD}$ | LDO1 Load Transient | $I_{OUT1}$ = 1mA <–> 1000 mA, 150 mA/µs, $V_{VSYS}$ ≥ $V_{OUT1}$ + 1.95 V, $V_{VIN1}$ = 1.0 to 1.7 V and $V_{VIN1}$ ≥ $V_{OUT1}$ + 200 mV; $V_{OUT1}$ = 0.8 to 1.5 V | −40 | – | +40 | mV |
| **CHANNEL 2 STARTUP** | | | | | | |
| $T_{SS_LDO2}$ | LDO2 Startup Time | Measured from CHAN2_EN bit = High to 90% of $V_{OUT2}$ = 2.85 V with $I_{OUT2}$ = 10 mA | – | 150 | – | µs |
| $T_{SS_LS2}$ | LS2 Startup Time | Measured from CHAN2_EN bit = High to 90% of $V_{VIN2}$ = 5.0 V with $I_{OUT2}$ = 10 mA | – | 75 | – | µs |
| **CHANNEL 2 PSRR & NOISE** | | | | | | |
| $PSRR_{L2_VIN}$ | Power Supply Rejection Ratio on LDO2 | (Note 10). Freq = 100 kHz | – | 55 | – | dB |
| $V_{N_L2}$ | LDO2 Output Noise | $V_{VIN2}$ = 3.45 V, $V_{OUT2}$ = 2.85, Freq: 10 Hz to 100 kHz, $I_{OUT2}$ = 300 mA | – | 20 | – | $\mu V_{rms}$ |
| **CHANNEL 2 REGULATION & TRANSIENT PERFORMANCE** | | | | | | |
| $REG_{L2_LD}$ | LDO2 Load Regulation | $I_{OUT2}$ = 100 µA to 300 mA, $V_{VSYS}$ = $V_{VIN2}$ = 3.45 V, $V_{OUT2}$ = 2.85 V, Load used for comparison = 150 mA. | −0.1 | – | +0.1 | % |

**SYSTEM CHARACTERISTICS** (continued)
Unless otherwise noted, the device is characterized for minimums and maximums across the ranges listed in the Recommended Operating Conditions. All limits are characterized using components from Recommended External Components table.

Production testing and testing for typical values is performed at $T_A$ = 25°C, For LDO Mode: $V_{VSYS}$ = 3.45 V, $V_{VIN1}$ = 1.3 V, $V_{VIN2}$ = 3.45 V, $V_{VIN3}$ and $V_{VIN4}$ = 1.95 V; For LS Mode: $V_{VSYS}$ = 3.80 V, $V_{VIN1}$ = $V_{VIN3}$ = $V_{VIN4}$ = 1.8 V and $V_{VIN2}$ = 5.0 V.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **CHANNEL 2 REGULATION & TRANSIENT PERFORMANCE** | | | | | | |
| $REG_{L2_LN}$ | LDO2 Line Regulation | $V_{OUT2}$ = 2.85 V, $V_{VSYS}$ = 2.6 to 5.5 V, $V_{VIN2}$ = 3.15 V and $V_{OUT2}$ + 300 mV ≤ $V_{VIN2}$ ≤ 5.5 V, $V_{VSYS}$ = 3.45 V, $V_{OUT2}$ = 1.5 to 3.412, $I_{OUT2}$ = 50 mA | −0.10 | – | +0.10 | % |
| $V_{L2\ TR_LD}$ | LDO1 Load Transient | $I_{OUT2}$ = 1 mA <–> 300 mA, 50 mA/μs, $V_{VSYS}$ = 3.45 V, $V_{VIN2}$ ≥ 3.00 V to 5.5 V and $V_{VIN2}$ ≥ $V_{OUT2}$ + 300 mV, $V_{OUT2}$ = 2.7 to 3.4 V | −26 | – | +20 | mV |
| **CHANNEL 3 STARTUP** | | | | | | |
| $T_{SS_LDO3}$ | LDO3 Startup Time | Measured from CHAN3_EN bit = High to 90% of $V_{OUT3}$ = 1.8 V with $I_{OUT3}$ = 10 mA | – | 150 | – | μs |
| $T_{SS_LS3}$ | LS3 Startup Time | Measured from CHAN3_EN bit = High to 90% of $V_{VIN3}$ = 1.8 V, $I_{OUT3}$ = 10 mA | – | 150 | – | μs |
| **CHANNEL 3 PSRR & NOISE** | | | | | | |
| $PSRR_{L3_VIN}$ | Power Supply Rejection Ratio on LDO3 | (Note 11) Freq = 100 kHz | – | 41 | – | dB |
| $V_{N_L3}$ | LDO3 Output Noise | Freq: 10 Hz to 100 kHz, $I_{OUT}$ = 300 mA | – | 20 | – | $\mu V_{rms}$ |
| **CHANNEL 3 REGULATION & TRANSIENT PERFORMANCE** | | | | | | |
| $REG_{L3_LD}$ | LDO3 Load Regulation | $I_{OUT3}$ = 100 μA to 300 mA, $V_{VSYS}$ = 3.45 V, $V_{VIN3}$ = 1.95 V, $V_{OUT3}$ = 1.8 V, Load used for comparison = 150 mA. | −0.1 | – | +0.1 | % |
| $REG_{L3_LN}$ | LDO3 Line Regulation | $V_{OUT3}$ = 1.8 V, $V_{VSYS}$ = 2.6 to 5.5 V, $V_{VIN3}$ = 2.3 V and $V_{VSYS}$ = 3.45 V, $V_{VIN3}$ = 2.3 to 5.5 V, $I_{OUT3}$ = 50 mA | −0.10 | – | +0.10 | % |
| $V_{L3\ TR_LD}$ | LDO3 Load Transient | $I_{OUT3}$ = 1 mA <–> 300 mA, 50 mA/μs, $V_{VIN3}$ ≥ 9 V & $V_{VIN3}$ ≥ $V_{OUT3}$ + 200 mV, $V_{OUT3}$ = 1.5 to 3.4 V | −30 | – | +15 | mV |
| **CHANNEL 4 STARTUP** | | | | | | |
| $T_{SS_LDO4}$ | LDO4 Startup Time | Measured to CHAN4_EN bit = High to 90% of $V_{OUT4}$ = 1.80 V, $I_{OUT4}$ = 10 mA | – | 175 | – | μs |
| $T_{SS_LS4}$ | LS4 Startup Time | Measured to CHAN4_EN bit = High to 90% of $V_{VIN4}$ = 1.8 V, $I_{OUT4}$ = 10 mA | – | 150 | – | μs |
| **CHANNEL 4 PSRR & NOISE** | | | | | | |
| $PSRR_{L4_VIN}$ | Power Supply Rejection Ratio on LDO4 | (Note 12) Freq = 100 kHz | – | 41 | – | dB |

**SYSTEM CHARACTERISTICS** (continued)
Unless otherwise noted, the device is characterized for minimums and maximums across the ranges listed in the Recommended Operating Conditions. All limits are characterized using components from Recommended External Components table.

Production testing and testing for typical values is performed at $T_A$ = 25°C, For LDO Mode: $V_{VSYS}$ = 3.45 V, $V_{VIN1}$ = 1.3 V, $V_{VIN2}$ = 3.45 V, $V_{VIN3}$ and $V_{VIN4}$ = 1.95 V; For LS Mode: $V_{VSYS}$ = 3.80 V, $V_{VIN1}$ = $V_{VIN3}$ = $V_{VIN4}$ = 1.8 V and $V_{VIN2}$ = 5.0 V.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **CHANNEL 4 PSRR & NOISE** | | | | | | |
| $V_{N_L4}$ | LDO4 Output Noise | Freq: 10 Hz to 100 kHz, $I_{OUT4}$ = 300 mA | – | 20 | – | $\mu V_{rms}$ |
| **CHANNEL 4 REGULATION & TRANSIENT PERFORMANCE** | | | | | | |
| $REG_{L4_LD}$ | LDO4 Load Regulation | $I_{OUT4}$ = 100 μA to 300 mA, $V_{VIN4}$ = 1.95 V, $V_{VSYS}$ = 3.45 V, $V_{OUT4}$ = 1.8 V, Load used for comparison = 150 mA. | −0.1 | – | +0.1 | % |
| $REG_{L4_LN}$ | LDO4 Line Regulation | $V_{OUT4}$ = 1.8 V, $V_{VSYS}$ = 2.6 to 5.5 V, $V_{VIN4}$ = 2.3 V and $V_{VSYS}$ = 3.45 V, $V_{VIN4}$ = 2.3 to 5.5 V, $I_{OUT4}$ = 50 mA | −0.10 | – | +0.10 | % |
| $V_{L4\ TR_LD}$ | LDO3 Load Transient | $I_{OUT4}$ = 1 mA <–> 300 mA, 50 mA/μs, $V_{VIN4} \geq$ 1.9 V & $V_{VIN4} \geq V_{OUT4}$ + 200 mV, $V_{OUT4}$ = 1.5 to 3.4 V | −30 | – | +15 | mV |
| **THERMAL PROTECTION** | | | | | | |
| $T_{WRN}$ | Thermal Warning | | 115 | 125 | 135 | °C |
| $T_{SD}$ | Thermal Shutdown | | 125 | 140 | 155 | °C |
| $T_{HYS}$ | Thermal Hysteresis | | 15 | 20 | 25 | °C |

9. $V_{VIN1}$ = 1.3 V, $V_{VSYS}$ = 3.45 V, $V_{OUT1}$ = 1.2 V, $I_{OUT1}$ = 150 mA, $C_{VIN1}$ = 1.0 μF, $C_{LDO1}$ = 10 μF.
10. $V_{VIN2}$ = 3.45 V, $V_{VSYS}$ = 3.45 V, $V_{OUT2}$ = 2.85 V, $I_{OUT2}$ = 100 mA, $C_{VIN2}$ = 1.0 μF, $C_{LDO2}$ = 2.2 μF.
11. $V_{VIN3}$ = 1.95 V, $V_{VSYS}$ = 3.45 V, $V_{OUT3}$ = 1.8 V, $I_{OUT3}$ = 100 mA, $C_{VIN3}$ = 1.0 μF, $C_{LDO3}$ = 2.2 μF.
12. $V_{VIN4}$ = 1.95 V, $V_{VSYS}$ = 3.45 V, $V_{OUT4}$ = 1.8 V, $I_{OUT4}$ = 100 mA, $C_{VIN4}$ = 1.0 μF, $C_{LDO4}$ = 2.2 μF.

## TYPICAL CHARACTERISTICS

(Unless otherwise noted, $T_A$ = 25°C, For LDO Mode: $V_{VSYS}$ = 3.45 V, $V_{VIN1}$ = 1.3 V, $V_{VIN2}$ = 3.45 V, $V_{VIN3}$ and $V_{VIN4}$ = 1.95 V; For LS Mode: $V_{VSYS}$ = 3.80 V, $V_{VIN1}$ = $V_{VIN3}$ = $V_{VIN4}$ = 1.8 V and $V_{VIN2}$ = 5.0 V. Using components from Recommended External Components.)

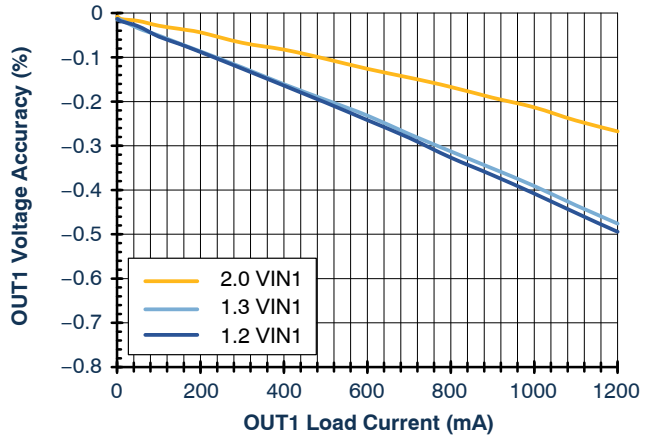



**Figure 5. LDO1 Output Voltage Accuracy vs. Load Current and Input Voltage, $V_{OUT1}$ = 1.05 V**

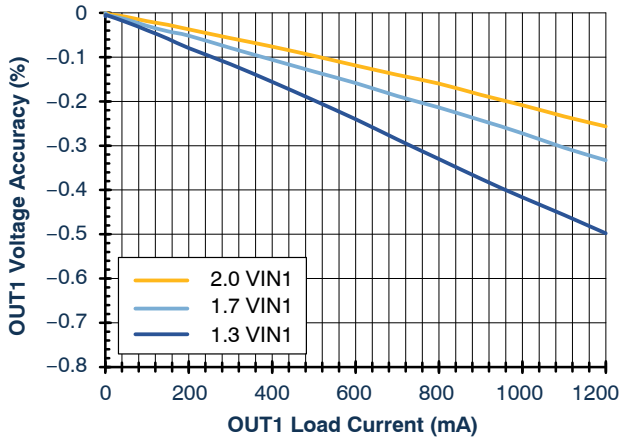



**Figure 6. LDO1 Output Voltage Accuracy vs. Load Current and Input Voltage, $V_{OUT1}$ = 1.2 V**

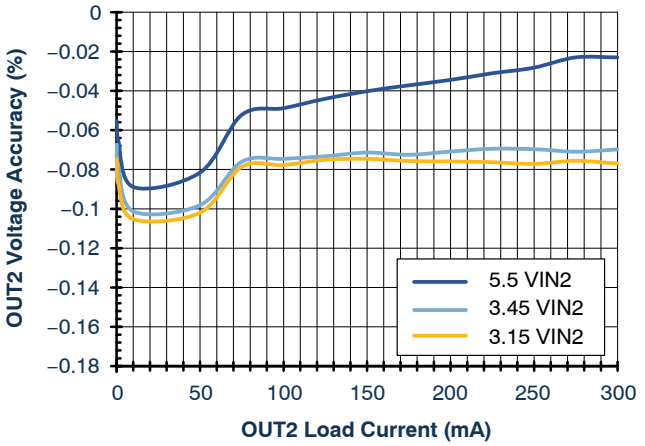



**Figure 7. LDO2 Output Voltage Accuracy vs. Load Current and Input Voltage, $V_{OUT2}$ = 2.85 V**

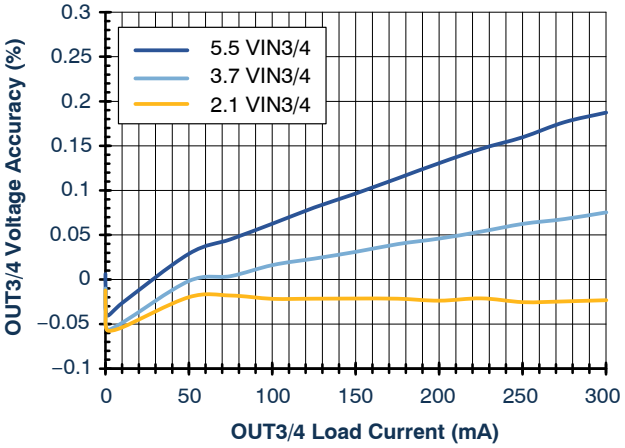



**Figure 8. LDO3/4 Output Voltage Accuracy vs. Load Current and Input Voltage, $V_{OUT3/4}$ = 1.8 V**

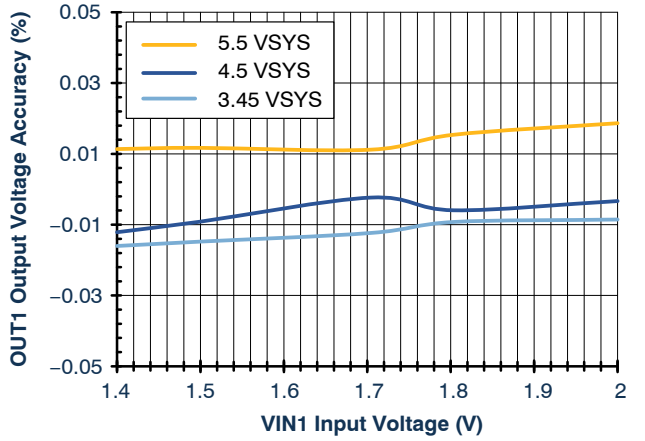



**Figure 9. LDO1 Output Voltage Accuracy vs. Input and System Voltage, $V_{OUT1}$ = 1.2 V and $I_{OUT1}$ = 50 mA**

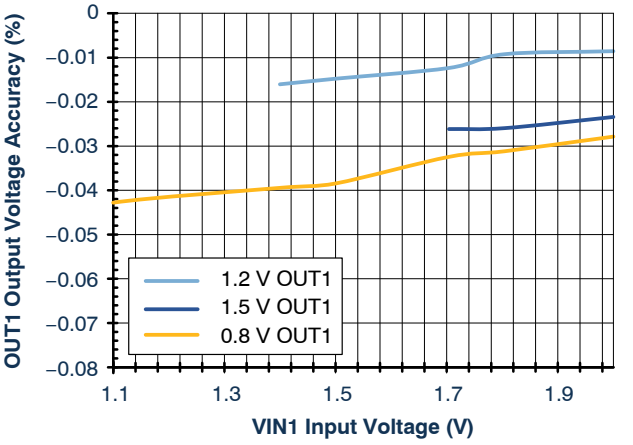



**Figure 10. LDO1 Output Voltage Accuracy vs. Input and Output Voltage, $I_{OUT1}$ = 50 mA**

## TYPICAL CHARACTERISTICS (continued)

(Unless otherwise noted, $T_A$ = 25°C, For LDO Mode: $V_{VSYS}$ = 3.45 V, $V_{VIN1}$ = 1.3 V, $V_{VIN2}$ = 3.45 V, $V_{VIN3}$ and $V_{VIN4}$ = 1.95 V; For LS Mode: $V_{VSYS}$ = 3.80 V, $V_{VIN1}$ = s$V_{VIN3}$ = $V_{VIN4}$ = 1.8 V and $V_{VIN2}$ = 5.0 V. Using components from Recommended External Components.)

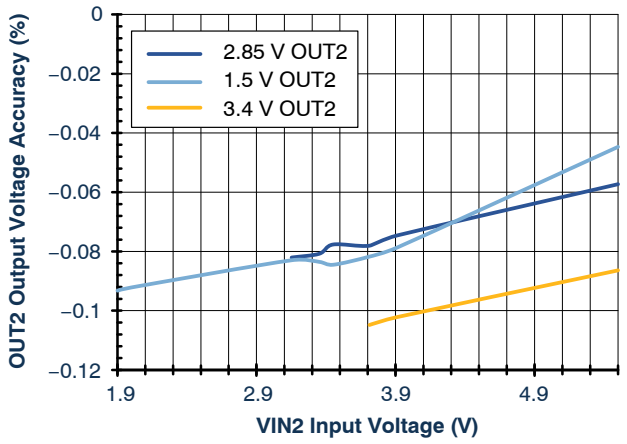



**Figure 11. LDO2 Output Voltage Accuracy vs. Input and Output Voltage, $I_{OUT2}$ = 50 mA**

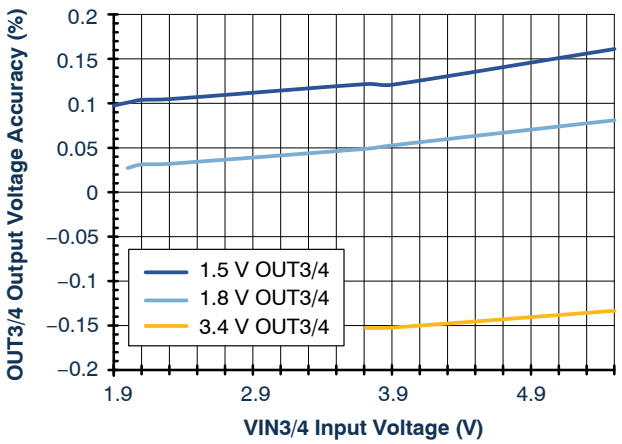



**Figure 12. LDO3/4 Output Voltage Accuracy vs. Input and Output Voltage, $I_{OUT3/4}$ = 50 mA**

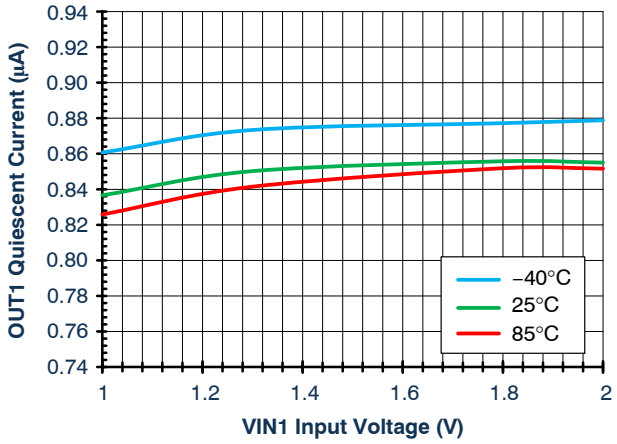



**Figure 13. LS1 Quiescent Current vs. Input Voltage and Temperature**

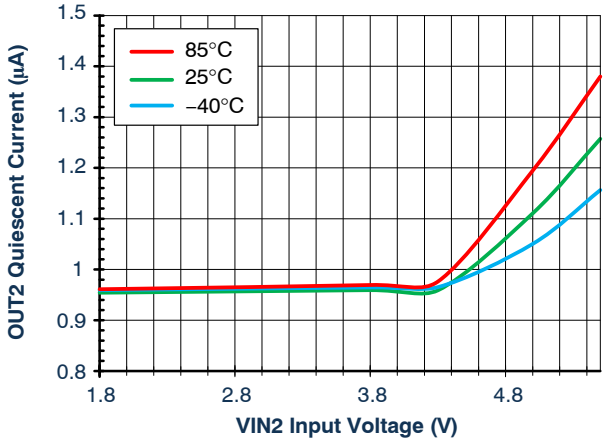



**Figure 14. LS2 Quiescent Current vs. Input Voltage and Temperature**

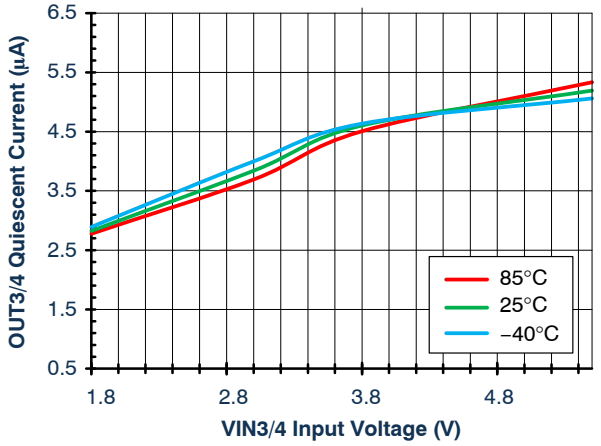



**Figure 15. LS3/4 Quiescent Current vs. Input Voltage and Temperature**

## TYPICAL CHARACTERISTICS (continued)

(Unless otherwise noted, $T_A$ = 25°C, For LDO Mode: $V_{VSYS}$ = 3.45 V, $V_{VIN1}$ = 1.3 V, $V_{VIN2}$ = 3.45 V, $V_{VIN3}$ and $V_{VIN4}$ = 1.95 V; For LS Mode: $V_{VSYS}$ = 3.80 V, $V_{VIN1}$ = $V_{VIN3}$ = $V_{VIN4}$ = 1.8 V and $V_{VIN2}$ = 5.0 V. Using components from Recommended External Components.)

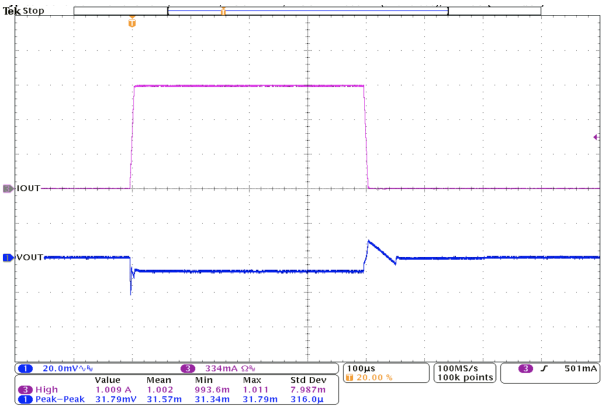



**Figure 16. LDO1 Load Transient, $V_{VSYS}$ = 3.45 V, $V_{VIN1}$ = 1.4 V, $V_{OUT1}$ = 1.2 V, 1 mA <–> 1000 mA, 6 µs Edge**

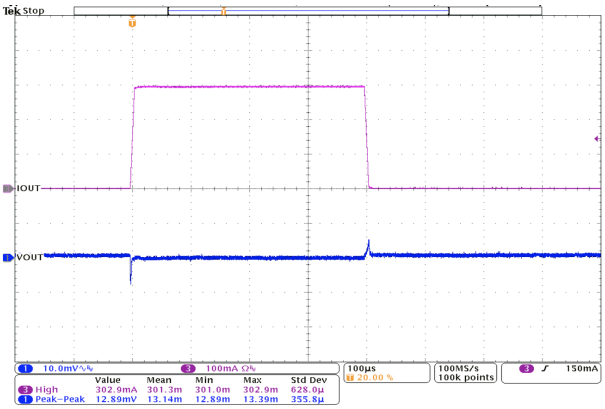



**Figure 17. LDO2 Load Transient, $V_{VSYS}$ = 3.45 V, $V_{VIN2}$ = 3.45 V, $V_{OUT2}$ = 2.85 V, 1 mA <–> 300 mA, 6 µs Edge**

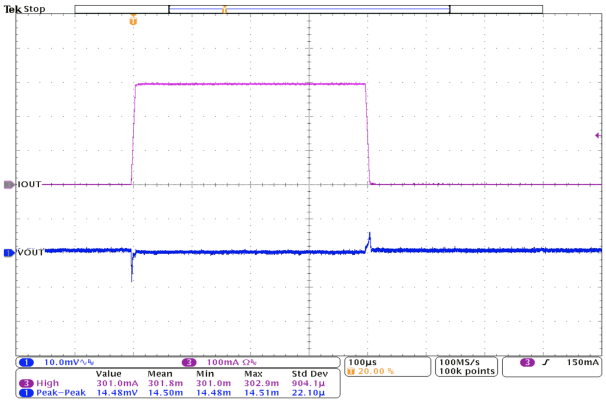



**Figure 18. LDO3/4 Load Transient, $V_{VSYS}$ = 3.45 V, $V_{VIN3/4}$ = 2.0 V, $V_{OUT3/4}$ = 1.8 V, 1 mA <–> 300 mA, 6 µs Edge**

## TYPICAL CHARACTERISTICS (continued)

(Unless otherwise noted, $T_A$ = 25°C, For LDO Mode: $V_{VSYS}$ = 3.45 V, $V_{VIN1}$ = 1.3 V, $V_{VIN2}$ = 3.45 V, $V_{VIN3}$ and $V_{VIN4}$ = 1.95 V; For LS Mode: $V_{VSYS}$ = 3.80 V, $V_{VIN1}$ = $V_{VIN3}$ = $V_{VIN4}$ = 1.8 V and $V_{VIN2}$ = 5.0 V. Using components from Recommended External Components.)

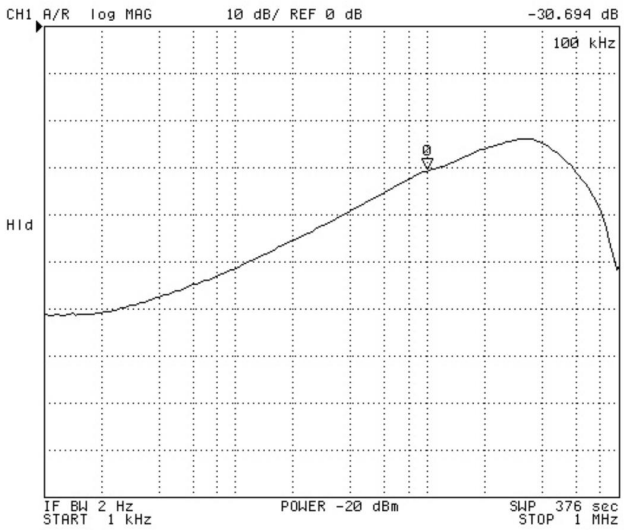



**Figure 19. LDO1 PSRR vs. Frequency, $V_{OUT1}$ = 1.2 V, $I_{OUT1}$ = 150 mA**

**Figure 20. LDO1 PSRR vs. Frequency, $V_{OUT1}$ = 1.05 V, $I_{OUT1}$ = 150 mA**

**Figure 21. LDO2 PSRR vs. Frequency, $V_{OUT2}$ = 2.85 V, $I_{OUT2}$ = 100 mA**

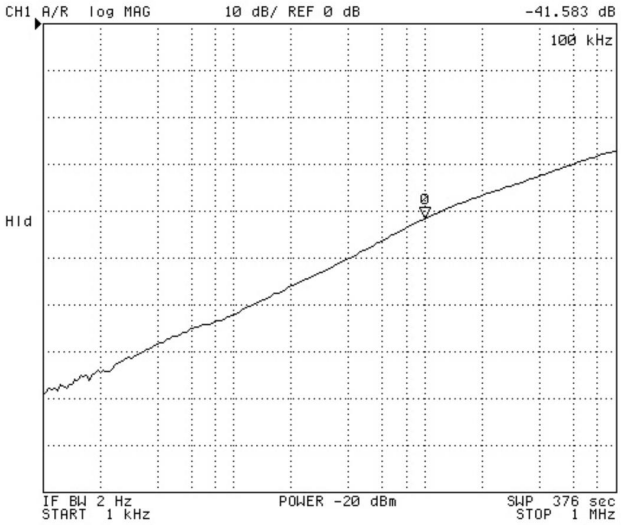



**Figure 22. LDO3/4 PSRR vs. Frequency, $V_{OUT3/4}$ = 1.8 V, $I_{OUT3/4}$ = 100 mA**

## FUNCTIONAL SPECIFICATIONS

### Device Operation

*Overview*

The FAN53840 PMIC is optimized to supply different sub systems of battery powered mobile and IoT applications. It integrates four channels that can be set to operate as LDOs or Load−Switches (LS). The LDOs are low−dropout regulators: one high−current and three high PSRR/low noise LDOs. The LS are very low $R_{DS(on)}$ and operate at low currents.

The features of the FAN53840 can be programmed through an $I^2C$ interface.

*Under Voltage Lockout (UVLO)*

The device features system and LDO UVLO protections. When all channels are not selected as LDOs and LS, if the system voltage ($V_{sys}$) falls below its UVLO falling threshold, system UVLO interrupt and status bits will be set and INT_B asserted low. The status bit will remain set until $V_{sys}$ rises above its UVLO rising threshold. If all LS are selected (By selecting all ldo_lsx bits), no bits will be set; selecting all LS disables system UVLO protection faults. In this state it is possible to operate the four load−switches with their $V_{IN}$ below the range stated in the Recommended Operating Conditions table. This is likely to increase LS $RDS_{ON2}$ and therefore output current derating should be expected.

When enabling LDOs, if $V_{sys}$ is above the Power On Reset (POR) voltage of 2 V but below its UVLO rising threshold, or, if $V_{sys}$ is above its UVLO rising threshold but LDO input voltages are below their UVLO rising thresholds, corresponding UVLO interrupt and status bits will be set and INT_B asserted low. The status bits remain set as long the UVLO fault condition is present.

Similarly, bits and INT_B will be set and asserted low, respectively, when $V_{sys}$ falls below its UVLO falling threshold and channels are not all configured as LS, or, $V_{sys}$ is above its UVLO rising threshold but LDO input voltages fall below their UVLO falling threshold.

In the cases above, the LDOs will not be restarted for a minimum of 20ms and until $V_{sys}$ rises above its rising threshold. Individual LDOs are permanently disabled after four cumulative faults including UVLO faults. The LDOs need to be enabled to return to operation. If the four cumulative faults are a combination of thermal−shutdown and system UVLO faults, then prior to enabling the LDOs, RESET_B pin needs to be toggled from low to high.

*Thermal Management*

When the die temperature rises to the Thermal Warning ($T_{WRN}$) threshold, interrupt and status bits indicating thermal−warning are set and INT_B asserted low. The status bit remains set until the die temperature drops to a nominal 105°C.

If the die temperature continues to rise to the Thermal Shutdown threshold, interrupt and status bits indicating thermal−shutdown will be set and INT_B asserted low. All channels will be disabled but $I^2C$ communication will remain. The status bit will remain set until the die temperature drops to $T_{WRN}$. The chip suspension bit is set upon shutdown.

After the die temperature falls below $T_{WRN}$, the thermal status and chip suspension bits will be cleared, and the device will return to the operating conditions prior to the thermal−shutdown event. Individual LDOs are permanently disabled after four cumulative faults including thermal faults. If the four cumulative faults are a combination of thermal−shutdown and system UVLO faults, then prior to enabling the LDOs, RESET_B pin needs to be toggled from low to high.

Similarly to system UVLO, selecting all LS will render thermal protection faults inactive.

*Enabling/Disabling*

The channels can be enabled and disabled independently with the ldo*x*_en bits. To enable LDOs, with RESET_B set high, select desired ldo*x*_en bits while setting *all* ldo_ls*x* bits to “0”. The LDOs have internal soft−start which limits the inrush current to the current−limit setting of the LDO. The LDOs will ignore faults during the first 1.5 ms while starting−up.

To enable LS, with RESET_B set high, select desired ldo*x*_en bits while setting *all* ldo_ls*x* bits to “1”. The ldo*x*_en and ldo_lsx bits can be found in the ENABLE and LDO_LS_SELECT registers, respectively.

The device features active discharge. This feature is enabled through the ldo*x*_discharge_enabled bits. A 100 Ω resistor is connected internally between channel outputs and GND to discharge the output capacitors. The ldo*x*_discharge_enabled bits can be found in the ENABLE register.

To do a global shutdown of all channels, set RESET_B pin to low.

It is not recommended to change configuration from LS to LDO operation while the output is loaded. The channel will attempt a restart and the output may drop significantly. It is recommended to first de−select the channels (with ldo*x*_en bits), de−select *all* ldo_ls*x* bits, then select the channels for LDO operation.

*Over−Current Protection (OCP)*

The LDOs are protected from short−circuits and excessive loads. When a short−circuit or excessive load condition occurs on an output, the current is limited to the Current Limit value of the LDO and, depending on the difference between input and programmed output voltage, the output voltage may drop. The resultant output voltage is the product of Current Limit and load impedance.

When a current−limit event is detected, the LDOs’ associated OCP status bit is set. If the LDO remains in current−limit for 1 ms, the corresponding interrupt bit is set and INT_B asserted low. The LDO will be shutdown and a restarts attempted every 20 ms. Individual LDOs are

permanently disabled after four cumulative faults including OCP faults. The LDOs need to be enabled to return to operation.

*Multiple Fault Shutdown*

To prevent repetitive starting and faulting of an LDO or of the IC itself, detection of four faults will result in a complete shutdown of an LDO or, if system faults, the IC will shutdown.

Individual LDO Fault: the LDO will be shutdown after the fourth fault for any combination of UVLO and/or OCP faults. The LDO will automatically be de−selected and will require enabling to return to operation.

System Fault: all channels will be shutdown after the fourth chip fault for any combination of thermal−shutdown and/or system UVLO faults. All channels will automatically be de−selected. Enabling of the channels will require RESET_B pin to be toggled from low to high first.

*Reset*

When the RESET_B pin is pulled LOW, the INTERRUPTx and STATUSx bits will be cleared. All the other registers will remain set to their programmed values, but $I^2C$ communication with the device is disabled. Additionally, all internal fault counters will reset to 0.

When the RESET_B pin is pulled HIGH, the $I^2C$ block is turned on. The Reset_B pin should not be asserted high while there is data transmission on the $I^2C$ bus. This will ensure the FAN53840 doesn't mis−interpret a logic low on SDA as a falling edge and inadvertently create a "Start" condition, and unintended data written to the FAN53840 registers. It is recommended that the FAN53840 is enabled when there is a brief break in $I^2C$ data transmissions.

The SOFT_RESET bits in the RESET register can be used to clear all registers to their default values.

*No Fault Shutdown*

When No Fault Shutdown feature is selected, LDOs are prevented from shutting down during an OCP event but are not prevented from shutting down due to a UVLO fault event. When these events occur, the interrupt and status bits will indicate a fault but the fault counter will not be incremented.

This feature is activated by setting no_fault_shudown bit in RESET register to "1".

### $I^2C$ Functionality

*$I^2C$ Interface*

The FAN53840 serial interface is compatible with Standard, Fast and Fast Plus Mode $I^2C$ Bus specifications. The SCL line is an input and its SDA line is a bi−directional open−drain output; it can only pull down the bus when active. The SDA line only pulls LOW during data reads and when signaling ACK. All data is shifted in MSB (bit 7) first.

Please refer to the *Reset* section for guidance on RESET_B LOW to HIGH pin timing for proper enabling of the $I^2C$ block.

*I2C Slave Address*

The FAN53840 provides three different $I^2C$ addresses. The addresses can be set by connecting the ADDR pin according to the settings in Table 2. Depending on the setting of the ADDR Pin when RESET_B is asserted high, the device address will be selected. To reset the address, disable the device by pulling RESET_B low. Reconfigure the ADDR pin to the desired setting then enable the device by asserting RESET_B high.

The $I^2C$ is accessible approximately 300 μs after enabling the device through asserting RESET_B high. For reliable reads of the ADDR pin setting, it is recommended for ADDR pin not to change states during the 300 μs detection period. Providing the system power pin voltage does not fall below POR level, register values will be retained while RESET_B pin is maintained low.

A precautionary measure: registers should be reprogrammed to desired values anytime a system UVLO fault is detected.

Other default slave addresses can be accommodated by contacting an **onsemi** representative.

**Table 2. $I^2C$ SLAVE ADDRESS**

| C3, ADDR Pin Connected to | Address |
|---|---|
| VSYS | 7'h72 |
| Floating | 7'h61 |
| Ground | 7'h20 |

*Bus Timing*

As shown in Figure 23, data is normally transferred when SCL is LOW. Data is clocked in on the rising edge of SCL. Typically, data transitions shortly at or after the falling edge of SCL to allow ample time for the data to set up before the next SCL rising edge.

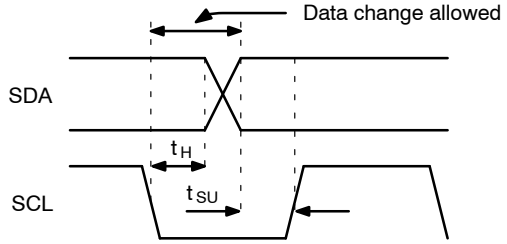



**Figure 23. Data Transfer Timing**

Each bus transaction begins and ends with SDA and SCL HIGH. A transaction begins with a START condition, which is defined as SDA transitioning from 1 to 0 with SCL HIGH, as shown in Figure 24.

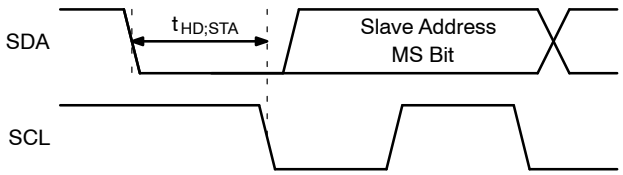



**Figure 24. Start Bit**

Transactions end with a STOP condition, which is SDA transitioning from 0 to 1 with SCL HIGH, as shown in Figure 25.

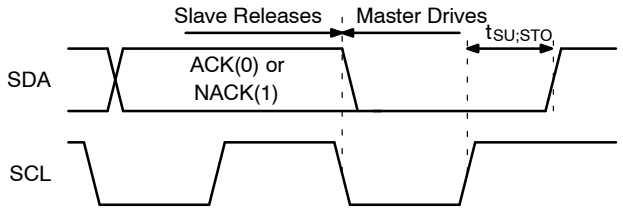



**Figure 25. Stop Bit**

During a read from the FAN53840, the master issues a Repeated Start after sending the register address and before resending the slave address. The Repeated Start is a 1−to−0 transition on SDA while SCL is HIGH, as shown in Figure 26.

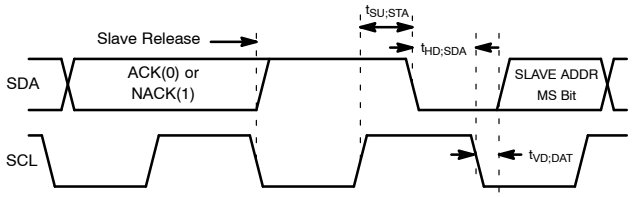



**Figure 26. Repeated Start Timing**

*Read and Write Transactions*

The figures below outline the sequences for data read and write. Bus control is signified by the shading of the packet, defined as Master Drives Bus and Slave Drives Bus. All addresses and data are MSB first.

*Multi−Byte (Sequential) Read and Write Transactions*

Sequential Write (Figure 29)

The Slave Address, Reg Addr address, and the first data byte are transmitted to the FAN53840 in the same way as in a single−byte write (Figure 27). However, instead of generating a Stop condition, the master transmits additional bytes that are written to consecutive sequential registers after the falling edge of the eighth bit. After the last byte written and its ACK bit received, the master issues a STOP bit. The IC contains an 8−bit counter that increments the address pointer after each byte is written.

Sequential Read (Figure 30)

Sequential reads are initiated in the same way as a single−byte read (Figure 28), except that once the slave transmits the first data byte, the master issues an acknowledge instead of a STOP condition. This directs the slave's $I^2C$ logic to transmit the next sequentially addressed 8−bit word. The FAN53840 contains an 8−bit counter that increments the address pointer after each byte is read, which allows the entire memory contents to be read during one $I^2C$ transaction.

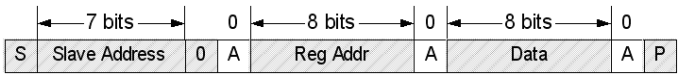



**Figure 27. Single−Byte Write Transaction**

**Figure 28. Single−Byte Read Transaction**

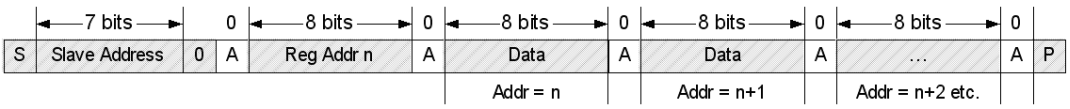



**Figure 29. Multi−Byte (Sequential) Write Transaction**

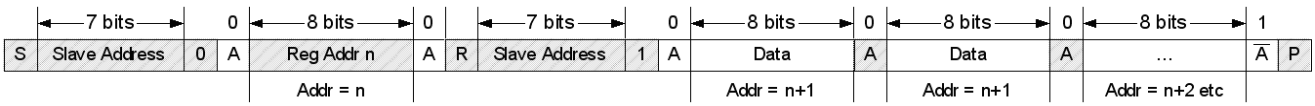



**Figure 30. Multi−Byte (Sequential) Read Transaction**

## REGISTER MAPPING TABLE

**Table 3. REGISTER MAPPING**

| | | | | | Read Only | Write Only | Read/Write | Read/Clear | Write/Clear |
|---|---|---|---|---|---|---|---|---|---|
| **Address** | **Name** | **Bit[7]** | **Bit[6]** | **Bit[5]** | **Bit[4]** | **Bit[3]** | **Bit[2]** | **Bit[1]** | **Bit[0]** |
| 0x00 | PRODUCT ID | Product ID | | | | | | | |
| 0x01 | SILICON REV ID | Revision | | | | | | | |
| 0x02 | ENABLE | OUT4_DIS | OUT3_DIS | OUT2_DIS | OUT1_DIS | CHAN4_EN | CHAN3_EN | CHAN2_EN | CHAN1_EN |
| 0x03 | CHAN1 | UNUSED | LDO1_VOUT | | | | | | |
| 0x04 | CHAN2 | LDO2_VOUT | | | | | | | |
| 0x05 | CHAN3 | LDO3_VOUT | | | | | | | |
| 0x06 | CHAN4 | LDO4_VOUT | | | | | | | |
| 0x07 | RESET | SOFT_RESET | | | | UNUSED | OCP_TIMER | | FLT_SD_B |
| 0x08 | LDO_COMP0 | LDO4_COMP_SEL | | LDO3_COMP_SEL | | LDO2_COMP_SEL | | LDO1_COMP_SEL | |
| 0x09 | INTERRUPT1 | UNUSED | UNUSED | UNUSED | UNUSED | LDO4_OCP_INT | LDO3_OCP_INT | LDO2_OCP_INT | LDO1_OCP_INT |
| 0x0A | INTERRUPT2 | UNUSED | TSD_INT | TSD_WRN_INT | VSYS_UVLO_INT | CHAN4_UVLO_INT | CHAN3_UVLO_INT | CHAN2_UVLO_INT | CHAN1_UVLO_INT |
| 0x0B | STATUS1 | UNUSED | UNUSED | UNUSED | UNUSED | LDO4_OCP_STAT | LDO3_OCP_STAT | LDO2_OCP_STAT | LDO1_OCP_STAT |
| 0x0C | STATUS2 | UNUSED | TSD_STAT | TSD_WRN_STAT | VSYS_UVLO_STAT | CHAN4_UVLO_STAT | CHAN3_UVLO_STAT | CHAN2_UVLO_STAT | CHAN1_UVLO_STAT |
| 0x0D | STATUS3 | UNUSED | UNUSED | UNUSED | CHIP_SUSD | CHAN4_SUSD | CHAN3_SUSD | CHAN2_SUSD | CHAN1_SUSD |
| 0x0E | MINT1 | UNUSED | UNUSED | UNUSED | UNUSED | MASK_LDO4_OCP | MASK_LDO3_OCP | MASK_LDO2_OCP | MASK_LDO1_OCP |
| 0x0F | MINT2 | UNUSED | MASK_TSD | MASK_TSD_WRN | MASK_VSYS_UVLO | MASK_CHAN4_UVLO | MASK_CHAN3_UVLO | MASK_CHAN2_UVLO | MASK_CHAN1_UVLO |
| 0x10 | LDO_LS_SELECT | UNUSED | UNUSED | UNUSED | UNUSED | LDO_LS4_SELECT | LDO_LS3_SELECT | LDO_LS2_SELECT | LDO_LS1_SELECT |

## REGISTER DETAILS

**Table 4. REGISTER DETAILS – 0x00 PRODUCT ID**

| 0x00 PRODUCT ID | | | | Default = 00000001 | |
|---|---|---|---|---|---|
| **Bit** | **Name** | **Default** | **Type** | **Description** | |
| 7:0 | Product ID | 00000001 | Read | **Allows Customers to Identify Manufacturer and Version** | |
| | | | | **Product ID Table** | |
| | | | | **Code** | **Product** |
| | | | | 00000000 | – |
| | | | | 00000001 | FAN53840 |
| | | | | 00000010 | Reserved |
| | | | | 00000011 | Reserved |
| | | | | 00000100 | Reserved |
| | | | | 00000101 | Reserved |
| | | | | 00000110 | Reserved |
| | | | | 00000111 | Reserved |
| | | | | 00001000 | Reserved |
| | | | | 00001001 | Reserved |
| | | | | 00001010 | Reserved |
| | | | | 00001011 | Reserved |
| | | | | 00001100 | Reserved |
| | | | | 00001101 | Reserved |
| | | | | 00001110 | Reserved |
| | | | | 00001111 | Reserved |

**Table 5. REGISTER DETAILS – 0X01 SILICON REV ID**

| 0x01 SILICON REV ID | | | | Default = 00000000 | | |
|---|---|---|---|---|---|---|
| **Bit** | **Name** | **Default** | **Type** | **Description** | | |
| 7:0 | Revision | 00000000 | Read | **Provides the Silicon Revision** | | |
| | | | | **REG 01 [7:0] SILICON REV ID** | **REG 84 [3:0] INTERNAL REVISION** | **Revision** |
| | | | | 00000000 | 0000 | A_REVA |
| | | | | 00000001 | 0001 | |
| | | | | 00000010 | 0010 | |
| | | | | 00000011 | 0011 | |
| | | | | 00000100 | 0100 | |

**Table 6. REGISTER DETAILS – 0X02 ENABLE**

| 0x02 ENABLE | | | | Default = 00000000 | |
|---|---|---|---|---|---|
| **Bit** | **Name** | **Default** | **Type** | **Description** | |
| 7 | OUT4_DIS | 0 | R/W | **Code** | **Discharge Enabled/Disabled** |
| | | | | 0 | OUT4 Active Discharge feature is disabled. Pull down will not be activated when OUT4 is disabled by any event. |
| | | | | 1 | OUT4 Active Discharge feature is enabled. See description of Active Pulldowns in the Device Operation. |
| 6 | OUT3_DIS | 0 | R/W | **Code** | **Discharge Enabled/Disabled** |
| | | | | 0 | OUT3 Active Discharge feature is disabled. Pull down will not be activated when LDO3 is disabled by any event. |
| | | | | 1 | OUT3 Active Discharge feature is enabled. See description of Active Pulldowns in the Device Operation. |
| 5 | OUT2_DIS | 0 | R/W | **Code** | **Discharge Enabled/Disabled** |
| | | | | 0 | OUT2 Active Discharge feature is disabled. Pull down will not be activated when LDO2 is disabled by any event. |
| | | | | 1 | OUT2 Active Discharge feature is enabled. See description of Active Pulldowns in the Device Operation. |
| 4 | OUT1_DIS | 0 | R/W | **Code** | **Discharge Enabled/Disabled** |
| | | | | 0 | OUT1 Active Discharge feature is disabled. Pull down will not be activated when LDO1 is disabled by any event. |
| | | | | 1 | OUT1 Active Discharge feature is enabled. See description of Active Pulldowns in the Device Operation. |
| 3 | CHAN4_EN | 0 | R/W | Enable bit for CHAN #4. | |
| | | | | **Code** | **Status of CHAN4** |
| | | | | 0 | Disabled |
| | | | | 1 | Enabled |
| 2 | CHAN3_EN | 0 | R/W | Enable bit for CHAN #3. | |
| | | | | **Code** | **Status of CHAN3** |
| | | | | 0 | Disabled |
| | | | | 1 | Enabled |
| 1 | CHAN2_EN | 0 | R/W | Enable bit for CHAN #2. | |
| | | | | **Code** | **Status of CHAN2** |
| | | | | 0 | Disabled |
| | | | | 1 | Enabled |
| 0 | CHAN1_EN | 0 | R/W | Enable bit for CHAN #1. | |
| | | | | **Code** | **Status of CHAN1** |
| | | | | 0 | Disabled |
| | | | | 1 | Enabled |

**Table 7. REGISTER DETAILS – 0X03 CHAN1**

| 0x03 CHAN1 | | | | Default = 00000000 | | | |
|---|---|---|---|---|---|---|---|
| **Bit** | **Name** | **Default** | **Type** | **Description** | | | |
| 7 | UNUSED | 0 | Read | | | | |
| 6:0 | LDO1_VOUT | 0000000 | R/W | When LDO_LS1_SELECT bit is set to “0”, these register bits sets LDO1 regulation target voltage.<br>Equation: Vout = 0.800 V + [(d – 35) * 8 mV];<br>Where d is the decimal value of the register.<br>The Default (0000000) points to the OTP programmed default value. If this register is not reprogrammed, a read of the register will return 00h. | | | |
| | | | | **Hex** | **VOUT** | **Hex** | **VOUT** |
| | | | | 00 | DEFAULT | 40 | 1.032 V |
| | | | | 01 | Reserved | 41 | 1.040 V |
| | | | | 02 | Reserved | 42 | 1.048 V |
| | | | | 03 | Reserved | 43 | 1.056 V |
| | | | | 04 | Reserved | 44 | 1.064 V |
| | | | | 05 | Reserved | 45 | 1.072 V |
| | | | | 06 | Reserved | 46 | 1.080 V |
| | | | | 07 | Reserved | 47 | 1.088 V |
| | | | | 08 | Reserved | 48 | 1.096 V |
| | | | | 09 | Reserved | 49 | 1.104 V |
| | | | | 0A | Reserved | 4A | 1.112 V |
| | | | | 0B | Reserved | 4B | 1.120 V |
| | | | | 0C | Reserved | 4C | 1.128 V |
| | | | | 0D | Reserved | 4D | 1.136 V |
| | | | | 0E | Reserved | 4E | 1.144 V |
| | | | | 0F | Reserved | 4F | 1.152 V |
| | | | | 10 | Reserved | 50 | 1.160 V |
| | | | | 11 | Reserved | 51 | 1.168 V |
| | | | | 12 | Reserved | 52 | 1.176 V |
| | | | | 13 | Reserved | 53 | 1.184 V |
| | | | | 14 | Reserved | 54 | 1.192 V |
| | | | | 15 | Reserved | 55 | 1.200 V |
| | | | | 16 | Reserved | 56 | 1.208 V |
| | | | | 17 | Reserved | 57 | 1.216 V |
| | | | | 18 | Reserved | 58 | 1.224 V |
| | | | | 19 | Reserved | 59 | 1.232 V |
| | | | | 1A | Reserved | 5A | 1.240 V |
| | | | | 1B | Reserved | 5B | 1.248 V |
| | | | | 1C | Reserved | 5C | 1.256 V |
| | | | | 1D | Reserved | 5D | 1.264 V |
| | | | | 1E | Reserved | 5E | 1.272 V |
| | | | | 1F | Reserved | 5F | 1.280 V |
| | | | | 20 | Reserved | 60 | 1.288 V |
| | | | | 21 | Reserved | 61 | 1.296 V |

**Table 7. REGISTER DETAILS – 0X03 CHAN1** (continued)

| 0x03 CHAN1 | | | | Default = 00000000 | | | |
|---|---|---|---|---|---|---|---|
| **Bit** | **Name** | **Default** | **Type** | **Description** | | | |
| 6:0 | LDO1_VOUT | 0000000 | R/W | 22 | Reserved | 62 | 1.304 V |
| | | | | 23 | 0.800 V | 63 | 1.312 V |
| | | | | 24 | 0.808 V | 64 | 1.320 V |
| | | | | 25 | 0.816 V | 65 | 1.328 V |
| | | | | 26 | 0.824 V | 66 | 1.336 V |
| | | | | 27 | 0.832 V | 67 | 1.344 V |
| | | | | 28 | 0.840 V | 68 | 1.352 V |
| | | | | 29 | 0.848 V | 69 | 1.360 V |
| | | | | 2A | 0.856 V | 6A | 1.368 V |
| | | | | 2B | 0.864 V | 6B | 1.376 V |
| | | | | 2C | 0.872 V | 6C | 1.384 V |
| | | | | 2D | 0.880 V | 6D | 1.392 V |
| | | | | 2E | 0.888 V | 6E | 1.400 V |
| | | | | 2F | 0.896 V | 6F | 1.408 V |
| | | | | 30 | 0.904 V | 70 | 1.416 V |
| | | | | 31 | 0.912 V | 71 | 1.424 V |
| | | | | 32 | 0.920 V | 72 | 1.432 V |
| | | | | 33 | 0.928 V | 73 | 1.440 V |
| | | | | 34 | 0.936 V | 74 | 1.448 V |
| | | | | 35 | 0.944 V | 75 | 1.456 V |
| | | | | 36 | 0.952 V | 76 | 1.464 V |
| | | | | 37 | 0.960 V | 77 | 1.472 V |
| | | | | 38 | 0.968 V | 78 | 1.480 V |
| | | | | 39 | 0.976 V | 79 | 1.488 V |
| | | | | 3A | 0.984 V | 7A | 1.496 V |
| | | | | 3B | 0.992 V | 7B | 1.504 V |
| | | | | 3C | 1.000 V | 7C | Reserved |
| | | | | 3D | 1.008 V | 7D | Reserved |
| | | | | 3E | 1.016 V | 7E | Reserved |
| | | | | 3F | 1.024 V | 7F | Reserved |

**Table 8. REGISTER DETAILS – 0X04 CHAN2**

| 0x04 CHAN2 | | | | Default = 00000000 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Bit** | **Name** | **Default** | **Type** | **Description** | | | | | | | |
| 7:0 | LDO2_VOUT | 00000000 | R/W | When LDO_LS2_SELECT bit is set to “0”, these register bits sets LDO2 regulation target voltage.<br>Equation: Vout = 1.500 V + [(d – 16) * 8 mV];<br>where d is the decimal value of the register.<br>The Default (00h) points to the OTP programmed default value. If this register is not reprogrammed, a read of the register will return 00h. | | | | | | | |
| | | | | **Hex** | **VOUT** | **Hex** | **VOUT** | **Hex** | **VOUT** | **Hex** | **VOUT** |
| | | | | 00 | DEFAULT | 40 | 1.884 V | 80 | 2.396 V | C0 | 2.908 V |
| | | | | 01 | Reserved | 41 | 1.892 V | 81 | 2.404 V | C1 | 2.916 V |
| | | | | 02 | Reserved | 42 | 1.900 V | 82 | 2.412 V | C2 | 2.924 V |
| | | | | 03 | Reserved | 43 | 1.908 V | 83 | 2.420 V | C3 | 2.932 V |
| | | | | 04 | Reserved | 44 | 1.916 V | 84 | 2.428 V | C4 | 2.940 V |
| | | | | 05 | Reserved | 45 | 1.924 V | 85 | 2.436 V | C5 | 2.948 V |
| | | | | 06 | Reserved | 46 | 1.932 V | 86 | 2.444 V | C6 | 2.956 V |
| | | | | 07 | Reserved | 47 | 1.940 V | 87 | 2.452 V | C7 | 2.964 V |
| | | | | 08 | Reserved | 48 | 1.948 V | 88 | 2.460 V | C8 | 2.972 V |
| | | | | 09 | Reserved | 49 | 1.956 V | 89 | 2.468 V | C9 | 2.980 V |
| | | | | 0A | Reserved | 4A | 1.964 V | 8A | 2.476 V | CA | 2.988 V |
| | | | | 0B | Reserved | 4B | 1.972 V | 8B | 2.484 V | CB | 2.996 V |
| | | | | 0C | Reserved | 4C | 1.980 V | 8C | 2.492 V | CC | 3.004 V |
| | | | | 0D | Reserved | 4D | 1.988 V | 8D | 2.500 V | CD | 3.012 V |
| | | | | 0E | Reserved | 4E | 1.996 V | 8E | 2.508 V | CE | 3.020 V |
| | | | | 0F | Reserved | 4F | 2.004 V | 8F | 2.516 V | CF | 3.028 V |
| | | | | 10 | 1.500 V | 50 | 2.012 V | 90 | 2.524 V | D0 | 3.036 V |
| | | | | 11 | 1.508 V | 51 | 2.020 V | 91 | 2.532 V | D1 | 3.044 V |
| | | | | 12 | 1.516 V | 52 | 2.028 V | 92 | 2.540 V | D2 | 3.052 V |
| | | | | 13 | 1.524 V | 53 | 2.036 V | 93 | 2.548 V | D3 | 3.060 V |
| | | | | 14 | 1.532 V | 54 | 2.044 V | 94 | 2.556 V | D4 | 3.068 V |
| | | | | 15 | 1.540 V | 55 | 2.052 V | 95 | 2.564 V | D5 | 3.076 V |
| | | | | 16 | 1.548 V | 56 | 2.060 V | 96 | 2.572 V | D6 | 3.084 V |
| | | | | 17 | 1.556 V | 57 | 2.068 V | 97 | 2.580 V | D7 | 3.092 V |
| | | | | 18 | 1.564 V | 58 | 2.076 V | 98 | 2.588 V | D8 | 3.100 V |
| | | | | 19 | 1.572 V | 59 | 2.084 V | 99 | 2.596 V | D9 | 3.108 V |
| | | | | 1A | 1.580 V | 5A | 2.092 V | 9A | 2.604 V | DA | 3.116 V |
| | | | | 1B | 1.588 V | 5B | 2.100 V | 9B | 2.612 V | DB | 3.124 V |
| | | | | 1C | 1.596 V | 5C | 2.108 V | 9C | 2.620 V | DC | 3.132 V |
| | | | | 1D | 1.604 V | 5D | 2.116 V | 9D | 2.628 V | DD | 3.140 V |
| | | | | 1E | 1.612 V | 5E | 2.124 V | 9E | 2.636 V | DE | 3.148 V |
| | | | | 1F | 1.620 V | 5F | 2.132 V | 9F | 2.644 V | DF | 3.156 V |
| | | | | 20 | 1.628 V | 60 | 2.140 V | A0 | 2.652 V | E0 | 3.164 V |
| | | | | 21 | 1.636 V | 61 | 2.148 V | A1 | 2.660 V | E1 | 3.172 V |
| | | | | 22 | 1.644 V | 62 | 2.156 V | A2 | 2.668 V | E2 | 3.180 V |
| | | | | 23 | 1.652 V | 63 | 2.164 V | A3 | 2.676 V | E3 | 3.188 V |
| | | | | 24 | 1.660 V | 64 | 2.172 V | A4 | 2.684 V | E4 | 3.196 V |
| | | | | 25 | 1.668 V | 65 | 2.180 V | A5 | 2.692 V | E5 | 3.204 V |

**Table 8. REGISTER DETAILS – 0X04 CHAN2** (continued)

| 0x04 CHAN2 | | | | Default = 00000000 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Bit** | **Name** | **Default** | **Type** | **Description** | | | | | | | |
| | | | | 26 | 1.676 V | 66 | 2.188 V | A6 | 2.700 V | E6 | 3.212 V |
| | | | | 27 | 1.684 V | 67 | 2.196 V | A7 | 2.708 V | E7 | 3.220 V |
| | | | | 28 | 1.692 V | 68 | 2.204 V | A8 | 2.716 V | E8 | 3.228 V |
| | | | | 29 | 1.700 V | 69 | 2.212 V | A9 | 2.724 V | E9 | 3.236 V |
| | | | | 2A | 1.708 V | 6A | 2.220 V | AA | 2.732 V | EA | 3.244 V |
| | | | | 2B | 1.716 V | 6B | 2.228 V | AB | 2.740 V | EB | 3.252 V |
| | | | | 2C | 1.724 V | 6C | 2.236 V | AC | 2.748 V | EC | 3.260 V |
| | | | | 2D | 1.732 V | 6D | 2.244 V | AD | 2.756 V | ED | 3.268 V |
| | | | | 2E | 1.740 V | 6E | 2.252 V | AE | 2.764 V | EE | 3.276 V |
| | | | | 2F | 1.748 V | 6F | 2.260 V | AF | 2.772 V | EF | 3.284 V |
| | | | | 30 | 1.756 V | 70 | 2.268 V | B0 | 2.780 V | F0 | 3.292 V |
| | | | | 31 | 1.764 V | 71 | 2.276 V | B1 | 2.788 V | F1 | 3.300 V |
| | | | | 32 | 1.772 V | 72 | 2.284 V | B2 | 2.796 V | F2 | 3.308 V |
| | | | | 33 | 1.780 V | 73 | 2.292 V | B3 | 2.804 V | F3 | 3.316 V |
| | | | | 34 | 1.788 V | 74 | 2.300 V | B4 | 2.812 V | F4 | 3.324 V |
| | | | | 35 | 1.796 V | 75 | 2.308 V | B5 | 2.820 V | F5 | 3.332 V |
| | | | | 36 | 1.804 V | 76 | 2.316 V | B6 | 2.828 V | F6 | 3.340 V |
| | | | | 37 | 1.812 V | 77 | 2.324 V | B7 | 2.836 V | F7 | 3.348 V |
| | | | | 38 | 1.820 V | 78 | 2.332 V | B8 | 2.844 V | F8 | 3.356 V |
| | | | | 39 | 1.828 V | 79 | 2.340 V | B9 | 2.852 V | F9 | 3.364 V |
| | | | | 3A | 1.836 V | 7A | 2.348 V | BA | 2.860 V | FA | 3.372 V |
| | | | | 3B | 1.844 V | 7B | 2.356 V | BB | 2.868 V | FB | 3.380 V |
| | | | | 3C | 1.852 V | 7C | 2.364 V | BC | 2.876 V | FC | 3.388 V |
| | | | | 3D | 1.860 V | 7D | 2.372 V | BD | 2.884 V | FD | 3.396 V |
| | | | | 3E | 1.868 V | 7E | 2.380 V | BE | 2.892 V | FE | 3.404 V |
| | | | | 3F | 1.876 V | 7F | 2.388 V | BF | 2.900 V | FF | 3.412 V |

**Table 9. REGISTER DETAILS – 0X05 CHAN3**

| 0x05 CHAN3 | | | | Default = 00000000 |
|---|---|---|---|---|
| **Bit** | **Name** | **Default** | **Type** | **Description** |
| 7:0 | LDO3_VOUT | 00000000 | R/W | When LDO_LS3_SELECT bit is set to “0”, these register bits sets LDO3 regulation target voltage.<br>Equation: Vout = 1.500 V + [(d – 16) * 8 mV];<br>where d is the decimal value of the register.<br>The Default (00h) points to the OTP programmed default value. If this register is not reprogrammed, a read of the register will return 00h. |

| Hex | VOUT | Hex | VOUT | Hex | VOUT | Hex | VOUT |
|---|---|---|---|---|---|---|---|
| 00 | DEFAULT | 40 | 1.884 V | 80 | 2.396 V | C0 | 2.908 V |
| 01 | Reserved | 41 | 1.892 V | 81 | 2.404 V | C1 | 2.916 V |
| 02 | Reserved | 42 | 1.900 V | 82 | 2.412 V | C2 | 2.924 V |
| 03 | Reserved | 43 | 1.908 V | 83 | 2.420 V | C3 | 2.932 V |
| 04 | Reserved | 44 | 1.916 V | 84 | 2.428 V | C4 | 2.940 V |
| 05 | Reserved | 45 | 1.924 V | 85 | 2.436 V | C5 | 2.948 V |
| 06 | Reserved | 46 | 1.932 V | 86 | 2.444 V | C6 | 2.956 V |
| 07 | Reserved | 47 | 1.940 V | 87 | 2.452 V | C7 | 2.964 V |
| 08 | Reserved | 48 | 1.948 V | 88 | 2.460 V | C8 | 2.972 V |
| 09 | Reserved | 49 | 1.956 V | 89 | 2.468 V | C9 | 2.980 V |
| 0A | Reserved | 4A | 1.964 V | 8A | 2.476 V | CA | 2.988 V |
| 0B | Reserved | 4B | 1.972 V | 8B | 2.484 V | CB | 2.996 V |
| 0C | Reserved | 4C | 1.980 V | 8C | 2.492 V | CC | 3.004 V |
| 0D | Reserved | 4D | 1.988 V | 8D | 2.500 V | CD | 3.012 V |
| 0E | Reserved | 4E | 1.996 V | 8E | 2.508 V | CE | 3.020 V |
| 0F | Reserved | 4F | 2.004 V | 8F | 2.516 V | CF | 3.028 V |
| 10 | 1.500 V | 50 | 2.012 V | 90 | 2.524 V | D0 | 3.036 V |
| 11 | 1.508 V | 51 | 2.020 V | 91 | 2.532 V | D1 | 3.044 V |
| 12 | 1.516 V | 52 | 2.028 V | 92 | 2.540 V | D2 | 3.052 V |
| 13 | 1.524 V | 53 | 2.036 V | 93 | 2.548 V | D3 | 3.060 V |
| 14 | 1.532 V | 54 | 2.044 V | 94 | 2.556 V | D4 | 3.068 V |
| 15 | 1.540 V | 55 | 2.052 V | 95 | 2.564 V | D5 | 3.076 V |
| 16 | 1.548 V | 56 | 2.060 V | 96 | 2.572 V | D6 | 3.084 V |
| 17 | 1.556 V | 57 | 2.068 V | 97 | 2.580 V | D7 | 3.092 V |
| 18 | 1.564 V | 58 | 2.076 V | 98 | 2.588 V | D8 | 3.100 V |
| 19 | 1.572 V | 59 | 2.084 V | 99 | 2.596 V | D9 | 3.108 V |
| 1A | 1.580 V | 5A | 2.092 V | 9A | 2.604 V | DA | 3.116 V |
| 1B | 1.588 V | 5B | 2.100 V | 9B | 2.612 V | DB | 3.124 V |
| 1C | 1.596 V | 5C | 2.108 V | 9C | 2.620 V | DC | 3.132 V |
| 1D | 1.604 V | 5D | 2.116 V | 9D | 2.628 V | DD | 3.140 V |
| 1E | 1.612 V | 5E | 2.124 V | 9E | 2.636 V | DE | 3.148 V |
| 1F | 1.620 V | 5F | 2.132 V | 9F | 2.644 V | DF | 3.156 V |
| 20 | 1.628 V | 60 | 2.140 V | A0 | 2.652 V | E0 | 3.164 V |
| 21 | 1.636 V | 61 | 2.148 V | A1 | 2.660 V | E1 | 3.172 V |
| 22 | 1.644 V | 62 | 2.156 V | A2 | 2.668 V | E2 | 3.180 V |
| 23 | 1.652 V | 63 | 2.164 V | A3 | 2.676 V | E3 | 3.188 V |
| 24 | 1.660 V | 64 | 2.172 V | A4 | 2.684 V | E4 | 3.196 V |
| 25 | 1.668 V | 65 | 2.180 V | A5 | 2.692 V | E5 | 3.204 V |

**Table 9. REGISTER DETAILS – 0X05 CHAN3** (continued)

| 0x05 CHAN3 | | | | Default = 00000000 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Bit** | **Name** | **Default** | **Type** | **Description** | | | | | | | |
| | | | | 26 | 1.676 V | 66 | 2.188 V | A6 | 2.700 V | E6 | 3.212 V |
| | | | | 27 | 1.684 V | 67 | 2.196 V | A7 | 2.708 V | E7 | 3.220 V |
| | | | | 28 | 1.692 V | 68 | 2.204 V | A8 | 2.716 V | E8 | 3.228 V |
| | | | | 29 | 1.700 V | 69 | 2.212 V | A9 | 2.724 V | E9 | 3.236 V |
| | | | | 2A | 1.708 V | 6A | 2.220 V | AA | 2.732 V | EA | 3.244 V |
| | | | | 2B | 1.716 V | 6B | 2.228 V | AB | 2.740 V | EB | 3.252 V |
| | | | | 2C | 1.724 V | 6C | 2.236 V | AC | 2.748 V | EC | 3.260 V |
| | | | | 2D | 1.732 V | 6D | 2.244 V | AD | 2.756 V | ED | 3.268 V |
| | | | | 2E | 1.740 V | 6E | 2.252 V | AE | 2.764 V | EE | 3.276 V |
| | | | | 2F | 1.748 V | 6F | 2.260 V | AF | 2.772 V | EF | 3.284 V |
| | | | | 30 | 1.756 V | 70 | 2.268 V | B0 | 2.780 V | F0 | 3.292 V |
| | | | | 31 | 1.764 V | 71 | 2.276 V | B1 | 2.788 V | F1 | 3.300 V |
| | | | | 32 | 1.772 V | 72 | 2.284 V | B2 | 2.796 V | F2 | 3.308 V |
| | | | | 33 | 1.780 V | 73 | 2.292 V | B3 | 2.804 V | F3 | 3.316 V |
| | | | | 34 | 1.788 V | 74 | 2.300 V | B4 | 2.812 V | F4 | 3.324 V |
| | | | | 35 | 1.796 V | 75 | 2.308 V | B5 | 2.820 V | F5 | 3.332 V |
| | | | | 36 | 1.804 V | 76 | 2.316 V | B6 | 2.828 V | F6 | 3.340 V |
| | | | | 37 | 1.812 V | 77 | 2.324 V | B7 | 2.836 V | F7 | 3.348 V |
| | | | | 38 | 1.820 V | 78 | 2.332 V | B8 | 2.844 V | F8 | 3.356 V |
| | | | | 39 | 1.828 V | 79 | 2.340 V | B9 | 2.852 V | F9 | 3.364 V |
| | | | | 3A | 1.836 V | 7A | 2.348 V | BA | 2.860 V | FA | 3.372 V |
| | | | | 3B | 1.844 V | 7B | 2.356 V | BB | 2.868 V | FB | 3.380 V |
| | | | | 3C | 1.852 V | 7C | 2.364 V | BC | 2.876 V | FC | 3.388 V |
| | | | | 3D | 1.860 V | 7D | 2.372 V | BD | 2.884 V | FD | 3.396 V |
| | | | | 3E | 1.868 V | 7E | 2.380 V | BE | 2.892 V | FE | 3.404 V |
| | | | | 3F | 1.876 V | 7F | 2.388 V | BF | 2.900 V | FF | 3.412 V |

**Table 10. REGISTER DETAILS – 0X06 CHAN4**

| 0x06 CHAN4 | | | | Default = 00000000 |
|---|---|---|---|---|
| **Bit** | **Name** | **Default** | **Type** | **Description** |
| 7:0 | LDO4_VOUT | 00000000 | R/W | When LDO_LS4_SELECT bit is set to “0”, these register bits sets LDO4 regulation target voltage.<br>Equation: Vout = 1.500 V + [(d – 16) * 8 mV],<br>where d is the decimal value of the register.<br>The Default (00h) points to the OTP programmed default value. If this register is not reprogrammed, a read of the register will return 00h. |

| Hex | VOUT | Hex | VOUT | Hex | VOUT | Hex | VOUT |
|---|---|---|---|---|---|---|---|
| 00 | DEFAULT | 40 | 1.884 V | 80 | 2.396 V | C0 | 2.908 V |
| 01 | Reserved | 41 | 1.892 V | 81 | 2.404 V | C1 | 2.916 V |
| 02 | Reserved | 42 | 1.900 V | 82 | 2.412 V | C2 | 2.924 V |
| 03 | Reserved | 43 | 1.908 V | 83 | 2.420 V | C3 | 2.932 V |
| 04 | Reserved | 44 | 1.916 V | 84 | 2.428 V | C4 | 2.940 V |
| 05 | Reserved | 45 | 1.924 V | 85 | 2.436 V | C5 | 2.948 V |
| 06 | Reserved | 46 | 1.932 V | 86 | 2.444 V | C6 | 2.956 V |
| 07 | Reserved | 47 | 1.940 V | 87 | 2.452 V | C7 | 2.964 V |
| 08 | Reserved | 48 | 1.948 V | 88 | 2.460 V | C8 | 2.972 V |
| 09 | Reserved | 49 | 1.956 V | 89 | 2.468 V | C9 | 2.980 V |
| 0A | Reserved | 4A | 1.964 V | 8A | 2.476 V | CA | 2.988 V |
| 0B | Reserved | 4B | 1.972 V | 8B | 2.484 V | CB | 2.996 V |
| 0C | Reserved | 4C | 1.980 V | 8C | 2.492 V | CC | 3.004 V |
| 0D | Reserved | 4D | 1.988 V | 8D | 2.500 V | CD | 3.012 V |
| 0E | Reserved | 4E | 1.996 V | 8E | 2.508 V | CE | 3.020 V |
| 0F | Reserved | 4F | 2.004 V | 8F | 2.516 V | CF | 3.028 V |
| 10 | 1.500 V | 50 | 2.012 V | 90 | 2.524 V | D0 | 3.036 V |
| 11 | 1.508 V | 51 | 2.020 V | 91 | 2.532 V | D1 | 3.044 V |
| 12 | 1.516 V | 52 | 2.028 V | 92 | 2.540 V | D2 | 3.052 V |
| 13 | 1.524 V | 53 | 2.036 V | 93 | 2.548 V | D3 | 3.060 V |
| 14 | 1.532 V | 54 | 2.044 V | 94 | 2.556 V | D4 | 3.068 V |
| 15 | 1.540 V | 55 | 2.052 V | 95 | 2.564 V | D5 | 3.076 V |
| 16 | 1.548 V | 56 | 2.060 V | 96 | 2.572 V | D6 | 3.084 V |
| 17 | 1.556 V | 57 | 2.068 V | 97 | 2.580 V | D7 | 3.092 V |
| 18 | 1.564 V | 58 | 2.076 V | 98 | 2.588 V | D8 | 3.100 V |
| 19 | 1.572 V | 59 | 2.084 V | 99 | 2.596 V | D9 | 3.108 V |
| 1A | 1.580 V | 5A | 2.092 V | 9A | 2.604 V | DA | 3.116 V |
| 1B | 1.588 V | 5B | 2.100 V | 9B | 2.612 V | DB | 3.124 V |
| 1C | 1.596 V | 5C | 2.108 V | 9C | 2.620 V | DC | 3.132 V |
| 1D | 1.604 V | 5D | 2.116 V | 9D | 2.628 V | DD | 3.140 V |
| 1E | 1.612 V | 5E | 2.124 V | 9E | 2.636 V | DE | 3.148 V |
| 1F | 1.620 V | 5F | 2.132 V | 9F | 2.644 V | DF | 3.156 V |
| 20 | 1.628 V | 60 | 2.140 V | A0 | 2.652 V | E0 | 3.164 V |
| 21 | 1.636 V | 61 | 2.148 V | A1 | 2.660 V | E1 | 3.172 V |
| 22 | 1.644 V | 62 | 2.156 V | A2 | 2.668 V | E2 | 3.180 V |
| 23 | 1.652 V | 63 | 2.164 V | A3 | 2.676 V | E3 | 3.188 V |
| 24 | 1.660 V | 64 | 2.172 V | A4 | 2.684 V | E4 | 3.196 V |
| 25 | 1.668 V | 65 | 2.180 V | A5 | 2.692 V | E5 | 3.204 V |

**Table 10. REGISTER DETAILS – 0X06 CHAN4** (continued)

| 0x06 CHAN4 | | | | Default = 00000000 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Bit** | **Name** | **Default** | **Type** | **Description** | | | | | | | |
| | | | | 26 | 1.676 V | 66 | 2.188 V | A6 | 2.700 V | E6 | 3.212 V |
| | | | | 27 | 1.684 V | 67 | 2.196 V | A7 | 2.708 V | E7 | 3.220 V |
| | | | | 28 | 1.692 V | 68 | 2.204 V | A8 | 2.716 V | E8 | 3.228 V |
| | | | | 29 | 1.700 V | 69 | 2.212 V | A9 | 2.724 V | E9 | 3.236 V |
| | | | | 2A | 1.708 V | 6A | 2.220 V | AA | 2.732 V | EA | 3.244 V |
| | | | | 2B | 1.716 V | 6B | 2.228 V | AB | 2.740 V | EB | 3.252 V |
| | | | | 2C | 1.724 V | 6C | 2.236 V | AC | 2.748 V | EC | 3.260 V |
| | | | | 2D | 1.732 V | 6D | 2.244 V | AD | 2.756 V | ED | 3.268 V |
| | | | | 2E | 1.740 V | 6E | 2.252 V | AE | 2.764 V | EE | 3.276 V |
| | | | | 2F | 1.748 V | 6F | 2.260 V | AF | 2.772 V | EF | 3.284 V |
| | | | | 30 | 1.756 V | 70 | 2.268 V | B0 | 2.780 V | F0 | 3.292 V |
| | | | | 31 | 1.764 V | 71 | 2.276 V | B1 | 2.788 V | F1 | 3.300 V |
| | | | | 32 | 1.772 V | 72 | 2.284 V | B2 | 2.796 V | F2 | 3.308 V |
| | | | | 33 | 1.780 V | 73 | 2.292 V | B3 | 2.804 V | F3 | 3.316 V |
| | | | | 34 | 1.788 V | 74 | 2.300 V | B4 | 2.812 V | F4 | 3.324 V |
| | | | | 35 | 1.796 V | 75 | 2.308 V | B5 | 2.820 V | F5 | 3.332 V |
| | | | | 36 | 1.804 V | 76 | 2.316 V | B6 | 2.828 V | F6 | 3.340 V |
| | | | | 37 | 1.812 V | 77 | 2.324 V | B7 | 2.836 V | F7 | 3.348 V |
| | | | | 38 | 1.820 V | 78 | 2.332 V | B8 | 2.844 V | F8 | 3.356 V |
| | | | | 39 | 1.828 V | 79 | 2.340 V | B9 | 2.852 V | F9 | 3.364 V |
| | | | | 3A | 1.836 V | 7A | 2.348 V | BA | 2.860 V | FA | 3.372 V |
| | | | | 3B | 1.844 V | 7B | 2.356 V | BB | 2.868 V | FB | 3.380 V |
| | | | | 3C | 1.852 V | 7C | 2.364 V | BC | 2.876 V | FC | 3.388 V |
| | | | | 3D | 1.860 V | 7D | 2.372 V | BD | 2.884 V | FD | 3.396 V |
| | | | | 3E | 1.868 V | 7E | 2.380 V | BE | 2.892 V | FE | 3.404 V |
| | | | | 3F | 1.876 V | 7F | 2.388 V | BF | 2.900 V | FF | 3.412 V |

**Table 11. REGISTER DETAILS – 0X07 RESET**

| 0X07 RESET | | | | Default = 00000110 | |
|---|---|---|---|---|---|
| **Bit** | **Name** | **Default** | **Type** | **Description** | |
| 7:4 | SOFT_RESET | 0000 | Write | **Code** | **Software Reset** |
| | | | | 1011 | Writing a “1011” begins a soft reset of the device $I^2C$ registers to their default values. These bits are cleared upon execution of the Reset function. |
| | | | | | Any other value than “1011” will be ignored. |
| 3 | UNUSED | 0 | Read | | |
| 2:1 | OCP_TIMER | 11 | R/W | Option bits to control the length of the deglitch timer for current limit on all LDOs before a fault is triggered. | |
| | | | | **Code** | **Deglitch Timer** |
| | | | | 00 | 125 μs |
| | | | | 01 | 250 μs |
| | | | | 10 | 500 μs |
| | | | | 11 | 1 ms |
| 0 | FLT_SD_B | 0 | R/W | **Code** | **Prevents Shutdown When a Fault Occurs** |
| | | | | 0 | LDO is shutdown if a OCP event occurs or if the LDO’s input VIN1, VIN2, VIN3, or VIN4 have a UVLO event. |
| | | | | 1 | LDO is not shutdown if a OCP event occurs. If the LDO’s input VIN1, VIN2, VIN3, or VIN4 have a UVLO event, the associated LDO will be shutdown until the supply returns, but the fault will not be counted. |
| | | | | Note: If this bit function is desired, FLT_SD_B should be set to “1” prior to enabling any LDOs after a Power−On−Reset. | |

**Table 12. REGISTER DETAILS – 0x08 LDO_COMP0**

| 0x08 LDO_COMP0 | | | | Default = 00000001 | | |
|---|---|---|---|---|---|---|
| **Bit** | **Name** | **Default** | **Type** | **Description** | | |
| 7:6 | LDO4_COMP_SEL | 00 | R/W | The LDO4 Compensation is selected by modifying these bits to account for different COUT values.<br>The Cout_min and Cout_max values are nominal 0DCV bias capacitance values utilized with the following DC de−rating: | | |
| | | | | **Code** | **Cout_min** | **Cout_max** |
| | | | | 00 | 1.0 μF | < 4.7 μF |
| | | | | 01 | 4.7 μF | < 15 μF |
| | | | | 10 | 15 μF | < 47 μF |
| | | | | 11 | NA | NA |
| 5:4 | LDO3_COMP_SEL | 00 | R/W | The LDO3 Compensation is selected by modifying these bits to account for different COUT value.<br>The Cout_min and Cout_max values are nominal 0DCV bias capacitance values utilized with the following DC de−rating: | | |
| | | | | **Code** | **Cout_min** | **Cout_max** |
| | | | | 00 | 1.0 μF | < 4.7 μF |
| | | | | 01 | 4.7 μF | < 15 μF |
| | | | | 10 | 15 μF | < 47 μF |
| | | | | 11 | NA | NA |
| 3:2 | LDO2_COMP_SEL | 00 | R/W | The LDO2 Compensation is selected by modifying these bits to account for different COUT value. | | |
| | | | | **Code** | **Cout_min** | **Cout_max** |
| | | | | 00 | 1.0 μF | < 4.7 μF |
| | | | | 01 | 4.7 μF | < 15 μF |
| | | | | 10 | 15 μF | < 47 μF |
| | | | | 11 | NA | NA |
| 1:0 | LDO1_COMP_SEL | 01 | R/W | The LDO1 Compensation is selected by modifying these bits to account for different COUT value. | | |
| | | | | **Code** | **Cout_min** | **Cout_max** |
| | | | | 00 | – | < 5.5 μF |
| | | | | 01 | 5.5 μF | 17 μF |
| | | | | 10 | 17 μF | 34 μF |
| | | | | 11 | – | > 34 μF |

**Table 13. REGISTER DETAILS – 0X09 INTERRUPT1**

| 0X09 INTERRUPT1 | | | | Default = 00000000 | |
|---|---|---|---|---|---|
| **Bit** | **Name** | **Default** | **Type** | **Description** | |
| 7 | UNUSED | 0 | Read | | |
| 6 | UNUSED | 0 | Read | | |
| 5 | UNUSED | 0 | Read | | |
| 4 | UNUSED | 0 | Read | | |
| 3 | LDO4_OCP_INT | 0 | R/CLR | **Code** | **LDO4 OCP Interrupt** |
| | | | | 0 | Clear |
| | | | | 1 | Over−Current event detected on LDO4 output or that a successful restart has occurred after an OCP event. |
| 2 | LDO3_OCP_INT | 0 | R/CLR | **Code** | **LDO3 OCP Interrupt** |
| | | | | 0 | Clear |
| | | | | 1 | Over−Current event detected on LDO3 output or that a successful restart has occurred after an OCP event. |
| 1 | LDO2_OCP_INT | 0 | R/CLR | **Code** | **LDO2 OCP Interrupt** |
| | | | | 0 | Clear |
| | | | | 1 | Over−Current event detected on LDO2 output or that a successful restart has occurred after an OCP event. |
| 0 | LDO1_OCP_INT | 0 | R/CLR | **Code** | **LDO1 OCP Interrupt** |
| | | | | 0 | Clear |
| | | | | 1 | Over−Current event detected on LDO1 output or that a successful restart has occurred after an OCP event. |

**Table 14. REGISTER DETAILS – 0X0A INTERRUPT2**

| 0X0A INTERRUPT2 | | | | Default = 00000000 | |
|---|---|---|---|---|---|
| **Bit** | **Name** | **Default** | **Type** | **Description** | |
| 7 | UNUSED | 0 | Read | | |
| 6 | TSD_INT | 0 | R/CLR | **Code** | **Thermal Shutdown Interrupt** |
| | | | | 0 | Clear |
| | | | | 1 | A Thermal Shutdown event detected or that the temperature has fallen below the hysteresis level. |
| 5 | TSD_WRN_INT | 0 | R/CLR | **Code** | **Thermal Warning Interrupt** |
| | | | | 0 | Clear |
| | | | | 1 | Thermal Shutdown Warning threshold was surpassed or that the temperature has fallen below the hysteresis level. |
| 4 | VSYS_UVLO_INT | 0 | R/CLR | **Code** | **VSYS Under−Voltage−Lock−Out Interrupt** |
| | | | | 0 | Normal operation |
| | | | | 1 | Indicates that the VSYS power fell below the UVLO input threshold or that the supplies have risen above the rising thresholds after a UVLO fault. |
| | | | | Reading the the associated status bit provides present state of the input voltage. | |

**Table 14. REGISTER DETAILS – 0X0A INTERRUPT2** (continued)

| 0X0A INTERRUPT2 | | | | Default = 00000000 | |
|---|---|---|---|---|---|
| **Bit** | **Name** | **Default** | **Type** | **Description** | |
| 3 | CHAN4_UVLO_INT | 0 | R/CLR | **Code** | **VIN4 Under−Voltage−Lock−Out Interrupt** |
| | | | | 0 | Normal Operation |
| | | | | 1 | Indicates VIN4 fell below the UVLO threshold while CHAN4 was enabled or that the supply has risen above the rising thresholds after a UVLO fault. |
| | | | | | Reading the associated status bit provides present state of the input voltage. |
| 2 | CHAN3_UVLO_INT | 0 | R/CLR | **Code** | **VIN3 Under−Voltage−Lock−Out Interrupt** |
| | | | | 0 | Normal Operation |
| | | | | 1 | Indicates VIN3 fell below the UVLO threshold while CHAN3 was enabled or that the supply has risen above the rising thresholds after a UVLO fault. |
| | | | | | Reading the associated status bit provides present state of the input voltage. |
| 1 | CHAN2_UVLO_INT | 0 | R/CLR | **Code** | **VIN2 Under−Voltage−Lock−Out Interrupt** |
| | | | | 0 | Normal Operation |
| | | | | 1 | Indicates that the VIN2 fell below the UVLO threshold while CHAN2 was enabled or that the supply has risen above the rising thresholds after a UVLO fault. |
| | | | | | Reading the associated status bit provides present state of the input voltage. |
| 0 | CHAN1_UVLO_INT | 0 | R/CLR | **Code** | **VIN1 Under−Voltage−Lock−Out Interrupt** |
| | | | | 0 | Normal operation |
| | | | | 1 | Indicates VIN1 fell below the UVLO threshold while CHAN1 is enabled or that the supply has risen above the rising thresholds after a UVLO fault. |
| | | | | | Reading the associated status bit provides present state of the input voltage. |

**Table 15. REGISTER DETAILS – 0X0B STATUS1**

| 0X0B STATUS1 | | | | Default = 00000000 | |
|---|---|---|---|---|---|
| **Bit** | **Name** | **Default** | **Type** | **Description** | |
| 7 | UNUSED | 0 | Read | | |
| 6 | UNUSED | 0 | Read | | |
| 5 | UNUSED | 0 | Read | | |
| 4 | UNUSED | 0 | Read | | |
| 3 | LDO4_OCP_STAT | 0 | Read | **Code** | **LDO4 OCP Status** |
| | | | | 0 | Clear |
| | | | | 1 | An Over−Current condition exists on LDO4 output |
| 2 | LDO3_OCP_STAT | 0 | Read | **Code** | **LDO3 OCP Status** |
| | | | | 0 | Clear |
| | | | | 1 | An Over−Current condition exists on LDO3 output |
| 1 | LDO2_OCP_STAT | 0 | Read | **Code** | **LDO2 OCP Status** |
| | | | | 0 | Clear |
| | | | | 1 | An Over−Current condition exists on LDO2 output |
| 0 | LDO1_OCP_STAT | 0 | Read | **Code** | **LDO1 OCP Status** |
| | | | | 0 | Clear |
| | | | | 1 | An Over−Current condition exists on LDO1 output |

**Table 16. REGISTER DETAILS – 0X0C STATUS2**

| 0X0C STATUS2 | | | | Default = 00000000 | |
|---|---|---|---|---|---|
| **Bit** | **Name** | **Default** | **Type** | **Description** | |
| 7 | UNUSED | 0 | Read | | |
| 6 | TSD_STAT | 0 | Read | **Code** | **Temperature Shutdown Status** |
| | | | | 0 | Normal Operation |
| | | | | 1 | Device is in Thermal Shutdown |
| 5 | TSD_WRN_STAT | 0 | Read | **Code** | **Temperature Warning Status** |
| | | | | 0 | Normal Operation |
| | | | | 1 | The temperature is above the thermal warning level and shutdown is impending. |
| 4 | VSYS_UVLO_STAT | 0 | Read | **Code** | **VSYS Under−Voltage−Lock−Out Status** |
| | | | | 0 | Normal Operation |
| | | | | 1 | VSYS is below the UVLO threshold. |
| 3 | CHAN4_UVLO_STAT | 0 | Read | **Code** | **VIN4 Under−Voltage−Lock−Out Status** |
| | | | | 0 | Normal Operation |
| | | | | 1 | Indicates VIN4 is below the UVLO threshold while LDO4 is enabled. |
| 2 | CHAN3_UVLO_STAT | 0 | Read | **Code** | **VIN3 Under−Voltage−Lock−Out Status** |
| | | | | 0 | Normal Operation |
| | | | | 1 | Indicates VIN3 is below the UVLO threshold while LDO3 is enabled. |

**Table 16. REGISTER DETAILS – 0X0C STATUS2** (continued)

| 0X0C STATUS2 | | | | Default = 00000000 | |
|---|---|---|---|---|---|
| **Bit** | **Name** | **Default** | **Type** | **Description** | |
| 1 | CHAN2_UVLO_STAT | 0 | Read | **Code** | **VIN2 Under−Voltage−Lock−Out Status** |
| | | | | 0 | Normal Operation |
| | | | | 1 | Indicates VIN2 power rail is below the UVLO threshold while LDO2 is enabled. |
| 0 | CHAN1_UVLO_STAT | 0 | Read | **Code** | **VIN1 Under−Voltage−Lock−Out Status** |
| | | | | 0 | Normal Operation |
| | | | | 1 | Indicates VIN1 is below the UVLO threshold while LDO1 is enabled. |

**Table 17. REGISTER DETAILS – 0X0D STATUS3**

| 0X0D STATUS3 | | | | Default = 00000000 | |
|---|---|---|---|---|---|
| **Bit** | **Name** | **Default** | **Type** | **Description** | |
| 7 | UNUSED | 0 | Read | | |
| 6 | UNUSED | 0 | Read | | |
| 5 | UNUSED | 0 | Read | | |
| 4 | CHIP_SUSD | 0 | Read | **Code** | **Chip Suspension** |
| | | | | 0 | Chip normal state |
| | | | | 1 | The entire chip has been suspended due to a global fault condition. |
| 3 | CHAN4_SUSD | 0 | Read | **Code** | **CHAN4 Output Suspended** |
| | | | | 0 | CHAN4 in normal state. |
| | | | | 1 | CHAN4 has been suspended due to a fault condition. |
| 2 | CHAN3_SUSD | 0 | Read | **Code** | **CHAN3 Output Suspended** |
| | | | | 0 | CHAN3 in a normal state |
| | | | | 1 | CHAN3 has been suspended due to a fault condition. |
| 1 | CHAN2_SUSD | 0 | Read | **Code** | **CHAN2 Output Suspended** |
| | | | | 0 | CHAN2 in normal state |
| | | | | 1 | CHAN2 has been suspended due to a fault condition. |
| 0 | CHAN1_SUSD | 0 | Read | **Code** | **CHAN1 Output Suspended** |
| | | | | 0 | CHAN1 is in normal state |
| | | | | 1 | CHAN1 has been suspended due to a fault condition. |

**Table 18. REGISTER DETAILS – 0X0E MINT1**

| 0X0E MINT1 | | | | Default = 00000000 | |
|---|---|---|---|---|---|
| **Bit** | **Name** | **Default** | **Type** | **Description** | |
| 7 | UNUSED | 0 | Read | | |
| 6 | UNUSED | 0 | Read | | |
| 5 | UNUSED | 0 | Read | | |
| 4 | UNUSED | 0 | Read | | |
| 3 | MASK_LDO4_OCP | 0 | R/W | **Code** | **LDO4 OCP MASK** |
| | | | | 0 | No masking of interrupt. |
| | | | | 1 | INT(B) pin will not change states when LDO4 Over−Current interrupt occurs. |
| 2 | MASK_LDO3_OCP | 0 | R/W | **Code** | **LDO3 OCP MASK** |
| | | | | 0 | No masking of interrupt. |
| | | | | 1 | INT(B) pin will not change states when LDO3 Over−Current interrupt occurs. |
| 1 | MASK_LDO2_OCP | 0 | R/W | **Code** | **LDO2 OCP MASK** |
| | | | | 0 | No masking of interrupt. |
| | | | | 1 | INT(B) pin will not change states when LDO2 Over−Current interrupt occurs. |
| 0 | MASK_LDO1_OCP | 0 | R/W | **Code** | **LDO1 OCP MASK** |
| | | | | 0 | No masking of interrupt. |
| | | | | 1 | INT(B) pin will not change states when LDO1 Over−Current interrupt occurs. |

**Table 19. REGISTER DETAILS – 0X0F MINT2**

| 0X0F MINT2 | | | | Default = 00000000 | |
|---|---|---|---|---|---|
| **Bit** | **Name** | **Default** | **Type** | **Description** | |
| 7 | UNUSED | 0 | Read | | |
| 6 | MASK_TSD | 0 | R/W | **Code** | **Thermal Shutdown MASK** |
| | | | | 0 | No masking of interrupt. |
| | | | | 1 | INT(B) pin will not change states when a Thermal Shutdown interrupt occurs. |
| 5 | MASK_TSD_WRN | 0 | R/W | **Code** | **Thermal Warning MASK** |
| | | | | 0 | No masking of interrupt. |
| | | | | 1 | INT(B) pin will not change states when LDO7 Over−Current interrupt occurs. |
| 4 | MASK_VSYS_UVLO | 0 | R/W | **Code** | **VSYS UVLO MASK** |
| | | | | 0 | No masking of interrupt. |
| | | | | 1 | INT(B) pin will not change states when VSYS Input Power Under Voltage interrupt occurs. |
| 3 | MASK_CHAN4_UVLO | 0 | R/W | **Code** | **VIN4 UVLO MASK** |
| | | | | 0 | No masking of interrupt. |
| | | | | 1 | INT(B) pin will not change states when VIN4 Input Power Under Voltage interrupt occurs |

**Table 19. REGISTER DETAILS – 0X0F MINT2** (continued)

| 0X0F MINT2 | | | | Default = 00000000 | |
|---|---|---|---|---|---|
| **Bit** | **Name** | **Default** | **Type** | **Description** | |
| 2 | MASK_CHAN3_UVLO | 0 | R/W | **Code** | **VIN3 UVLO MASK** |
| | | | | 0 | No masking of interrupt. |
| | | | | 1 | INT(B) pin will not change states when VIN3 Input Power Under Voltage interrupt occurs. |
| 1 | MASK_CHAN2_UVLO | 0 | R/W | **Code** | **VIN2 UVLO MASK** |
| | | | | 0 | No masking of interrupt. |
| | | | | 1 | INT(B) pin will not change states when VIN2 Input Power Under Voltage interrupt occurs. |
| 0 | MASK_CHAN1_UVLO | 0 | R/W | **Code** | **VIN1 UVLO MASK** |
| | | | | 0 | No masking of interrupt. |
| | | | | 1 | INT(B) pin will not change states when VIN1 Input Power Under Voltage interrupt occurs. |

**Table 20. REGISTER DETAILS – 0X10 LDO_LS_SELECT**

| 0X10 LDO_LS_SELECT | | | | Default = 00000000 | |
|---|---|---|---|---|---|
| **Bit** | **Name** | **Default** | **Type** | **Description** | |
| 7 | UNUSED | 0 | Read | | |
| 6 | UNUSED | 0 | Read | | |
| 5 | UNUSED | 0 | Read | | |
| 4 | UNUSED | 0 | Read | | |
| 3 | LDO_LS4_SELECT | 0 | R/W | Configuration of Output 4 | |
| | | | | **Code** | **Configuration** |
| | | | | 0 | Configured to operate as an LDO |
| | | | | 1 | Configured to operate as a Load Switch |
| 2 | LDO_LS3_SELECT | 0 | R/W | Configuration of Output 3 | |
| | | | | **Code** | **Configuration** |
| | | | | 0 | Configured to operate as an LDO |
| | | | | 1 | Configured to operate as a Load Switch |
| 1 | LDO_LS2_SELECT | 0 | R/W | Configuration of Output 2 | |
| | | | | **Code** | **Configuration** |
| | | | | 0 | Configured to operate as an LDO |
| | | | | 1 | Configured to operate as a Load Switch |
| 0 | LDO_LS1_SELECT | 0 | R/W | Configuration of Output 1 | |
| | | | | **Code** | **Configuration** |
| | | | | 0 | Configured to operate as an LDO |
| | | | | 1 | Configured to operate as a Load Switch |

## APPLICATION GUIDELINES

### LDO Input Capacitor Considerations

If long wires are used to bring power to an evaluation board, additional “bulk” capacitance should be placed on the evaluation board between the local input capacitor(s) and the power source lead(s) to reduce ringing caused by inductance lead length. Use only X5R and X7R ceramic capacitors with adequate voltage rating for local input capacitors.

The effective capacitance value decreases as the voltage across the capacitor increases due to DC bias effects. Adding additional capacitance to the minimum recommended ensures reliable operation.

### LDO Output Capacitor Considerations

FAN53840 LDOs are initially set at the factory for a range of 4.7 µF to 10 µF (unbiased) on LDO1. LDO2/3/4 are initially set for a range of 1 µF to 4.7 µF (unbiased). All LDOs can be trimmed at the factory for up to 47 µF total (unbiased) capacitance. When evaluating and ordering the FAN53840, to ensure optimum performance and stability, specify the amount of capacitance each LDO output will have with an **onsemi** representative.

Use only X5R and X7R ceramic capacitors with adequate voltage rating for the output capacitors.

### PCB Layout Recommendations

Local input and output capacitors should be placed close to the corresponding input and output pins. The ground terminal of the capacitors should be connected to a good ground plane – preferably on the surface of the board. Input power should be routed to the input capacitor first, then to the input pin(s) of the IC. Power from layers other than the layer on which a capacitor sits, should be routed to the capacitor layer with vias close to the positive terminal of the capacitor. Power traces from outputs should be routed to the output capacitor first, then to other layers if necessary.

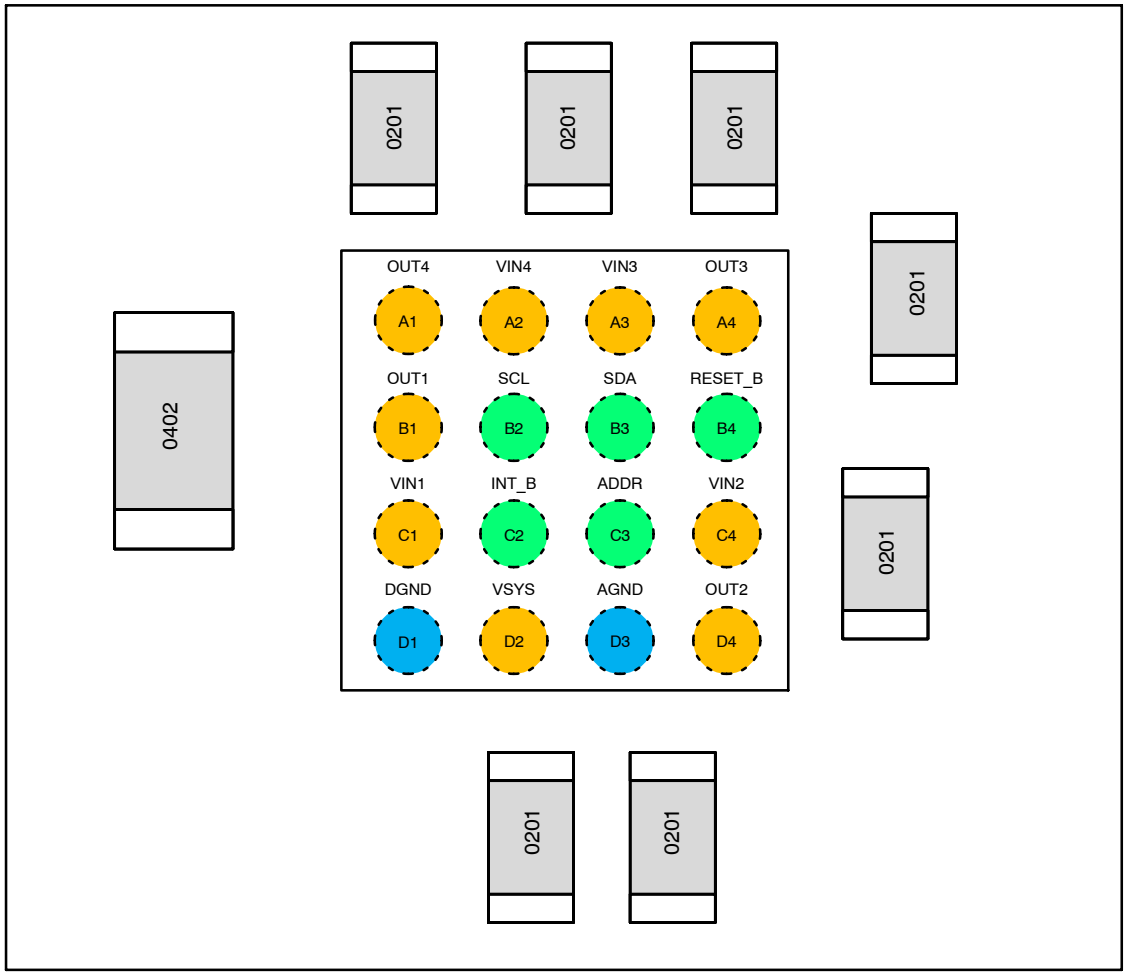



**Figure 31. Recommended PCB Assembly (Top View)**

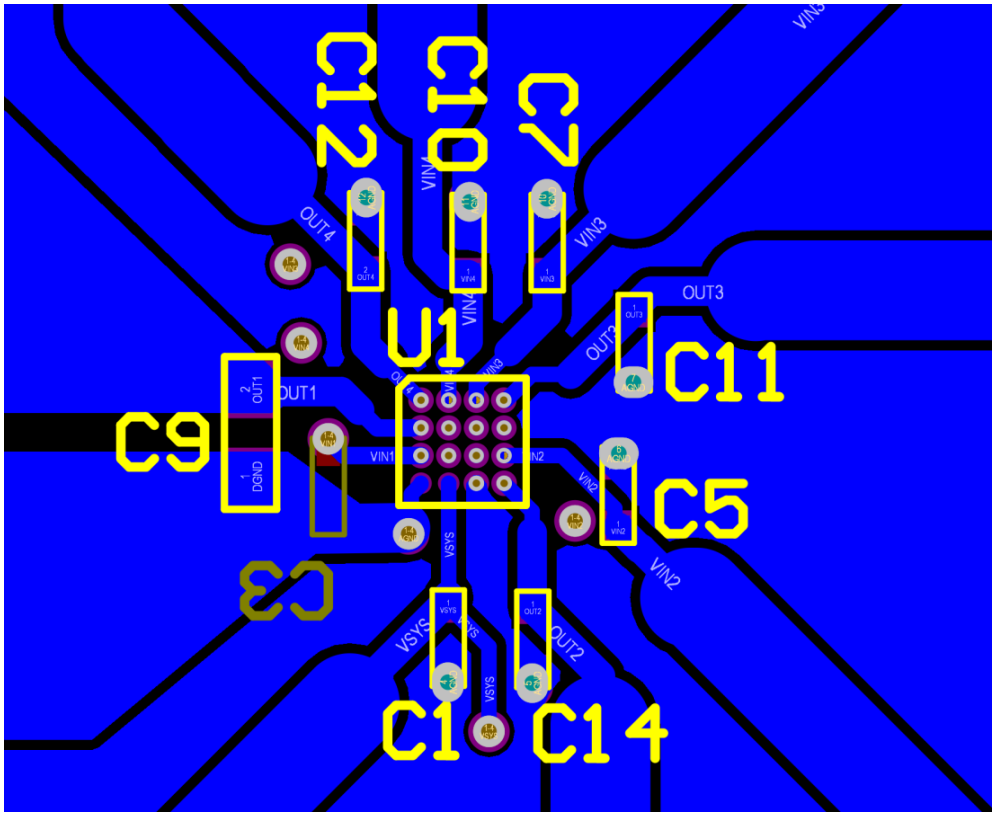
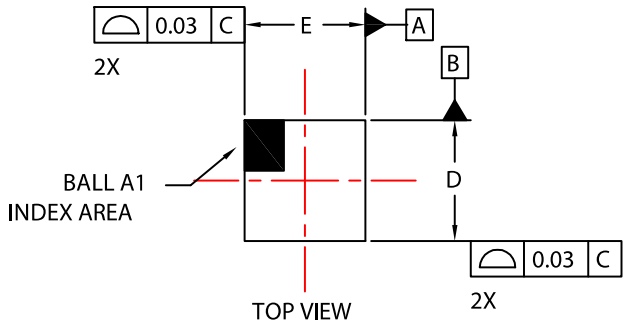
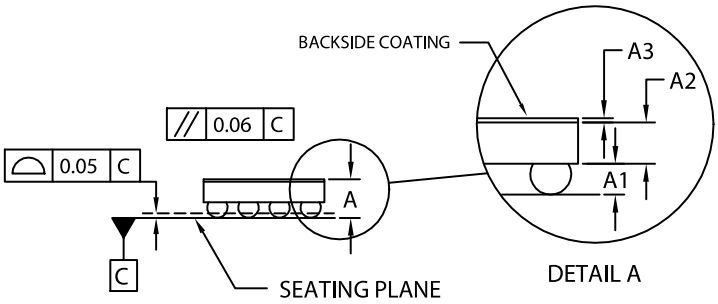


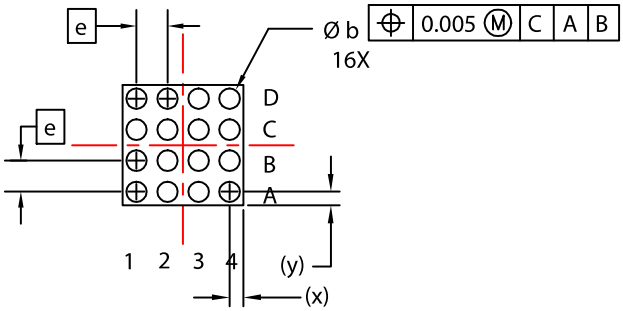

Figure 32. Recommended PCB Layout

**WLCSP16 1.52x1.52x0.432**
CASE 567ZM
ISSUE O

DATE 14 SEP 2020



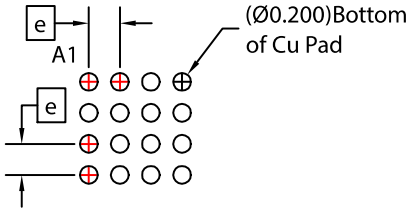




NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS

| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 0.391 | 0.432 | 0.473 |
| A1 | 0.154 | 0.174 | 0.194 |
| A2 | 0.215 | 0.233 | 0.251 |
| A3 | 0.022 | 0.025 | 0.028 |
| b | 0.211 | 0.231 | 0.251 |
| D | 1.49 | 1.52 | 1.55 |
| E | 1.49 | 1.52 | 1.55 |
| e | 0.35 BSC | | |
| x | 0.220 | 0.235 | 0.250 |
| y | 0.220 | 0.235 | 0.250 |




RECOMMENDED
MOUNTING FOOTPRINT*
(NSMD PAD TYPE)

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| DESCRIPTION: | WLCSP16 1.52x1.52x0.432 | PAGE 1 OF 1 |

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