NB639

High Efficiency, Fast Transient, 8A, 28V Synchronous Step-down Converter In a Tiny QFN20 (3x4mm) Package

The Future of Analog IC Technology®

END OF LIFE, REFER TO NB700 OR NB693A

DESCRIPTION

The NB639 is a fully integrated, high frequency synchronous rectified step-down switch mode converter. It offers a very compact solution to achieve 8A continuous output current over a wide input supply range with excellent load and line regulation. The NB639 operates at high efficiency over a wide output current load range.

To further optimize efficiency at light load, this device's V_{CC} supply is designed to be biased externally.

Constant-On-Time (COT) control mode provides fast transient response and eases loop stabilization.

Full protection features include SCP, OCP, OVP, UVP and thermal shutdown.

The NB639 requires a minimum number of readily available standard external components and is available in a space-saving QFN20 (3x4mm) package.

FEATURES

- Wide 4.5V to 28V Operating Input Range
- 8A Output Current
- Internal 30mΩ High-Side, 12mΩ Low-Side Power MOSFETs
- Proprietary Switching Loss Reduction Technique
- 1% Reference Voltage
- Programmable Soft Start Time
- Soft Shutdown
- Programmable Switching Frequency
- SCP, OCP, OVP, UVP Protection and Thermal Shutdown
- Output Adjustable from 0.8V to 13V
- Available in a QFN20 (3x4mm) Package

APPLICATIONS

- Notebook Systems and I/O Power
- Networking Systems
- Optical Communication Systems
- Distributed Power POL Systems

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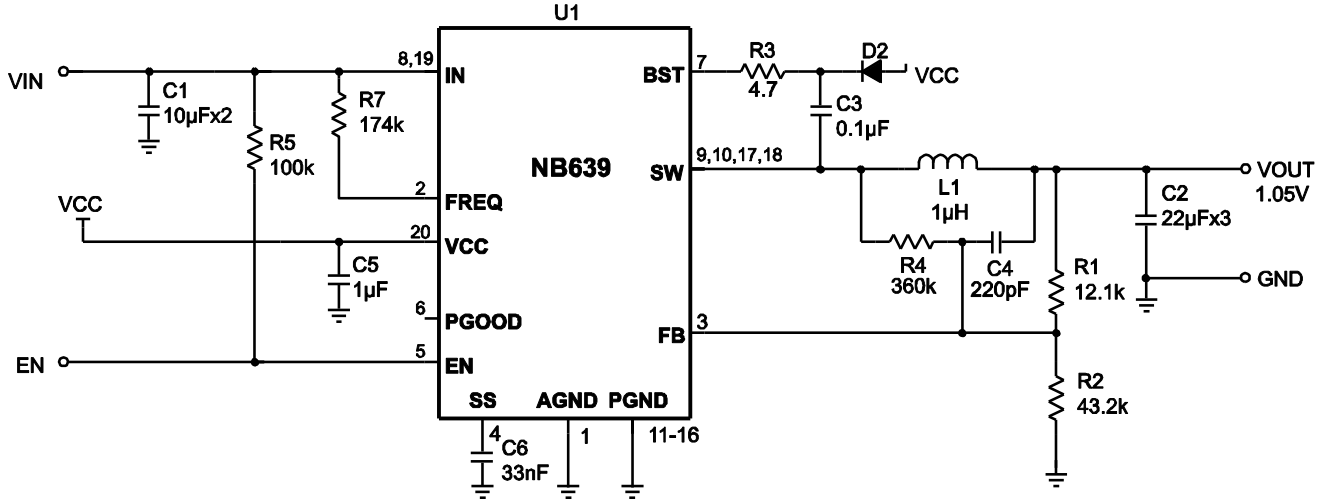
TYPICAL APPLICATION



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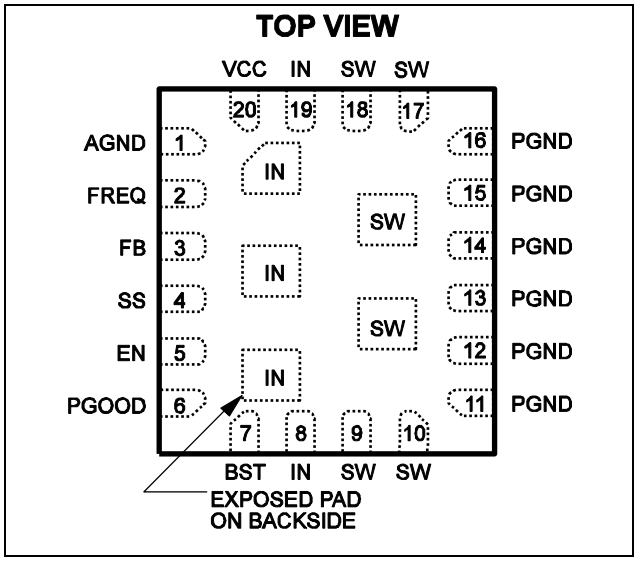
ORDERING INFORMATION

Part Number*	Package	Top Marking
NB639DL	QFN20 (3x4mm)	639

***** For Tape & Reel, add suffix –Z (e.g. NB639DL–Z)
For RoHS compliant packaging, add suffix –LF (e.g. NB639DL–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} 30V
Supply Voltage V_{CC} 6V
V_{SW} ..... -0.3V to V_{IN} + 0.3V
V_{BST} ..... V_{SW} + 6V
$I_{VIN\ (RMS)}$ 3.5A
V_{PGOOD} ..... -0.3V to V_{CC} +0.6V
All Other Pins ..... -0.3V to +6V
Continuous Power Dissipation (T_A = +25°C) (2)
..... 2.6W
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} ..... 4.5V to 28V
Supply Voltage V_{CC} 5V
Output Voltage V_{OUT} ..... 0.8V to 13V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN20 (3x4mm) ..... 48 ..... 10 ... °C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX)=(T_J(MAX)-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{CC}=5V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input Supply Current (Shutdown)	I_{IN}	V_{EN} = 0V		0		μA
Input Supply Current (Quiescent)	I_{IN}	V_{EN} = 2V, V_{FB} = 1V		40		μA
V_{CC} Supply Current (Quiescent)	Ivcc	V_{EN} = 2V, V_{FB} = 1V		350		μA
HS Switch On Resistance (5)	HS_{RDS-ON}			30		mΩ
LS Switch On Resistance (5)	LS_{RDS-ON}			12		mΩ
Switch Leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 0V or 12V		0	10	μA
Current Limit	I_{LIMIT}			16.5		A
One-Shot On Time	T_{ON}	R_{FREQ}=348kΩ, V_{OUT}=1.05V		360		ns
Minimum Off Time(5)	T_{OFF}			100		ns
Fold-back Off Time(5)	T_{FB}	I_{LIM}=1 (HIGH)		7.5		μs
OCP hold-off time(5)	T_{OC}	I_{LIM}=1 (HIGH)			40	μs
Feedback Voltage	V_{FB}		807	815	823	mV
Feedback Current	I_{FB}	V_{FB} = 815mV		10	50	nA
Soft Start Charging Current	$+I_{SS}$	V_{SS}=0V		8.5		μA
Soft Stop Discharging Current	$-I_{SS}$	V_{SS}=0.815V		8.5		μA
Power Good Rising Threshold	$PGOOD_{Vth-Hi}$			0.9		V_{FB}
Power Good Falling Threshold	$PGOOD_{Vth-Lo}$			0.85		V_{FB}
Power Good Rising Delay	T_{PGOOD}	Tss = 1ms			1	ms
Power Good Rising Delay	T_{PGOOD}	Tss = 2ms			1.5	ms
Power Good Rising Delay	T_{PGOOD}	Tss = 3ms			2	ms
EN Rising Threshold	EN_{Vth-Hi}		1.05	1.35	1.60	V
EN Threshold Hysteresis	$EN_{Vth-Hys}$		250	420	550	mV
EN Input Current	I_{EN}	V_{EN} = 2V		2		μA
V_{CC} Under-Voltage Lockout Threshold Rising	$V_{CC}UV_{Vth}$		3.8	4.0	4.2	V
V_{CC} Under-Voltage Lockout Threshold Hysteresis	$V_{CC}UV_{HYS}$			880		mV
V_{OUT} Over-Voltage Protection Threshold	V_{OVP}			1.25		V_{FB}
V_{OUT} Under-Voltage Detection Threshold	V_{UVP}			0.7		V_{FB}
Thermal Shutdown	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{SD-HYS}			25		°C

Notes:
5) Guaranteed by design.

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PIN FUNCTIONS

Pin #	Name	Description
1	AGND	Analog Ground.
2	FREQ	Frequency Set during CCM operation. The ON period is determined by the input voltage and the frequency-set resistor connected to FREQ pin. Connect a resistor to IN for line feed-forward. Decouple with a 1nF capacitor.
3	FB	Feedback. An external resistor divider from the output to GND, tapped to the FB pin, sets the output voltage.
4	SS	Soft Start. Connect an external SS capacitor to program the soft start time for the switch mode regulator. When the EN pin becomes high, an internal current source (8.5uA) charges up the SS capacitor and the SS voltage slowly ramps up from 0 to V_{FB} smoothly. When the EN pin becomes low, an internal current source (8.5μA) discharges the SS capacitor and the SS voltage slowly ramps down.
5	EN	EN=1 to enable the NB639. For automatic start-up, connect EN pin to IN with a 100kΩ resistor. It includes an internal 1MΩ pull-down resistor.
6	PGOOD	Power Good Output. The output of this pin is an open drain and is high if the output voltage is higher than 90% of the nominal voltage. There is delay from FB ≥ 90% to PGOOD high, which is 50% of SS time plus 0.5ms.
7	BST	Bootstrap. A capacitor connected between SW and BS pins is required to form a floating supply across the high-side switch driver.
8, 19	IN	Supply Voltage. The NB639 operates from a +4.5V to +28V input rail. C1 is needed to decouple the input rail. Use wide PCB traces and multiple vias to make the connection.
9, 10, 17, 18	SW	Switch Output. Use wide PCB traces and multiple vias to make the connection.
11-16	PGND	System Ground. This pin is the reference ground of the regulated output voltage. For this reason care must be taken in PCB layout.
20	VCC	External 5V Supply. This 5V supply has to be applied in order to bias the device. Decouple with a 1μF capacitor as close to this pin as possible.

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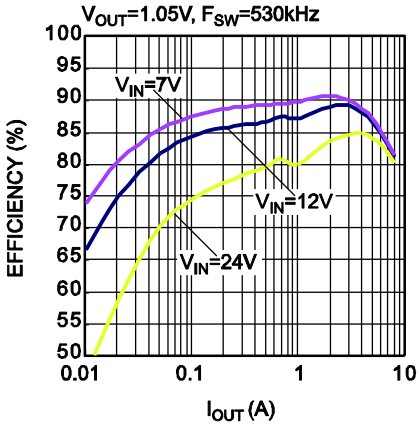
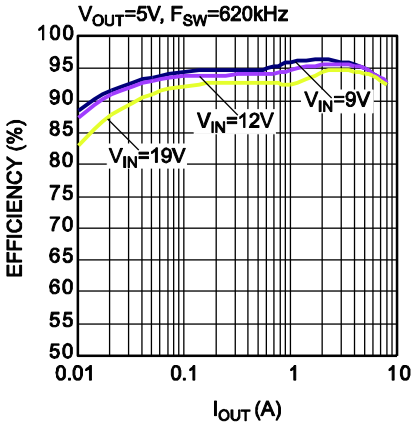
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=12V, V_{OUT} =1.05V, L=1.0μH, T_A=+25°C, unless otherwise noted.

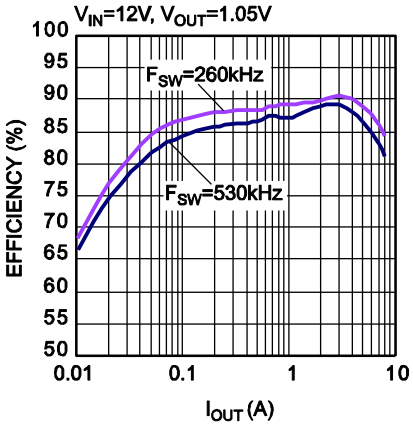
Efficiency



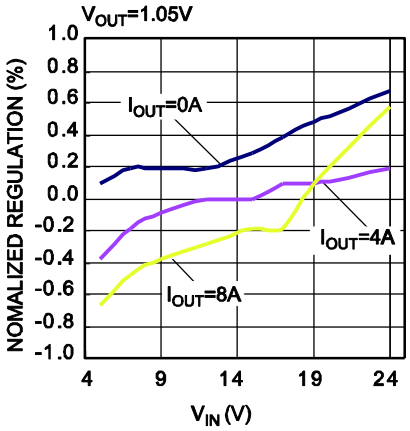
Efficiency



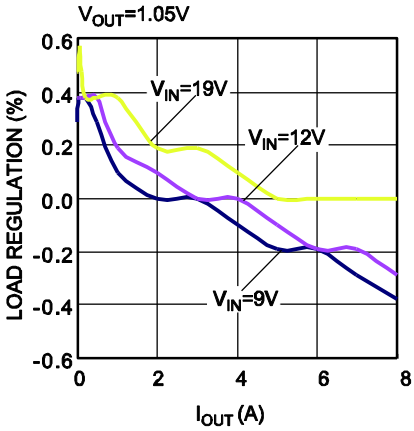
Efficiency



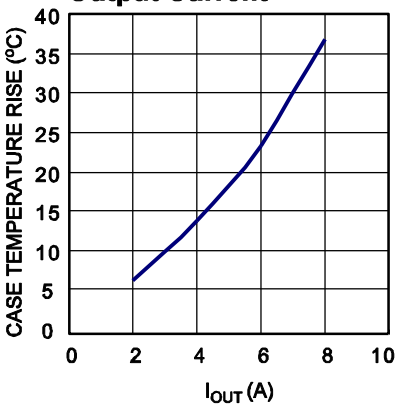
Line Regulation



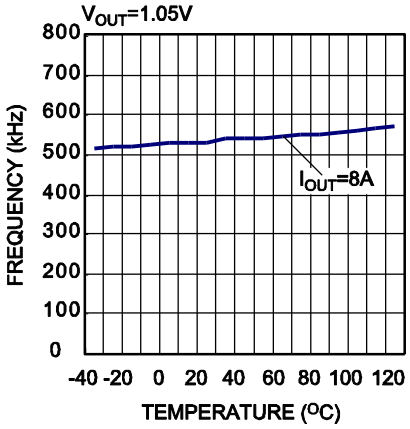
Load Regulation



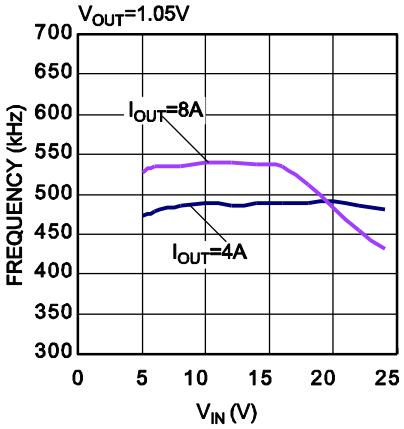
Case Temperature Rise vs. Output Current



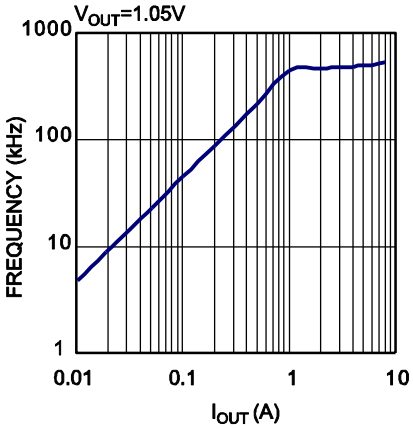
Frequency vs. Temperature



Frequency vs.V_{IN}



Frequency vs. Load Current



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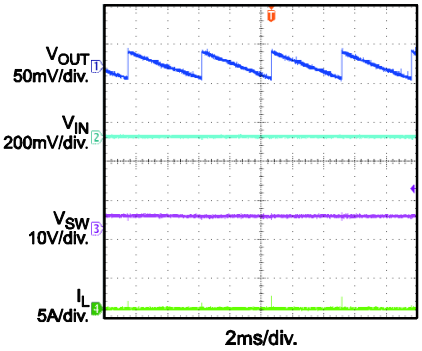
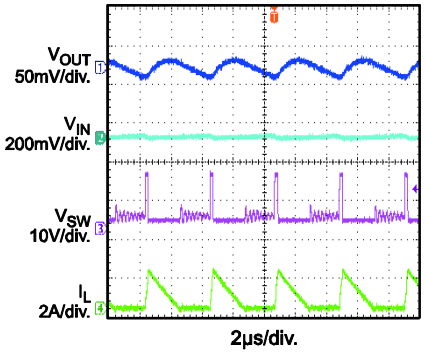
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=12V, V_{OUT} =1.05V, L=1.0µH, T_A=+25°C, unless otherwise noted.

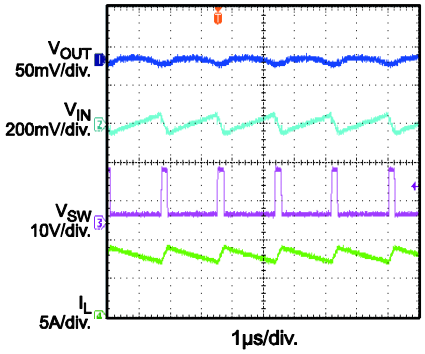
Input & Output Voltage Ripple
I_{OUT} = 4mA



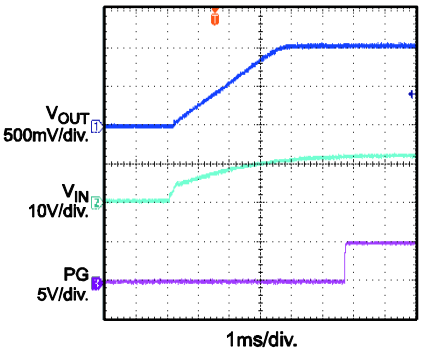
Input & Output Voltage Ripple
I_{OUT} = 0.5A



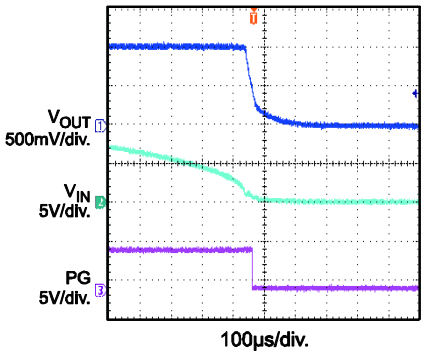
Input & Output Voltage Ripple
I_{OUT} = 8A



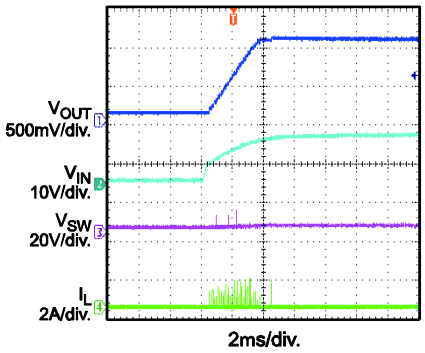
Power Good Through V_{IN} Start-Up
I_{OUT} = 8A



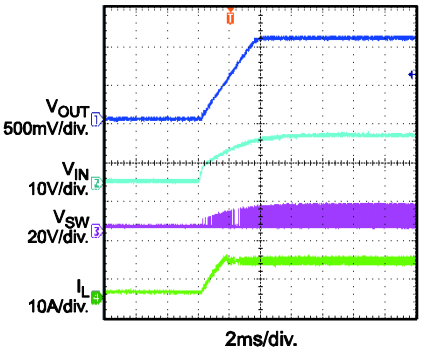
Power Good Through V_{IN} Shutdown
I_{OUT} = 8A



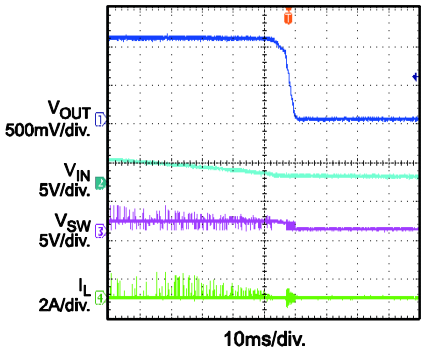
Start-Up Through V_{IN}
I_{OUT} = 0A



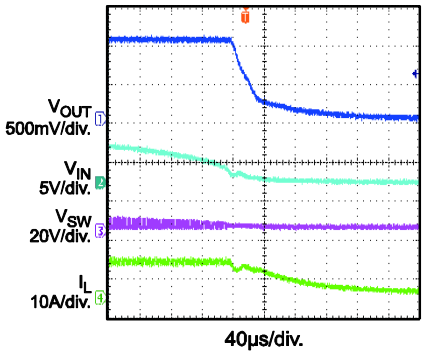
Start-Up Through V_{IN}
I_{OUT} = 8A



Shutdown Through V_{IN}
I_{OUT} = 0A



Shutdown Through V_{IN}
I_{OUT} = 8A



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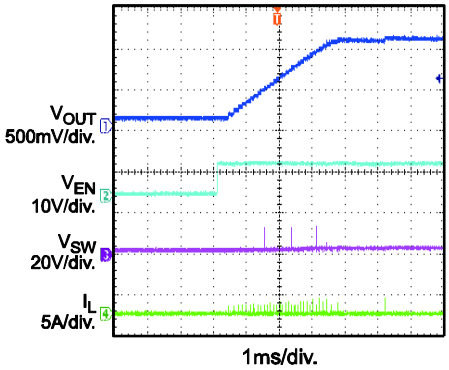
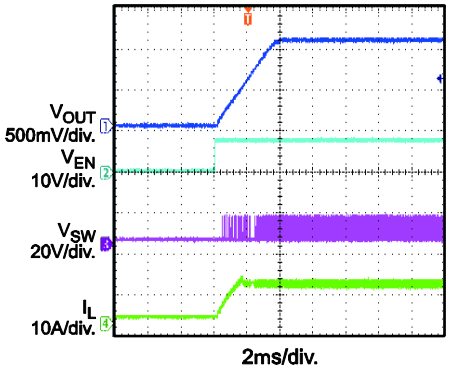
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=12V, V_{OUT} =1.05V, L=1.0µH, T_A=+25°C, unless otherwise noted.

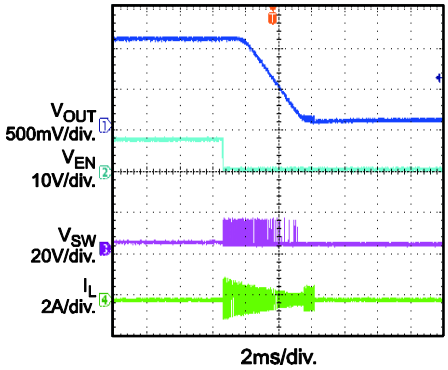
Start-Up Through EN
I_{OUT} = 0A



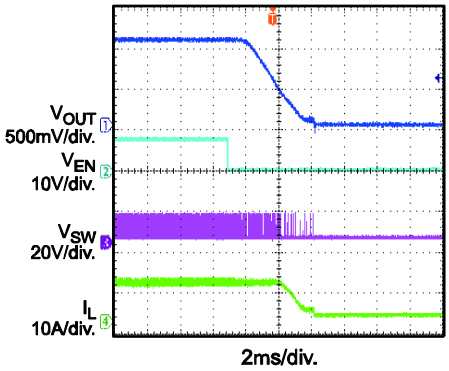
Start-Up Through EN
I_{OUT} = 8A



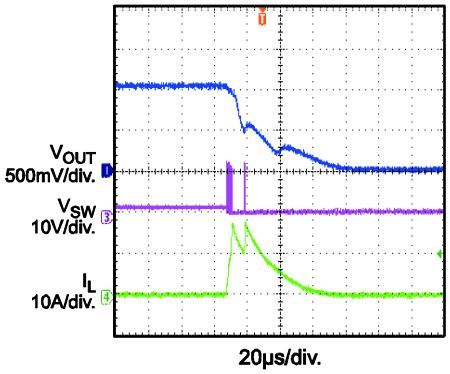
Shutdown Strough EN
I_{OUT} = 0A



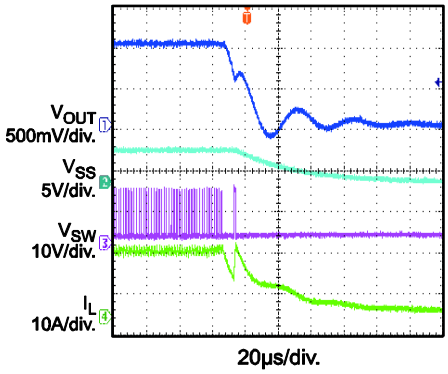
Shutdown Strough EN
I_{OUT} = 8A



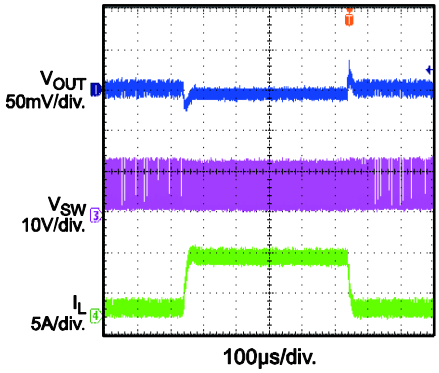
Short Circuit Protection



OCP Protection



Transient
I_{OUT} =0.8A-7.2A@2.5A/µs,
F_{SW} = 530kHz, C_{OUT} =3x22µF



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BLOCK DIAGRAM

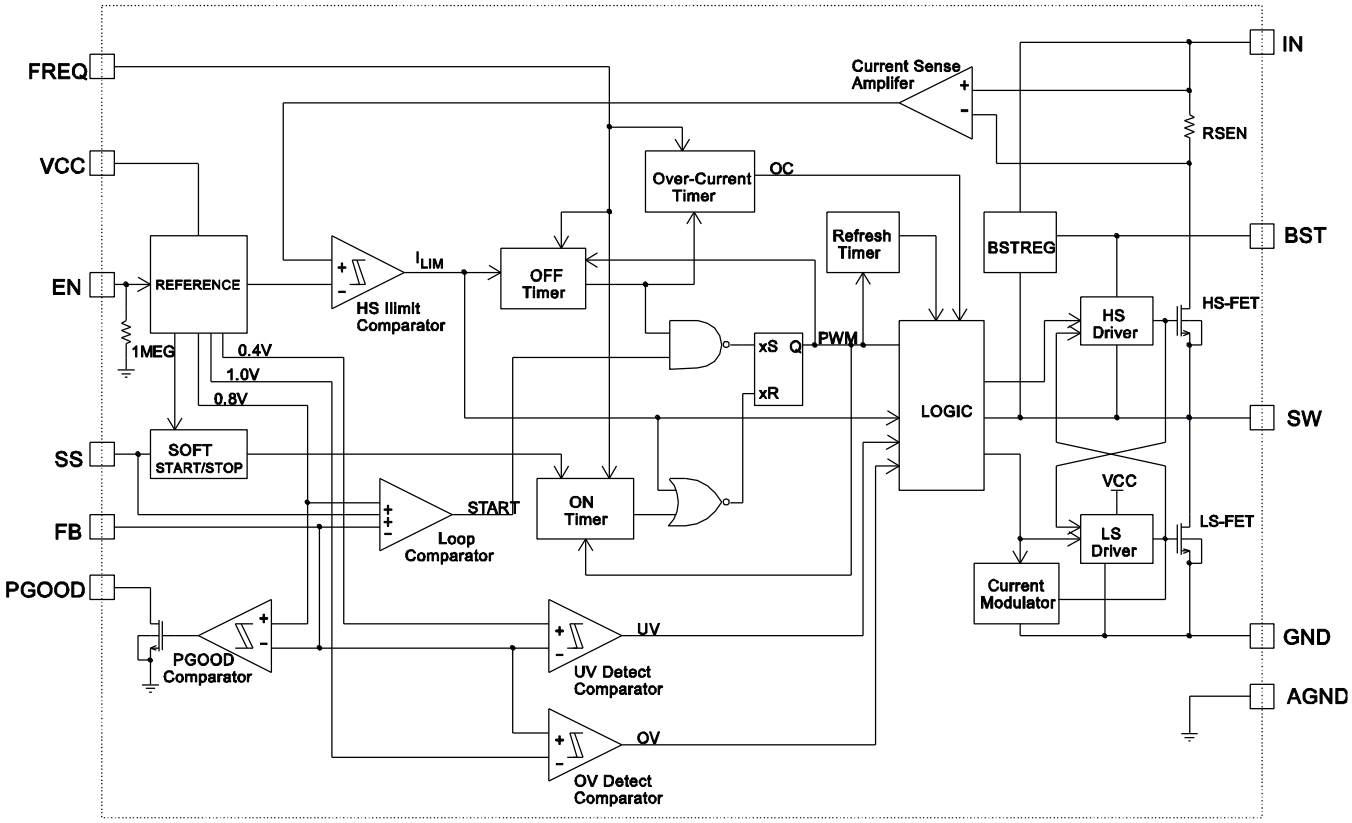

Figure 1—Functional Block Diagram

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OPERATION

PWM Operation

The NB639 is a fully integrated synchronous rectified step-down switch mode converter. Constant-on-time (COT) control is employed to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned on when the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}) which indicates insufficient output voltage. The ON period is determined by the input voltage and the frequency-set resistor as follows:

$$T_{ON}(ns) = \frac{12 \times R_{FREQ}(k\Omega)}{V_{IN}(V) - 0.4} \quad (1)$$

After the ON period elapses, the HS-FET is turned off, or becomes OFF state. It is turned ON again when V_{FB} drops below V_{REF}. By repeating operation this way, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) is turned on when the HS-FET is in its OFF state to minimize the conduction loss. There will be a dead short between input and GND if both HS-FET and LS-FET are turned on at the same time. It's called shoot-through. In order to avoid shoot-through, a dead-time (DT) is internally generated between HS-FET off and LS-FET on, or LS-FET off and HS-FET on.

Heavy-Load Operation

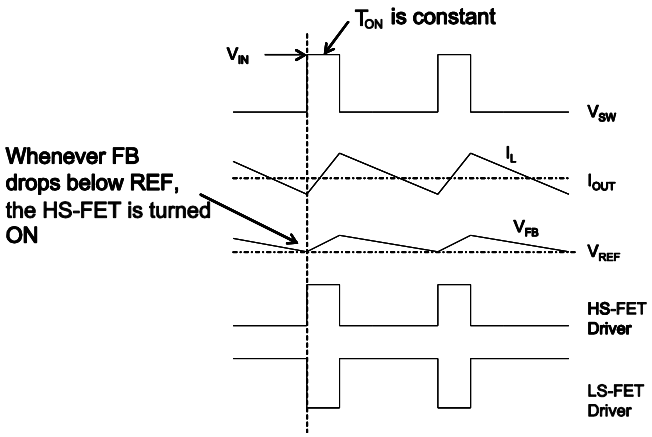

Figure 2—Heavy Load Operation

As Figure 2 shows, when the output current is high, the HS-FET and LS-FET repeat on/off as described above. In this operation, the inductor current will never go to zero. It's called continuous-conduction-mode (CCM) operation. In CCM operation, the switching frequency (F_{SW}) is fairly constant.

Light-Load Operation

When the load current decreases, The NB639 reduces the switching frequency automatically to maintain high efficiency. The light load operation is shown in Figure 3. The V_{FB} does not reach V_{REF} when the inductor current is approaching zero. As the output current reduces from heavy-load condition, the inductor current also decreases, and eventually comes close to zero. The LS-FET driver turns into tri-state (high Z) whenever the inductor current reaches zero level. A current modulator takes over the control of LS-FET and limits the inductor current to less than 600μA. Hence, the output capacitors discharge slowly to GND through LS-FET as well as R1 and R2. As a result, the efficiency at light load condition is greatly improved. At light load condition, the HS-FET is not turned ON as frequently as at heavy load condition. This is called skip mode.

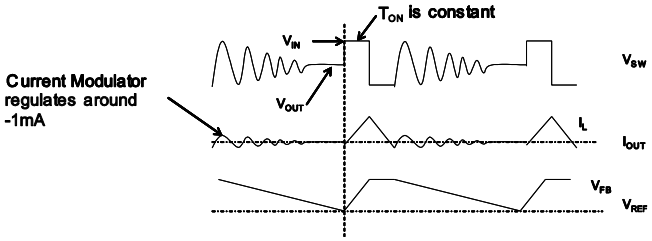

Figure 3—Light Load Operation

As the output current increases from the light load condition, the time period within which the current modulator regulates becomes shorter. The HS-FET is turned on more frequently. Hence, the switching frequency increases correspondingly. The output current reaches the critical level when the current modulator time is zero. The critical level of the output current is determined as follows:

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$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (2)$$

It turns into PWM mode once the output current exceeds the critical level. After that, the switching frequency stays fairly constant over the output current range.

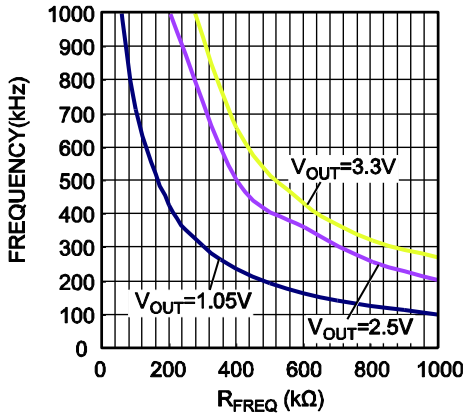
Switching Frequency

Constant-on-time (COT) control is used in the NB639 and there is no dedicated oscillator in the IC. The input voltage is feed-forwarded to the on-time one-shot timer through the resistor R_{FREQ}. The duty ratio is kept as V_{OUT}/V_{IN}. Hence, the switching frequency is fairly constant over the input voltage range. The switching frequency can be set as follows:

$$F_{SW}(kHz) = \frac{10^6}{\frac{12 \times R_{FREQ}(k\Omega)}{V_{IN}(V) - 0.4} \times \frac{V_{IN}(V)}{V_{OUT}(V)} + T_{DELAY}(ns)} \quad (3)$$

Where T_{DELAY} is the comparator delay. It's about 40ns.

Frequency vs. R_{FREQ}



NB639 is optimized to operate at high switching frequency with high efficiency. High switching frequency makes it possible to utilize small sized LC filter components to save system PCB space.

RAMP Compensation

Figure 4 and Figure 5 show jitter occurring in both PWM mode and skip mode. When there is noise in the V_{FB} downward slope, the ON time of the HS-FET driver deviates from its intended location and produces jitter. It is necessary to understand that there is a relationship between a system's stability and the steepness of the V_{FB} ripple's downward slope. The slope steepness of the V_{FB} ripple dominates in noise immunity. The magnitude of the V_{FB} ripple doesn't affect the noise immunity directly.

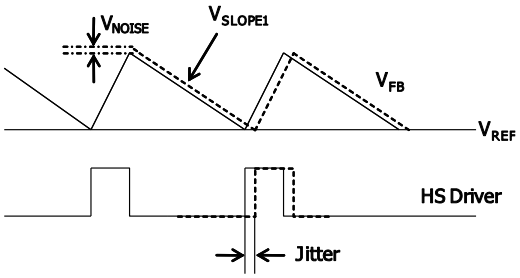


Figure 4—Jitter in PWM Mode

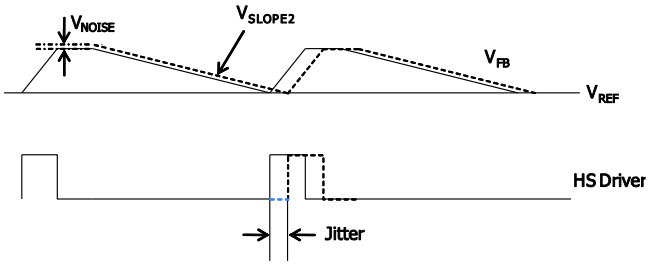


Figure 5—Jitter in Skip Mode

When the output capacitors are ceramic ones, the ESR ripple is not high enough to stabilize the system, and external ramp compensation is needed.

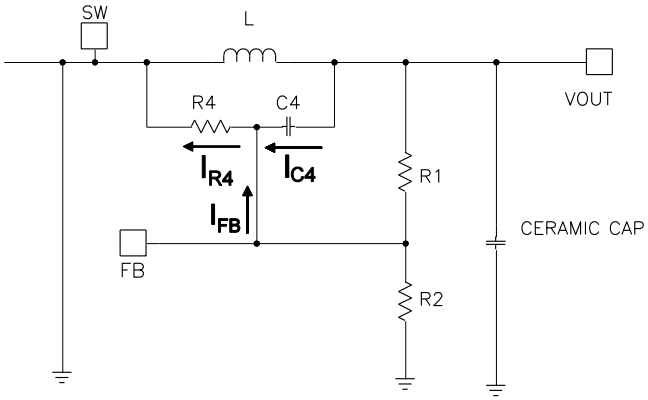


Figure 6—Simplified Circuit in PWM Mode with External Ramp Compensation

In PWM mode, an equivalent circuit with HS-FET off and the use of an external ramp compensation circuit (R4, C4) is simplified in Figure 6. The external ramp is derived from the inductor ripple current. If one chooses C4, R1, and R2 to meet the following condition:

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$$\frac{1}{2\pi \times F_{SW} \times C_4} < \frac{1}{5} \times \left(\frac{R_1 \times R_2}{R_1 + R_2} \right) \quad (4)$$

Then one can have:

$$I_{R4} = I_{C4} + I_{FB} \approx I_{C4} \quad (5)$$

The downward slope of the V_{FB} ripple can be estimated as:

$$V_{SLOPE1} = \frac{-V_{OUT}}{R4 \times C4} \quad (6)$$

As one can see from equation (6), if there is instability in PWM mode, one can reduce either R4 or C4. If C4 can not be reduced further due to limitation from equation (4), then one can only reduce R4. From bench experiments, VSLOPE1 is expected to be around 20~40V/ms.

In the case of POSCAP or other types of capacitor with higher ESR, the external ramp is not necessary.

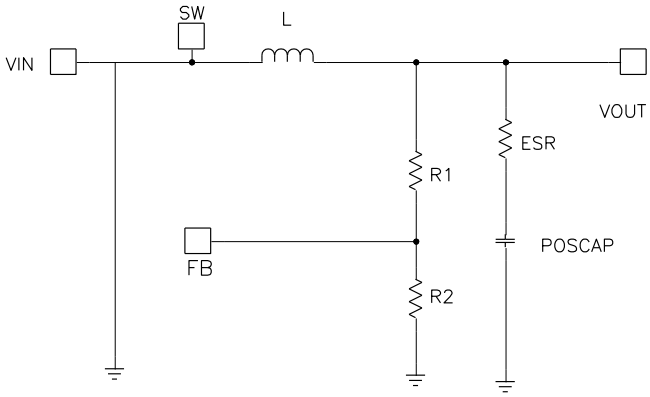

Figure 7—Simplified Circuit in PWM Mode without External Ramp Compensation

Figure 7 shows the equivalent circuit in PWM mode with the HS-FET off and without an external ramp circuit. The ESR ripple dominates the output ripple. The downward slope of the V_{FB} ripple is:

$$V_{SLOPE1} = \frac{-ESR \times V_{REF}}{L} \quad (7)$$

From equation (7), one can see that the downward slope of V_{FB} ripple is proportional to ESR/L. Therefore, it's necessary to know the minimum ESR value of the output capacitors when no external ramp is used. There is also a limitation with inductance in this case. The smaller the inductance, the more stable it will be.

From our bench experiments, it is recommended to keep VSLOPE1 around 15~30V/ms.

While in skip mode, the downward slope is not related to the external ramp.

In skip mode, the downward slope of the V_{FB} ripple is the same whether the external ramp is used or not. Figure 8 shows an equivalent circuit with HS-FET off and the current modulator regulating the LS-FET. The downward slope of the V_{FB} ripple can be determined as follows (I_{MOD} is ignored here):

$$V_{SLOPE2} = \frac{-V_{REF}}{(R_1 + R_2) \times C_{OUT}} \quad (8)$$

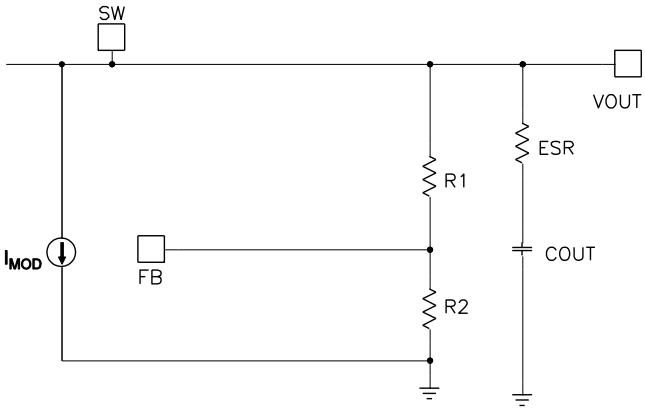

Figure 8—Simplified Circuit in Skip Mode

To keep the system stable during light load condition, the values of the FB resistors should not be too big. It is recommended to keep the V_{SLOPE2} value around 0.4~0.8mV/ms. It should be noted that $_{IMOD}$ is excluded from the equation because it does not impact the system's stability at light load conditions.

Bootstrap Charging

The floating power MOSFET driver is recommended to be powered by an external V_{CC} through D2 as shown in Figure 9. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.2V with a hysteresis of 150mV. U1 will regulate to maintain BST voltage across C4 If (V_{CC}-V_{SW}) is less than 3.5V. The recommended external BST diode D2 is IN4148, and the BST cap C4 is 0.1~1μF.

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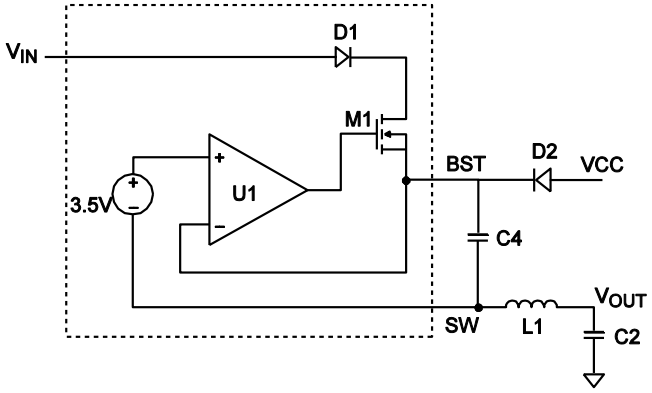

Figure 9—Bootstrap Charging Circuit

Soft Start/Stop

The NB639 employs soft start/stop (SS) mechanism to ensure smooth output during power-up and power shutdown. When the EN pin becomes high, an internal current source (8.5μA) charges up the SS CAP. The SS CAP voltage takes over the V_{REF} voltage to the PWM comparator. The output voltage smoothly ramps up with the SS voltage. Once the SS voltage reaches the same level as the REF voltage, it keeps ramping up while REF takes over the PWM comparator. At this point, the soft start finishes and it enters into steady state operation.

When the EN pin becomes low, the SS CAP voltage is discharged through an 8.5μA internal current source. Once the SS voltage reaches REF voltage, it takes over the PWM comparator. The output voltage will decrease smoothly with SS voltage until zero level. The SS CAP value can be determined as follows:

$$C_{SS}(nF) = \frac{T_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} \quad (9)$$

If the output capacitors have large capacitance value, it's not recommended to set the SS time too small. A minimal value of 4.7nF should be used if the output capacitance value is larger than 330uF.

Power Good (PGOOD)

The NB639 has power-good (PGOOD) output. The PGOOD pin is the open drain of a MOSFET. It should be connected to V_{CC} or other voltage source through a resistor (e.g. 100k). After the input voltage is applied, the MOSFET is turned on, so that the PGOOD pin is pulled to GND before SS ready. After FB voltage reaches 90% of REF voltage, the PGOOD pin is pulled high after a delay.

The PGOOD delay time is determined as follows:

$$T_{PGOOD}(ms) = 0.5 \times T_{SS}(ms) + 0.5 \quad (10)$$

When the FB voltage drops to 85% of the REF voltage, the PGOOD pin will be pulled low.

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

The NB639 has cycle-by-cycle over-current limit control. The inductor current is monitored during the ON state. Once it detects that the inductor current is higher than the current limit, the HS-FET is turned off. At the same time, the OCP timer is started. The OCP timer is set as 40μs. If in the following 40μs, the current limit is hit for every cycle, then it'll trigger OCP. The converter needs power cycle to restart after it triggers OCP.

When the current limit is hit and the FB voltage is lower than 50% of the REF voltage, the device considers this as a dead short on the output and triggers OCP immediately. This is short circuit protection (SCP).

Over/Under-voltage Protection (OVP/UVP)

The NB639 monitors the output voltage through a resistor divider feedback (FB) voltage to detect overvoltage and undervoltage on the output. When the FB voltage is higher than 125% of the REF voltage, it'll trigger OVP. Once it triggers OVP, the LS-FET is always on while the HS-FET is always off. It needs power cycle to power up again. When the FB voltage is below 50% of the REF voltage (0.815V), UVP will be triggered. Usually, UVP accompanies a hit in current limit and this results in SCP.

UVLO protection

The NB639 has under-voltage lock-out protection (UVLO). When V_{CC} is higher than the UVLO rising threshold voltage, the NB639 will be powered up. It shuts off when V_{CC} is lower than the UVLO falling threshold voltage. This is non-latch protection.

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Thermal Shutdown

Thermal shutdown is employed in the NB639. The junction temperature of the IC is internally monitored. If the junction temperature exceeds the threshold value (typically 150ºC), the converter shuts off. This is non-latch protection. There is about 25ºC hysteresis. Once the junction temperature drops to around 125ºC, it initiates a soft start.

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APPLICATION INFORMATION

Setting the Output Voltage

The output voltage is set by using a resistor divider from the output voltage to FB pin.

When there is no external ramp employed, the output voltage is set by feedback resistors R1 and R2. First, choose a value for R2. A value within 5kΩ-40kΩ is recommended to ensure stable operation. Then, R1 is determined as follows:

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (11)$$

When low ESR ceramic capacitor is used in the output, an external voltage ramp should be added to FB through resistor R4 and capacitor C4.The output voltage is influenced by ramp voltage V_{RAMP} except R divider. The V_{RAMP} can be calculated as shown in equation 19. Choose a value within 5kΩ-40kΩ for R2. The value of R1 then is determined as follows:

$$R1 = \frac{1}{\frac{V_{REF} + \frac{1}{2}V_{RAMP}}{R2 \times \left(V_{OUT} - V_{REF} - \frac{1}{2}V_{RAMP}\right)} - \frac{1}{R4}} \quad (12)$$

Using equation 12 to calculate the output voltage can be complicated. Furthermore, as V_{RAMP} changes due to changes in V_{OUT} and V_{IN}, V_{FB} also varies. To improve the output voltage accuracy and simplify the calculation of R2 in equation 12, a DC-blocking capacitor Cdc can be added. Figure 10 shows a simplified circuit with external ramp compensation and a DC-blocking capacitor. With this capacitor, R1 can easily be obtained by using equation 11.

Cdc is suggested to be 1-4.7μF for better DC blocking performance.

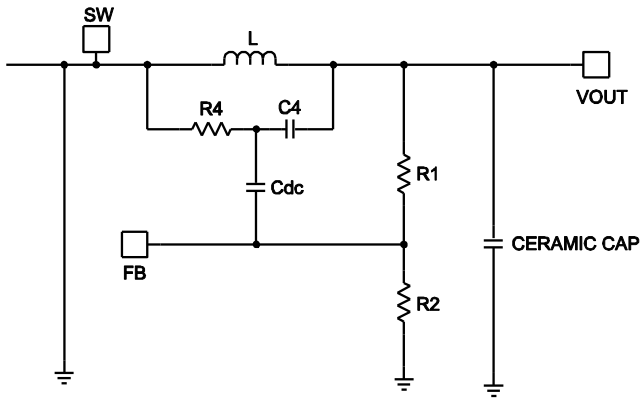

Figure 10—Simplified Circuit with External Ramp Compensation and DC-Blocking Capacitor.

Input Capacitor

The input current to the step-down converter is discontinuous. Therefore, a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Ceramic capacitors are recommended for best performance. In the layout, it's recommended to put the input capacitors as close to the IN pin as possible.

The capacitance varies significantly over temperature. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable over temperature.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated as follows:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (13)$$

The worst-case condition occurs at:

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (14)$$

For simplification, choose the input capacitor whose RMS current rating is greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is input voltage ripple requirement in the system design, choose the input capacitor that meets the specification.

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The input voltage ripple can be estimated as follows:

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (15)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (16)$$

Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (17)$$

Where R_{ESR} is the equivalent series resistance (ESR) of the output capacitor.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (18)$$

The output voltage ripple caused by ESR is very small. Therefore, an external ramp is needed to stabilize the system. The voltage ramp is expected to be around 30mV. The external ramp can be generated through resistor R4 and capacitor C4 using the following equation:

$$V_{RAMP} = \frac{(V_{IN} - V_{OUT}) \times T_{ON}}{R4 \times C4} \quad (19)$$

The C4 should be chosen so that it meets the following condition:

$$\frac{1}{2\pi \times F_{SW} \times C4} < \frac{1}{5} \times (\frac{R_1 \times R_2}{R_1 + R_2}) \quad (20)$$

In the case of POSCAP capacitors, the ESR dominates the impedance at the switching frequency. The ramp voltage generated from the ESR is high enough to stabilize the system. Therefore, an external ramp is not needed. A minimum ESR value of 12mΩ is required to ensure stable operation of the converter. For simplification, the output ripple can be approximated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (21)$$

Inductor

The inductor is required to supply constant current to the output load while being driven by the switching input voltage. A larger value inductor will result in less ripple current that will result in lower output ripple voltage. However, a larger value inductor will have a larger physical size, higher series resistance, and/or lower saturation current. A good rule for determining the inductor value is to allow the peak-to-peak ripple current in the inductor to be approximately 30~40% of the maximum switch current limit. Also, make sure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated as:

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (22)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated as:

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (23)$$

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Table 1—Inductor Selection Guide

Part Number	Manufacturer	Inductance (μH)	DCR (mΩ)	Current Rating (A)	Dimensions L x W x H (mm^3)	Switching Frequency (kHz)
PCMC-135T-R68MF	Cyntec	0.68	1.7	34	13.5 x 12.6 x 4.8	600
FDA1254-1R0M	TOKO	1	2	25.2	13.5 x 12.6 x 5.4	300~600
FDA1254-1R2M	TOKO	1.2	2.05	20.2	13.5 x 12.6 x 5.4	300~600

Typical Design Parameter Tables

The following tables include recommended component values for typical output voltages (1.05V, 1.2V, 1.8V, 2.5V, 3.3V) and switching frequencies (300kHz, 500kHz, and 700kHz). Refer to Tables 2-4 for design cases without external ramp compensation and Tables 5-7 for design cases with external ramp compensation. External ramp is not needed when high-ESR capacitors, such as electrolytic or POSCAPs are used. External ramp is needed when low-ESR capacitors, such as ceramic capacitors are used. For cases not listed in this datasheet, a calculator in excel spreadsheet can also be requested through a local sales representative to assist with the calculation.

Table 2—300kHz, 12V_{IN}

V_{OUT} (V)	L (μH)	R1 (kΩ)	R2 (kΩ)	R_{FREQ} (kΩ)
1.05	2.2	12.1	43	301
1.2	2.2	12.1	24	360
1.8	2.2	19.6	15.8	499
2.5	2.2	30	14.7	680
3.3	2.2	40.2	13.3	806

Table 3—500kHz, 12V_{IN}

V_{OUT} (V)	L (μH)	R1 (kΩ)	R2 (kΩ)	R_{FREQ} (kΩ)
1.05	1	12.1	43	180
1.2	1	12.1	24	200
1.8	1	19.6	15.8	309
2.5	1	30	14.7	402
3.3	1	40.2	13.3	523

Table 4—700kHz, 12V_{IN}

V_{OUT} (V)	L (μH)	R1 (kΩ)	R2 (kΩ)	R_{FREQ} (kΩ)
1.05	1	12.1	43	120
1.2	1	12.1	24	140
1.8	1	19.6	15.8	210
2.5	1	30	14.7	309
3.3	1	40.2	12.4	402

Table 5—300kHz, 12V_{IN}

V_{OUT} (V)	L (μH)	R1 (kΩ)	R2 (kΩ)	R4 (kΩ)	C4 (pF)	R_{FREQ} (kΩ)
1.05	2.2	12.1	43	330	220	301
1.2	2.2	12.1	24	330	220	360
1.8	2.2	19.6	15.2	499	220	499
2.5	2.2	30	14.7	499	220	680
3.3	2.2	40.2	13	604	220	806

Table 6—500kHz, 12V_{IN}

V_{OUT} (V)	L (μH)	R1 (kΩ)	R2 (kΩ)	R4 (kΩ)	C4 (pF)	R_{FREQ} (kΩ)
1.05	1	12.1	43	330	220	180
1.2	1	12.1	24	330	220	196
1.8	1	19.6	15.8	330	220	309
2.5	1	30	14.7	383	220	402
3.3	1	40.2	12	499	220	522

Table 7—700kHz, 12V_{IN}

V_{OUT} (V)	L (μH)	R1 (kΩ)	R2 (kΩ)	R4 (kΩ)	C4 (pF)	R_{FREQ} (kΩ)
1.05	1	12.1	43	220	220	120
1.2	1	12.1	24	220	220	140
1.8	1	19.6	15.8	261	220	210
2.5	1	30	14.3	261	220	270
3.3	1	40.2	12	360	220	383

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TYPICAL APPLICATION

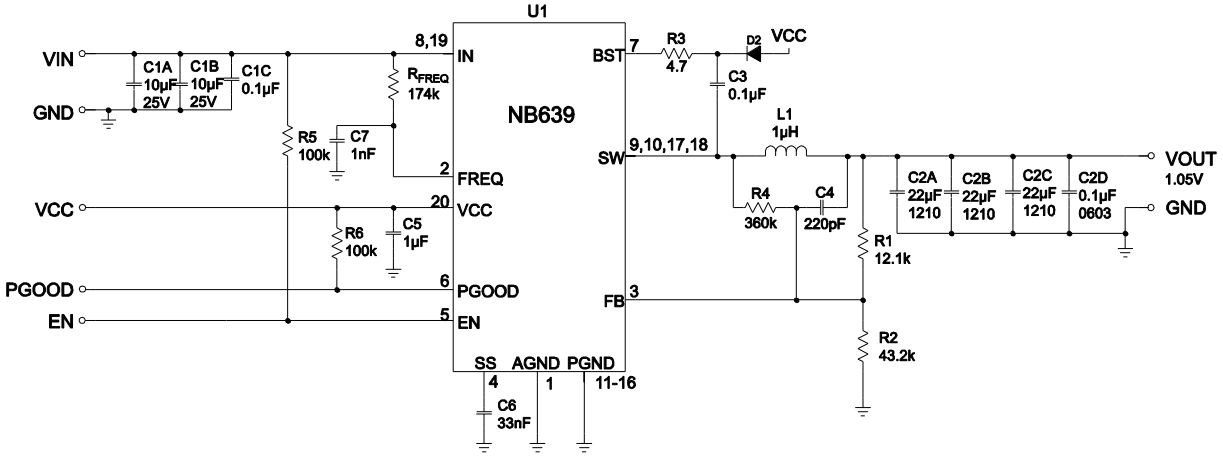

Figure 11 — Typical Application Circuit with Low ESR Ceramic Capacitor

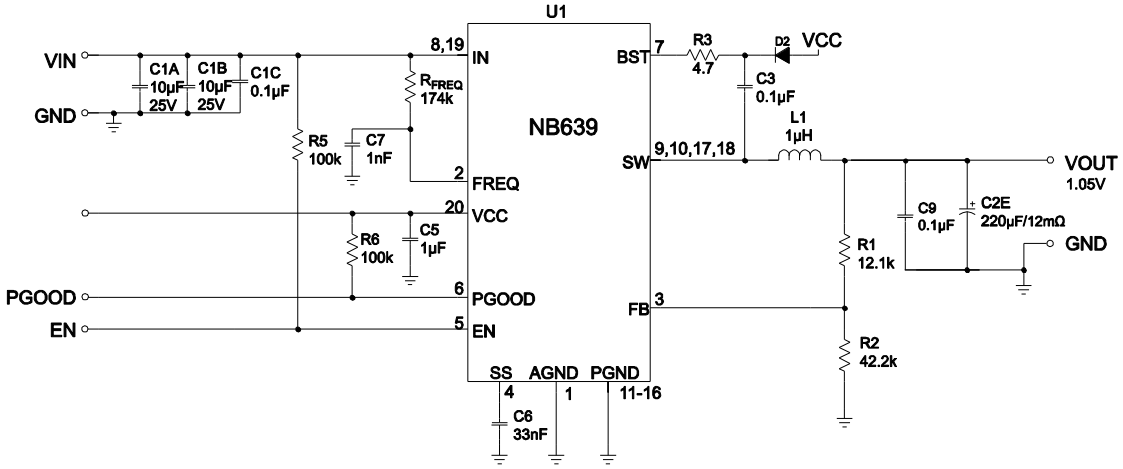

Figure 12 — Typical Application Circuit with No External Ramp

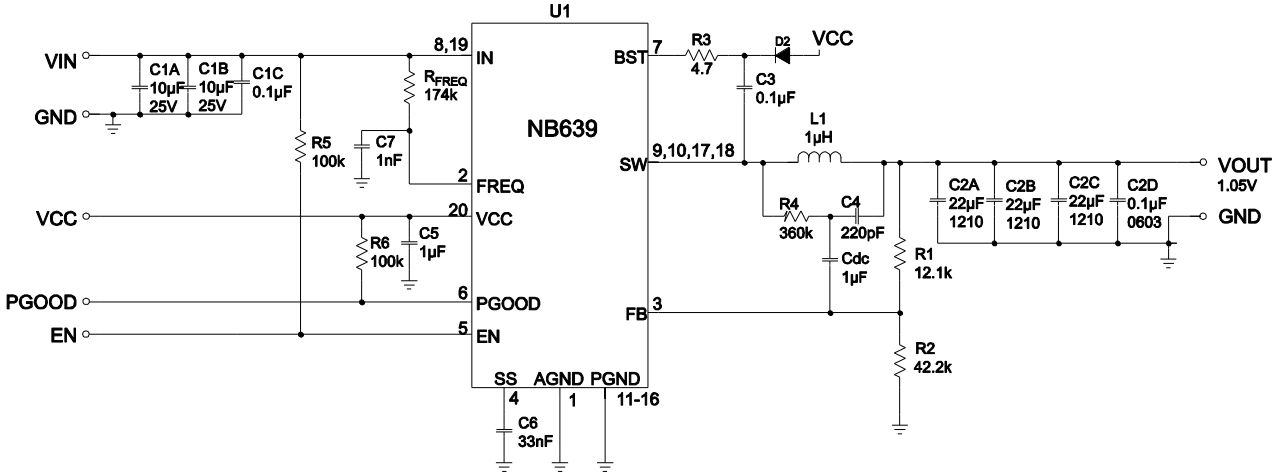

Figure 13 — Typical Application Circuit with Low ESR Ceramic Capacitor and DC-Blocking Capacitor.

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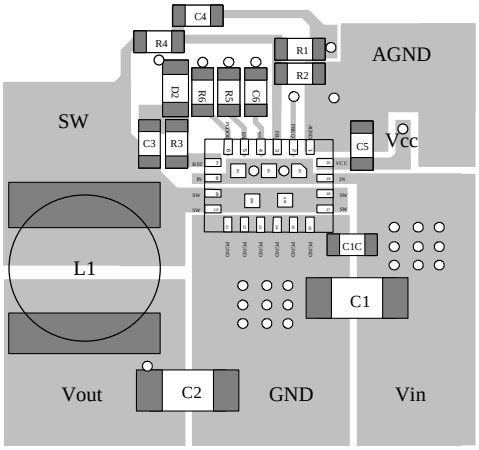
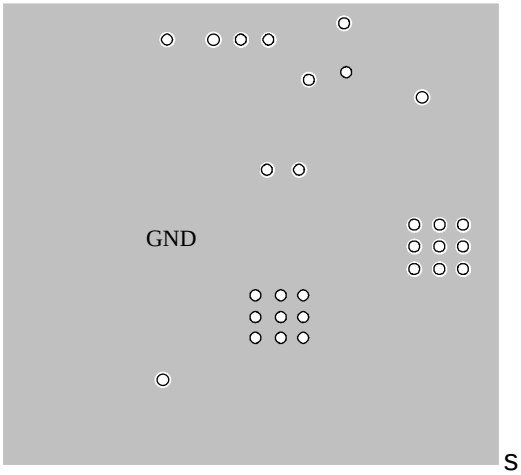
LAYOUT RECOMMENDATION

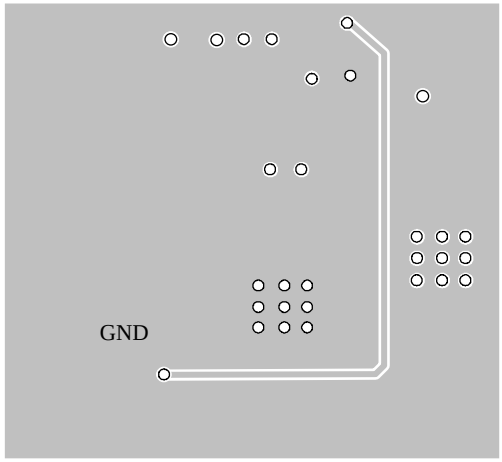
1. The high current paths (GND, IN, and SW) should be placed very close to the device with short, direct and wide traces.
2. Put the input capacitors as close to the IN and GND pins as possible.
3. Put the decoupling capacitor as close to the V_{CC} and GND pins as possible.
4. Keep the switching node SW short and away from the feedback network.
5. The external feedback resistors should be placed next to the FB pin. Make sure that there is no via on the FB trace.
6. Keep the BST voltage path (BST, $C_{BST,}$ and SW) as short as possible.
7. Keep the bottom IN and SW pads connected with large copper to achieve better thermal performance.
8. Four-layer layout is strongly recommended to achieve better thermal performance.



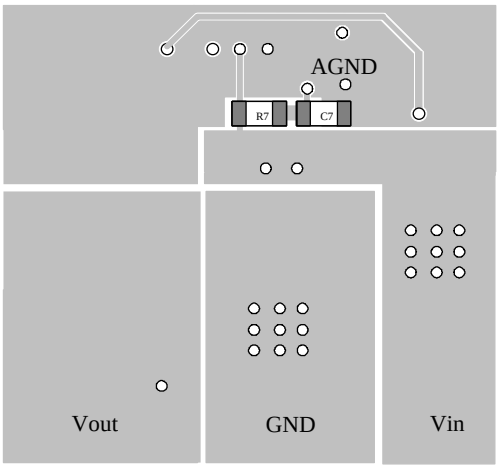
Top Layer



Inner1 Layer



Inner2 Layer



Bottom Layer

Figure 14—PCB Layout

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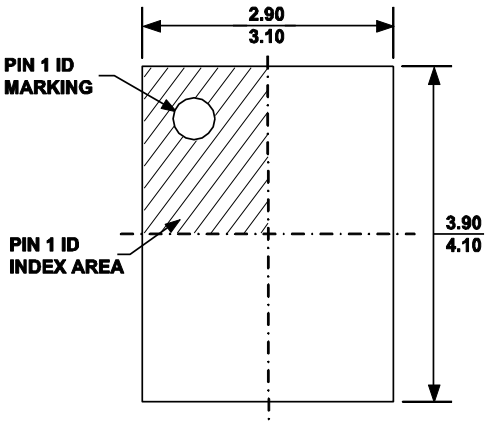
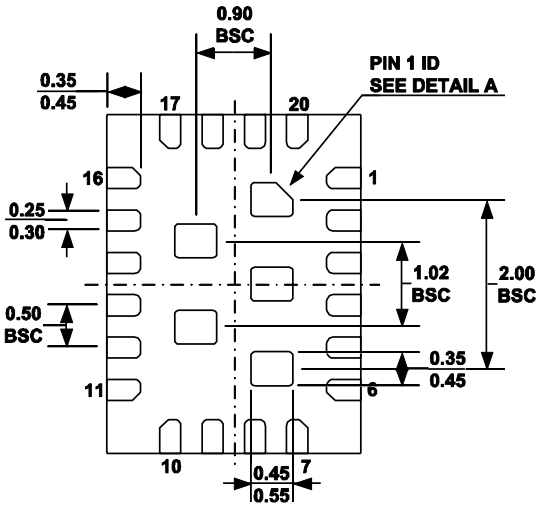
END OF LIFE, REFER TO NB700 OR NB693A

PACKAGE INFORMATION

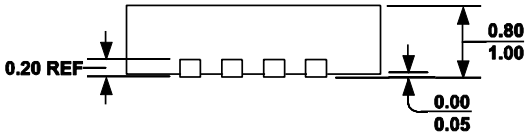
QFN20 (3x4mm)



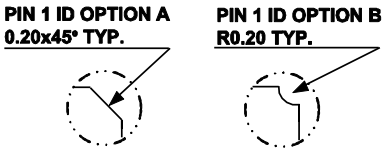
TOP VIEW



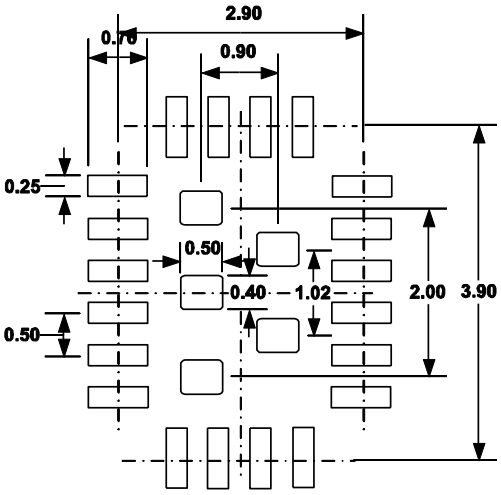
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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